Advance Information

MPC8240EC/D
Rev. 2, 7/2002

MPC8240 Integrated Processor Hardware Specifications

The MPC8240 combines a MPC603e core microprocessor with a PCI bridge. The MPC8240 PCI support will allow system designers to rapidly create systems using peripherals already designed for PCI and other standard interfaces. The MPC8240 also integrates a high-performance memory controller which supports various types of DRAM and ROM. The MPC8240 is the first of a family of products that provide system-level support for industry standard interfaces with PowerPC microprocessor cores.

This document describes pertinent electrical and physical characteristics of the MPC8240. For functional characteristics of the processor, refer to the *MPC8240 Integrated Processor User's Manual* (MPC8240UM/D).

This document contains the following topics:

To locate any published errata or updates for this document, refer to the web site at http://www.motorola.com/semiconductors.

1.1 Overview

The MPC8240 integrated processor is comprised of a peripheral logic block and a 32-bit superscalar MPC603e core, as shown in Figure 1.

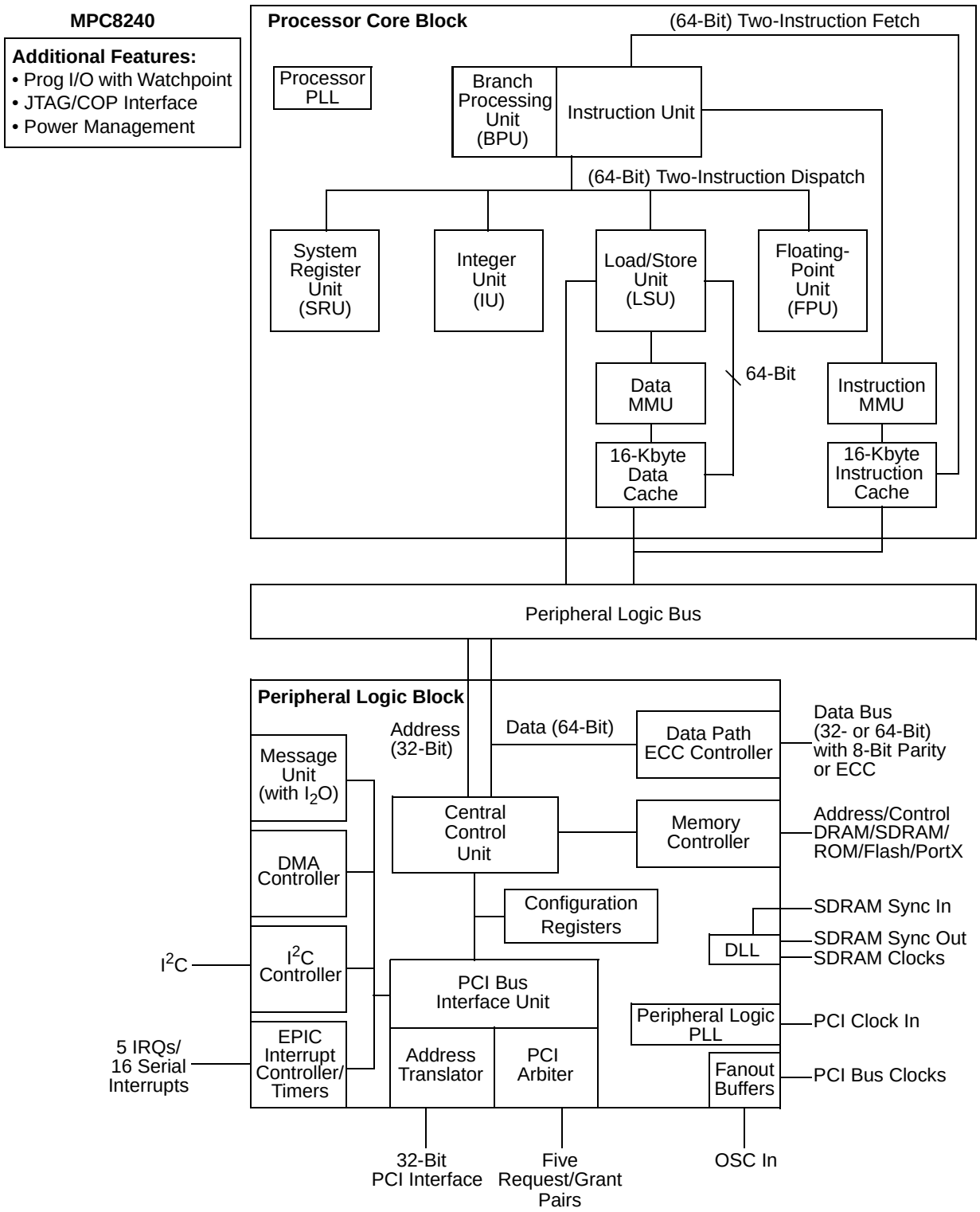


Figure 1. MPC8240 Block Diagram

The peripheral logic integrates a PCI bridge, memory controller, DMA controller, EPIC interrupt controller, I_2O controller, and an I^2C controller. The MPC603e core is a full-featured, high-performance processor with floating-point support, memory management, 16-Kbyte instruction cache, 16-Kbyte data cache, and power management features. The integration reduces the overall packaging requirements and the number of discrete devices required for an embedded system.

The MPC8240 contains an internal peripheral logic bus that interfaces the MPC603e core to the peripheral logic. The core can operate at a variety of frequencies, allowing the designer to trade off performance for power consumption. The MPC603e core is clocked from a separate PLL, which is referenced to the peripheral logic PLL. This allows the microprocessor and the peripheral logic block to operate at different frequencies, while maintaining a synchronous bus interface. The interface uses a 64- or 32-bit data bus (depending on memory data bus width) and a 32-bit address bus along with control signals that enable the interface between the processor and peripheral logic to be optimized for performance. PCI accesses to the MPC8240 memory space are passed to the processor bus for snooping purposes when snoop mode is enabled.

The MPC8240 features serve a variety of embedded applications. In this way, the MPC603e core and peripheral logic remain general-purpose. The MPC8240 can be used as either a PCI host or an agent controller.

1.2 Features

This section summarizes features of the MPC8240. Major features of the MPC8240 are as follows:

- Peripheral logic
  - Memory interface
    - Programmable timing supporting either FPM DRAM, EDO DRAM, or SDRAM
    - High-bandwidth bus (32-/64-bit data bus) to DRAM
    - Supports one to eight banks of 4-, 16-, 64-, or 128-Mbit memory devices
    - Supports 1-Mbyte to 1-Gbyte DRAM memory
    - 16 Mbytes of ROM space
    - 8-, 32-, or 64-bit ROM
    - Write buffering for PCI and processor accesses
    - Supports normal parity, read-modify-write (RMW), or ECC
    - Data-path buffering between memory interface and processor
    - Low-voltage TTL logic (LVTTL) interfaces
    - PortX: 8-, 32-, or 64-bit general-purpose I/O port using ROM controller interface with programmable address strobe timing
  - 32-bit PCI interface operating up to 66 MHz
    - PCI 2.1-compliant
    - PCI 5.0-V tolerance
    - Support for PCI locked accesses to memory
    - Support for accesses to PCI memory, I/O, and configuration spaces
    - Selectable big- or little-endian operation
    - Store gathering of processor-to-PCI write and PCI-to-memory write accesses

  - Memory prefetching of PCI read accesses
  - Selectable hardware-enforced coherency
  - PCI bus arbitration unit (five request/grant pairs)
  - PCI agent mode capability
  - Address translation unit
  - Some internal configuration registers accessible from PCI
- Two-channel integrated DMA controller (writes to ROM/PortX not supported)
  - Supports direct mode or chaining mode (automatic linking of DMA transfers)
  - Supports scatter gathering—read or write discontinuous memory
  - Interrupt on completed segment, chain, and error
  - Local-to-local memory
  - PCI-to-PCI memory
  - PCI-to-local memory
  - PCI memory-to-local memory
- Message unit
  - Two doorbell registers
  - Two inbound and two outbound messaging registers
  - I_2O message controller
- I^2C controller with full master/slave support (except broadcast all)
- Embedded programmable interrupt controller (EPIC)
  - Five hardware interrupts (IRQs) or 16 serial interrupts
  - Four programmable timers
- Integrated PCI bus, CPU, and SDRAM clock generation
- Programmable PCI bus, 60x, and memory interface output drivers

- Dynamic power management—Supports 60x nap, doze, and sleep modes
- Programmable input and output signals with watchpoint capability
- Built-in PCI bus performance monitor facility
- Debug features
  - Memory attribute and PCI attribute signals
  - Debug address signals
  - $\overline{\text{MIV}}$ signal: marks valid address and data bus cycles on the memory bus
  - Error injection/capture on data path
  - IEEE 1149.1 (JTAG)/test interface
- Processor core interface
- High-performance, superscalar processor core
- Integer unit (IU), floating-point unit (FPU) (software enabled or disabled), load/store unit (LSU), system register unit (SRU), and a branch processing unit (BPU)
- 16-Kbyte instruction cache

— 16-Kbyte data cache
— Lockable L1 cache, entire cache or on a per-way basis

1.3 General Parameters

The following list provides a summary of the general parameters of the MPC8240:

Technology	0.29 µm CMOS, five-layer metal
Die size	73 mm^2
Transistor count	3.1 million
Logic design	Fully-static
Packages	Surface mount 352 tape ball grid array (TBGA)
Core power supply	2.5 V ±5% V DC (nominal; see Table 2 for recommended operating conditions)
I/O power supply	3.0 to 3.6 V DC

1.4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8240.

1.4.1 DC Electrical Characteristics

The following sections describe the MPC8240 absolute maximum ratings, recommended operating conditions, DC electrical specifications, output driver characteristics, and power data characteristics.

1.4.1.1 Absolute Maximum Ratings

The tables in this section describe the MPC8240 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings

Characteristic [1]	Symbol	Range	Unit
Supply voltage—CPU core and peripheral logic	V_{DD}	–0.3 to 2.75	V
Supply voltage—memory bus drivers	GV_{DD}	–0.3 to 3.6	V
Supply voltage—PCI and standard I/O buffers	OV_{DD}	–0.3 to 3.6	V
Supply voltage—PLLs and DLL	$AV_{DD}/AV_{DD}2/LAV_{DD}$	–0.3 to 2.75	V
Supply voltage—PCI reference	LVD_{DD}	–0.3 to 5.4	V
Input voltage [2]	V_{in}	–0.3 to 3.6	V
Operational die-junction temperature range	T_j	0 to 105	°C
Storage temperature range	T_{stg}	–55 to 150	°C

Notes:
1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. PCI inputs with LV_{DD} = 5 V ±5% V DC may be correspondingly stressed at voltages exceeding LV_{DD} + 0.5 V DC.

1.4.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8240.

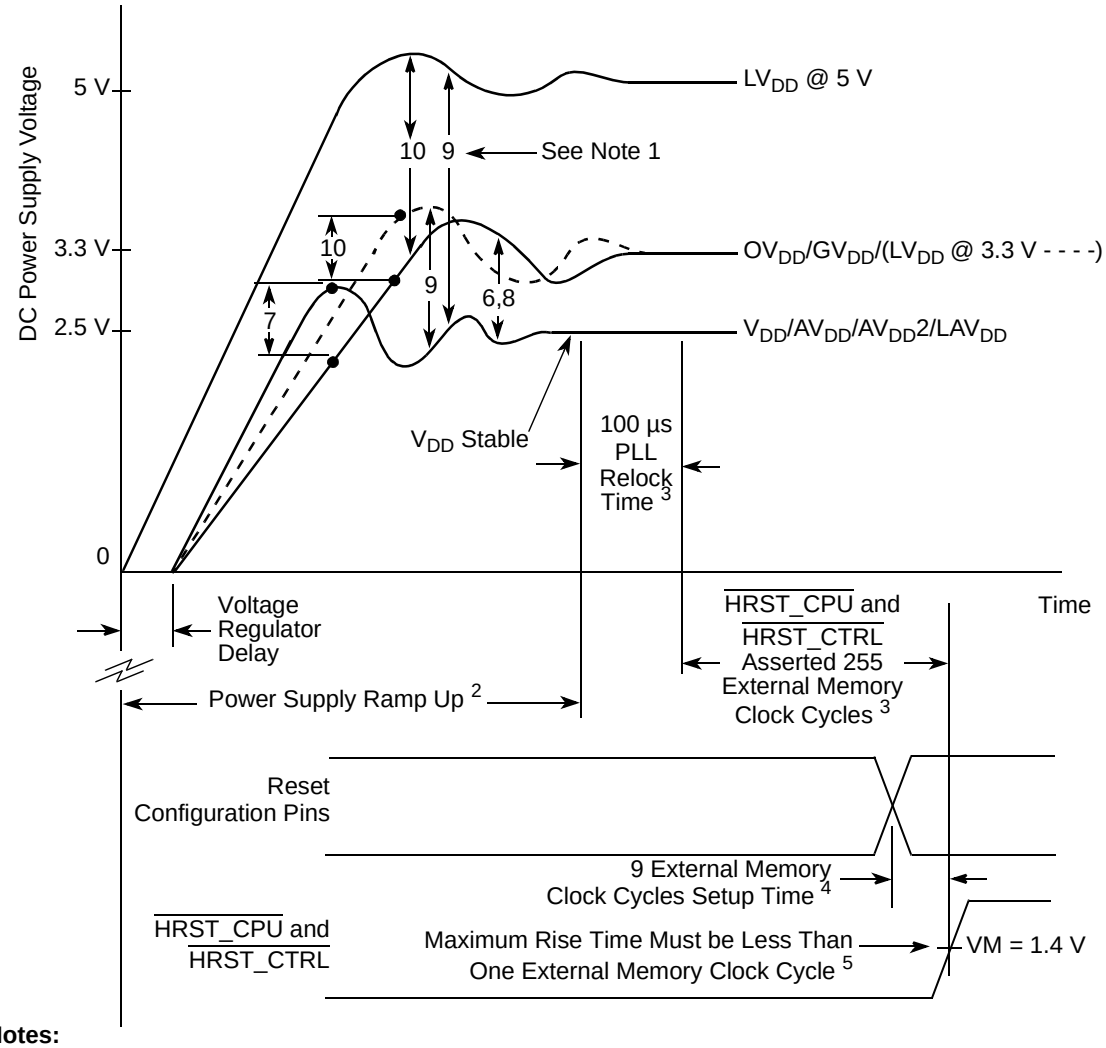
Table 2. Recommended Operating Conditions [1]

Characteristic		Symbol	Recommended Value	Unit	Notes
Supply voltage		V_{DD}	2.5 ±5%	V	4,6
Supply voltage for PCI and standard bus standards		OV_{DD}	3.3 ±0.3	V	6
Supply voltages for memory bus drivers		GV_{DD}	3.3 ±5%	V	8
PLL supply voltage—CPU core logic		AV_{DD}	2.5 ±5%	V	4, 6
PLL supply voltage—peripheral logic		$AV_{DD}2$	2.5 ±5%	V	4, 7
DLL supply voltage		LAV_{DD}	2.5 ±5%	V	4, 7
PCI reference		LV_{DD}	5.0 ±5%	V	9, 10
			3.3 ±0.3	V	9, 10
Input voltage	LV_{DD} input tolerant signals	V_{in}	0 to 3.6 or 5.75	V	2, 3
	All other inputs		0 to 3.6	V	5
Die-junction temperature		T_j	0 to 105	°C	

Notes:
1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. These signals are designed to withstand LV_{DD} + 0.5 V DC when LV_{DD} is connected to a 3.3- or 5.0-V DC power supply.
3. LV_{DD} input tolerant signals: PCI interface, EPIC control, and OSC_IN signals.
4. See Section 1.9, “Ordering Information,” for details on a modified voltage (V_{DD}) version device.

Cautions:
5. Input voltage (V_{in}) must not be greater than the supply voltage (V_{DD}/AV_{DD}/$AV_{DD}2$/LAV_{DD}) by more than 2.5 V at all times, including during power-on reset.
6. OV_{DD} must not exceed V_{DD}/AV_{DD}/$AV_{DD}2$/LAV_{DD} by more than 1.8 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. V_{DD}/AV_{DD}/$AV_{DD}2$/LAV_{DD} must not exceed OV_{DD} by more than 0.6 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
8. GV_{DD} must not exceed V_{DD}/AV_{DD}/$AV_{DD}2$/LAV_{DD} by more than 1.8 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
9. LV_{DD} must not exceed V_{DD}/AV_{DD}/$AV_{DD}2$/LAV_{DD} by more than 5.4 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
10. LV_{DD} must not exceed OV_{DD} by more than 3.6 V at any time, including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

Figure 2 shows the supply voltage sequencing and separation cautions.



Notes:
1. Numbers associated with waveform separations correspond to caution numbers listed in Table 2.
2. Refer to Table 7 for additional information on PLL relock and reset signal assertion timing requirements.
3. Refer to Table 8 for additional information on reset configuration pin setup timing requirements.
4. For the device to be in the non-reset state, HRST_CPU/HRST_CTRL must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle.

Figure 2. Supply Voltage Sequencing and Separation Cautions

Figure 3 shows the undershoot and overshoot voltage of the memory interface of the MPC8240.

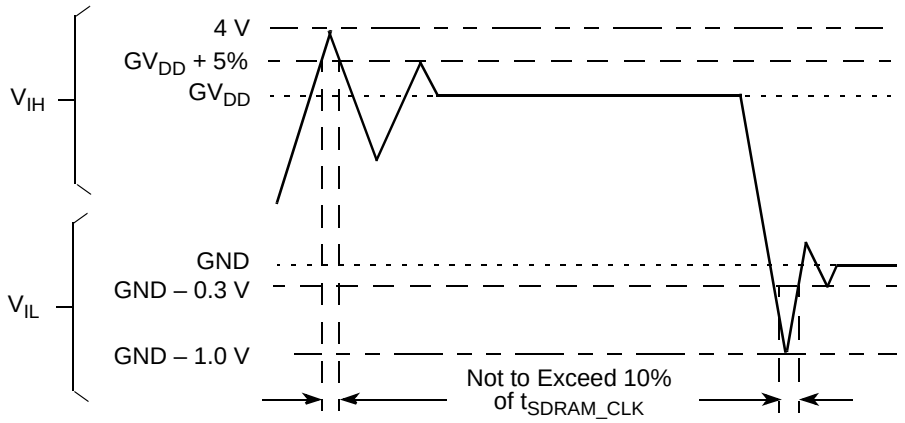


Figure 3. Overshoot/Undershoot Voltage

1.4.1.3 DC Electrical Specifications

Table 3 provides the DC electrical characteristics for the MPC8240.

Table 3. DC Electrical Specifications

At recommended operating conditions (see Table 2)

Characteristic	Condition [3]	Symbol	Min	Max	Unit
Input high voltage [5]	PCI only	V_{IH}	$0.65 \times OV_{DD}$	LV_{DD}	V
Input low voltage	PCI only	V_{IL}	—	$0.3 \times OV_{DD}$	V
Input high voltage	All other pins (GV_{DD} = 3.3 V)	V_{IH}	2.0	3.3	V
Input low voltage	All inputs except PCI_SYNC_IN	V_{IL}	GND	0.8	V
PCI_SYNC_IN input high voltage		CV_{IH}	2.4	—	V
PCI_SYNC_IN input low voltage		CV_{IL}	—	0.4	V
Input leakage current [4] for pins using DRV_PCI driver	$0.5 V \le V_{in} \le 2.7 V$ @ LV_{DD} = 4.75	I_L	—	±70	µA
Input leakage current [4] all others	LV_{DD} = 3.6 V $GV_{DD} \le 3.465$	I_L	—	±10	µA
Output high voltage	I_{OH} = Driver Dependent [2] (GV_{DD} = 3.3 V)	V_{OH}	2.4	—	V
Output low voltage	I_{OL} = Driver Dependent [2] (GV_{DD} = 3.3 V)	V_{OL}	—	0.4	V

Table 3. DC Electrical Specifications (continued)

At recommended operating conditions (see Table 2)

Characteristic	Condition [3]	Symbol	Min	Max	Unit
Capacitance	V_{in} = 0 V, f = 1 MHz	C_{in}	—	7.0	pF

Notes:
1. See Table 17 for pins with internal pull-up resistors.
2. See Table 4 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 17.
3. These specifications are for the default driver strengths indicated in Table 4.
4. Leakage current is measured on input pins and on output pins in the high impedance state. The leakage current is measured for nominal OV_{DD}/LV_{DD} and V_{DD} or both OV_{DD}/LV_{DD} and V_{DD} must vary in the same direction.
5. The minimum input high voltage is not compliant with the *PCI Local Bus Specification* (Rev 2.1) which specifies $0.5 \times OV_{DD}$ for minimum input high voltage.

1.4.1.4 Output Driver Characteristics

Table 4 provides information on the characteristics of the output drivers referenced in Table 17. The values are from the MPC8240 IBIS model (v1.1 IBIS, v1.2 file) and are not tested. For additional detailed information see the complete IBIS model listing at: http://www.mot.com/SPS/PowerPC/teksupport/tools/IBIS/kahlua_1.ibs.txt

Table 4. Drive Capability of MPC8240 Output Pins

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	I_{OH}	I_{OL}	Unit	Notes
DRV_STD	20	OV_{DD} = 3.3 V	36.7	30.0	mA	2, 4
	40 (default)	OV_{DD} = 3.3 V	18.7	15.0	mA	2, 4
DRV_PCI	25	OV_{DD} = 3.3 V	11.0	20.6	mA	1, 3
	50 (default)	OV_{DD} = 3.3 V	5.6	10.3	mA	1, 3
DRV_MEM_ADDR DRV_PCI_CLK	8 (default)	GV_{DD} = 3.3 V	89.0	76.3	mA	2, 4
	13.3	GV_{DD} = 3.3 V	55.9	46.4	mA	2, 4
	20	GV_{DD} = 3.3 V	36.7	30.0	mA	2, 4
	40	GV_{DD} = 3.3 V	18.7	15.0	mA	2, 4
DRV_MEM_DATA	20 (default)	GV_{DD} = 3.3 V	36.7	30.0	mA	2, 4
	40	GV_{DD} = 3.3 V	18.7	15.0	mA	2, 4

Notes:
1. For DRV_PCI, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.33-V label by interpolating between the 0.3- and 0.4-V table entries' current values which corresponds to the PCI $V_{OH} = 2.97 = 0.9 \times OV_{DD}$ (OV_{DD} = 3.3 V) where table entry voltage = OV_{DD} – PCI V_{OH}.
2. For all others with GV_{DD} or OV_{DD} = 3.3 V, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.9-V table entry which corresponds to the V_{OH} = 2.4 V where table entry voltage = $GV_{DD}/OV_{DD} – V_{OH}$.
3. For DRV_PCI, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at 0.33 V = PCI $V_{OL} = 0.1 \times OV_{DD}$ (OV_{DD} = 3.3 V) by interpolating between the 0.3- and 0.4-V table entries.

1.4.1.5 Power Characteristics

Table 5 provides power consumption data for the MPC8240.

Table 5. Preliminary Power Consumption

Mode	PCI Bus Clock/Memory Bus Clock CPU Clock Frequency (MHz)				Unit	Notes
	33/66/166	33/66/200	33/100/200	66/100/200		
Typical	2.5	2.8	3.0	3.0	W	1, 5
Maximum—FP	2.9	3.3	3.5	3.5	W	1, 2
Maximum—INT	2.6	2.9	3.2	3.3	W	1, 3
Doze	1.8	1.9	2.1	2.1	W	1, 4, 6
Nap	667	667	858	858	mW	1, 4, 6
Sleep	477	477	477	762	mW	1, 4, 6
I/O Power Supplies						
Mode	**Min**		**Max**		**Unit**	**Notes**
Typical—OV_{DD}	200		600		mW	7, 8
Typical—GV_{DD}	300		900		mW	7, 9

Notes:
1. The values include V_{DD}, AV_{DD}, $AV_{DD}2$, and LAV_{DD} but do not include I/O supply power; see Section 1.7.2, “Power Supply Sizing,” for information on OV_{DD} and GV_{DD} supply power. One DIMM used for memory loading.
2. Maximum—FP power is measured at V_{DD} = 2.5 V with dynamic power management enabled while running an entirely cache-resident, looping, floating-point multiplication instruction.
3. Maximum—INT power is measured at V_{DD} = 2.5 V with dynamic power management enabled while running entirely cache-resident, looping, integer instructions.
4. Power saving mode maximums are measured at V_{DD} = 2.5 V while the device is in doze, nap, or sleep mode.
5. Typical power is measured at V_{DD} = AV_{DD} = 2.5 V, OV_{DD} = 3.3 V where a nominal FP value, a nominal INT value, and a value where there is a continuous flush of cache lines with alternating ones and zeros on 64-bit boundaries to local memory are averaged.
6. Power saving mode data measured with only two PCI_CLKs and two SDRAM_CLKs enabled.
7. The typical minimum I/O power values were results of the MPC8240 performing cache resident integer operations at the slowest frequency combination of 33:66:166 (PCI:Mem:CPU) MHz.
8. The typical maximum OV_{DD} value resulted from the MPC8240 operating at the fastest frequency combination of 66:100:250 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeros to PCI memory.
9. The typical maximum GV_{DD} value resulted from the MPC8240 operating at the fastest frequency combination of 66:100:250 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeros on 64-bit boundaries to local memory.
10. Power consumption on the PLL supply pins (AV_{DD} and $AV_{DD}2$) and the DLL supply pin (LAV_{DD}) less than15 mW. This parameter is guaranteed by design and is not tested.

1.4.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC8240. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Table 6 and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (PCI_SYNC_IN)

clock frequency and the settings of the PLL_CFG[0:4] signals. Parts are sold by maximum processor core frequency; see Section 1.9, “Ordering Information.”

1.4.2.1 AC Operating Frequency Data

Table 6 provides the operating frequency information for the MPC8240.

Table 6. Operating Frequency

At recommended operating conditions (see Table 2) with GV_{DD} = 3.3 V ±5% and LV_{DD} = 3.3 V ±5%

Characteristic [1]	200 MHz		250 MHz [2]		Unit
	Min	Max	Min	Max	
Processor frequency (CPU)	100	200	100	250	MHz
Memory bus frequency	33–100				MHz
PCI input frequency	25–66				MHz

Note:
1. **Caution:** The PCI_SYNC_IN frequency and PLL_CFG[0:4] settings must be chosen such that the resulting peripheral logic/memory bus frequency and CPU (core) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in Section 1.6, “PLL Configuration,” for valid PLL_CFG[0:4] settings and PCI_SYNC_IN frequencies.

2.) The 250 MHz processor is only available as an R spec part. See Section 1.9.2, “Part Numbers Not Fully Addressed by This Document,” for more information.

1.4.2.2 Clock AC Specifications

Table 7 provides the clock AC timing specifications as defined in Section 1.4.2.3, “Input AC Timing Specifications.”

Table 7. Clock AC Timing Specifications

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ±0.3 V

Num	Characteristic and Condition [1]	Min	Max	Unit	Notes
1a	Frequency of operation (PCI_SYNC_IN)	25	66	MHz	
1b	PCI_SYNC_IN cycle time	40	15	ns	
2, 3	PCI_SYNC_IN rise and fall times	—	2.0	ns	2
4	PCI_SYNC_IN duty cycle measured at 1.4 V	40	60	%	
5a	PCI_SYNC_IN pulse width high measured at 1.4 V	6	9	ns	3
5b	PCI_SYNC_IN pulse width low measured at 1.4 V	6	9	ns	3
7	PCI_SYNC_IN jitter	—	150	ps	
8a	PCI_CLK[0:4] skew (pin to pin)	—	500	ps	
8b	SDRAM_CLK[0:3] skew (pin to pin)	—	350	ps	8
10	Internal PLL relock time	—	100	µs	3, 4, 6
15	DLL lock range with DLL_EXTEND = 0 disabled (default)	$0 \le (NT_{clk} - t_{loop} - t_{fix0}) \le 7$		ns	7
16	DLL lock range with DLL_EXTEND = 1 enabled	$0 \le (NT_{clk} - T_{clk}/2 - t_{loop} - t_{fix0}) \le 7$		ns	7

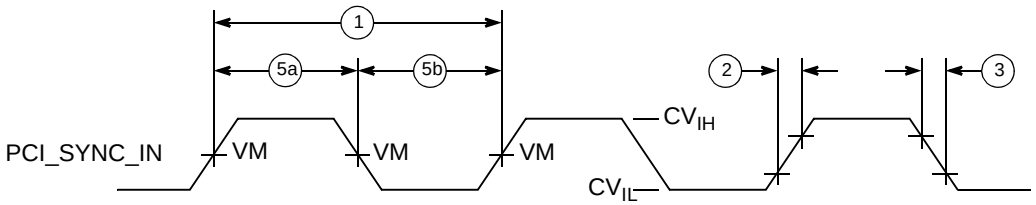
Table 7. Clock AC Timing Specifications (continued)

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ±0.3 V

Num	Characteristic and Condition [1]	Min	Max	Unit	Notes
17	Frequency of operation (OSC_IN)	25	66	MHz	
18	OSC_IN cycle time	40	15	ns	
19	OSC_IN rise and fall times	—	5	ns	5
20	OSC_IN duty cycle measured at 1.4 V	40	60	%	
21	OSC_IN frequency stability	—	100	ppm	
22	OSC_IN V_{IH} (loaded)	2.0		V	
23	OSC_IN V_{IL} (loaded)		0.8	V	

Notes:
1. These specifications are for the default driver strengths indicated in Table 4.
2. Rise and fall times for the PCI_SYNC_IN input are measured from 0.4 to 2.4 V.
3. Specification value at maximum frequency of operation.
4. Relock time is guaranteed by design and characterization. Relock time is not tested.
5. Rise and fall times for the OSC_IN input is guaranteed by design and characterization. OSC_IN input rise and fall times are not tested.
6. Relock timing is guaranteed by design. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and PCI_SYNC_IN are reached during the reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRST_CPU/HRST_CTRL must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the reset sequence.
7. DLL_EXTEND is bit 7 of the PMC2 register <72>. N is a non-zero integer (1 or 2). T_{clk} is the period of one SDRAM_SYNC_OUT clock cycle in ns. t_{loop} is the propagation delay of the DLL synchronization feedback loop (PC board runner) from SDRAM_SYNC_OUT to SDRAM_SYNC_IN in ns; 6.25 inches of loop length (unloaded PC board runner) corresponds to approximately 1 ns of delay. t_{fix0} is a fixed delay inherent in the design when the DLL is at tap point 0 and the DLL is contributing no delay; t_{fix0} equals approximately 3 ns. See Figure 5 for DLL3 locking ranges.
8. Pin-to-pin skew includes quantifying the additional amount of clock skew (or jitter) from the DLL besides any intentional skew added to the clocking signals from the variable length DLL synchronization feedback loop, that is, the amount of variance between the internal sys_logic_clk and the SDRAM_SYNC_IN signal after the DLL is locked. While pin to pin skew between SDRAM_CLKs can be measured, the relationship between the internal sys_logic_clk and the external SDRAM_SYNC_IN cannot be measured and is guaranteed by design.

Figure 4 shows the PCI_SYNC_IN input clock timing diagram and Figure 5 shows the DLL locking range loop delay versus frequency of operation.



VM = Midpoint Voltage (1.4 V)

Figure 4. PCI_SYNC_IN Input Clock Timing Diagram

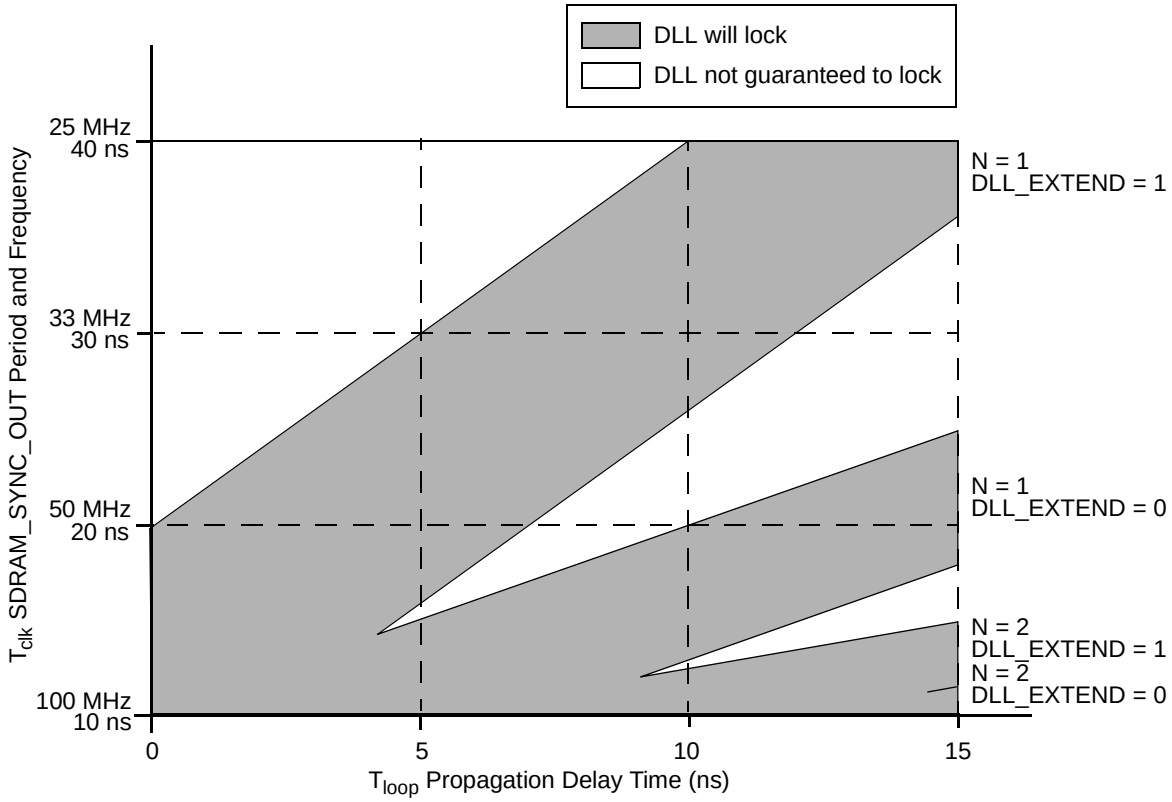


Figure 5. DLL Locking Range Loop Delay vs. Frequency of Operation

1.4.2.3 Input AC Timing Specifications

Table 8 provides the input AC timing specifications. See Figure 6 and Figure 7.

Table 8. Input AC Timing Specifications

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ±0.3 V

Num	Characteristic	Min	Max	Unit	Notes
10a	PCI input signals valid to PCI_SYNC_IN (input setup)	2.0	—	ns	2, 3
10b1	Memory control and data input signals in flow through mode valid to SDRAM_SYNC_IN (input setup)	3.0	—	ns	1, 3
10b2	Memory control and data input signals in registered/in-line mode valid to SDRAM_SYNC_IN (input setup)	2.5	—	ns	1, 3
10b3	Memory control and data signals accessing non-DRAM valid to SDRAM_SYNC_IN (input setup)	3.0	—	ns	1, 3
10c	EPIC, miscellaneous debug input signals valid to SDRAM_SYNC_IN (input setup)	3.0	—	ns	1, 3
10d	I^2C input signals valid to SDRAM_SYNC_IN (input setup)	2.0	—	ns	1, 3
10e	Mode select Inputs Valid to $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ (input setup)	$9 \times t_{CLK}$	—	ns	1, 3–5

Table 8. Input AC Timing Specifications (continued)

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ±0.3 V

Num	Characteristic	Min	Max	Unit	Notes
11a	PCI_SYNC_IN (SDRAM_SYNC_IN) to inputs invalid (input hold)	1.0	—	ns	1, 2, 3
11b	$\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ to mode select inputs invalid (input hold)	0	—	ns	1, 3, 5

Notes:
1. All memory and related interface input signal specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the memory bus clock, SDRAM_SYNC_IN. SDRAM_SYNC_IN is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 6.
2. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels. See Figure 7.
3. Input timings are measured at the pin.
4. t_{CLK} is the time of one SDRAM_SYNC_IN clock cycle.
5. All mode select input signals specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ signal. See Figure 8.

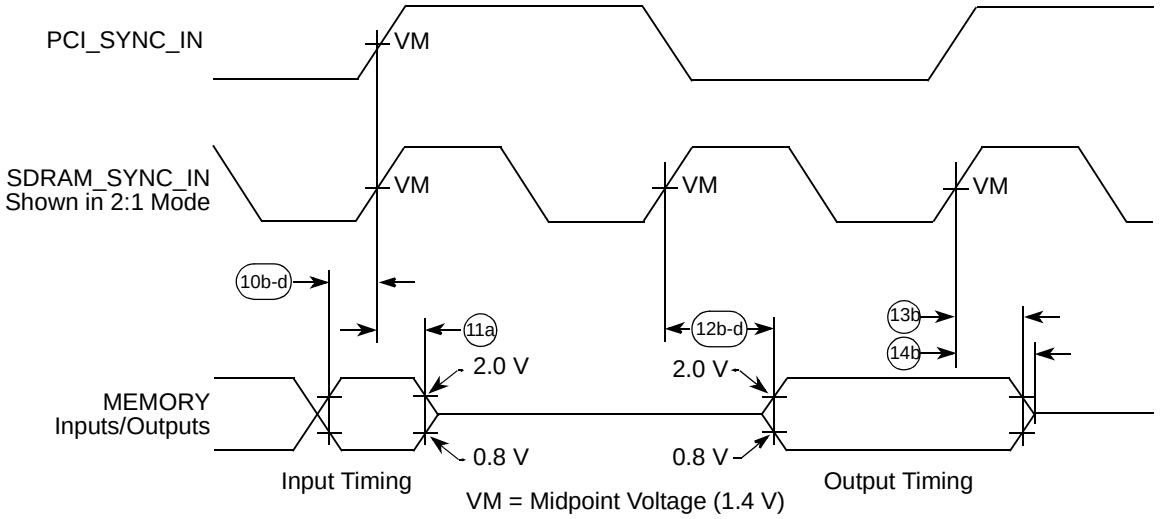


Figure 6. Input-Output Timing Diagram Referenced to SDRAM_SYNC_IN

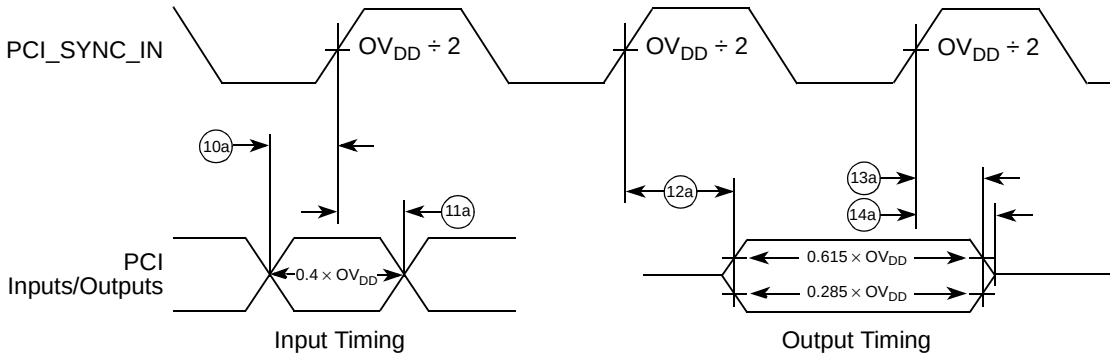


Figure 7. Input-Output Timing Diagram Referenced to PCI_SYNC_IN

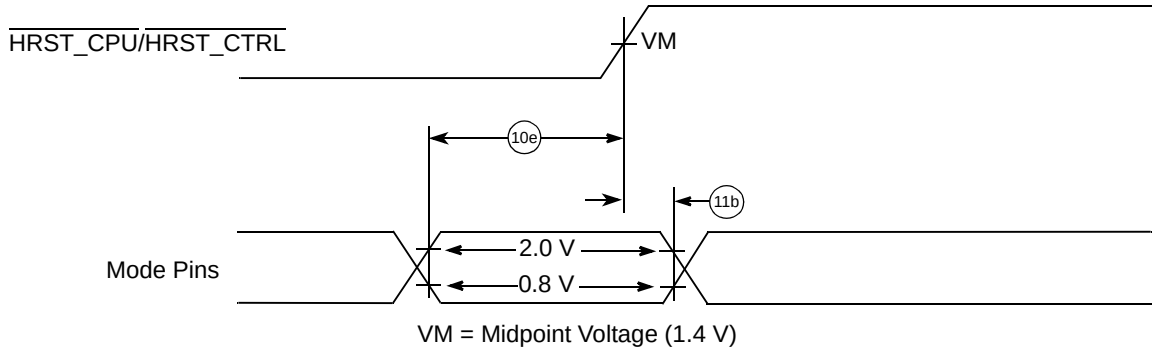


Figure 8. Input Timing Diagram for Mode Select Signals

1.4.2.4 Output AC Timing Specification

Table 9 provides the processor bus AC timing specifications for the MPC8240. See Figure 6 and Figure 7.

Table 9. Output AC Timing Specifications

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ±0.3 V

Num	Characteristic [3, 6]	Min	Max	Unit	Notes
12a	PCI_SYNC_IN to output valid, 66 MHz PCI, with $\overline{\text{MCP}}$ in the default logic 1 state and CKE pulled down to logic 0 state (see Figure 10)	—	6.0	ns	2, 4
	PCI_SYNC_IN to output valid, 33 MHz PCI, with $\overline{\text{MCP}}$ and CKE in the default logic 1 state (see Figure 10)	—	8.0	ns	2, 4
12b1	SDRAM_SYNC_IN to output valid (for memory control address and data signals accessing DRAM in flow-through mode)	—	7.0	ns	1
12b2	SDRAM_SYNC_IN to output valid (for memory control address and data signals accessing DRAM in registered mode)	—	6.0	ns	1
12b3	SDRAM_SYNC_IN to output valid (for memory control address and data signals accessing non-DRAM)	—	7.0	ns	1
12c	SDRAM_SYNC_IN to output valid (for all others)	—	7.0	ns	1
12d	SDRAM_SYNC_IN to output valid (for I^2C)	—	5.0	ns	1
13a	Output hold, 66 MHz PCI, with $\overline{\text{MCP}}$ in the default logic 1 state and CKE pulled down to logic 0 state (see Figure 10)	1.0	—	ns	2, 4, 5
	Output hold, 33 MHz PCI, with $\overline{\text{MCP}}$ and CKE in the default logic 1 state (see Figure 10)	2.0	—	ns	2, 4, 5
13b	Output hold (all others)	0	—	ns	1
14a	PCI_SYNC_IN to output high impedance (for PCI)	—	14.0	ns	2, 4

Table 9. Output AC Timing Specifications (continued)

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ±0.3 V

Num	Characteristic [3, 6]	Min	Max	Unit	Notes
14b	SDRAM_SYNC_IN to output high impedance (for all others)	—	4.0	ns	1

Notes:
1. All memory and related interface output signal specifications are specified from the VM = 1.4 V of the rising edge of the memory bus clock, SDRAM_SYNC_IN to the TTL level (0.8 or 2.0 V) of the signal in question. SDRAM_SYNC_IN is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 6.
2. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.285 \times OV_{DD}$ or $0.615 \times OV_{DD}$ of the signal in question for 3.3 V PCI signaling levels. See Figure 7.
3. All output timings assume a purely resistive 50-Ω load (see Figure 9). Output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
4. PCI bused signals are composed of the following signals: $\overline{\text{LOCK}}$, $\overline{\text{IRDY}}$, $\overline{\text{C/BE}}$[0:3], PAR, $\overline{\text{TRDY}}$, $\overline{\text{FRAME}}$, $\overline{\text{STOP}}$, $\overline{\text{DEVSEL}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, AD[0:31], $\overline{\text{REQ}}$[4:0], $\overline{\text{GNT}}$[4:0], $\overline{\text{IDSEL}}$, and $\overline{\text{INTA}}$.
5. PCI hold times can be varied; see Section 1.4.2.4.1, “PCI Signal Output Hold Timing,” for information on programmable PCI output hold times. The values shown for item 13a are for PCI compliance.
6. These specifications are for the default driver strengths indicated in Table 4.

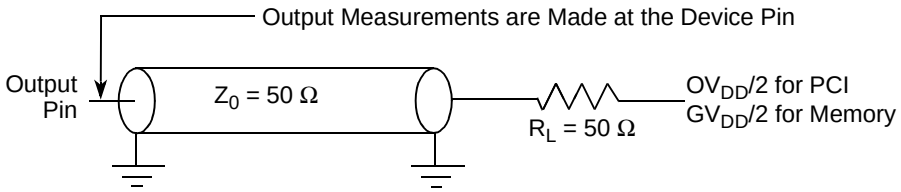


Figure 9. AC Test Load for the MPC8240

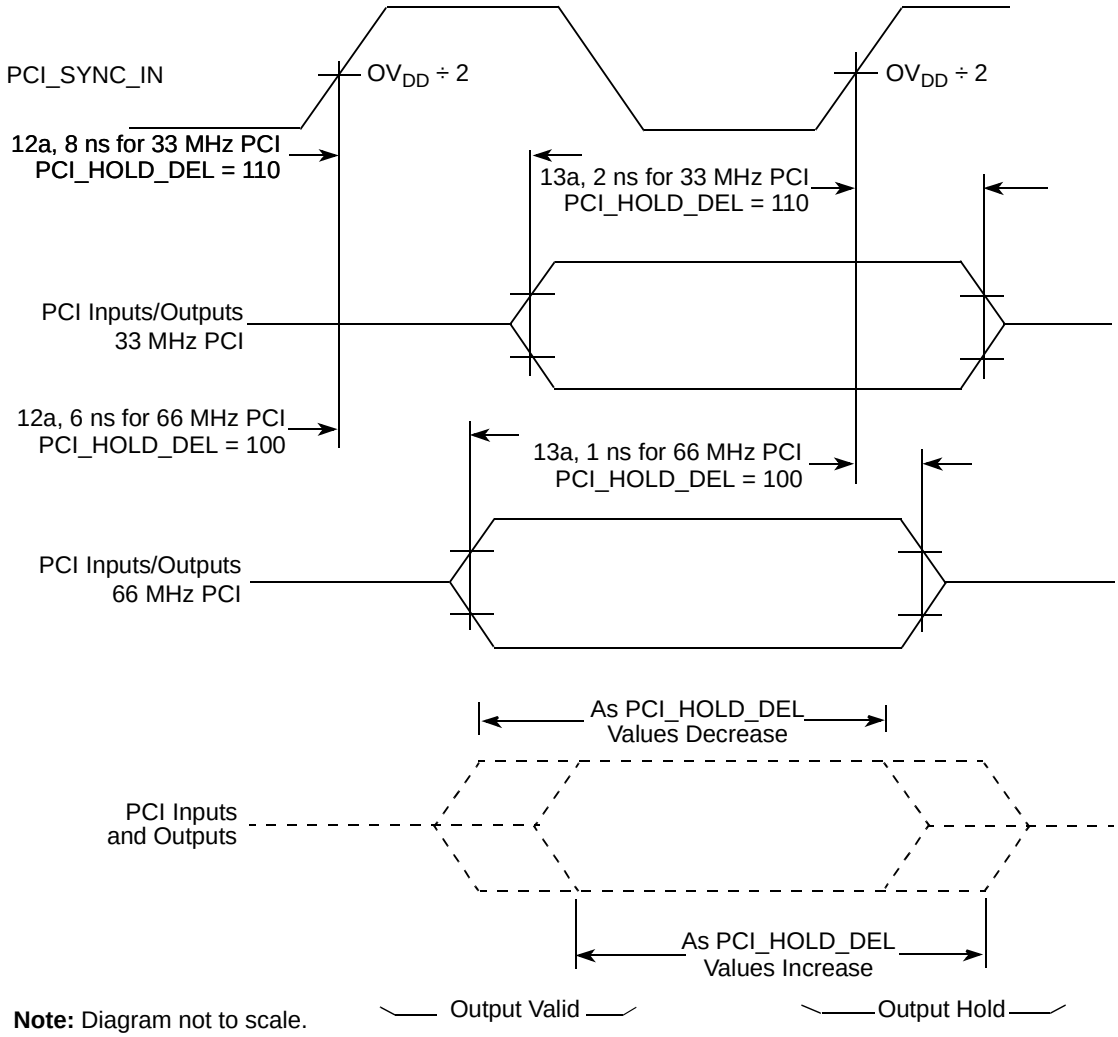
1.4.2.4.1 PCI Signal Output Hold Timing

In order to meet minimum output hold specifications relative to PCI_SYNC_IN for both 33 and 66 MHz PCI systems, the MPC8240 has a programmable output hold delay for PCI signals. The initial value of the output hold delay is determined by the values on the $\overline{\text{MCP}}$ and CKE reset configuration signals. Further output hold delay values are available by programming the PCI_HOLD_DEL value of the PMCR2 configuration register.

Table 10 describes the bit values for the PCI_HOLD_DEL values in PMCR2.

Table 10. Power Management Configuration Register 2 at 0x72

Bit	Name	Reset Value	Description
6–4	PCI_HOLD_DEL	xx0	PCI output hold delay values relative to PCI_SYNC_IN. The initial values of bits 6 and 5 are determined by the reset configuration pins MCP and CKE, respectively. As these two pins have internal pull-up resistors, the default value after reset is 0b110. While the minimum hold times are guaranteed at shown values, changes in the actual hold time can be made by incrementing or decrementing the value in these bit fields of this register via software or hardware configuration. The increment is in approximately 400 picosecond steps. Lowering the value in the 3-bit field decreases the amount of output hold available. 000 For Silicon Rev. 1.0/1.1: 66 MHz PCI. Pull-down CKE configuration pin with a 2-kΩ or less value resistor. This setting guarantees the minimum output hold, item 13a, and the maximum output valid, item 12a, times as specified in Figure 9 are met for a 66 MHz PCI system. See Figure 10. 001 010 011 100 For Silicon Rev. 1.2/1.3: 66 MHz PCI. Pull-down CKE configuration pin with a 2-kΩ or less value resistor. This setting guarantees the minimum output hold, item 13a, and the maximum output valid, item 12a, times as specified in Figure 9 are met for a 66 MHz PCI system. See Figure 10. For Silicon Rev. 1.0/1.1: 33 MHz PCI. This setting guarantees the minimum output hold, item 13a, and the maximum output valid, item 12a, times as specified in Figure 9 are met for a 33 MHz PCI system. See Figure 10. 101 110 For Silicon Rev. 1.2/1.3: 33 MHz PCI. This setting guarantees the minimum output hold, item 13a, and the maximum output valid, item 12a, times as specified in Figure 9 are met for a 33 MHz PCI system. See Figure 10. (Default if reset configuration pins left unconnected.) For Silicon Rev. 1.0/1.1: Default if reset configuration pins left unconnected. 111



Note: Diagram not to scale.

Figure 10. PCI_HOLD_DEL Affect on Output Valid and Hold Time

1.4.2.5 I^2C AC Timing Specifications

Table 11 provides the I^2C input AC timing specifications for the MPC8240.

Table 11. I^2C Input AC Timing Specifications

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ±0.3 V

Num	Characteristic	Min	Max	Unit	Notes
1	Start condition hold time	4.0	—	CLKs	1,2
2	Clock low period (the time before the MPC8240 will drive SCL low as a transmitting slave after detecting SCL low as driven by an external master)	$8.0 + (16 \times 2^{FDR[4:2]}) \times (5 – 4(\{FDR[5],FDR[1]\} == b'10) – 3(\{FDR[5],FDR[1]\} == b'11) – 2(\{FDR[5],FDR[1]\} == b'00) – 1(\{FDR[5],FDR[1]\} == b'01))$	—	CLKs	1, 2, 4, 5
3	SCL/SDA rise time (from 0.5 to 2.4 V)	—	1	ms	
4	Data hold time	0	—	ns	2
5	SCL/SDA fall time (from 2.4 to 0.5 V)	—	1	ms	
6	Clock high period (time needed to either receive a data bit or generate a START or STOP)	5.0	—	CLKs	1, 2, 5
7	Data setup time	3.0	—	ns	3
8	Start condition setup time (for repeated start condition only)	4.0	—	CLKs	1, 2
9	Stop condition setup time	4.0	—	CLKs	1, 2

Notes:
1. Units for these specifications are in SDRAM_CLK units.
2. The actual values depend on the setting of the digital filter frequency sampling rate (DFFSR) bits in the frequency divider register I2CFDR. Therefore, the noted timings in this table are all relative to qualified signals. The qualified SCL and SDA are delayed signals from what is seen in real time on the I^2C bus. The qualified SCL, SDA signals are delayed by the SDRAM_CLK clock times DFFSR times 2 plus 1 SDRAM_CLK clock. The resulting delay value is added to the value in the table (where this note is referenced). See Figure 11.
3. Timing is relative to the sampling clock (not SCL).
4. FDR[x] refers to the frequency divider register I2CFDR bit *n*.
5. Input clock low and high periods in combination with the FDR value in the frequency divider register (I2CFDR) determine the maximum I^2C input frequency. See Table 12.

Table 12 provides the I^2C frequency divider register (I2CFDR) information for the MPC8240.

Table 12. MPC8240 Maximum I^2C Input Frequency

FDR Hex [2]	Divider [2] (Dec)	Max I^2C Input Frequency [1]		
		SDRAM_CLK @ 33 MHz	SDRAM_CLK @ 50 MHz	SDRAM_CLK @ 100 MHz
20, 21	160, 192	1.13 MHz	1.72 MHz	3.44 MHz
22, 23, 24, 25	224, 256, 320, 384	733	1.11 MHz	2.22 MHz
0, 1	288, 320	540	819	1.63 MHz
2, 3, 26, 27, 28, 29	384, 448, 480, 512, 640, 768	428	649	1.29 MHz
4, 5	576, 640	302	458	917
6, 7, 2A, 2B, 2C, 2D	768, 896, 960, 1024, 1280, 1536	234	354	709
8, 9	1152, 1280	160	243	487
A, B, 2E, 2F, 30, 31	1536, 1792, 1920, 2048, 2560, 3072	122	185	371
C, D	2304, 2560	83	125	251
E, F, 32, 33, 34, 35	3072, 3584, 3840, 4096, 5120, 6144	62	95	190
10, 11	4608, 5120	42	64	128
12, 13, 36, 37, 38, 39	6144, 7168, 7680, 8192, 10240, 12288	31	48	96
14, 15	9216, 10240	21	32	64
16, 17, 3A, 3B, 3C, 3D	12288, 14336, 15360, 16384, 20480, 24576	16	24	48
18, 19	18432, 20480	10	16	32
1A, 1B, 3E, 3F	24576, 28672, 30720, 32768	8	12	24
1C, 1D	36864, 40960	5	8	16
1E, 1F	49152, 61440	4	6	12

Notes:
1. Values are in kHz, unless otherwise specified.
2. FDR hex and divider (Dec) values are listed in corresponding order.
3. Multiple divider (Dec) values will generate the same input frequency, but each divider (Dec) value will generate a unique output frequency as shown in Table 13.

Table 13 provides the I^2C output AC timing specifications for the MPC8240.

Table 13. I^2C Output AC Timing Specifications

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ±0.3 V

Num	Characteristic	Min	Max	Unit	Notes
1	Start condition hold time	(FDR[5] == 0) × (D_{FDR}/16)/2N + (FDR[5] == 1) × (D_{FDR}/16)/2M	—	CLKs	1, 2, 5
2	Clock low period	D_{FDR}/2	—	CLKs	1, 2, 5
3	SCL/SDA rise time (from 0.5 to 2.4 V)	—	—	ms	3
4	Data hold time	8.0 + (16 × $2^{FDR[4:2]}$) × (5 – 4({FDR[5],FDR[1]} == b'10) – 3({FDR[5],FDR[1]} == b'11) – 2({FDR[5],FDR[1]} == b'00) – 1({FDR[5],FDR[1]} == b'01))	—	CLKs	1, 2, 5
5	SCL/SDA fall time (from 2.4 to 0.5 V)	—	< 5	ns	4
6	Clock high time	D_{FDR}/2	—	CLKs	1, 2, 5
7	Data setup time (MPC8240 as a master only)	(D_{FDR}/2) – (Output data hold time)	—	CLKs	1, 5
8	Start condition setup time (for repeated start condition only)	D_{FDR} + (Output start condition hold time)	—	CLKs	1, 2, 5
9	Stop condition setup time	4.0	—	CLKs	1, 2

Notes:
1. Units for these specifications are in SDRAM_CLK units.
2. The actual values depend on the setting of the digital filter frequency sampling rate (DFFSR) bits in the frequency divider register I2CFDR. Therefore, the noted timings in this table are all relative to qualified signals. The qualified SCL and SDA are delayed signals from what is seen in real time on the I^2C bus. The qualified SCL, SDA signals are delayed by the SDRAM_CLK clock times DFFSR times 2 plus 1 SDRAM_CLK clock. The resulting delay value is added to the value in the table (where this note is referenced). See Figure 12.
3. Since SCL and SDA are open-drain type outputs, which the MPC8240 can only drive low, the time required for SCL or SDA to reach a high level depends on external signal capacitance and pull-up resistor values.
4. Specified at a nominal 50 pF load.
5. D_{FDR} is the decimal divider number indexed by FDR[5:0] value. Refer to the I^2C Interface chapter's serial bit clock frequency divider selections table. FDR[*n*] refers to the frequency divider register I2CFDR bit *n*. N is equal to a variable number that would make the result of the divide (data hold time value) equal to a number less than 16. M is equal to a variable number that would make the result of the divide (data hold time value) equal to a number less than 9.

Figure 11 through Figure 14 show I^2C timings.

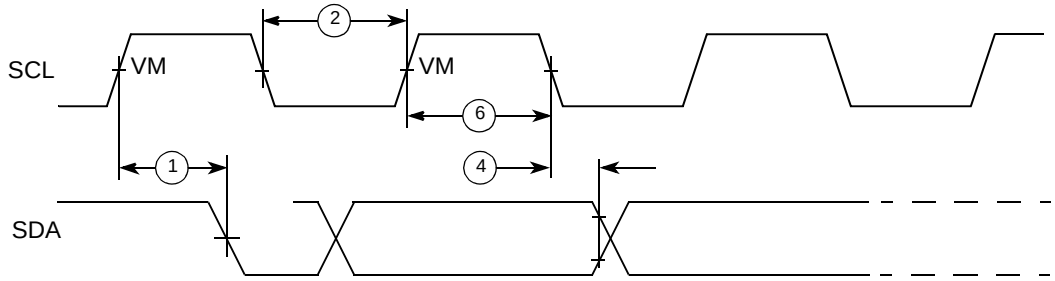


Figure 11. I^2C Timing Diagram I

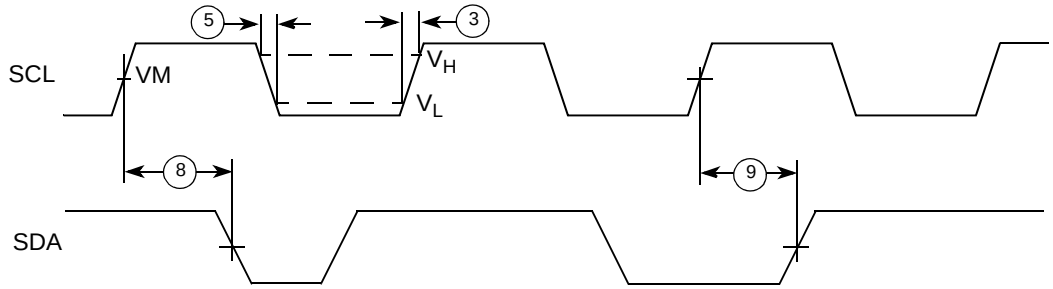
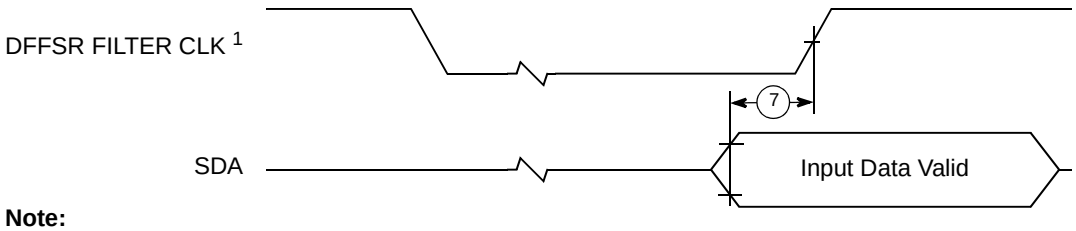
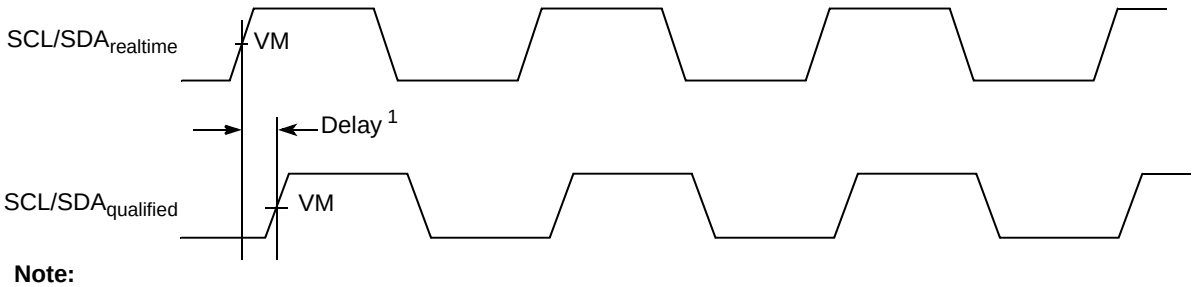


Figure 12. I^2C Timing Diagram II



Note:
1. DFFSR filter clock is the SDRAM_CLK clock times DFFSR value.

Figure 13. I^2C Timing Diagram III



Note:
1. The delay is the local memory clock times DFFSR times 2 plus 1 local memory clock.

Figure 14. I^2C Timing Diagram IV (Qualified Signal)

1.4.2.6 EPIC Serial Interrupt Mode AC Timing Specifications

Table 14 provides the EPIC serial interrupt mode AC timing specifications for the MPC8240.

Table 14. EPIC Serial Interrupt Mode AC Timing Specifications

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ±0.3 V

Num	Characteristic	Min	Max	Unit	Notes
1	S_CLK frequency	1/14 SDRAM_SYNC_IN	1/2 SDRAM_SYNC_IN	MHz	1
2	S_CLK duty cycle	40	60	%	
3	S_CLK output valid time	—	6	ns	
4	Output hold time	0	—	ns	
5	$\overline{\text{S\_FRAME}}$, S_RST output valid time	—	1 sys_logic_clk period + 6	ns	2
6	S_INT input setup time to S_CLK	1 sys_logic_clk period + 2	—	ns	2
7	S_INT inputs invalid (hold time) to S_CLK	—	0	ns	2

Notes:
1. See the *MPC8240 Integrated Processor User's Manual*, for a description of the EPIC interrupt control register (EICR) describing S_CLK frequency programming.
2. S_RST, $\overline{\text{S\_FRAME}}$, and S_INT shown in Figure 15. Figure 16 depict timing relationships to sys_logic_clk and S_CLK and do not describe functional relationships between S_RST, $\overline{\text{S\_FRAME}}$, and S_INT. See the *MPC8240 Integrated Processor User's Manual*, for a complete description of the functional relationships between these signals.
3. The sys_logic_clk waveform is the clocking signal of the internal peripheral logic from the output of the peripheral logic PLL; sys_logic_clk is the same as SDRAM_SYNC_IN when the SDRAM_SYNC_OUT to SDRAM_SYNC_IN feedback loop is implemented and the DLL is locked. See the *MPC8240 Integrated Processor User's Manual*, for a complete clocking description.

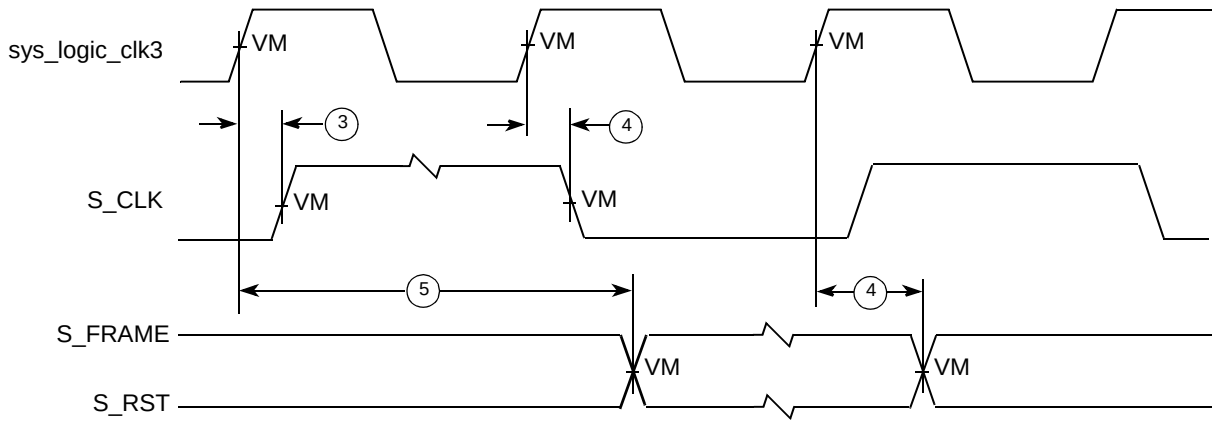


Figure 15. EPIC Serial Interrupt Mode Output Timing Diagram

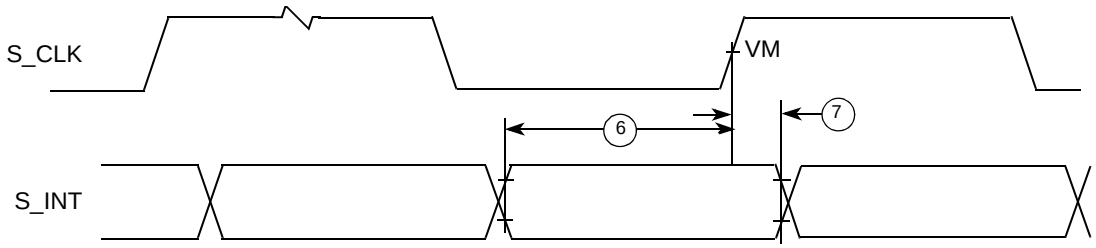


Figure 16. EPIC Serial Interrupt Mode Input Timing Diagram

1.4.2.7 IEEE 1149.1 (JTAG) AC Timing Specifications

Table 15 provides the JTAG AC timing specifications for the MPC8240 while in the JTAG operating mode.

Table 15. JTAG AC Timing Specification (Independent of PCI_SYNC_IN)

At recommended operating conditions (see Table 2) with LV_{DD} = 3.3 V ±0.3 V

Num	Characteristic [4]	Min	Max	Unit	Notes
	TCK frequency of operation	0	25	MHz	
1	TCK cycle time	40	—	ns	
2	TCK clock pulse width measured at 1.5 V	20	—	ns	
3	TCK rise and fall times	0	3	ns	
4	$\overline{\text{TRST}}$_ setup time to TCK falling edge	10	—	ns	1
5	$\overline{\text{TRST}}$_ assert time	10	—	ns	
6	Input data setup time	5	—	ns	2
7	Input data hold time	15	—	ns	2
8	TCK to output data valid	0	30	ns	3
9	TCK to output high impedance	0	30	ns	3
10	TMS, TDI data setup time	5	—	ns	
11	TMS, TDI data hold time	15	—	ns	
12	TCK to TDO data valid	0	15	ns	
13	TCK to TDO high impedance	0	15	ns	

Notes:
1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2. Non-test (other than TDI and TMS) signal input timing with respect to TCK.
3. Non-test (other than TDO) signal output timing with respect to TCK.
4. Timings are independent of the system clock (PCI_SYNC_IN).

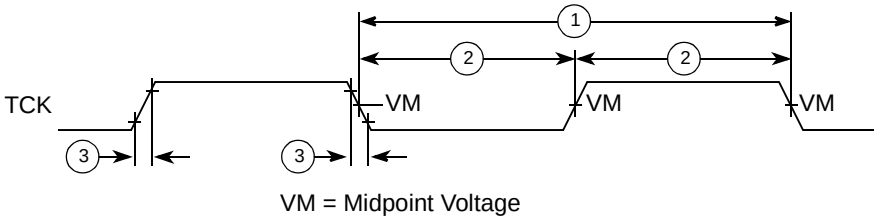


Figure 17. JTAG Clock Input Timing Diagram

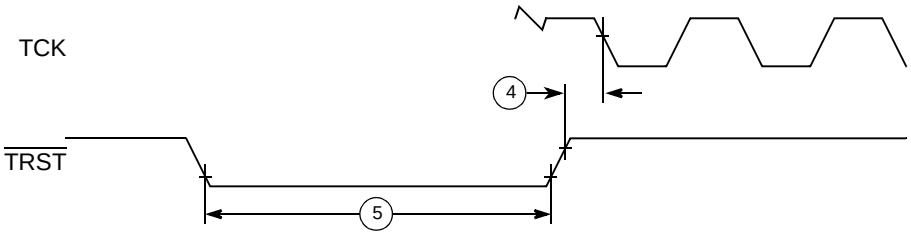


Figure 18. JTAG $\overline{\text{TRST}}$ Timing Diagram

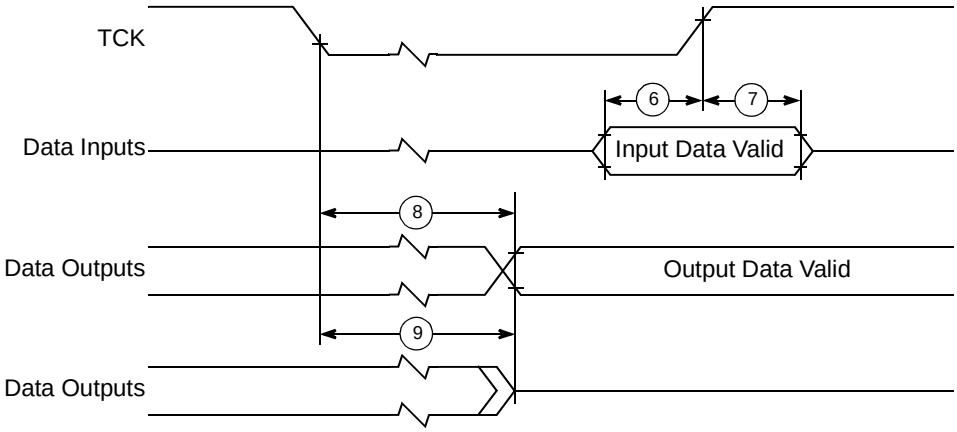


Figure 19. JTAG Boundary Scan Timing Diagram

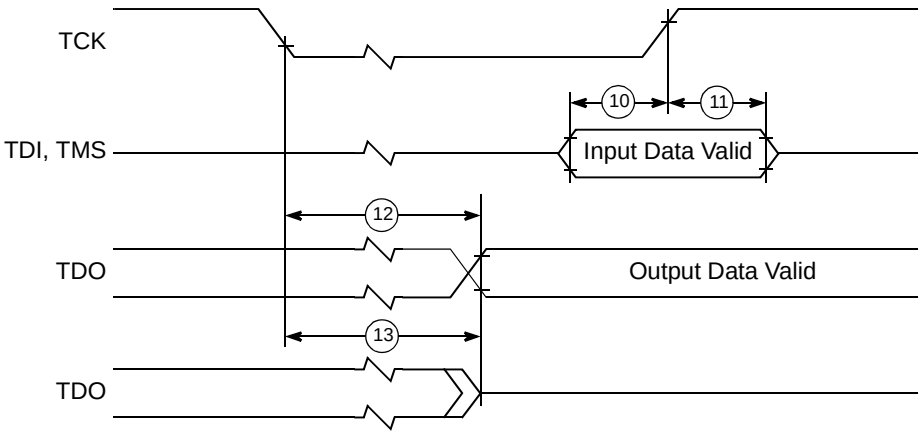


Figure 20. Test Access Port Timing Diagram

1.4.3 Thermal Characteristics

Table 16 provides the package thermal characteristics for the MPC8240.

Table 16. Package Thermal Characteristics

Characteristic [1]	Symbol	Value	Unit
Die junction-to-case thermal resistance	θ_{JC}	1.8	°C/W
Die junction-to-board thermal resistance	θ_{JB}	4.8	°C/W

Note:
1. Refer to Section 1.7, “System Design Information,” for more details about thermal management.

1.5 Package Description

The following sections provide the package parameters and mechanical dimensions for the MPC8240, 352 TBGA package.

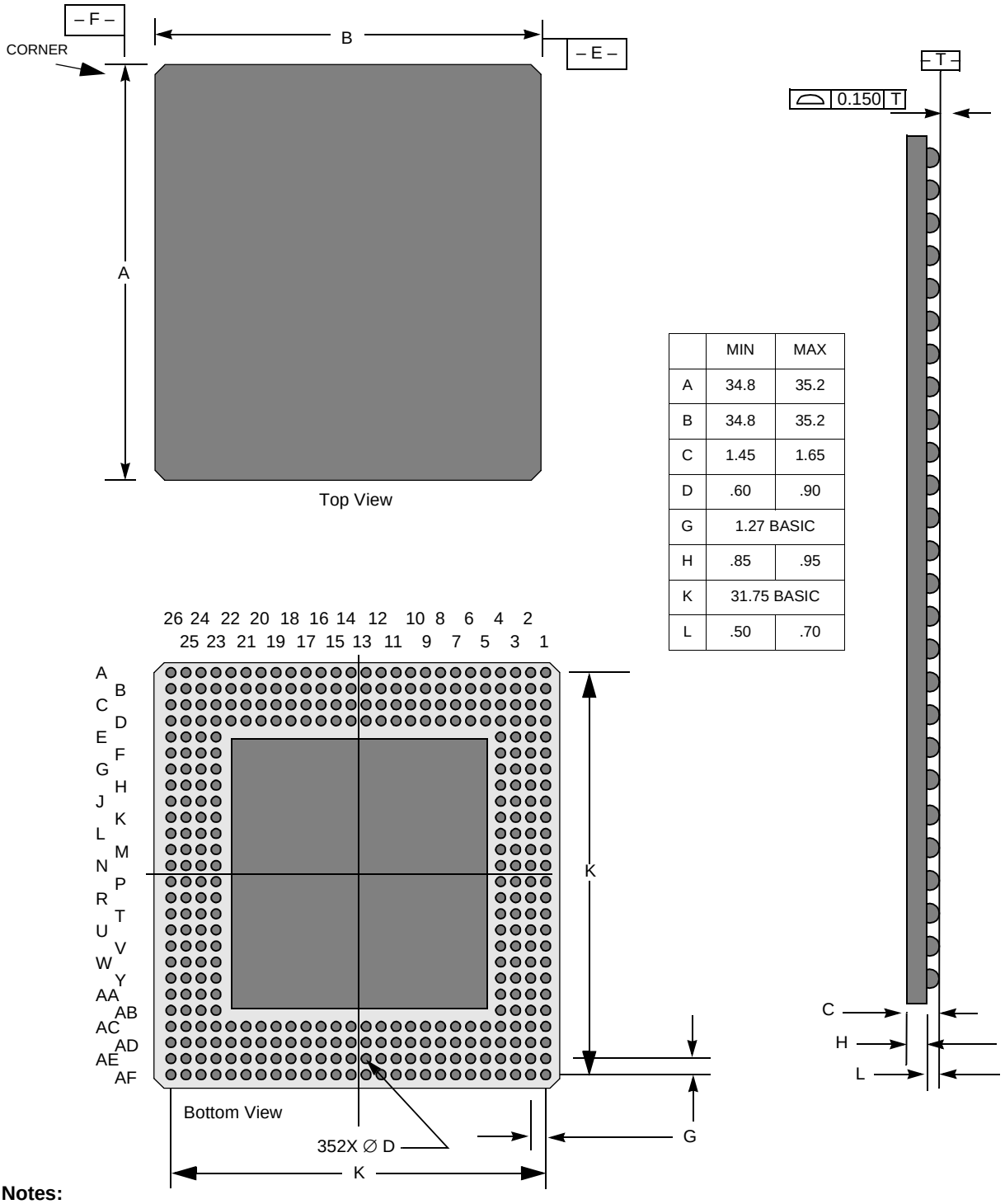
1.5.1 Package Parameters

The MPC8240 uses a 35 mm × 35 mm, cavity down, 352 pin tape ball grid array (TBGA) package. The package parameters are as provided in the following list.

Package outline	35 mm × 35 mm
Interconnects	352
Pitch	1.27 mm
Solder balls	62 Sn/36 Pb/2 Ag
Solder ball diameter	0.75 mm
Maximum module height	1.65 mm
Co-planarity specification	0.15 mm
Maximum force	6.0 lbs. total, uniformly distributed over package (8 grams/ball)

1.5.2 Mechanical Dimensions

Figure 21 provides the mechanical dimensions, top surface, side profile, and pinout for the MPC8240, 352 TBGA package.



	MIN	MAX
A	34.8	35.2
B	34.8	35.2
C	1.45	1.65
D	.60	.90
G	1.27 BASIC	
H	.85	.95
K	31.75 BASIC	
L	.50	.70

Notes:
1. Drawing not to scale.
2. All measurements are in millimeters (mm).

Figure 21. Mechanical Dimensions and Pinout Assignments for the MPC8240, 352 TBGA

1.5.3 Pinout Listings

Table 17 provides the pinout listing for the MPC8240, 352 TBGA package.

Table 17. MPC8240 Pinout Listing

Signal Name	Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
PCI Interface Signals					
$\overline{\text{C/BE}}$[3:0]	P25 K23 F23 A25	I/O	OV_{DD}	DRV_PCI	6, 15
$\overline{\text{DEVSEL}}$	H26	I/O	OV_{DD}	DRV_PCI	8, 15
$\overline{\text{FRAME}}$	J24	I/O	OV_{DD}	DRV_PCI	8, 15
$\overline{\text{IRDY}}$	K25	I/O	OV_{DD}	DRV_PCI	8, 15
$\overline{\text{LOCK}}$	J26	Input	OV_{DD}	—	8
AD[31:0]	V25 U25 U26 U24 U23 T25 T26 R25 R26 N26 N25 N23 M26 M25 L25 L26 F24 E26 E25 E23 D26 D25 C26 A26 B26 A24 B24 D19 B23 B22 D22 C22	I/O	OV_{DD}	DRV_PCI	6, 15
PAR	G25	I/O	OV_{DD}	DRV_PCI	15
$\overline{\text{GNT}}$[3:0]	W25 W24 W23 V26	Output	OV_{DD}	DRV_PCI	6, 15
$\overline{\text{GNT4}}$/DA5	W26	Output	OV_{DD}	DRV_PCI	7, 15
$\overline{\text{REQ}}$[3:0]	Y25 AA26 AA25 AB26	Input	OV_{DD}	—	6, 12
$\overline{\text{REQ4}}$/DA4	Y26	I/O	OV_{DD}	—	12
$\overline{\text{PERR}}$	G26	I/O	OV_{DD}	DRV_PCI	8, 15, 18
$\overline{\text{SERR}}$	F26	I/O	OV_{DD}	DRV_PCI	8, 15, 16
$\overline{\text{STOP}}$	H25	I/O	OV_{DD}	DRV_PCI	8, 15
$\overline{\text{TRDY}}$	K26	I/O	OV_{DD}	DRV_PCI	8, 15
$\overline{\text{INTA}}$	AC26	Output	OV_{DD}	DRV_PCI	8, 15, 16
IDSEL	P26	Input	OV_{DD}	—	
Memory Interface Signals					
MDL[0:31]	AD17 AE17 AE15 AF15 AC14 AE13 AF13 AF12 AF11 AF10 AF9 AD8 AF8 AF7 AF6 AE5 B1 A1 A3 A4 A5 A6 A7 D7 A8 B8 A10 D10 A12 B11 B12 A14	I/O	GV_{DD}	DRV_MEM_DATA	5, 6, 13
MDH[0:31]	AC17 AF16 AE16 AE14 AF14 AC13 AE12 AE11 AE10 AE9 AE8 AC7 AE7 AE6 AF5 AC5 E4 A2 B3 D4 B4 B5 D6 C6 B7 C9 A9 B10 A11 A13 B13 A15	I/O	GV_{DD}	DRV_MEM_DATA	6, 13

Table 17. MPC8240 Pinout Listing (continued)

Signal Name	Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
$\overline{\text{CAS}}$/DQM[0:7]	AB1 AB2 K3 K2 AC1 AC2 K1 J1	Output	GV_{DD}	DRV_MEM_ADDR	6
$\overline{\text{RAS}}/\overline{\text{CS}}$[0:7]	Y4 AA3 AA4 AC4 M2 L2 M1 L1	Output	GV_{DD}	DRV_MEM_ADDR	6
$\overline{\text{FOE}}$	H1	I/O	GV_{DD}	DRV_MEM_ADDR	3, 4
$\overline{\text{RCS0}}$	N4	I/O	GV_{DD}	DRV_MEM_ADDR	3, 4
$\overline{\text{RCS1}}$	N2	Output	GV_{DD}	DRV_MEM_ADDR	
SDMA[11:0]	N1 R1 R2 T1 T2 U4 U2 U1 V1 V3 W1 W2	Output	GV_{DD}	DRV_MEM_ADDR	6, 14
SDMA12/SDBA1	P1	Output	GV_{DD}	DRV_MEM_ADDR	14
SDBA0	P2	Output	GV_{DD}	DRV_MEM_ADDR	
PAR[0:7]	AF3 AE3 G4 E2 AE4 AF4 D2 C2	I/O	GV_{DD}	DRV_MEM_DATA	6, 13, 14
$\overline{\text{SDRAS}}$	AD1	Output	GV_{DD}	DRV_MEM_ADDR	3
$\overline{\text{SDCAS}}$	AD2	Output	GV_{DD}	DRV_MEM_ADDR	3
CKE	H2	Output	GV_{DD}	DRV_MEM_ADDR	3, 4
$\overline{\text{WE}}$	AA1	Output	GV_{DD}	DRV_MEM_ADDR	
$\overline{\text{AS}}$	Y1	Output	GV_{DD}	DRV_MEM_ADDR	3, 4
EPIC Control Signals					
IRQ_0/S_INT	C19	Input	OV_{DD}	—	19
IRQ_1/S_CLK	B21	I/O	OV_{DD}	DRV_PCI	19
IRQ_2/S_RST	AC22	I/O	OV_{DD}	DRV_PCI	19
IRQ_3/$\overline{\text{S\_FRAME}}$	AE24	I/O	OV_{DD}	DRV_PCI	19
IRQ_4/$\overline{\text{L\_INT}}$	A23	I/O	OV_{DD}	DRV_PCI	19
I^2C Control Signals					
SDA	AE20	I/O	OV_{DD}	DRV_STD	10, 16
SCL	AF21	I/O	OV_{DD}	DRV_STD	10, 16
Clock Out Signals					
PCI_CLK [0:3]	AC25 AB25 AE26 AF25	Output	GV_{DD}	DRV_PCI_CLK	6
PCI_CLK4/DA3	AF26	Output	GV_{DD}	DRV_PCI_CLK	
PCI_SYNC_OUT	AD25	Output	GV_{DD}	DRV_PCI_CLK	
PCI_SYNC_IN	AB23	Input	GV_{DD}	—	
SDRAM_CLK [0:3]	D1 G1 G2 E1	Output	GV_{DD}	DRV_MEM_ADDR	6
SDRAM_SYNC_OUT	C1	Output	GV_{DD}	DRV_MEM_ADDR	

Table 17. MPC8240 Pinout Listing (continued)

Signal Name	Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
SDRAM_SYNC_IN	H3	Input	GV_{DD}	—	
CKO/DA1	B15	Output	OV_{DD}	DRV_STD	
OSC_IN	AD21	Input	OV_{DD}	—	19
Miscellaneous Signals					
$\overline{\text{HRST\_CTRL}}$	A20	Input	OV_{DD}	—	
$\overline{\text{HRST\_CPU}}$	A19	Input	OV_{DD}	—	
$\overline{\text{MCP}}$	A17	Output	OV_{DD}	DRV_STD	3, 4, 17
NMI	D16	Input	OV_{DD}	—	
$\overline{\text{SMI}}$	A18	Input	OV_{DD}	—	10
$\overline{\text{SRESET}}$	B16	Input	OV_{DD}	—	10
TBEN	B14	Input	OV_{DD}	—	10
$\overline{\text{QACK}}$/DA0	F2	Output	OV_{DD}	DRV_STD	3, 4
$\overline{\text{CHKSTOP\_IN}}$	D14	Input	OV_{DD}	—	10
MAA[0:2]	AF2 AF1 AE1	Output	GV_{DD}	DRV_MEM_DATA	3, 4, 6
$\overline{\text{MIV}}$	A16	Output	OV_{DD}	DRV_STD	
PMAA[0:2]	AD18 AF18 AE19	Output	OV_{DD}	DRV_STD	3, 4, 6,15
TRIG_IN	AF20	Input	OV_{DD}	—	10
TRIG_OUT	AC18	I/O	OV_{DD}	DRV_STD	
Test/Configuration Signals					
PLL_CFG[0:4]/ DA[10:6]	A22 B19 A21 B18 B17	I/O	OV_{DD}	—	4, 6
$\overline{\text{TEST0}}$	AD22	Input	OV_{DD}	—	1, 9
$\overline{\text{TEST1}}$	B20	Input	OV_{DD}	—	9, 10
$\overline{\text{TEST2}}$	Y2	Input	GV_{DD}	—	11
TCK	AF22	Input	OV_{DD}	—	9, 12
TDI	AF23	Input	OV_{DD}	—	9, 12
TDO	AC21	Output	OV_{DD}	DRV_PCI	
TMS	AE22	Input	OV_{DD}	—	9, 12
$\overline{\text{TRST}}$	AE23	Input	OV_{DD}	—	9, 12

Table 17. MPC8240 Pinout Listing (continued)

Signal Name	Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
Power and Ground Signals					
GND	AA2 AA23 AC12 AC15 AC24 AC3 AC6 AC9 AD11 AD14 AD16 AD19 AD23 AD4 AE18 AE2 AE21 AE25 B2 B25 B6 B9 C11 C13 C16 C23 C4 C8 D12 D15 D18 D21 D24 D3 F25 F4 H24 J25 J4 L24 L3 M23 M4 N24 P3 R23 R4 T24 T3 V2 V23 W3	Ground	—	—	
LV_{DD}	AC20 AC23 D20 D23 G23 P23 Y23	Reference Voltage 3.3 V, 5.0 V	LV_{DD}	—	
GV_{DD}	AB3 AB4 AC10 AC11 AC8 AD10 AD13 AD15 AD3 AD5 AD7 C10 C12 C3 C5 C7 D13 D5 D9 E3 G3 H4 K4 L4 N3 P4 R3 U3 V4 Y3	Power for Memory Drivers 2.5 V, 3.3 V	GV_{DD}	—	
OV_{DD}	AB24 AD20 AD24 C14 C20 C24 E24 G24 J23 K24 M24 P24 T23 Y24	PCI/Stnd 3.3 V	OV_{DD}	—	
V_{DD}	AA24 AC16 AC19 AD12 AD6 AD9 C15 C18 C21 D11 D8 F3 H23 J3 L23 M3 R24 T4 V24 W4	Power for Core 2.5 V	V_{DD}	—	
LAV_{DD}	D17	Power for DLL 2.5 V	LAV_{DD}	—	
AV_{DD}	C17	Power for PLL (CPU Core Logic) 2.5 V	AV_{DD}	—	
$AV_{DD}2$	AF24	Power for PLL (Peripheral Logic) 2.5 V	$AV_{DD}2$	—	

Table 17. MPC8240 Pinout Listing (continued)

Signal Name	Pin Number	Pin Type	Power Supply	Output Driver Type	Notes
Manufacturing Pins					
DA2	C25	Output	OV_{DD}	DRV_PCI	2
DA[11:13]	AD26 AF17 AF19	Output	OV_{DD}	DRV_PCI	2, 6
DA[14:15]	F1 J2	Output	GV_{DD}	DRV_MEM_ADDR	2, 6

Notes:
1. Place pull-up resistors of 120 Ω or less on the $\overline{\text{TEST0}}$ pin.
2. Treat these pins as no connects unless using debug address functionality.
3. This pin has an internal pull-up resistor which is enabled only when the MPC8240 is in the reset state. The value of the internal pull-up resistor is not guaranteed, but is sufficient to ensure that a one is read into configuration bits during reset.
4. This pin is a reset configuration pin.
5. DL[0] is a reset configuration pin and has an internal pull-up resistor which is enabled only when the MPC8240 is in the reset state.The value of the internal pull-up resistor is not guaranteed, but is sufficient to ensure that a one is read into configuration bits during reset.
6. Multi-pin signals such as AD[0:31] or DL[0:31] have their physical package pin numbers listed in order corresponding to the signal names. Example: AD0 is on pin C22, AD1 is on pin D22,... AD31 is on pin V25.
7. $\overline{\text{GNT4}}$ is a reset configuration pin and has an internal pull-up resistor which is enabled only when the MPC8240 is in the reset state.The value of the internal pull-up resistor is not guaranteed, but is sufficient to ensure that a one is read into configuration bits during reset.
8. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this PCI control pin to LV_{DD}.
9. V_{IH} and V_{IL} for these signals are the same as the PCI V_{IH} and V_{IL} entries in Table 3.
10. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV_{DD}.
11. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to GV_{DD}.
12. This pin has an internal pull-up resistor; the value of the internal pull-up resistor is not guaranteed, but is sufficient to prevent unused inputs from floating.
13. Output valid specifications for this pin are memory interface mode dependent (registered or flow-through), see Table 9.
14. Non-DRAM access output valid specification applies to this pin during non-DRAM accesses, see specification 12b3 in Table 9.
15. This pin is affected by programmable PCI_HOLD_DEL parameter, see Section 1.4.2.4.1, “PCI Signal Output Hold Timing.”
16. This pin is an open drain signal.
17. This pin can be programmed to be driven (default) or can be programmed to be open drain; see PMCR2 register description in the *MPC8240 Integrated Processor User’s Manual*, for details.
18. This pin is a sustained three-state pin as defined by the *PCI Local Bus Specification.*
19. Maximum input voltage tolerance is LV_{DD}-based. See Table 2 for details.

1.6 PLL Configuration

The MPC8240 internal PLLs are configured by the PLL_CFG[0:4] signals. For a given PCI_SYNC_IN (PCI bus) frequency, the PLL configuration signals set both the peripheral logic/memory bus PLL (VCO) frequency of operation for the PCI-to-memory frequency multiplying and the MPC603e CPU PLL (VCO) frequency of operation for memory-to-CPU frequency multiplying. The PLL configurations for the MPC8240 is shown in Table 18.

Table 18. MPC8240 Microprocessor PLL Configurations

Ref	PLL_CFG [0:4] [2]	CPU [1] HID1 [0:4]	200 MHz Part [8,9]			Ratios [3,4]	
			PCI Clock Input (PCI_SYNC_IN) Range (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI-to-Mem (Mem VCO) Multiplier	Mem-to-CPU (CPU VCO) Multiplier
0	00000	00110	25–26	75–80	188–200	3 (6)	2.5 (5)
1	00001	11000	Not Usable			3 (6)	3 (6)
2	00010	00101	50–56 [5]	50 – 56	100–112	1 (4)	2 (8)
3	00011	00101	Bypass			Bypass	2 (8)
4	00100	00101	25–28 [5]	50–56	100–113	2 (8)	2 (8)
5	00101	00110	Bypass			Bypass	2.5 (5)
7	00111	11000	Bypass			Bypass	3 (6)
8	01000	11000	33 [6]–56 [5]	33–56	100–168	1 (4)	3 (6)
A	01010	00111	Not Usable			2 (4)	4.5 (9)
C	01100	00110	25–40	50–80	125–200	2 (4)	2.5 (5)
E	01110	11000	25–33	50–66	150–200	2 (4)	3 (6)
10	10000	00100	25–33	75–100	150–200	3 (6)	2 (4)
12	10010	00100	33 [7]–66	50–100	100–200	1.5 (3)	2 (4)
14	10100	11110	25–28	50–56	175–200	2 (4)	3.5 (7)
16	10110	11010	25	50	200	2 (4)	4 (8)
18	11000	11000	25–26	62–65	186–200	2.5 (5)	3 (6)
1A	11010	11010	50	50	200	1 (2)	4 (8)
1C	11100	11000	33 [7]–44	50–66	150–200	1.5 (3)	3 (6)
1D	11101	00110	33 [7]–53	50–80	125–200	1.5 (3)	2.5 (5)
1E	11110	01111	Not Usable			Off	Off
1F	11111	11111				Off	Off

Notes:
1. The processor HID1 values only represent the multiplier of the processor's PLL (memory-to-processor multiplier); thus, multiple MPC8240 PLL_CFG[0:4] values may have the same processor HID1 value. This implies that system software cannot read the HID1 register and associate it with a unique PLL_CFG[0:4] value.
2. PLL_CFG[0:4] settings not listed (00110, 01001, 01011, 01101, 01111, 10001, 10011, 10101, 10111, 11001, and 11011) are reserved.
3. In PLL-bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for hardware modeling support. The AC timing specifications given in this document do not apply in the PLL-bypass mode.
4. In clock off mode, no clocking occurs inside the MPC8240 regardless of the PCI_SYNC_IN input.
5. Limited due to maximum memory VCO = 225 MHz.
6. Limited due to minimum CPU VCO = 200 MHz.
7. Limited due to minimum memory VCO = 100 MHz.
8. For clarity, range values are shown rounded down to the nearest whole number (decimal place accuracy removed).
9. Note that the 250-MHz part is available only in the XPC8240RZU*nnnx* number series.

1.7 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8240.

1.7.1 PLL Power Supply Filtering

The AV_{DD}, $AV_{DD}2$, and LAV_{DD} power signals are provided on the MPC8240 to provide power to the peripheral logic/memory bus PLL, MPC603e processor PLL, and SDRAM clock delay-locked loop (DLL), respectively. To ensure stability of the internal clocks, the power supplied to the AV_{DD}, $AV_{DD}2$, and LAV_{DD} input signals should be filtered of any noise in the 500-kHz to 10-MHz resonant frequency range of the PLLs. Three separate circuits similar to the one shown in Figure 22 using surface mount capacitors with minimum effective series inductance (ESL) is recommended for AV_{DD}, $AV_{DD}2$, and LAV_{DD} power signal pins. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over using multiple values.

The circuits should be placed as close as possible to the respective input signal pins to minimize noise coupled from nearby circuits. Routing directly as possible from the capacitors to the input signal pins with minimal inductance of vias is important.

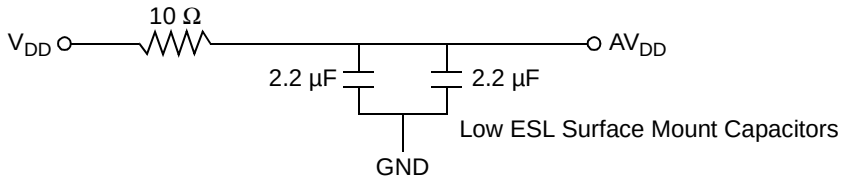


Figure 22. PLL Power Supply Filter Circuit

1.7.2 Power Supply Sizing

The power consumption numbers provided in Table 5 do not reflect power from the OV_{DD} and GV_{DD} power supplies which are non-negligible for the MPC8240. In typical application measurements, the OV_{DD} power ranged from 200 to 600 mW and the GV_{DD} power ranged from 300 to 900 mW. The ranges' low-end power numbers were results of the MPC8240 performing cache resident integer operations at the slowest frequency combination of 33:66:166 (PCI:Mem:CPU) MHz. The OV_{DD} high-end range's value resulted from the MPC8240 performing continuous flushes of cache lines with alternating ones and zeros to PCI memory. The GV_{DD} high-end range's value resulted from the MPC8240 operating at the fastest frequency combination of 66:100:250 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeros on 64-bit boundaries to local memory.

1.7.3 Decoupling Recommendations

Due to the MPC8240 dynamic power management feature, large address and data buses, and high operating frequencies, the MPC8240 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8240 system, and the MPC8240 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pin of the MPC8240. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, OV_{DD}, GV_{DD}, and GND power planes in the PCB, utilizing short

traces to minimize inductance. These capacitors should have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603, oriented such that connections are made along the length of the part.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors: 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

1.7.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, GV_{DD}, LV_{DD}, and GND pins of the MPC8240.

The PCI_SYNC_OUT signal is intended to be routed halfway out to the PCI devices and then returned to the PCI_SYNC_IN input of the MPC8240.

The SDRAM_SYNC_OUT signal is intended to be routed halfway out to the SDRAM devices and then returned to the SDRAM_SYNC_IN input of the MPC8240. The trace length may be used to skew or adjust the timing window as needed. See Motorola Application Note AN1794/D for more information on this topic.

1.7.5 Pull-Up/Pull-Down Resistor Requirements

The data bus input receivers are normally turned off when no read operation is in progress; therefore, they do not require pull-up resistors on the bus. The data bus signals are: DH[0:31], DL[0:31], and PAR[0:7].

If the 32-bit data bus mode is selected, the input receivers of the unused data and parity bits ($\overline{\text{DL}}$[0:31] and $\overline{\text{PAR}}$[4:7]) will be disabled, and their outputs will drive logic zeros when they would otherwise normally be driven. For this mode, these pins do not require pull-up resistors, and should be left unconnected by the system to minimize possible output switching.

The $\overline{\text{TEST0}}$ pins require pull-up resistors of 120 Ω or less connected to OV_{DD}.

It is recommended that $\overline{\text{TEST2}}$ have a weak pull-up resistor (2–10 kΩ) connected to GV_{DD}.

It is recommended that the following signals be pulled up to OV_{DD} with weak pull-up resistors (2–10 kΩ): SDA, SCL, $\overline{\text{SMI}}$, $\overline{\text{SRESET}}$, TBEN, $\overline{\text{CHKSTOP\_IN}}$, and $\overline{\text{TEST1}}$.

It is recommended that the following PCI control signals be pulled up to LV_{DD} with weak pull-up resistors (2–10 kΩ): $\overline{\text{DEVSEL}}$, $\overline{\text{FRAME}}$, $\overline{\text{IRDY}}$, $\overline{\text{LOCK}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, $\overline{\text{STOP}}$, $\overline{\text{TRDY}}$, and $\overline{\text{INTA}}$. The resistor values may need to be adjusted stronger to reduce induced noise on specific board designs.

The following pins have internal pull-up resistors enabled at all times: $\overline{\text{REQ}}$[0:3], $\overline{\text{REQ4}}$/DA4, TCK, TDI, TMS, and $\overline{\text{TRST}}$. See Table 17 for more information.

The following pins have internal pull-up resistors enabled only while the MPC8240 is in the reset state: $\overline{\text{GNT4}}$/DA5, DL0, $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, CKE, $\overline{\text{AS}}$, $\overline{\text{MCP}}$, MAA[0:2], PMAA[0:2], and $\overline{\text{QACK}}$/DA0. See Table 17 for more information.

The following pins are reset configuration pins: $\overline{\text{GNT4}}$/DA5, DL0, $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, CKE, $\overline{\text{AS}}$, $\overline{\text{MCP}}$, $\overline{\text{QACK}}$/DA0, MAA[0:2], PMAA[0:2], and PLL_CFG[0:4]/DA[10:6]. These pins are sampled during reset to configure the device.

Reset configuration pins should be tied to GND via 1-kΩ pull-down resistors to ensure a logic zero level is read into the configuration bits during reset if the default logic one level is not desired.

Any other unused active-low input pins should be tied to a logic one level via weak pull-up resistors (2–10 kΩ) to the appropriate power supply. Unused active-high input pins should be tied to GND via weak pull-down resistors (2–10 kΩ).

1.7.6 JTAG Configuration Signals

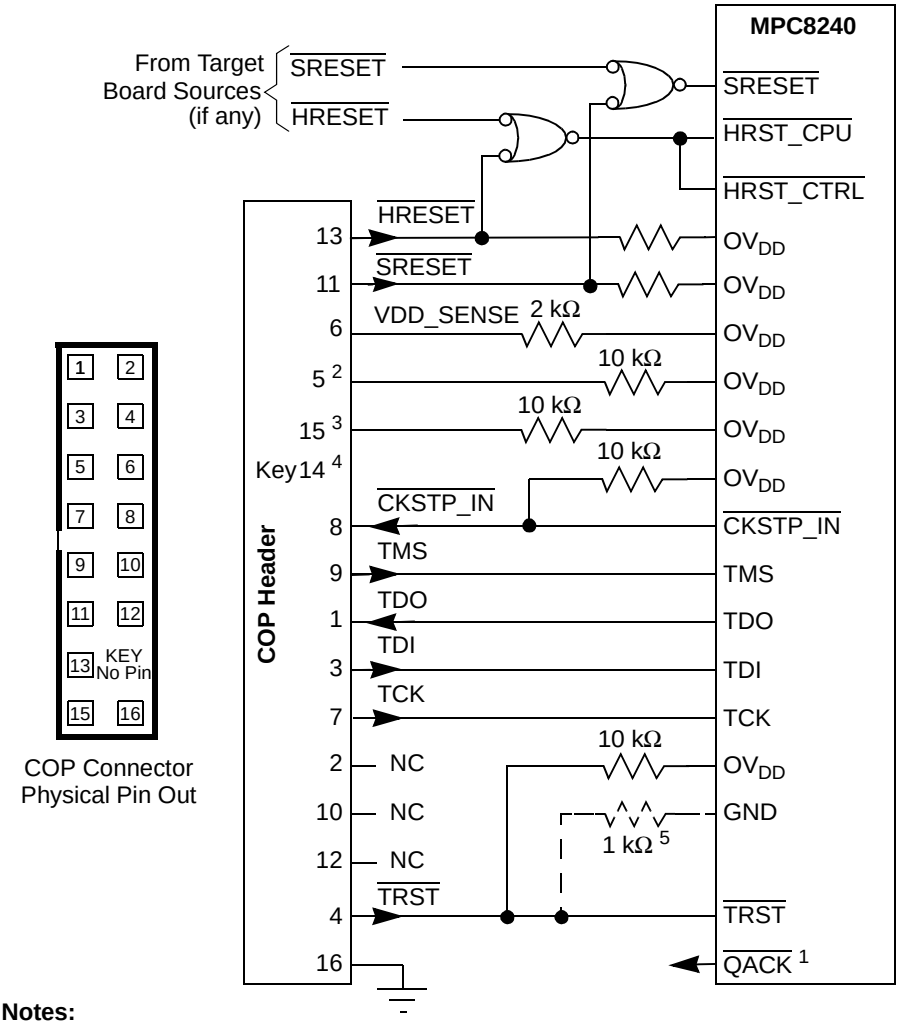
Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 23 allows the COP to independently assert $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ or $\overline{\text{TRST}}$ while ensuring that the target can drive $\overline{\text{HRST\_CPU}}$/$\overline{\text{HRST\_CTRL}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted ensuring that the JTAG scan chain is initialized during power-on.

The COP header shown in Figure 23 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). There is no standardized way to number the COP header shown in Figure 23; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 23 is common to all known emulators.



Notes:

1. $\overline{\text{QACK}}$ is an output on the MPC8240 and is not required at the COP header for emulation.
2. RUN/$\overline{\text{STOP}}$ normally found on pin 5 of the COP header is not implemented on the MPC8240. Connect pin 5 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
3. $\overline{\text{CKSTP\_OUT}}$ normally found on pin 15 of the COP header is not implemented on the MPC8240. Connect pin 15 of the COP header to OV_{DD} with a 10-kΩ pull-up resistor.
4. Pin 14 is not physically present on the COP header.
5. Component not populated.

Figure 23. COP Connector Diagram

1.7.7 PCI Reference Voltage—LV_{DD}

The MPC8240 PCI reference voltage (LV_{DD}) pins should be connected to 3.3 ±0.3 V power supply if interfacing the MPC8240 into a 3.3-V PCI bus system. Similarly, the LV_{DD} pins should be connected to 5.0 ±5% V power supply if interfacing the MPC8240 into a 5-V PCI bus system. For either reference voltage, the MPC8240 always performs 3.3-V signaling as described in the *PCI Local Bus Specification,* (r2.1). The MPC8240 only tolerates 5-V signals when interfaced into a 5-V PCI bus system.

1.7.8 Thermal Management Information

This section provides thermal management information for the tape ball grid array (TBGA) package for air-cooled applications. Proper thermal control design is primarily dependent upon the system-level design—the heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods: adhesive, spring clip to holes in the printed-circuit board, or package and mounting clip and screw assembly. See Figure 24.

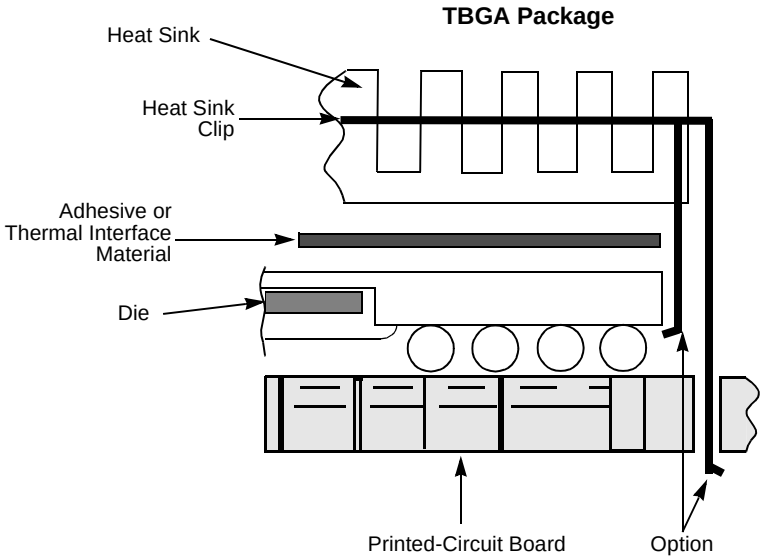


Figure 24. Package Exploded Cross-Sectional View with Several Heat Sink Options

Figure 25 depicts the die junction-to-ambient thermal resistance for four typical cases:

- A heat sink is not attached to the TBGA package and there exists high board-level thermal loading of adjacent components.
- A heat sink is not attached to the TBGA package and there exists low board-level thermal loading of adjacent components.
- A heat sink (for example, ChipCoolers #HTS255-P) is attached to the TBGA package and there exists high board-level thermal loading of adjacent components.
- A heat sink (for example, ChipCoolers #HTS255-P) is attached to the TBGA package and there exists low board-level thermal loading of adjacent components.

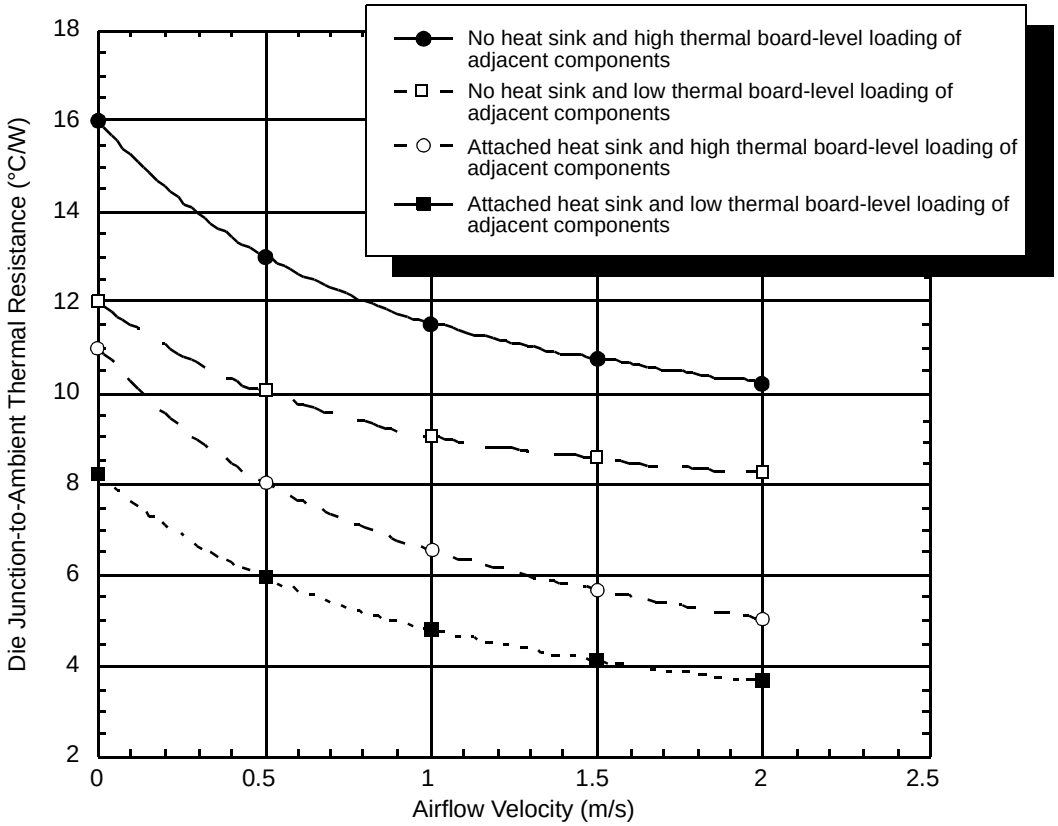


Figure 25. Die Junction-to-Ambient Resistance

The board designer can choose between several types of heat sinks to place on the MPC8240. There are several commercially available heat sinks for the MPC8240 provided by the following vendors:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #15 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-749-7601
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277

Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

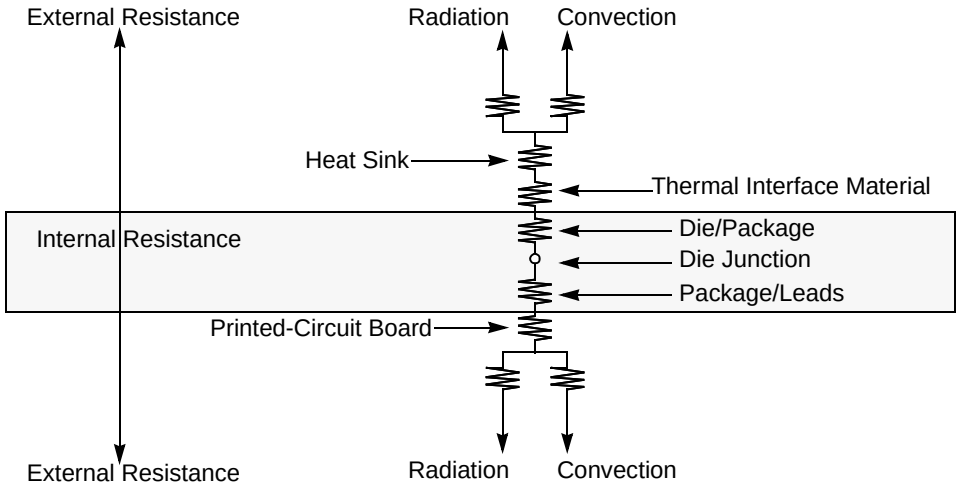
Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

1.7.8.1 Internal Package Conduction Resistance

For the TBGA, cavity down, packaging technology shown in Figure 24, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-ball thermal resistance

Figure 26 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 26. TBGA Package with Heat Sink Mounted to a Printed-Circuit Board

For this cavity-down, wire-bond TBGA package, heat generated on the active side of the chip is conducted through the silicon, the die attach, and package spreader, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

1.7.8.2 Adhesives and Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 27 shows the thermal performance of three thin-sheet thermal-interface materials (silicone,

graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than that of the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 24). Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure. Of course, the selection of any thermal interface material depends on many factors: thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, etc.

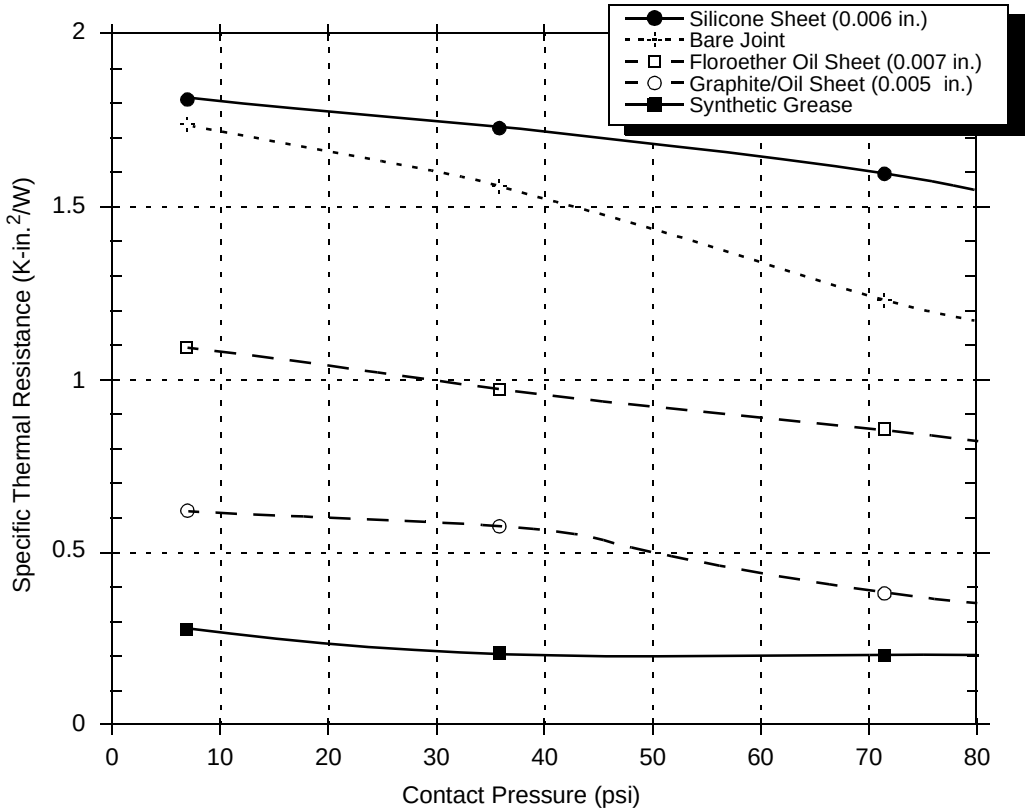


Figure 27. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several comm3rcially available thermal interfaces and adhesive materials provided by the following vendors:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01888-4014 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials 2200 W. Salzburg Rd. Midland, MI 48686-0997 Internet: www.dow.com	800-248-2481

Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
Thermagon Inc. 4707 Detroit Ave. Cleveland, OH 44102 Internet: www.thermagon.com	888-246-9050

The following section provides a heat sink selection example using one of the commercially available heat sinks.

1.7.8.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_J = T_A + T_R + (\theta_{JC} + \theta_{INT} + \theta_{SA}) * P_D$$

Where:

T_J is the die-junction temperature

T_A is the inlet cabinet ambient temperature

T_R is the air temperature rise within the computer cabinet

θ_{JC} is the junction-to-case thermal resistance

θ_{INT} is the adhesive or interface material thermal resistance

θ_{SA} is the heat sink base-to-ambient thermal resistance

P_D is the power dissipated by the device

During operation the die-junction temperatures (T_J) should be maintained less than the value specified in Table 2. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_A) may range from 30 to 40°C. The air temperature rise within a cabinet (T_R) may be in the range of 5 to 10°C. The thermal resistance of the thermal interface material (θ_{INT}) is typically about 1°C/W. Assuming a T_A of 30°C, a T_R of 5°C, a TBGA package θ_{JC} = 1.8, and a power consumption (P_D) of 5.0 watts, the following expression for T_J is obtained:

Die-junction temperature: $T_J = 30°C + 5°C + (1.8°C/W + 1.0°C/W + \theta_{SA}) \times 5.0\ W$

For preliminary heat sink sizing, the heat sink base-to-ambient thermal resistance is needed from the heat sink manufacturer.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure of merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when using only this metric in determining thermal management, because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature: airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today’s microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection,

and conduction) may vary widely. For these reasons, we recommend using conjugate heat-transfer models for the board, as well as system-level designs.

1.8 Document Revision History

Table 19 provides a revision history for this hardware specification.

Table 19. Document Revision History

Rev. No.	Substantive Change(s)
0	Preliminary release with some TBDs in the spec tables.
0.1	Updated notes for Table 2. Replaced TBDs in Table 3 with values for Output High and Low Voltages. Deleted 25/25/75 column from Table 5; inconsistent with PLL encoding 01000. Updated minimum processor frequencies in Table 6 from 80 MHz to 100 MHz. Updated values in Table 8. Spec 10b split for flow through and registered modes. Updated values in Table 9. Updated PCI_HOLD_DEL value guidelines in Table 10 and Figure 10. Relabeled DA[0:15] pins in opposite order and added Note 11 for $\overline{\text{TEST2}}$ in Table 17. Changed PLL configurations 01001 and 10001 in Table 18 to reserved configurations. Updated PLL configuration 00010's operation ranges in Table 18. Revised $\overline{\text{TRST}}$ connection recommendations in Figure 22 for COP interface.
0.2	Added Note 4 to Table 2, updated Note and Caution numbers in Table 2 and Figure 2. Modified Table 6: —Added 250 MHz column. —Changed maximum PCI Input Frequency for 200 MHz part from 33 MHz to 66 MHz. —Made one column common entries for Memory Bus and PCI Input Frequencies. Revised Note 7 of Table 7 to indicate a feedback loop length of 6.25 inches (formerly 11.8 inches) corresponds to approximately 1 ns of delay. Added 250 MHz column to Table 18. Corrected Document Revision number for previous version of this document in Table 19. Document Revision was indicated as 1, should have been 0.1. Removed P = Reduced Spec information from Figure 28; does not apply to MPC8240. Added R = Modified Voltage Spec information to Figure 28.

Table 19. Document Revision History (continued)

Rev. No.	Substantive Change(s)
0.3	Removed “PowerPC Platform compliant” from first sentence on cover sheet. Changed PCI 2.1 - “compatible” to “compliant” in Section 1.2. Updated Table 5 and its notes with preliminary power-consumption information. Updated Table 6 removing 266 MHz frequency information. Made corrections to Table 7. • Items 5a and 5b were changed to correct values for 66 MHz PCI_SYNC_IN. • OSC_IN Frequency Stability spec from 1000 ppm to 100 ppm. Table 9: • Changed item 12b1 from 8.0 ns to 7.0 ns. • Added item 12b3, Output Valid for ROM accesses. Table 11, item 2, “KAHLUA” terminology replaced with MPC8240. Added EPIC Serial Interrupt Timing Section with two new figures causing cross-references to subsequent figures to be updated. Updated formatting of pin out Table 17. Modified notes section of Table 17: • Split Note 3 into a new Notes 3 and 12. Notes 3, 5, and 7 cover internal pull-up resistors active only during the reset state. Note 12 covers internal pull-up resistors enabled at all times. • Note 11 has been revised. • Added Note 10 to SDA and SCL signals for consistency with MPC8240 User’s Manual. • Added Note 10 to SMI and TBEN; inputs which should have pull-ups and for consistency with reference designs. • Added Note 10 to SRESET and CHKSTOP_IN for consistency with Figure 23 (COP Connector) • Added Notes 13 and 14 for output valid specifications dependent upon memory mode. • Added Note 15 for pins affected by programmable PCI output valid and hold time. • Added Notes 16 –18 relating to open drain pins. Figure 18: • Revised 200 MHz column to reflect PCI_SYNC_IN 66 MHz upper limit. • Refs 1E and 1F not usable entries made to match others in the table. • Revised Notes 4 and 5 changing OSC_IN to PCI_SYNC_IN. • Removed 266 MHz column. • Removed Ref 0x06 for dual PLL bypass mode; added it to reserved list in Note 3. • Revised Note 4 describing PLL bypass mode. Added missing cross-reference in Section 1.7.2 and corrected Schottky reference to the 1N5820 diodes. Added Section 1.7.2 on power supply sizing. Modified internal pull-up resistor list in Section 1.7.5 to be consistent with Notes of Table 17; added reset configuration pin pull-down resistor value recommendation. Modified Figure 23, COP Connector Diagram: • Reversed direction of CKSTP_IN arrow to show it going in. • Added a pull-up resistor on TRST. Changed R-spec device’s V_{DD} range from 2.5 - 2.625 V to 2.5 - 2.75 V.
0.4	Modified DLL Lock Range with DLL_EXTEND = 1 equation in Table 7 from $0 \le (NT_{clk}/2 - t_{loop} - t_{fix0}) \le 7$ to $0 \le (NT_{clk} - T_{clk}/2 - t_{loop} - t_{fix0}) \le 7$. Modified Figure 5 to only show T_{loop} up to 15 ns, not practical to implement T_{loop} beyond 15 ns. Modified DL[0:31] and DH[0:31] signal names to MDL[0:31] and MDH[0:31], respectively, in Table 17 to be consistent with the MPC107 data bus naming convention. Several active low signal names in Table 17 inadvertently had the overline formatting removed during the final edit process of the previous revision. The signals are shown correctly with overlines in this version. Signals affected were: DEVSEL, FRAME, LOCK, PERR, SERR, STOP, TRDY, INTA, FOE, RCS0, RCS1, SDRAS, SDCAS, WE, AS, HRST_CTRL, HRST_CPU, MCP, SMI, SRESET, CHKSTOP_IN, and MIV.

Table 19. Document Revision History (continued)

Rev. No.	Substantive Change(s)
0.5	Removed references to GV_{DD} = 2.5 V until characterization of the memory interface at this voltage has been completed. Corrected Figure 2 power supply ramp-up time to be before the 100 ms PLL relock time. Table 3: • Deleted input leakage specification @ LV_{DD} = 5.5 V. • Changed minimum “Input High Voltage for PCI only” from 0.5*OVDD to 0.65*OVDD and added Note 6. • Changed condition on “Input Low Voltage,” V_{IL}, from “All inputs except OSC_IN” to “All inputs except PCI_SYNC_IN.” • Replaced minimum CV_{IH} formula, 0.5*OVDD, with 2.4 V value. • Replaced maximum CV_{IL} formula, 0.3*OVDD, with 0.4 V value. Added Note 10 to Table 5. Changed minimum memory bus frequency of operation from 25 MHz to 33 MHz in Table 6 to coincide with information shown in PLL_CFG Table 18. Updated clock specifications in Table 7. Updated input AC timing specifications in Table 8. Updated output AC timing specifications in Table 9. Replaced TBDs in Table 14 for specs 3, 5, and 6. Table 17 renamed TEST3 (pin AF20) to TRIG_IN and renamed TEST4 (pin AC18) to TRIG_OUT; moved both pins from Test/Configuration Signals group to Miscellaneous Signals group. Added external pull-up resistor to LVDD recommendation for INTA signal in Table 17 and Section 1.7.5. Added Note 19 to Table 17 about AVDD and LAVDD being internally connected; revised Section 1.7.1, on filtering these pins. Replaced HID1 column TBDs in Table 18 and deleted Note 1 resulting in renumbering notes throughout Table 18. Added Section 1.7.7, about PCI reference voltage. Added note in Section 1.9, indicating “L=Standard Spec.” part is only available in 200 MHz version of the device. Changed “XPC” to “MPC” for consistency with other references in the document.
0.6	Updated Technology in Section 1.3 from 0.32 µm to 0.29 µm. Updated Notes in Table 2. Changed line 2 to reflect supply voltage wording of the other lines. Changed notes 2 and 3 to include all LVDD input tolerant signals. Updated Table 4 eliminating LVDD=5.0V entries for DRV_PCI. Changed LVDD to OVDD for remaining DRV_PCI entries. Updated notes. Updated Table 6 to show minimum memory bus operating frequency is 33 MHz. Updated Table 8 with new characterization data for numbers 22 and 23. Updated Table 8 adding “/In-line” to “Registered” in Spec 10b2. Updated Table 9 to Table 10 to how changes for MCP and CKE reset configuration changes for PCI_HOLD_DEL. Updated Table 12 eliminating 25 MHz column since memory interface does not operate at this frequency. Updated Table 17: • REQ4/DA4 and PLL_CFG[0:4]/DA[10:6] changed Pin Type from Input to I/O. • DA2, DA[11:13], DA[14:15] changed Pin Type from I/O to Output. • Reversed vector ordering for the PCI Interface Signals: C/BE[0:3] changed to C/BE[3:0], AD[0:31] changed to AD[31:0], GNT[0:3] changed to GNT[3:0], and REQ[0:3] changed to REQ[3:0]. The package pin number orderings were also reversed meaning that pin functionality did NOT change. For example, AD0 is still on signal C22, AD1 is still on signal D22, ... AD31 is still on signal V25. This change was made to make the vectored PCI signals in the MPC8240 Hardware Specification consistent with the PCI Local Bus Specification and the MPC8240 User Manual vector ordering. • Deleted Note 19 indicating LAVDD and AVDD are internally connected. Added a new Note 19 about OSC_IN and EPIC control signals input voltage levels. Updated Section 1.7.1 eliminating references to LAVDD and AVDD being internally connected. Updated Table 23 changing 2K Ohm pull-up resistor on VDD_SENSE to 1K Ohm. Moved Section 1.7.7 to be at end of JTAG section. Changed erroneous “C4” reference in Figure 26 title to “TBGA.” Deleted references to FLOTHERM models in Section 1.7.8.3.

Table 19. Document Revision History (continued)

Rev. No.	Substantive Change(s)
1	Updated notes for Table 2, to include that the values maybe exceeded for up to 20 ms. Updated Figure 2 removed note 2 concerning voltage sequencing. Updated Solder Balls in Section 1.5.1 Package Parameters from 63/37 Sn/Pb to 62 Sn/36 Pb/2 Ag Updated Table 9 adding “address” to 12b1-3 Updated Table 10 to show the settings for silicon rev. 1.0/1.1 and for silicon rev. 1.2/1.3 Updated Table 17: • removed Note 10 from TRIG_OUT • Created separate rows for TEST0 and TEST1 to reflect the change made in note 1 • Changed note 1 to refer only to TEST0. Removed Section 1.7.2. Section 1.6.8—Updated list of heat sink and thermal interface vendors. Changed format of Section 1.8.
2	Section 1.3.1.5—Updated Table 5 to reflect power numbers for the L spec (2.5 V) part. The power numbers for the R spec (2.625 V) part are now in the part number specifications document MPC8240RZUPNS/D. Section 1.5—Table 18 now reflects the L spec parts (200 MHz). The R spec PLL table is now in the R spec (250 MHz) part number specifications document MPC8240RZUPNS/D. Section 1.6.6—Updated this section and Figure 26. Section 1.8.2—Updated reference to part number specifications document.

1.9 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 1.9.1, “Part Numbers Fully Addressed by This Document.” Section 1.9.2, “Part Numbers Not Fully Addressed by This Document,” lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a part number specification.

1.9.1 Part Numbers Fully Addressed by This Document

Table 20 provides the Motorola part numbering nomenclature for the MPC8240. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Motorola sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code that refers to the die mask revision number.

Table 20. Motorola Part Numbering Nomenclature

XPC	***nnnn***	**L**	***xx***	***nnn***	***x***	***x***
Product Code	**Part Identifier**	**Process Descriptor**	**Package [1]**	**Processor Frequency [2]**	**Application Modifier**	**Revision Level**
XPC	8240	L = Standard Spec.	ZU = TBGA	200	2.5 V ±125 mV 0 to 105°C	Contact local Motorola sales office

Notes:
1. See Section 1.5, “Package Description,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

1.9.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate part number specifications which supplement and supersede this document; see Table 21.

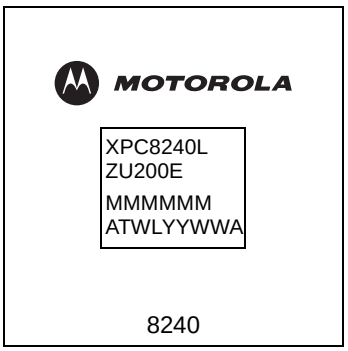
Table 21. Part Numbers with Separate Documentation

Part Number Series	Operating Conditions	Document Order Number of Applicable Specification
XPC8240RZU*nnn*x	2.625 V ±125 mV, 0 to 105°C 250 MHz	MPC8240RZUPNS/D

Note: For other differences, see applicable specifications.

1.9.3 Part Marking

Parts are marked as the example shown in Figure 28.



TBGA

Notes:
MMMMMM is the 6-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 28. Motorola Part Marking for TBGA Device

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