REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Corrections made to 1.3, 1.5 and Table I. - ksr	03-08-28	Raymond Monnin
B	Boilerplate update, part of 5 year review. - ksr	08-12-08	Robert M. Heber
C	Added BGA requirements per MIL-PRF-38535. Removed class M requirements. Updated in accordance with latest MIL-PRF-38535 requirements. - glg	14-09-19	Charles Saffle

REV	C	C	C	C	C	C	C	C	C	C										
SHEET	35	36	37	38	39	40	41	42	43	44										
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
02-09-02

REVISION LEVEL
C

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, ELECTRICALLY ALTERABLE (IN-SYSTEM REPROGRAMMABLE), 322,970 GATES, PROGRAMMABLE LOGIC DEVICE, MONOLITHIC SILICON

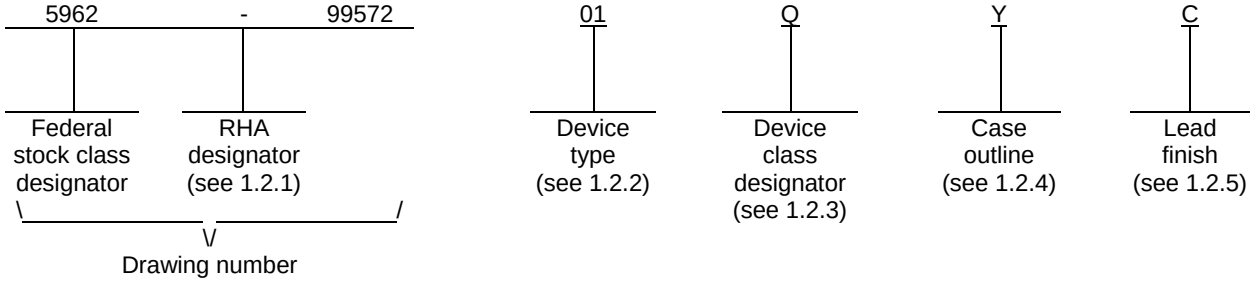
SIZE	CAGE CODE	
A	**67268**	**5962-99572**

SHEET 1 OF 44

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	XQV300-4	322970 gate programmable array	1.0 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
N	Certification and qualification to MIL-PRF-38535 with a nontraditional performance environment (encapsulated in plastic)
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Y	See figure 1	228	Quad flat package
Z	See figure 1	228	Quad flat package
U	LBGA-B-432 (JEDEC MO-192-BAU-1)	432	Ball grid array with four rows on each side (plastic) 1/
T	PQFP-G-240 (JEDEC MS-029-GA)	240	Quad flat package with heat sink molded in the package (plastic)
N	LBGA-B-352 (JEDEC MO-192-BAR-2)	352	Ball grid array 1/

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q, and V.

1/ Terminal lead finish A is tin lead alloy. Package case outlines U and N solder ball material is Sn = 63% and Pb = 37%.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range to ground potential (V_{CCINT}) --------	-0.5 V dc to +3.0 V dc
Supply voltage range to ground potential (V_{CCO}) ----------	-0.5 V dc to +4.0 V dc
DC input voltage range (V_{IN})Internal threshold ----------	-0.5 V to 5.5V
DC input voltage range (V_{IN}) using Ref----------	-0.5 V to 3.6 V
Voltage applied to three-state output(V_{TS}) ----------	-0.5 V to 5.5V
Lead temperature (soldering, 10 seconds) ----------	+260°C
Power dissipation (PD) ----------	2.0 W
Thermal resistance, junction-to-case (θ_{JC}):	
Case outlines Y, Z ----------	1.0°C/W 4/
Case outlines U ----------	0.9°C/W 4/
Case outlines T ----------	2.8°C/W 4/
Case outlines N ----------	1.0°C/W 4/
Junction temperature (T_J) for ceramic packages ----------	+150°C 5/
Junction temperature (T_J) for plastic packages ----------	+125°C 5/
Storage temperature range ----------	-65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage relative to ground(V_{CCINT})----------	+2.375 V dc minimum to +2.625 V dc maximum
Supply voltage relative to ground(V_{CCO}) ----------	+1.2 V dc minimum to +3.6 V dc maximum
Input high voltage (V_{IH}) ----------	2.0 V dc minimum
Input low voltage (V_{IL})----------	0.8 V dc maximum
Maximum input signal transition time (t_{IN}) ----------	250 ns
Case operating temperature range (T_C)----------	-55°C to +125°C
Junction operating temperature range (T_J)----------	-55°C to +125°C for Plastic packages

1.5 Radiation features. (RHA marked devices only)

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s) .....100K rads(Si)

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2/ All voltage values in this drawing are with respect to V_{SS}
3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
4/ When a thermal resistance for this case is specified in MIL-STD-1835 that value shall supersede the value indicated herein.
5/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; http://www.astm.org.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD78 - IC Latch-Up Test.
JEP 95 - Registered and Standard Outlines for Semiconductor Devices

(Copies of this document are available online at www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 247, Arlington, VA 22201).

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, Q, and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.1.1 Solderability test for BGA packages. Solderability testing for case outlines U and N for BGA packages have been verified during the solder ball attachment process in accordance with method 2003 of MIL-STD-883.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Logic block diagram. The logic block diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics are the preirradiation and postirradiation parameter limits as specified in table I and shall apply over the full case operating or junction temperature range as applicable.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, Q, and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes N, Q, and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes N, Q, and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-PRF-38535.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions 2.375 V ≤V_{CCINT} ≤2.625 V 1.2 V ≤ V_{CCO} ≤ 3.6 V (-55°C ≤ T_C ≤+125°C for ceramic packages) (-55°C ≤ T_J ≤+125°C for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Data retention V_{CCINT} voltage below which configuration may be lost	V_{DRINT}		1, 2, 3	01	2.0		V
Data retention V_{CCO} voltage below which configuration may be lost	V_{DRIO}		1, 2, 3	01	1.2		V
High-level output voltage	V_{OH}	I_{OH} = -2,-4, or -8 mA, V_{CCO} = 3.0 V and V_{CCINT}=min	1, 2, 3	01	2.4		V
High-level output voltage		I_{OH} = -8 mA, V_{CCO}= 1.4 V and V_{CCINT}=min (HSTL IV)	1, 2, 3	01	1.0		V
Low-level output voltage	V_{OL}	I_{OL} = 2.5,5, or 9 mA V_{CCO} = 3.0 V and V_{CCINT}=min	1, 2, 3	01		0.4	V
Low-level output voltage		I_{OL} = 16, or 24 mA V_{CCO} = 3.0 V and V_{CCINT}=min (SSTL2 II) (leg X)	1, 2, 3	01		.35	V
Quiescent VCCINT Supply current	I_{CCINTQ} 2/		1, 2, 3	01		250	mA
Quiescent VCCO Supply current	I_{CCOQ} 2/					10	
Input or output leakage current	I_L		1, 2, 3	01	-10	+10	µA
V_{REF} current per V_{REF} pin	I_{REF}		1, 2, 3	01		+20	µA
Input capacitance (sample tested) U, T and N case outlines	C_{IN}, C_{OUT}	See 4.4.1e, f = 1.0 MHz, V_{OUT} = 0 V	4	01		8	pF
Input capacitance (sample tested) Y and Z case outline						16	
Pad pull-up (when selected)	I_{RPU} 3/	V_{IN} = 0V, V_{CCO} = 3.3 V (sample tested)	1, 2, 3	01		0.25	mA
Pad pull-down (when selected)	I_{RPD} 3/	V_{IN} = 3.6V (sample tested)	1, 2, 3	01		0.15	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2.375 V $\leq V_{CCINT} \leq$2.625 V 1.2 V $\leq V_{CCO} \leq$ 3.6 V (-55°C $\leq T_C \leq$+125°C for ceramic packages) (-55°C $\leq T_J \leq$+125°C for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Functional test	FT	See 4.4.1c	7, 8A, 8B	01			
Power-On Supply Requirements							
Minimum required current supply		4/ 5/				2.5 6/	A
IOB Input Switching Characteristics Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in "IOB Input Switching Characteristics Standard Adjustments" below this section.							
Propagation Delays							
Pad to I output, no delay	T_{IOPI}		9, 10, 11	01		1.0	ns
Pad to I output, with delay	T_{IOPID}					1.9	
Pad to output IQ via transparent latch, no delay	T_{IOPLI}					2.0	
Pad to output IQ via transparent latch, with delay	T_{IOPLID}					5.1	
Sequential Delays							
Clock CLK to output IQ	T_{IOCKIQ}		9, 10, 11	01		0.8	ns
Setup and Hold Times with respect to Clock CLK at IOB input register	Setup / Hold Time 7/						
Pad, no delay	T_{IOPICK} / T_{IOICKP}		9, 10, 11	01	2.0/0		ns
Pad, with delay	$T_{IOPICKD}$/ $T_{IOICKPD}$				5.0/0		
ICE input	T_{IOCECK}/$T_{IOCKICE}$				1.0/0		
SR Input (IFF,synchronous)	$T_{IOSRCKI}$/$T_{IOCKISR}$				1.3/0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2.375 V $\leq V_{CCINT} \leq$2.625 V 1.2 V $\leq V_{CCO} \leq$ 3.6 V (-55°C $\leq T_C \leq$+125°C for ceramic packages) (-55°C $\leq T_J \leq$+125°C for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
IOB Input Switching Characteristics - Continued Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in "IOB Input Switching Characteristics Standard Adjustments" below this section.							
Set / Reset Delays							
SR input to IQ (asynchronous)	T_{IOSRIQ}		9, 10, 11	01		1.8	ns
GSR to output IQ	T_{GSRQ}					12.5	

See footnotes at end of table.

The following section is for reference only (**Not part of table I**):

IOB Input Switching Characteristics Standard Adjustments

Description	Symbol	Standard	Value	Units
Data Input Delay Adjustments				
Standard-specific data input delay adjustments	T_{ILVTTL}	LVTTL	0	ns
	$T_{ILVCMOS2}$	LVCMOS2	-0.05	
	T_{IPCI33_3}	PCI, 33 MHz, 3.3 V	-0.14	
	T_{IPCI33_5}	PCI, 33 MHz, 5.0 V	0.33	
	T_{IPC166_3}	POI, 66 MHz, 3.3 V	-0.14	
	T_{IGTL}	GTL	0.26	
	T_{IGTLP}	GTL+	0.14	
	T_{IHSTL}	HSTL	0.04	
	T_{ISSTL2}	SSTL2	-0.10	
	T_{ISSTL3}	SSTL3	-0.06	
	T_{ICTT}	CTT	0.02	
	T_{IAGP}	AGP	-0.08	
Input timing for LVTTL is measured at 1.4 V, LVCMOS2 at 1.125 V, PCI per PCI specifications, and all others listed here measured at V_{REF}.				

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2.375 V $\leq V_{CCINT} \leq$ 2.625 V 1.2 V $\leq V_{CCO} \leq$ 3.6 V (-55°C $\leq T_C \leq$ +125°C for ceramic packages) (-55°C $\leq T_J \leq$ +125°C for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
IOB Output Switching Characteristics Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" below this section.							
Propagation Delays							
O input to Pad	T_{IOOP}		9, 10, 11	01		3.5	ns
O input to Pad via transparent latch	T_{IOOLP}					4.0	
3-State Delays							
T input to Pad high-impedance 8/	T_{IOTHZ}		9, 10, 11	01		2.4	ns
T input to valid data on Pad	T_{IOTON}					3.7	
T input to Pad high-impedance via transparent latch 8/	$T_{IOTLPHZ}$					3.0	
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$					4.2	
GTS to Pad high impedance 8/	T_{GTS}					6.3	
Sequential Delays							
Clock CLK to Pad	T_{IOCKP}		9, 10, 11	01		3.5	ns
Clock CLK to Pad high-impedance (synchronous) 8/	T_{IOCKHZ}					2.9	
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}					4.1	
Setup and Hold Times before/after Clock CLK 7/	Setup Time /Hold Time						
O input	T_{IOOCK} / T_{IOCKO}		9, 10, 11	01	1.3/0		ns
O OCE input	$T_{IOOCECK}$ / $T_{IOCKOCE}$				1.0/0		
SR input (OFF)	$T_{IOSRCKO}$ / $T_{IOCKOSR}$				1.4/0		
3-State Setup Times, T input	T_{IOTCK} / T_{IOCKT}				0.9/0		
3-State Setup Times, TCE input	$T_{IOTCECK}$ $T_{IOCKTCE}$				1.1/0		
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}$ $T_{IOCKTSR}$				1.3/0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2.375 V ≤V_{CCINT} ≤2.625 V 1.2 V ≤ V_{CCO} ≤ 3.6 V (-55°C ≤ T_C ≤+125°C for ceramic packages) (-55°C ≤ T_J ≤+125°C for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Set/Reset Delays							
SR input to Pad (asynchronous)	T_{IOSRP}		9, 10, 11	01		4.6	ns
SR input to Pad high-impedance (asynchronous) 8/	T_{IOSRHZ}					3.9	
SR input to valid data on Pad (asynchronous)	T_{IOSRON}					5.1	

See footnotes at end of table.

The following section is for reference only (**Not part of table I**):

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

Data Input Delay Adjustments	Symbol	Standard		Value	Units
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T_{OLVTTL_S2}	LVTTL, Slow	2 mA	17.0	ns
	T_{OLVTTL_S4}		4 mA	8.6	
	T_{OLVTTL_S6}		6 mA	5.6	
	T_{OLVTTL_S8}		8 mA	3.5	
	T_{OLVTTL_S12}		12 mA	2.2	
	T_{OLVTTL_S16}		16 mA	2.0	
	T_{OLVTTL_S24}		24 mA	1.6	
	T_{OLVTTL_F2}	LVTTL, Fast	2 mA	15.1	
	T_{OLVTTL_F4}		4 mA	6.1	
	T_{OLVTTL_F6}		6 mA	3.6	
	T_{OLVTTL_F8}		8 mA	1.2	
	T_{OLVTTL_F12}		12 mA	0	
	T_{OLVTTL_F16}		16 mA	-0.05	
	T_{OLVTTL_F24}		24 mA	-0.23	
	$T_{OLVMOS2}$	LVCMOS2		0.12	
	T_{OPC133_3}	PCI, 33 MHz, 3.3 V		2.7	
	T_{OPC133_5}	PCI, 33 MHz, 5.0 V		3.3	
	T_{OPC166_3}	PCI, 66 MHz, 3.3 V		-0.46	
	T_{OGTL}	GTL		0.6	
	T_{OGTLP}	GTL+		1.0	
	T_{OHSTL_I}	HSTL I		-0.5	
	T_{OHSTL_III}	HSTL III		-1.0	
	T_{OHSTL_IV}	HSTL IV		-1.1	
	T_{OSSTL2_I}	SSTL2 I		-0.5	
	T_{OSSTL2_II}	SSTL2 II		-1.0	
	T_{OSSTL3_I}	SSTL3 I		-0.5	
	T_{OSSTL3_II}	SSTL3 II		-1.1	
	T_{OCCT}	CTT		-0.6	
	T_{OAGP}	AGP		-1.0	

The following information on calculating T_{IOOP} as a function of capacitance is placed here for continuity and useful technical information and is not part of Table I, which continues after this information.

Calculation of T_{IOOP} as a Function of Capacitance

The values for T_{IOOP} were based on the standard capacitive Load (Csl) for each IO standard as listed below. For other capacitive loads, use the formula below to calculate the corresponding T_{IOOP}.

$$T_{IOOP} = T_{IOOP} + T_{OPadjust} + (C_{load} - Csl) * fl$$

$T_{OPadjust}$ is reported in the Output Delay Adjustment section.
C_{load} is the capacitive load for design.

Constants for Use in Calculation of T_{IOOP}		
Standard	**Csl (pF)**	**fl (ns/pF)**
LVTTL Fast Slew Rate, 2mA drive	35	0.41
LVTTL Fast Slew Rate, 4mA drive	35	0.20
LVTTL Fast Slew Rate, 6mA drive	35	0.13
LVTTL Fast Slew Rate, 8mA drive	35	0.079
LVTTL Fast Slew Rate, 12mA drive	35	0.044
LVTTL Fast Slew Rate, 16mA drive	35	0.043
LVTTL Fast Slew Rate, 24mA drive	35	0.033
LVTTL Slow Slew Rate, 2mA drive	35	0.41
LVTTL Slow Slew Rate, 4mA drive	35	0.20
LVTTL Slow Slew Rate, 6mA drive	35	0.100
LVTTL Slow Slew Rate, 8mA drive	35	0.086
LVTTL Slow Slew Rate, 12mA drive	35	0.058
LVTTL Slow Slew Rate, 16mA drive	35	0.050
LVTTL Slow Slew Rate, 24mA drive	35	0.048
LVCMOS2	35	0.041
PCI 33MHz 5V	50	0.050
PCI 33MHZ 3.3 V	10	0.050
PCI 66 MHz 3.3 V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2.375 V ≤V_{CCINT} ≤ 2.625 V 1.2 V ≤ V_{CCO} ≤ 3.6 V (-55°C ≤ T_C ≤+125°C for ceramic packages) (-55°C ≤ T_J ≤+125°C for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Clock Distribution Guidelines **Global Clock Skew**							
Global clock skew between IOB flip-flops 9/	$T_{GSKEWIOB}$		9, 10, 11	01		0.18	ns
Clock Distribution Switching Characteristics **GCLK IOB and Buffer**							
Global clock pad to output	T_{GPIO}		9, 10, 11	01		0.9	ns
Global Clock Buffer I input to O output	T_{GIO}					0.9	
CLB Switching Characteristics Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer. **Combinatorial Delays**							
4-input function: F/G inputs to X/Y outputs	T_{ILO}		9, 10, 11	01		0.8	ns
5-input function: F/G inputs to F5 output	T_{IF5}					0.9	
5-input function: F/G inputs to X output	T_{IF5X}					1.0	
6-input function: F/G inputs to Y output via F6 MUX	T_{IF6Y}					1.2	
6-input function: F5IN input to Y output	T_{F5INY}					0.5	
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}					0.8	
BY input to YB output	T_{BYYB}					0.7	
Sequential Delays							
FF clock CLK to XQ/YQ outputs	T_{CKO}		9, 10, 11	01		1.4	ns
Latch clock CLK to XQ/YQ outputs	T_{CKLO}					1.6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2.375 V ≤V_{CCINT} ≤ 2.625 V 1.2 V ≤ V_{CCO} ≤ 3.6 V (-55°C ≤ T_C ≤+125°C for ceramic packages) (-55°C ≤ T_J ≤+125°C for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Setup and Hold times before/after Clock CLK 7/	**Setup/Hold**						
4-input function: F/G Inputs	T_{ICK}/T_{CKI}		9, 10, 11	01		1.5/0	ns
5-input function: F/G inputs	T_{IF5CK}/ T_{CKIF5}					1.7/0	
6-input function: F5IN input	T_{F5INCK} T_{CKF5IN}					1.2/0	
6-input function: F/G inputs via F6 MUX	T_{IF6CK} T_{CKIF6}					1.9/0	
BX/BY inputs	T_{DICK}/ T_{CKDI}					0.8/0	
CE input	T_{CECK}/ T_{CKCE}					1.0/0	
SR/BY inputs (synchronous)	$T_{RCKTCKR}$					0.9/0	
CLOCK CLK							
Minimum Pulse Width, High	T_{CH}		9, 10, 11	01		2.0	ns
Minimum Pulse Width, Low	T_{CL}					2.0	
Set/Reset							
Minimum Pulse Width, SR/BY inputs	T_{RPW}		9, 10, 11	01		3.3	ns
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}					1.4	
Delay from GSR to XQ/YQ outputs	T_{IOGSRQ}					12.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2.375 V ≤V_{CCINT} ≤2.625 V 1.2 V ≤ V_{CCO} ≤ 3.6 V (-55°C ≤ T_C ≤+125°C for ceramic packages) (-55°C ≤ T_J ≤+125°C for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
CLB Arithmetic Switching Characteristics Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.							
Combinatorial Delays							
F operand inputs to X via XOR	T_{OPX}		9, 10, 11	01		1.0	ns
F operand input to XB output	T_{OPXB}					1.4	
F operand input to Y via XOR	T_{OPY}					2.0	
F operand input to YB output	T_{OPYB}					2.0	
F operand input to COUT output	T_{OPCYF}					1.5	
G operand inputs to Y via XOR	T_{OPGY}					1.2	
G operand input to YB output	T_{OPGYB}					2.1	
G operand input to COUT output	T_{OPCYG}					1.6	
BX initialization input to COUT	T_{BXCY}					1.1	
CIN input to X output via XOR	T_{CINX}					0.6	
CIN input to XB	T_{CINXB}					0.1	
CIN input to Y via XOR	T_{CINY}					0.6	
CIN input to YB	T_{CINYB}					0.6	
CIN input to COUT output	T_{BYP}					0.2	
Multiplier Operation							
F1/2 operand inputs to XB output via AND	T_{FANDXB}		9, 10, 11	01		0.5	ns
F1/2 operand inputs to YB output via AND	T_{FANDYB}					1.1	
F1/2 operand inputs to COUT output via AND	T_{FANDCY}					0.6	
G1/2 operand inputs to YB output via AND	T_{GANDYB}					0.7	
G1/2 operand inputs to COUT output via AND	T_{GANDCY}					0.2	
Setup and Hold Times before/after Clock CLK 7/						**Setup/Hold**	
CIN input to FFX	T_{CCKX}/ T_{CKCX}		9, 10, 11	01		1.3/0	ns
CIN input to FFY	T_{CCKY}/ T_{CKCY}					1.4/0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2.375 V ≤V_{CCINT} ≤ 2.625 V 1.2 V ≤ V_{CCO} ≤ 3.6 V (-55°C ≤ T_C ≤+125°C for ceramic packages) (-55°C ≤ T_J ≤+125°C for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
CLB Select RAM Switching Characteristics **Sequential Delays**							
Clock CLK to X/Y outputs (WE active)	T_{SHCKO}		9, 10, 11	01		3.0	ns
Shift Register Mode							
Clock CLK to X/Y outputs						3.0	
Setup and Hold Times before/after Clock CLK 7/					**Setup/Hold**		
F/G address inputs	T_{AS}/T_{AH}		9, 10, 11	01	0.7/0		ns
BX/BY data inputs (DIN)	T_{DS}/T_{DH}				0.9/0		
CE input (WE)	T_{WS}/T_{WH}				1.0/0		
Shift Register Mode							
BX/BY data inputs (DIN)	T_{SHDICK}		9, 10, 11	01	0.9		ns
CE input (WS)	T_{SHCECK}				1.0		
Clock CLK							
Minimum Pulse Width, High	T_{WPH}		9, 10, 11	01	3.1		ns
Minimum Pulse Width, Low	T_{WPL}				3.1		
Minimum clock period to meet address write cycle time	T_{WC}				6.2		
Shift Register Mode							
Minimum Pulse Width, High	T_{SRPH}		9, 10, 11	01	3.1		ns
Minimum Pulse Width, Low	T_{SRPL}				3.1		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2.375 V ≤V_{CCINT} ≤2.625 V 1.2 V ≤ V_{CCO} ≤ 3.6 V (-55°C ≤ T_C ≤+125°C for ceramic packages) (-55°C ≤ T_J ≤+125°C for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Block RAM Switching Characteristics **Sequential Delays**							
Clock CLK to DOUT output	T_{BCKO}		9, 10, 11	01		4.1	ns
Setup and Hold Times **before/after Clock CLK** 7/					**Setup/Hold**		
ADDR inputs	T_{BACK}/ T_{BCKA}		9, 10, 11	01	1.5/0		ns
DIN inputs	T_{BDCK}/' T_{BCKD}				1.5/0		
EN input	T_{BECK}/ T_{BCKE}				3.4/0		
RST input	T_{BRCK}/ T_{BCKR}				3.2/0		
WEN input	T_{BWCK}/ T_{BCKW}				3.0/0		
Clock CLK							
Minimum Pulse Width, High	T_{BPWH}		9, 10, 11	01	2.0		ns
Minimum Pulse Width, Low	T_{BPWL}				2.0		
CLKA → CLKB setup time for different ports	T_{BCCS}				4.0		
TBUF Switching Characteristics **Combinatorial Delays**							
IN input to OUT output	T_{IO}		9, 10, 11	01	0		ns
TRI input to OUT output high-impedance	T_{OFF}				0.2		
TRI input to valid data on OUT output	T_{ON}				0.2		
JTAG Test Access Port Switching Characteristics							
TMS and TDI Setup times before TCK	T_{TAPTCK}		9, 10, 11	01	4.0		ns
TMS and TDI Hold times after TCK	T_{CKTAP}				2.0		
Output delay from clock TCK to output TDO	T_{TCKTDO}					11.0	
Maximum TCK clock frequency	F_{TCK}					33	MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2.375 V ≤V_{CCINT} ≤2.625 V 1.2 V ≤ V_{CCO} ≤ 3.6 V (-55°C ≤ T_C ≤+125°C for ceramic packages) (-55°C ≤ T_J ≤+125°C for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Pin-to-Pin Input Parameter Guidelines **Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL**							
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, with DLL. For data output with different standards, adjust delays with the values shown in Output Delay Adjustments. 10/	$T_{ICKOFDLL}$		9, 10, 11	01		3.6	ns
Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL							
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, without DLL. For data output with different standards, adjust delays with the values shown in Output Delay Adjustments. 11/	T_{ICKOF}		9, 10, 11	01		5.9	ns
Minimum Clock to Out **I/O Standard** 12/ 13/					**Minimum**		
					With DLL	**Without DLL**	
LVTTL-S2			9, 10, 11	01	5.2	6.1	ns
LVTTL-S4					3.5	4.4	
LVTTL S6					2.8	3.7	
LVTTL-S8					2.2	3.1	
LVTTL-S12					2.0	2.9	
LVTTL-S16					1.9	2.8	
LVTTL-S24					1.8	2.7	
LVTTL-F2					2.9	3.8	
LVTTL-F4					1.7	2.6	
LVTTL-F6					1.2	2.1	
LVTTL-F8					1.1	2.0	
LVTTL-F12					1.0	1.9	
LVTTL-F16					0.9	1.8	
LVTTL-F24					0.9	1.8	
LVCMOS2					1.1	2.0	
PCI33-3					1.5	2.4	
PCI33-5					1.4	2.3	
PCI66-3					1.1	2.0	
GTL					1.6	2.5	
GTL+					1.7	2.6	
HSTL I					1.1	2.0	
HSTL III					0.9	1.8	
HSTL IV					0.8	1.7	
SSTL2 I					0.9	1.8	
SSTL2 II					0.8	1.7	
SSTL3 I					0.8	1.7	
SSTL3 II					0.7	1.6	
CTT					1.0	1.9	
AGP					1.0	1.9	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2.375 V ≤V_{CCINT} ≤2.625 V 1.2 V ≤ V_{CCO} ≤ 3.6 V (-55°C ≤ T_C ≤+125°C for ceramic packages) (-55°C ≤ T_J ≤+125°C for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Pin-to-Pin Input Parameter Guidelines **Global Clock Set-Up and Hold for LVTTL Standard, *with* DLL** Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in Input Delay Adjustments							
No Delay, Global Clock and IFF, with DLL 7/ 14/ 15/	T_{PSDLL}/ T_{PHDLL}		9, 10, 11	01	2.1/-0.4		ns
Full Delay, Global Clock and IFF, without DLL 7/ 14/ 16/	T_{PSFD}/ T_{PHFD}				3.1/0.0		
DLL Timing Parameters							
Input Clock Frequency (CLKDLLHF)	$F_{CLKINHF}$		9, 10, 11	01	60	180	MHz
Input Clock Frequency (CLKDLL)	$F_{CLKINLF}$				25	90	
Input Clock Pulse Width (CLKDLLHF)	$T_{DLLPWHF}$				2.4		ns
Input Clock Pulse Width (CLKDLL)	$T_{DLLPWLF}$				3.0		
CLKDLLHF							
Input Clock Period Tolerance	T_{IPTOL}		9, 10, 11	01		1.0	ns
Input Clock Jitter (Cycle to Cycle)	T_{IJITCC}					±150	ps
Time Required for DLL to Acquire Lock	T_{LOCK}						
	F_{CLKIN}	>60MHz	9, 10, 11	01		20	µs
DLL Output skew (between any DLL output)	T_{SKEW}					±150	ps
DLL Output long term phase differential	T_{OPHASE}					±100	
DLL Output jitter cycle to cycle	T_{OJITCC}					±60	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Conditions 2.375 V ≤V_{CCINT} ≤2.625 V 1.2 V ≤ V_{CCO} ≤ 3.6 V (-55°C ≤ T_C ≤+125°C for ceramic packages) (-55°C ≤ T_J ≤+125°C for plastic packages)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
CLKDLL							
Input Clock Period Tolerance	T_{IPTOL}		9, 10, 11	01		1.0	ns
Input Clock Jitter (Cycle to Cycle)	T_{IJITCC}					±300	ps
Time Required for DLL to Acquire Lock	T_{LOCK}						
	F_{CLKIN}	>60MHz	9, 10, 11	01		20	µs
	F_{CLKIN}	50 - 60 MHz				25	
	F_{CLKIN}	40 - 50 MHz				50	
	F_{CLKIN}	30 - 40 MHz				90	
	F_{CLKIN}	25 - 30 MHz				120	
DLL Output skew (between any DLL output)	T_{SKEW}					±150	ps
DLL Output long term phase differential	T_{OPHASE}					±100	
DLL Output jitter cycle to cycle	T_{OJITCC}					±60	

1/ Pre-irradiation values for RHA marked devices shall also be the post-irradiation values, unless otherwise specified. When performing post-irradiation electrical measurements for any RHA level, T_A = +25°C. Limits shown are guaranteed at T_A = +25°C ±5°C.

2/ With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating

3/ Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

4/ Ramp rate used for this specification is from 0 - 2.7 V dc. Peak current occurs on or near the internal power-on reset threshold and lasts for less than 3 ms.

5/ Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.

6/ Larger currents may result if ramp rates are forced to be faster.

7/ A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", however, if a "0" is listed, there is no positive hold time.

8/ 3-state turn-off delays should not be adjusted.

9/ These clock-skew delays are provided for guidance only. They reflect the delays encountered in a typical design under worst-case conditions. Precise values for a particular design are provided by the timing analyzer.

10/ Listed above are representative values where one global clock-input drives one vertical clock line in each accessible column, and where all accessible lOB and CLB flip-flops are clocked by the global clock net. Output timing is measured at 50% Vcc threshold with 35 pF external capacitive load. For different loads, see page herein for the Calculation of T_{IOOP} as a Function of Capacitance. DLL output jitter is already included in the timing calculation.

11/ Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible lOB and CLB flip-flops are clocked by the global clock net. Output timing is measured at 50% Vcc threshold with 35 pF external capacitive load. For different loads, see page with Calculation of T_{IOOP} as a Function of Capacitance.

12/ S= Slow Slew Rate, F= Fast Slew Rate

13/ Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible lOB and CLB flip-flops are clocked by the global clock net. Output timing is measured at 50% Vcc threshold with 8 pF external capacitive load.

14/ IFF = Input Flip-Flop or Latch

15/ Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load. DLL output jitter is already included in the timing calculation.

16/ Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.

TABLE IB. SEP Test Limits. 1/ 2/ 3/

Symbol	Description	Min	Max	Units
TID	Total Ionizing Dose Method 1019, dose rate 50 - 300 rads(Si)/sec	100K		RAD(Si)
SEL	Single Event Latch-up Immunity LET $\leq$ 125MeV cm^2/mg		0	(cm^2/device)

1/ For SEP test conditions, see 4.4.4.4 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by TRB and qualifying activity.

3/ Worst case temperature T_A = +125°C.

***The following is not part of Table I, but is made available for information and convenience only*.**

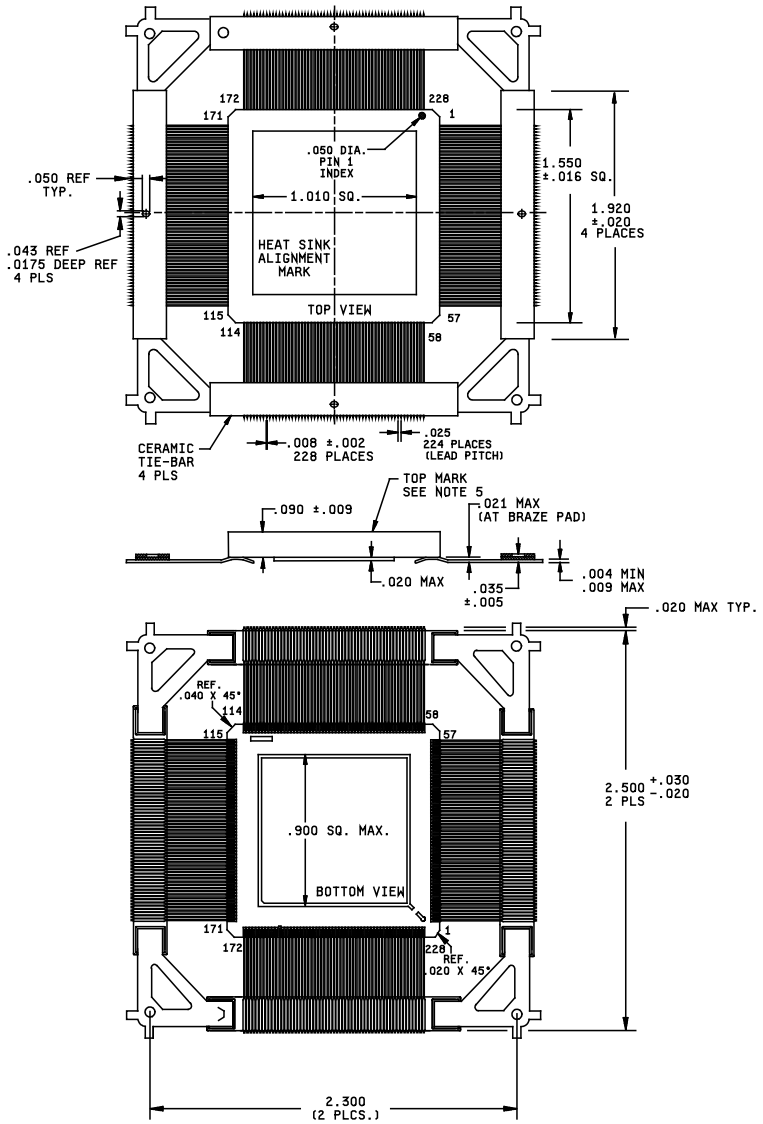
BIST AC Limits

Pattern Name	Description	Min	Max	Units
BX_X1n	CLB input BX to output X		34.0	ns
BX_X1p	CLB input BX to output X		34.0	
BX_X2n	CLB input BX to output X		34.0	
BX_X2p	CLB input BX to output X		34.0	
BX_X3n	CLB input BX to output X		34.0	
BX_X3p	CLB input BX to output X		34.0	
CRY_In	Carry Chain		37.3	
CRY_Ip	Carry Chain		37.3	
CRY_2n	Carry Chain		34.2	
CRY_2p	Carry Chain		34.2	
CRY_3n	Carry Chain		41.8	
CRY_3p	Carry Chain		41.8	
EW_Nn	Direct Lines		41.2	
EW_Np	Direct Lines		41.2	
EW_Sn	Direct Lines		41.2	
EW_Sp	Direct Lines		41.2	
G_F5 Yln	CLB input G to F5 to output Y		32.5	
G_F5 YIp	CLB input G to F5 to output Y		32.5	
G_F5 Y2n	CLB input G to F5 to output Y		32.5	
G_F5_Y2p	CLB input G to F5 to output Y		32.5	
G_Yln	CLB input G to output Y		38.0	
G_Ylp	CLB input G to output Y		38.0	
G Y2n	CLB input G to output Y		38.0	
G_Y2p	CLB input G to output Y		38.0	
GCLKn	Global Clock		41.5	
GCLKp	Global Clock		41.5	
HHEX_NWn	Horizontal Hex Lines		52.9	
HHEX_NWp	Horizontal Hex Lines		52.9	
HHEX_SEn	Horizontal Hex Lines		52.8	
HHEX_SEp	Horizontal Hex Lines		52.8	
HHEX SWn	Horizontal Hex Lines		52.9	
HHEX SWp	Horizontal Hex Lines		52.9	

This information continued on next page.

The following is not part of Table I, but is made available for information and convenience only. **BIST AC Limits**				
Pattern Name	Description	Min	Max	Units
HLL_Nn	Horizontal Long Lines		73.3	ns
HLL_Np '	Horizontal Long Lines		73.3	
HLL_Sn	Horizontal Long Lines		73.4	
HLL_Sp	Horizontal Long Lines		73.4	
NS_Nn ·	Direct Lines		36.4	
NS_Np	Direct Lines		36.4	
NS_Sn	Direct Lines		36.4	
NS_Sp	Direct Lines		36.4	
TBUF_En	3-State Buffer Lines		38.0	
TBUF_Ep	3-State Buffer Lines		38.0	
TBUF_FULLn	3-State Buffer Lines		50.5	
TBUF_FULLp	3-State Buffer Lines		50.5	
TBUF_Wn	3-State Buffer Lines		38.3	
TBUF_Wp	3-State Buffer Lines		38.3	
TILO_EWn	CLB to CLB using direct connect		47.8	
TILO_EWp	CLB to CLB using direct connect		47.8	
TILO_NEn	CLB to CLB using direct connect		47.8	
TILO_NEp	CLB to CLB using direct connect		47.8	
TILO_NWn	CLB to CLB using direct connect		47.8	
TILO_NWp	CLB to CLB using direct connect		47.8	
TILO_SEn	CLB to CLB using direct connect		47.8	
TILO_SEp	CLB to CLB using direct connect		47.8	
VHEX_NEn	Vertical Hex Lines		52.5	
VHEX_NEp	Vertical Hex Lines		52.5	
VHEX_NWn	Vertical Hex Lines		52.5	
VHEX_NWp	Vertical Hex Lines		52.5	
VHEX_SEn	Vertical Hex Lines		52.9	
VHEX_SEp	Vertical Hex Lines		52.9	
VLL_En	Vertical Long Lines		84.7	
VLL_Ep	Vertical Long Lines		84.7	
VLL_Wn	Vertical Long Lines		84.7	
VLL_Wp	Vertical Long Lines		84.7	
Pin to Pin AC Limits				
		Min	Max	Units
Itickof_4	Global Clock to Out		5.7	ns
nltickof_5	Global Clock to Out		5.7	
tnsd_l	Global Clock Setup	3.1		
tpsd_0	Global Clock Setup	3.1		
tnhd_l	Global Clock Hold	0.0		
tnhd_7	Global Clock Hold	0.0		
tphd_0	Global Clock Hold	0.0		
tphd_6	Global Clock Hold	0.0		

Case Y and Z



NOTES:

1. Dimensions are in inches.
2. Packages are shipped flat as depicted
3. Lead dimensions call out includes lead finish.
4. The leads of this package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true positions" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete. Package lead protection mechanisms (tie bars) are shown on the drawing for reference only. When microcircuit devices contained in this package style are shipped for use in Government equipment, or shipped directly to the Government as spare parts or mechanical qualification samples, lead "true position" and "coplanarity" protection shall be in place.
5. Case Y represents marking the device on the nonlid side of device, i.e., lid side facing down. When mounted in this position, the pin out is clockwise. Case Z represents marking the device on the lid side of the device i.e., lid side facing up. When mounted in this position, the pin out is counterclockwise.

FIGURE 1. Case outline.

Inch to metric conversion table for convenience only.

Inches	Metric mm
2.500	63.50
2.300	58.42
1.920	48.77
1.550	39.37
.900	22.86
.130	3.30
.125	3.18
.090	2.29
.075	1.91
.050	1.27
.043	1.09
.040	1.02
.035	.89
.030	.76
.025	.64
.021	.53
.020	.51
.0175	.44
.016	.41
.0125	.32
.009	.23
.008	.20
.005	.13
.004	.10
.002	.05

FIGURE 1. Case outline - Continued.

Cases U and N

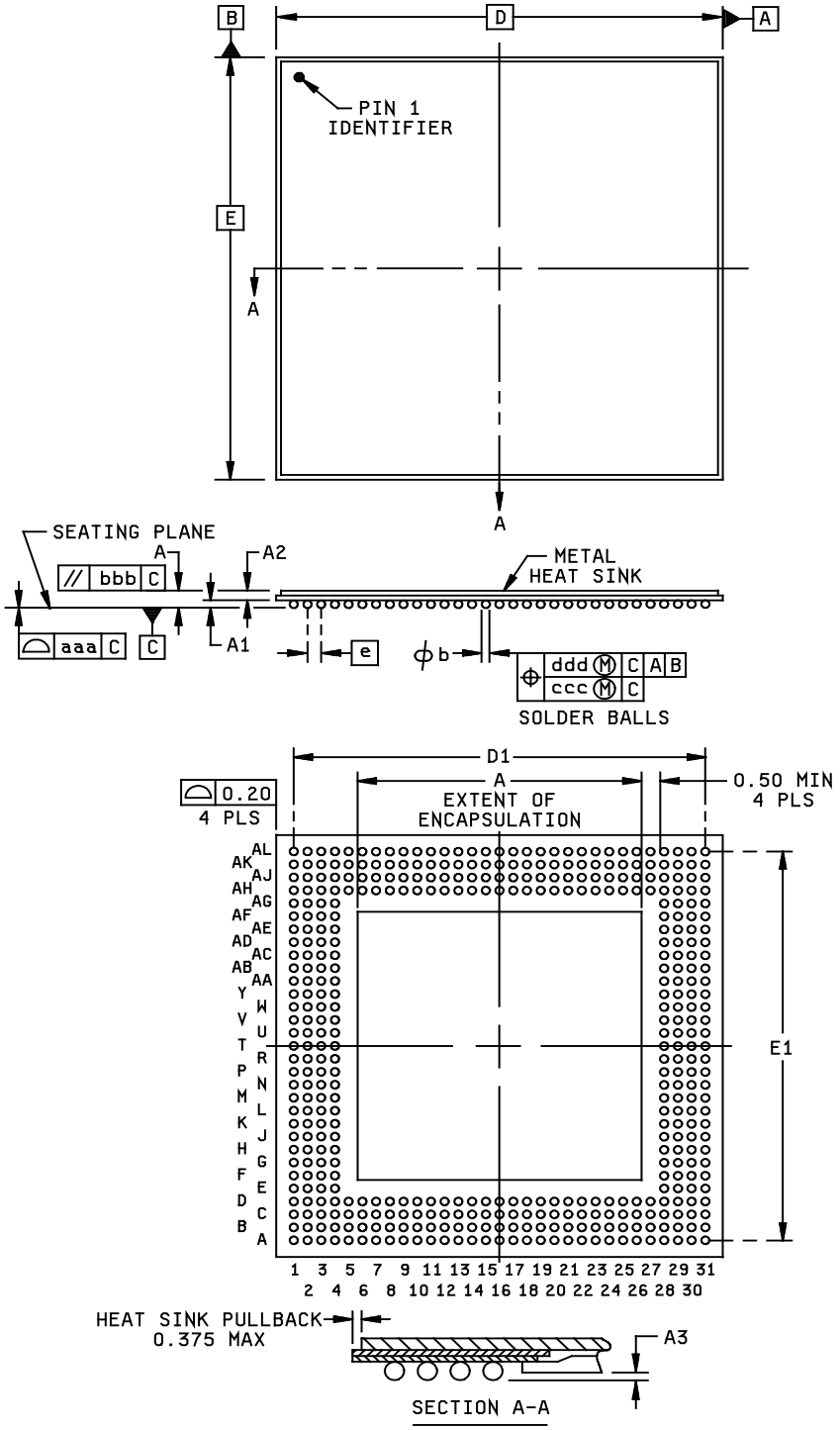


FIGURE 1. Case outline - Continued.

BG432			
Symbol	Millimeters		
	Min.	Nom.	Max.
A	1.10	1.40	1.70
A1	0.50	0.60	0.70
A2	0.60	---	1.00
A3	0.20	---	---
D/E	40.00 BSC		
D1/E1	38.10 REF		
e	1.27 BSC		
∅b	0.60	0.75	0.90
aaa	---	---	0.20
bbb	---	---	0.25
ccc	---	---	0.15
ddd	---	---	0.30
M	31 = U 26 = N		
REF	JEDEC MO-192-BAU-1 = U JEDEC MO-192-BAR-2 = N		

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M-1994.
2. Symbol "M" is the pin matrix size.
3. Conforms to JEDEC MO-192 (Depopulated).

FIGURE 1. Case outline - Continued.

Case outlines Y and Z

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
1	VSS		51	I/O_VREF_6		101	I/O
2	TMS		52	I/O		102	I/O_VREF_4
3	I/O		53	I/O		103	I/O
4	I/O		54	I/O		104	I/O
5	I/O_VREF_7		55	M1		105	I/O_VREF_4
6	I/O		56	VSS		106	VSS
7	I/O		57	M0		107	I/O
8	VSS		58	VCCO_6		108	I/O
9	I/O_VREF_7		59	M2		109	I/O_VREF_4
10	I/O		60	I/O		110	I/O
11	I/O		61	I/O		111	I/O
12	I/O_VREF_7		62	I/O		112	I/O
13	I/O		63	I/O_VREF_5		113	VSS
14	VSS		64	I/O		114	DONE
15	VCCINT		65	I/O		115	VCCO_4
16	I/O		66	VSS		116	PROGRAM
17	I/O		67	I/O_VREF_5		117	I/O_INIT
18	VCCO_7 N.C.		68	I/O		118	I/O_D7
19	I/O		69	I/O		119	I/O
20	I/O		70	I/O_VREF_5		120	I/O_VREF_3
21	I/O_VREF_7		71	I/O		121	I/O
22	I/O		72	VSS		122	I/O
23	I/O		73	VCCINT		123	VSS
24	I/O		74	I/O		124	I/O_VREF_3
25	I/O		75	I/O		125	I/O
26	I/O_IRDY		76	VCCO_5 N.C.		126	I/O
27	VSS		77	I/O		127	I/O_VREF_3
28	VCCO_7		78	I/O		128	I/O_D6
29	I/O_TRDY		79	I/O_VREF_5		129	VSS
30	VCCINT		80	I/O		130	VCCINT
31	I/O		81	I/O		131	I/O_D5
32	I/O		82	I/O		132	I/O
33	I/O		83	VCCINT		133	VCCO_3 N.C.
34	I/O_VREF_6		84	GCLK1		134	I/O
35	I/O		85	VCCO_5		135	I/O
36	I/O		86	VSS		136	I/O_VREF_3
37	VCCO_6 N.C.		87	GCLK0		137	I/O_D4
38	I/O		88	I/O		138	I/O
39	I/O		89	I/O		139	I/O
40	I/O		90	I/O		140	VCCINT
41	VCCINT		91	I/O		141	I/O_TRDY
42	VSS		92	I/O_VREF_4		142	VCCO_3
43	I/O		93	I/O		143	VSS
44	I/O_VREF_6		94	I/O		144	I/O_IRDY
45	I/O		95	VCCO_4 N.C.		145	I/O
46	I/O		96	I/O		146	I/O
47	I/O_VREF_6		97	I/O		147	I/O
48	VSS		98	I/O		148	I/O_D3
49	I/O		99	VCCINT		149	I/O_VREF_2
50	I/O		100	VSS		150	I/O

FIGURE 2. Terminal connections.

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
151	I/O		177	I/O		203	VCCINT
152	VCCO_2 N.C.		178	I/O_VREF_1		204	I/O
153	I/O		179	I/O		205	I/O
154	I/O		180	VSS		206	I/O
155	I/O_D2		181	I/O_VREF_1		207	I/O_VREF_0
156	VCCINT		182	I/O		208	I/O
157	VSS		183	I/O		209	I/O
158	I/O_D1		184	I/O_VREF_1		210	VCCO_0 N.C.
159	I/O_VREF_2		185	I/O		211	I/O
160	I/O		186	VSS		212	I/O
161	I/O		187	VCCINT		213	I/O
162	I/O_VREF_2		188	I/O		214	VCCINT
163	VSS		189	I/O		215	VSS
164	I/O		190	I/O		216	I/O
165	I/O		191	VCCO_1 N.C.		217	I/O_VREF_0
166	I/O_VREF_2		192	I/O		218	I/O
167	I/O		193	I/O		219	I/O
168	D0_DIN_I/O		194	I/O_VREF_1		220	I/O_VREF_0
169	I/O _DOUT_BUSY		195	I/O		221	VSS
170	CCLK		196	I/O		222	I/O
171	VCCO_2		197	I/O		223	I/O
172	TDO		198	I/O		224	I/O_VREF_0
173	VSS		199	GCK2		225	I/O
174	TDI		200	VSS		226	I/O
175	I/O_CS		201	VCCO_1		227	TCK
176	I/O_WRITE		202	GCK3		228	VCCO_0

FIGURE 2. Terminal connections - Continued.

Device type	All	Device type	All	Device type	All
Case outline	U	Case outline	U	Case outline	U
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	VCCO_1	B21	I/O	D10	I/O
A2	GND	B22	I/O	D11	VCC O_1
A3	GND	B23	VCCINT	D12	I/O
A4	I/O	B24	I/O	D13	I/O
A5	I/O	B25	I/O	D14	I/O
A6	I/O	B26	VCCINT	D15	I/O
A7	GND	B27	I/O	D16	GND
A8	I/O	B28	I/O	D17	GCK3
A9	GND	B29	I/O	D18	I/O
A10	VCCINT	B30	GND	D19	I/O
A11	VCCO_1	B31	GND	D20	I/O
A12	I/O	C1	GND	D21	VCCO_0
A13	I/O_VREF_1	C2	D0_DIN_I/O	D22	I/O_VREF_0
A14	GND	C3	VCCO_2	D23	I/O
A15	I/O	C4	TDO	D24	I/O_VREF_0
A16	GCK2	C5	I/O	D25	I/O
A17	VCCINT	C6	I/O_VREF_1	D26	I/O_VREF_0
A18	GND	C7	VCCINT	D27	I/O
A19	I/O	C8	I/O	D28	TCK
A20	I/O	C9	I/O	D29	TMS
A21	VCCO_0	C10	I/O	D30	I/O
A22	I/O	C11	I/O	D31	I/O
A23	GND	C12	I/O	E1	I/O
A24	I/O	C13	I/O	E2	I/O_VREF_2
A25	GND	C14	VCCINT	E3	I/O
A26	I/O	C15	I/O	E4	I/O
A27	I/O	C16	I/O	E28	I/O
A28	I/O	C17	I/O	E29	I/O
A29	GND	C18	I/O	E30	I/O
A30	GND	C19	VCCINT	E31	I/O
A31	VCCO_7	C20	I/O	F1	VCCINT
B1	GND	C21	I/O	F2	I/O
B2	GND	C22	I/O	F3	I/O
B3	TDI	C23	I/O	F4	I/O
B4	I/O_WRITE	C24	I/O	F28	I/O_VREF_7
B5	I/O	C25	I/O	F29	I/O
B6	I/O	C26	I/O	F30	VCCINT
B7	I/O_VREF-1	C27	I/O	F31	I/O_VREF_7
B8	I/O	C28	I/O	G1	GND
B9	I/O	C29	VCCO_0	G2	I/O
B10	I/O	C30	I/O	G3	I/O_VREF_2
B11	I/O	C31	GND	G4	I/O
B12	I/O	D1	I/O	G28	I/O
B13	I/O	D2	I/O	G29	I/O
B14	I/O	D3	I/O_DOUT_ BUSY	G30	I/O
B15	I/O	D4	CCLK	G31	GND
B16	I/O	D5	I/O_CS	H1	I/O
B17	I/O	D6	I/O	H2	I/O
B18	I/O	D7	I/O	H3	I/O
B19	I/O_VREF_0	D8	I/O	H4	I/O
B20	I/O	D9	I/O	H28	I/O
				H29	I/O
				H30	I/O
				H31	I/O

FIGURE 2. Terminal connections - Continued.

Device type	All	Device type	All	Device type	All
Case outline	U	Case outline	U	Case outline	U
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
J1	GND	T1	VCCINT	AC1	GND
J2	I/O_VREF_2	T2	I/O_TRDY	AC2	I/O
J3	I/O	T3	I/O_IRDY	AC3	I/O
J4	I/O	T4	GND	AC4	I/O
J28	I/O	T28	GND	AC28	I/O
J29	I/O	T29	VCCINT	AC29	I/O
J30	I/O_VREF_7	T30	I/O_TRDY	AC30	I/O
J31	GND	T31	I/O_IRDY	AC31	GND
K1	I/O	U1	I/O	AD1	I/O
K2	I/O_D2	U2	I/O	AD2	I/O
K3	VCCINT	U3	I/O	AD3	I/O
K4	I/O_D1	U4	I/O	AD4	I/O VREF_3
K28	I/O	U28	I/O	AD28	I/O
K29	VCCINT	U29	I/O	AD29	I/O
K30	I/O	U30	I/O	AD30	I/O
K31	I/O	U31	I/O	AD31	I/O
L1	VCCO_2	V1	GND	AE1	GND
L2	I/O	V2	I/O_VREF_3	AE2	I/O
L3	I/O	V3	I/O	AE3	I/O
L4	VCCO_2	V4	I/O_D4	AE4	I/O
L28	VCCO_7	V28	I/O_VREF_6	AE28	I/O
L29	I/O	V29	I/O	AE29	VCCINT
L30	I/O	V30	I/O	AE30	I/O VREF_6
L31	VCCO_7	V31	GND	AE31	GND
M1	I/O	W1	I/O	AF1	VCCINT
M2	I/O	W2	VCCINT	AF2	I/O
M3	I/O	W3	I/O	AF3	I/O_VREF_3
M4	I/O	W4	I/O	AF4	I/O
M28	I/O	W28	I/O	AF28	I/O_VREF_6
M29	I/O	W29	I/O	AF29	I/O
M30	I/O	W30	I/O	AF30	I/O
M31	I/O	W31	VCCINT	AF31	I/O
N1	I/O_VREF_2	Y1	I/O	AG1	I/O
N2	VCCINT	Y2	I/O	AG2	I/O
N3	I/O	Y3	I/O	AG3	I/O
N4	I/O	Y4	I/O	AG4	I/O_D7
N28	I/O	Y28	I/O	AG28	I/O
N29	VCCINT	Y29	I/O	AG29	I/O
N30	I/O_VREF_7	Y30	I/O	AG30	I/O
N31	I/O	Y31	I/O	AG31	I/O
P1	GND	AA1	VCCO_3	AH1	I/O
P2	I/O	AA2	I/O	AH2	I/O
P3	I/O	AA3	I/O	AH3	PROGRAM
P4	I/O_D3	AA4	VCCO_3	AH4	DONE
P28	I/O	AA28	VCCO_6	AH5	I/O
P29	I/O	AA29	I/O	AH6	I/O
P30	I/O	AA30	I/O	AH7	I/O
P31	GND	AA31	VCCO_6	AH8	VCCINT
R1	I/O	AB1	I/O_D5	AH9	I/O
R2	I/O	AB2	VCCINT	AH10	I/O
R3	I/O	AB3	I/O_D6	AH11	VCCO_4
R4	I/O	AB4	I/O VREF_3	AH12	I/O
R28	I/O	AB28	I/O VREF_6	AH13	I/O
R29	I/O	AB29	I/O	AH14	I/O
R30	I/O	AB30	VCCINT	AH15	I/O
R31	I/O	AB31	I/O		

FIGURE 2. Terminal connections - Continued.

Device type	All	Device type	All	Device type	All
Case outline	U	Case outline	U	Case outline	U
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
AH16	GND	AJ22	I/O	AK28	I/O
AH17	I/O	AJ23	I/O	AK29	DXP
AH18	I/O	AJ24	I/O	AK30	GND
AH19	I/O	AJ25	I/O_VREF_5	AK31	GND
AH20	I/O	AJ26	I/O	AL1	VCCO_4
AH21	VCCO_5	AJ27	I/O	AL2	GND
AH22	I/O	AJ28	M2	AL3	GND
AH23	I/O	AJ29	VCCO_5	AL4	I/O_VREF_4
AH24	VCCINT	AJ30	I/O	AL5	I/O
AH25	I/O	AJ31	GND	AL6	I/O
AH26	I/O	AK1	GND	AL7	GND
AH27	DXN	AK2	GND	AL8	I/O_VREF_4
AH28	M0	AK3	I/O	AL9	GND
AH29	M1	AK4	I/O	AL10	I/O
AH30	I/O	AK5	I/O	AL11	VCCO_4
AH31	I/O	AK6	I/O	AL12	I/O
AJ1	GND	AK7	I/O	AL13	I/O_VREF_4
AJ2	I/O_INIT	AK8	I/O	AL14	GND
AJ3	VCCO_3	AK9	I/O	AL15	I/O
AJ4	I/O	AK10	I/O	AL16	GCK0
AJ5	I/O	AK11	I/O	AL17	I/O
AJ6	I/O	AK12	I/O	AL18	GND
AJ7	I/O_VREF_4	AK13	VCCINT	AL19	I/O
AJ8	I/O	AK14	I/O	AL20	I/O
AJ9	I/O	AK15	I/O	AL21	VCCO_5
AJ10	VCCINT	AK16	GCK1	AL22	I/O
AJ11	I/O	AK17	I/O	AL23	GND
AJ12	I/O	AK18	I/O	AL24	I/O
AJ13	I/O	AK19	VCCINT	AL25	GND
AJ14	I/O	AK20	I/O	AL26	I/O
AJ15	I/O	AK21	I/O	AL27	I/O
AJ16	VCCINT	AK22	VCCINT	AL28	I/O
AJ17	I/O	AK23	I/O_VREF_5	AL29	GND
AJ18	I/O_VREF_5	AK24	I/O	AL30	GND
AJ19	I/O	AK25	I/O	AL31	VCCO_6
AJ20	I/O	AK26	I/O		
AJ21	I/O	AK27	I/O_VREF_5		

FIGURE 2. Terminal connections - Continued.

Device type	All	Device type	All	Device type	All
Case outline	T	Case outline	T	Case outline	T
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
P1	VSS	P50	I/O_VREF_6	P100	I/O
P2	TMS	P51	VSS	P101	I/O
P3	I/O	P52	I/O	P102	I/O
P4	I/O	P53	I/O	P103	I/O
P5	I/O_VREF_7	P54	I/O_VREF_6	P104	VCCINT
P6	I/O	P55	I/O	P105	VCCO_4
P7	I/O	P56	I/O	P106	VSS
P8	VSS	P57	I/O	P107	I/O
P9	I/O_VREF_7	P58	M1	P108	I/O_VREF_4
P10	I/O	P59	VSS	P109	I/O
P11	I/O	P60	M0	P110	I/O
P12	I/O_VREF_7	P61	VCCO_6	P111	I/O_VREF_4
P13	I/O	P62	M2	P112	VSS
P14	VSS	P63	I/O	P113	I/O
P15	VCCO_7	P64	I/O	P114	I/O
P16	VCCINT	P65	I/O	P115	I/O_VREF_4
P17	I/O	P66	I/O_VREF_5	P116	I/O
P18	I/O	P67	I/O	P117	I/O
P19	I/O	P68	I/O	P118	I/O
P20	I/O	P69	VSS	P119	VSS
P21	I/O	P70	I/O_VREF_5	P120	DONE
P22	VSS	P71	I/O	P121	VCCO_4
P23	I/O_VREF_7	P72	I/O		
P24	I/O	P73	I/O_VREF_5	P122	PROGRAM
P25	I/O	P74	I/O	P123	I/O_INIT
P26	I/O	P75	VSS	P124	I/O_D7
P27	I/O	P76	VCCO_5	P125	I/O
P28	I/O_IRDY	P77	VCCINT	P126	I/O_VREF_3
P29	VSS	P78	I/O	P127	I/O
P30	VCCO_6	P79	I/O	P128	I/O
P31	I/O_TRDY	P80	I/O	P129	VSS
P32	VCCINT	P81	I/O	P130	I/O_VREF_3
P33	I/O	P82	I/O	P131	I/O
P34	I/O	P83	VSS	P132	I/O
P35	I/O	P84	I/O_VREF_5	P133	I/O_VREF_3
P36	I/O_VREF_6	P85	I/O	P134	I/O_D6
P37	VSS	P86	I/O	P135	VSS
P38	I/O	P87	I/O	P136	VCCO_3
P39	I/O	P88	VCCINT	P137	VCCINT
P40	I/O	P89	GCK1	P138	I/O_D5
P41	I/O	P90	VCCO_5	P139	I/O
P42	I/O	P91	VSS	P140	I/O
P43	VCCINT	P92	GCK0	P141	I/O
P44	VCCO_6	P93	I/O	P142	I/O
P45	VSS	P94	I/O	P143	VSS
P46	I/O	P95	I/O	P144	I/O_VREF_3
P47	I/O	P96	I/O	P145	I/O_D4
P48	I/O	P97	I/O_VREF_4	P146	I/O
P49	I/O	P98	VSS	P147	I/O
		P99	I/O	P148	VCCINT
				P149	I/O_TRDY

FIGURE 2. Terminal connections - Continued.

Device type	All	Device type	All	Device type	All
Case outline	T	Case outline	T	Case outline	T
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
P150	VCCO_3	P180	VCCO_1	P211	VSS
P151	VSS	P181	TDO	P212	VCCO_0
P152	I/O_IRDY	P182	VSS	P213	GCK3
P153	I/O	P183	TDI	P214	VCCINT
P154	I/O	P184	I/O_CS	P215	I/O
P155	I/O	P185	I/O_WRITE	P216	I/O
P156	I/O_D3	P186	I/O	P217	I/O
P157	I/O_VREF_2	P187	I/O_VREF_1	P218	I/O_VREF_0
P158	VSS	P188	I/O	P219	VSS
P159	I/O	P189	I/O	P220	I/O
P160	I/O	P190	VSS	P221	I/O
P161	I/O	P191	I/O_VREF_1	P222	I/O
P162	I/O	P192	I/O	P223	I/O
P163	I/O_D2	P193	I/O	P224	I/O
P164	VCCINT	P194	I/O_VREF_1	P225	VCCINT
P165	VCCO_2	P195	I/O	P226	VCCO_0
P166	VSS	P196	VSS	P227	VSS
P167	I/O_D1	P197	VCCO_1	P228	I/O
P168	I/O_VREF_2	P198	VCCINT	P229	I/O_VREF_0
P169	I/O	P199	I/O	P230	I/O
P170	I/O	P200	I/O	P231	I/O
P171	I/O_VREF_2	P201	I/O	P232	I/O_VREF_0
P172	VSS	P202	I/O	P233	VSS
P173	I/O	P203	I/O	P234	I/O
P174	I/O	P204	VSS	P235	I/O
P175	I/O_VREF_2	P205	I/O_VREF_1	P236	I/O_VREF_0
P176	I/O	P206	I/O	P237	I/O
P177	D0_DIN_I/O	P207	I/O	P238	I/O
P178	I/O _DOUT_BUSY	P208	I/O	P239	TCK
P179	CCLK	P209	I/O	P240	VCCO_7
		P210	GCK2		

FIGURE 2. Terminal connections - Continued.

Device type	All	Device type	All	Device type	All
Case outline	N	Case outline	N	Case outline	N
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	GND	B21	I/O	D15	I/O
A2	GND	B22	I/O	D16	I/O
A3	I/O	B23	I/O	D17	I/O
A4	I/O	B24	I/O	D18	I/O
A5	GND	B25	VCCO_0	D19	VCCO_0
A6	I/O	B26	GND	D20	I/O
A7	I/O	C1	I/O	D21	I/O_VREF_0
A8	GND	C2	I/O	D22	I/O
A9	I/O	C3	CCLK	D23	TMS
A10	VCCO_1	C4	I/O_CS	D24	IO
A11	I/O	C5	I/O	D25	IO
A12	I/O	C6	I/O	D26	I/O_VREF_7
A13	I/O	C7	I/O	E1	GND
A14	GND	C8	I/O	E2	I/O_VREF_2
A15	I/O	C9	I/O_VREF_1	E3	I/O
A16	I/O_VREF_0	C10	I/O	E4	I/O_DOUT_BUSY
A17	VCCO_0	C11	I/O	E23	I/O
A18	I/O	C12	I/O_VREF_1	E24	I/O_VREF_7
A19	GND	C13	I/O	E25	I/O
A20	VCCINT	C14	VCCINT	E26	GND
A21	I/O	C15	I/O	F1	I/O
A22	GND	C16	I/O	F2	I/O
A23	I/O	C17	I/O	F3	I/O
A24	I/O	C18	I/O	F4	I/O
A25	GND	C19	I/O_VREF_0	F23	I/O
A26	GND	C20	I/O	F24	I/O
B1	GND	C21	I/O_VREF_0	F25	I/O
B2	VCCO_2	C22	I/O	F26	I/O
B3	TDI	C23	I/O	G1	I/O_D1
B4	I/O	C24	TCK	G2	I/O
B5	I/O	C25	I/O	G3	I/O
B6	I/O_VREF_1	C26	I/O	G4	I/O
B7	I/O	D1	I/O	G23	VCCO_7
B8	I/O	D2	I/O_VREF_2	G24	I/O
B9	I/O	D3	I/O_DIN_D0	G25	I/O
B10	I/O	D4	TDO	G26	I/O_VREF_7
B11	I/O	D5	I/O_WRITE	H1	GND
B12	I/O	D6	I/O_VREF_1	H2	I/O_VREF_2
B13	I/O	D7	VCCO_1	H3	I/O
B14	GCK2	D8	I/O	H4	VCCO_2
B15	I/O	D9	I/O	H23	I/O
B16	VCCINT	D10	VCCINT	H24	I/O
B17	I/O	D11	I/O	H25	I/O
B18	I/O	D12	VCCINT	H26	GND
B19	I/O	D13	VCCO_1		
B20	I/O	D14	GCK3		

FIGURE 2. Terminal connections - Continued.

Device type	All	Device type	All	Device type	All
Case outline	N	Case outline	N	Case outline	N
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
J1	I/O	R1	I/O	AA1	I/O
J2	I/O	R2	I/O	AA2	I/O
J3	I/O_D2	R3	I/O_D4	AA3	I/O
J4	I/O	R4	I/O_VREF_3	AA4	I/O
J23	I/O	R23	VCCINT	AA23	I/O
J24	VCCINT	R24	I/O_VREF_6	AA24	I/O
J25	I/O	R25	I/O	AA25	I/O_VREF_6
J26	I/O	R26	I/O	AA26	I/O
K1	VCCO_2	T1	VCCINT	AB1	GND
K2	I/O	T2	I/O	AB2	I/O
K3	I/O	T3	I/O	AB3	I/O
K4	VCCINT	T4	I/O	AB4	I/O
K23	I/O	T23	I/O	AB23	M1
K24	I/O	T24	I/O	AB24	I/O
K25	I/O	T25	I/O	AB25	I/O
K26	VCCO_7	T26	I/O	AB26	GND
L1	VCCINT	U1	VCCO_3	AC1	I/O
L2	I/O	U2	I/O	AC2	I/O_VREF_3
L3	I/O	U3	I/O	AC3	I/O_D7
L4	I/O	U4	I/O_D5	AC4	PROGRAM
L23	I/O	U23	I/O	AC5	I/O
L24	I/O	U24	I/O	AC6	I/O
L25	VCCINT	U25	I/O	AC7	I/O
L26	I/O_VREF_7	U26	VCCO_6	AC8	VCCO_4
M1	I/O	V1	I/O	AC9	I/O
M2	I/O	V2	I/O	AC10	VCCINT
M3	I/O_D3	V3	I/O_D6	AC11	I/O
M4	I/O_VREF_2	V4	I/O_VREF_3	AC12	I/O_VREF_4
M23	I/O	V23	I/O	AC13	I/O
M24	I/O	V24	VCCINT	AC14	VCCO_5
M25	I/O	V25	I/O	AC15	I/O_VREF_5
M26	I/O	V26	I/O	AC16	I/O
N1	GND	W1	GND	AC17	I/O
N2	I/O_IRDY	W2	VCCINT	AC18	I/O_VREF_5
N3	I/O	W3	I/O	AC19	I/O
N4	I/O	W4	I/O	AC20	VCCO_5
N23	VCCO_7	W23	VCCO_6	AC21	I/O
N24	I/O	W24	I/O	AC22	I/O
N25	I/O_IRDY	W25	I/O	AC23	M2
N26	I/O_TRDY	W26	GND	AC24	I/O
P1	I/O_TRDY	Y1	I/O	AC25	I/O
P2	VCCINT	Y2	I/O	AC26	I/O
P3	I/O	Y3	I/O_VREF_3		
P4	VCCO_3	Y4	VCCO_3		
P23	I/O	Y23	I/O		
P24	I/O	Y24	I/O		
P25	VCCINT	Y25	I/O		
P26	GND	Y26	I/O_VREF_6		

FIGURE 2. Terminal connections - Continued.

Device type	All	Device type	All	Device type	All
Case outline	N	Case outline	N	Case outline	N
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
AD1	I/O	AE1	GND	AF1	GND
AD2	I/O_INIT	AE2	VCCO_4	AF2	GND
AD3	DONE	AE3	I/O	AF3	I/O
AD4	I/O	AE4	I/O_VREF_4	AF4	I/O
AD5	I/O	AE5	I/O_VREF_4	AF5	GND
AD6	I/O	AE6	I/O	AF6	I/O
AD7	I/O	AE7	I/O	AF7	I/O
AD8	I/O	AE8	I/O_VREF_4	AF8	GND
AD9	I/O	AE9	I/O	AF9	I/O
AD10	I/O	AE10	I/O	AF10	VCCO_4
AD11	I/O	AE11	I/O	AF11	VCCINT
AD12	I/O	AE12	I/O	AF12	I/O
AD13	I/O	AE13	GCK0	AF13	GND
AD14	I/O	AE14	VCCINT	AF14	GCK1
AD15	I/O	AE15	I/O	AF15	I/O
AD16	I/O	AE16	I/O	AF16	VCCINT
AD17	I/O	AE17	I/O	AF17	VCCO_5
AD18	I/O	AE18	I/O	AF18	I/O
AD19	I/O	AE19	VCCINT	AF19	GND
AD20	I/O_VREF_5	AE20	I/O	AF20	I/O
AD21	I/O	AE21	I/O	AF21	I/O
AD22	I/O	AE22	I/O	AF22	GND
AD23	DXN	AE23	I/O_VREF_5	AF23	I/O
AD24	M0	AE24	DXP	AF24	I/O
AD25	I/O	AE25	VCCO_6	AF25	GND
AD26	I/O_VREF_6	AE26	GND	AF26	GND

FIGURE 2. Terminal connections - Continued.

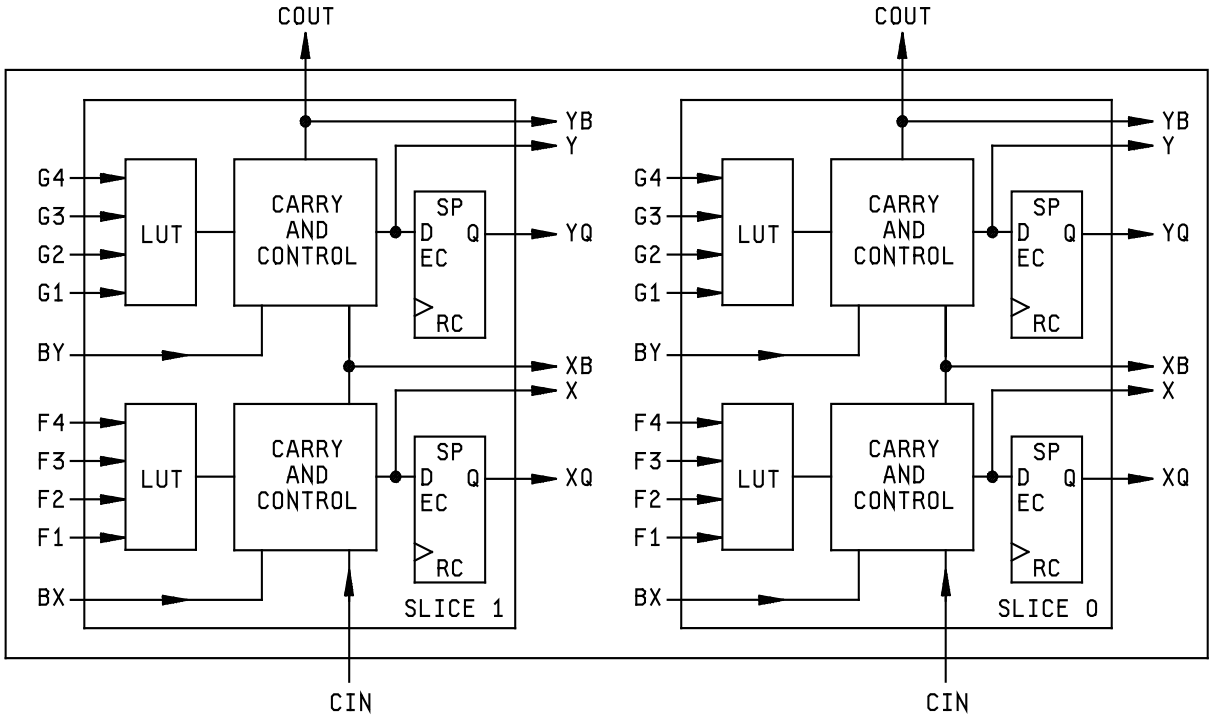


FIGURE 3. Logic block diagrams.

Detailed view of slice

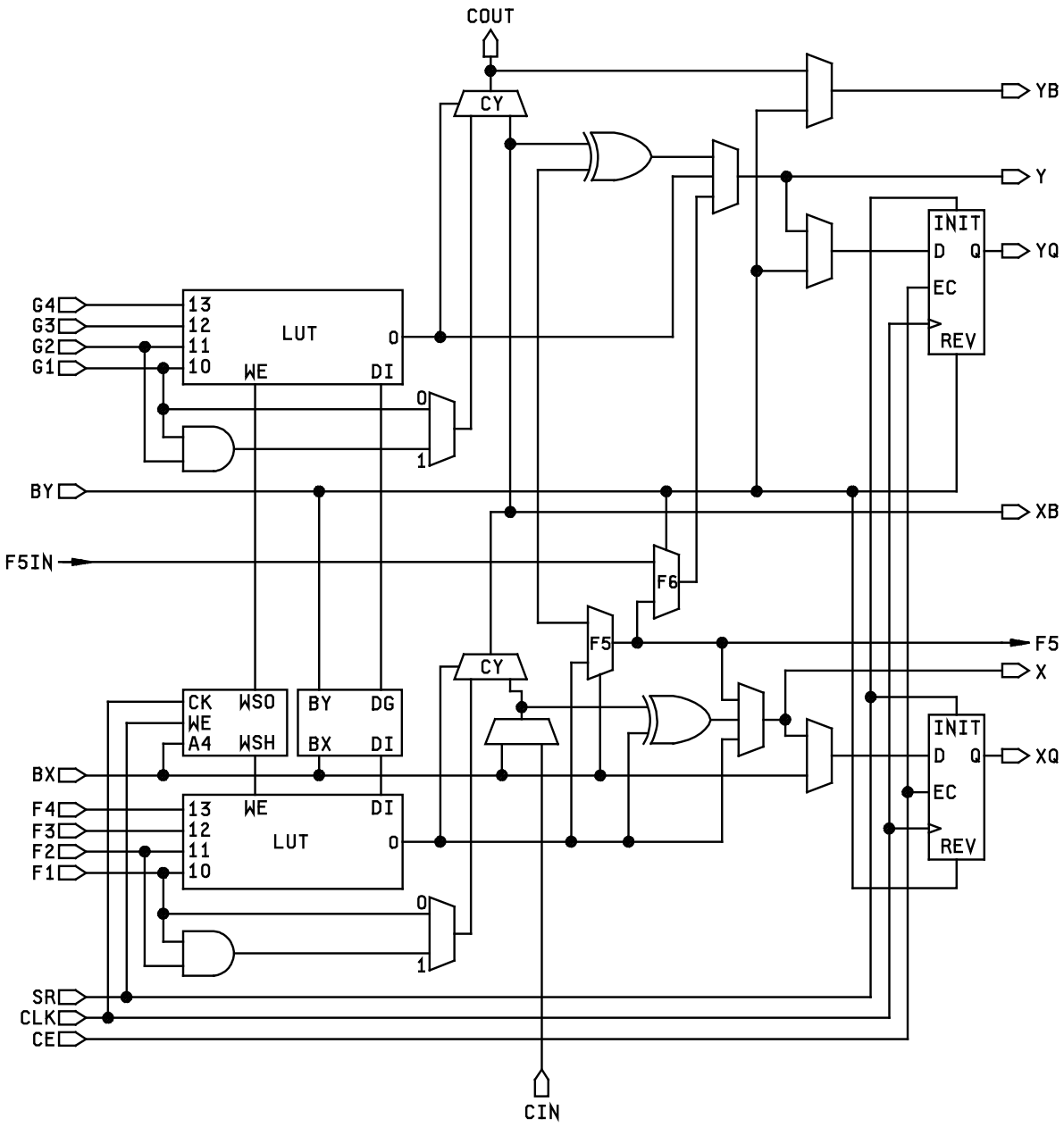


FIGURE 3. Logic block diagrams - Continued.

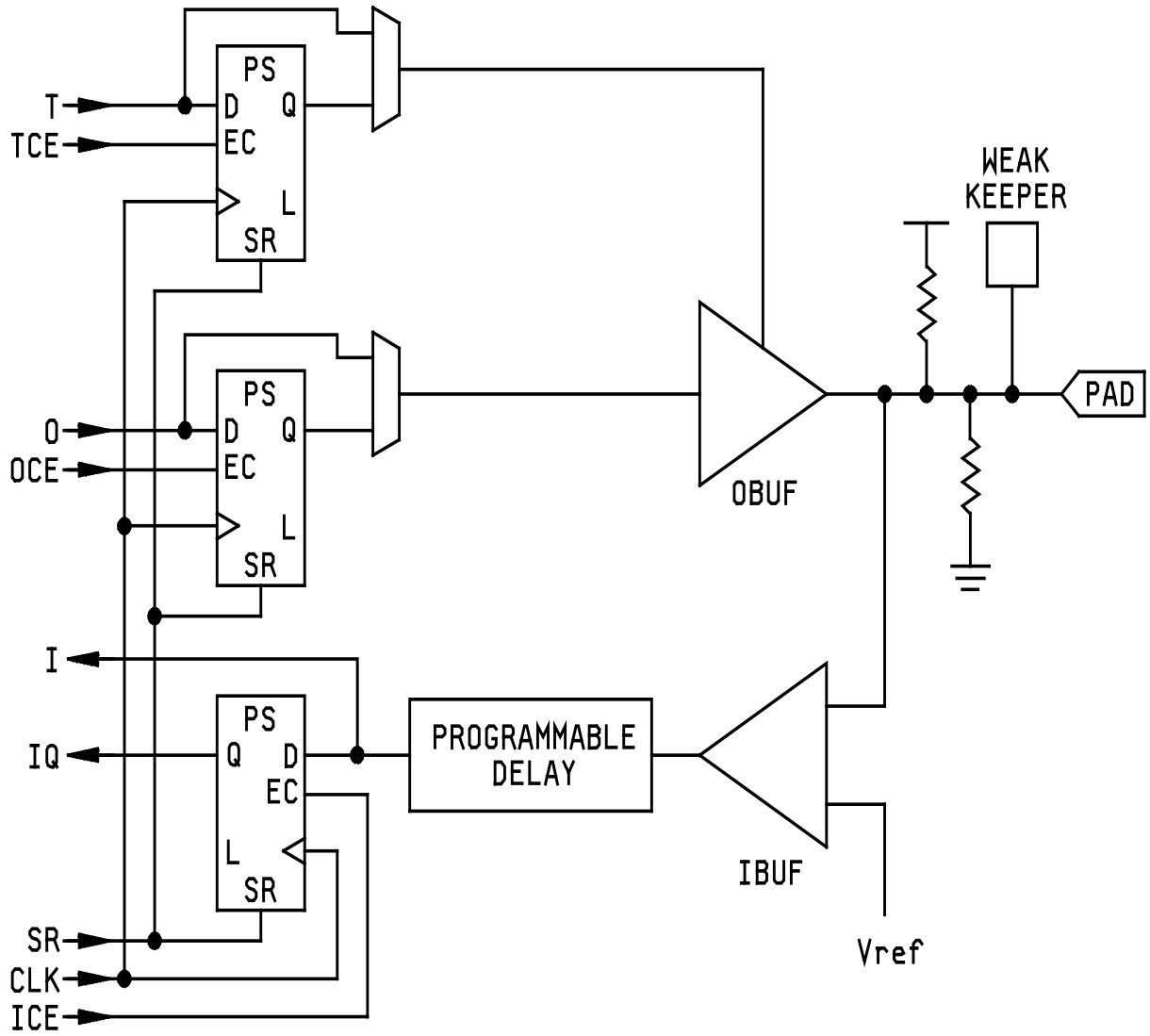
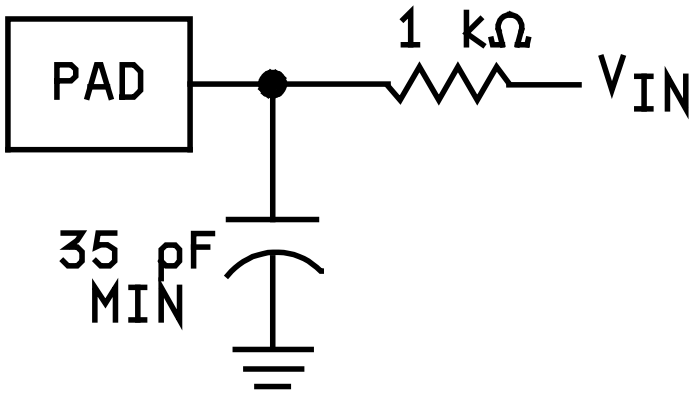
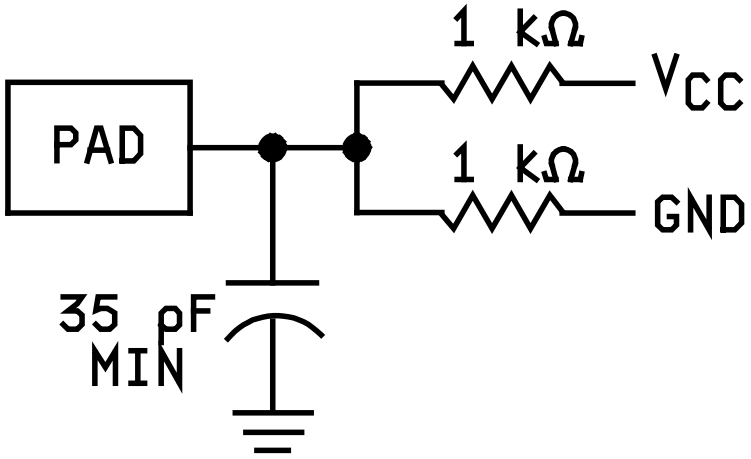


FIGURE 3. Logic block diagrams - Continued.



CIRCUIT A



CIRCUIT B

FIGURE 4. Load circuits.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device classes N, Q, and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device classes N, Q, and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on three devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is three (3) devices with no failures, and all input and output terminals tested.

(1) The following shall apply to device class N only. Sample size is five (5) devices with no failures. For C_{IN} and C_{OUT} a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, which by design will yield the same capacitance values when tested in accordance with table I herein. The device manufacturer shall set a functional group limit for the C_{IN} and C_{OUT} tests. The device manufacturer may then test one device function from a functional group to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I herein. Listings of the device functions in each functional group and the test results shall be under document control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes N, Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

Line no.	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)		
		Device class N	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1, 7, 9
2	Static burn-in I and II (method 1015)	Not Required	Required	Required
3	Same as line 1			1*, 7*
4	Dynamic burn-in (method 1015)	Not Required	Not Required	Required
5	Same as line 1			1*, 7*
6	Final electrical parameters	2, 8A, 10	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test parameters	2, 8A, 10	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11
9	Group D end-point electrical parameters	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7, 8A, and 8B functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ See 4.4.1d.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q, V, and N, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). Accelerated annealing tests shall be performed in accordance with MIL-STD-883 method 1019 condition B, and as specified herein. The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at +25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified in 1.5 herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and in 1.5 herein.

a. Transient dose rate upset testing for classes Q, V, and N devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on Q, V, and N devices marked as RHA devices, the SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be V_{DD} = 2.5 V dc for the upset measurements and V_{DD} = 2.5 V dc for the latchup measurements.

g. For SEP test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q, and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and vendor's data book.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes N, Q, and V. Sources of supply for device classes N, Q, and V are listed in QML-38535 and MIL-HDBK-103. The vendors listed in QML-38535 and MIL-HDBK-103 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 BGA packages lead finish: Microcircuit devices using ball grid array (BGA) packages are supplied to this drawing with terminal lead finish mark "A". Terminal lead finish A for devices listed on this drawing are a tin (Sn) and lead (Pb) alloy. The solder ball material contains compositions of Sn = 63% and Pb = 37%.

6.8 Additional operating data.

a. Power on delay is 2^{14} cycles from the non-master mode. This provides 11 to 33 ms of wait time.

b. Power on delay is 2^{16} cycles for the master mode. This provides 43 to 130 ms of wait time.

c. Clear is 375 cycles $\pm$25 cycles and may take as long as 250 to 750 μs.

d. During normal power up, V_{CCINT} must rise from 1.0 V to 2.375 V minimum in less than 50 ms. If this does not occur, configuration must be delayed by using RESET.

6.9 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latch-up (SEP).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-09-19

Approved sources of supply for SMD 5962-99572 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/ 2/	Vendor CAGE number	Vendor similar PIN 3/
5962-9957201QYC	68994	XQV300-4CB228
5962R9957201QYC	68994	XQVR300-4CB228
5962-9957201QZC	68994	XQV300-4CB228
5962R9957201QZC	68994	XQVR300-4CB228
5962-9957201NNA	68994	XQV300-4BG352N
5962-9957201NUA	68994	XQV300-4BG432
5962R9957201NUA	68994	XQVR300-4BG432
5962-9957201NTB	68994	XQV300-4PQ240
5962R9957201NTB	68994	XQVR300-4PQ240

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ See 1.2.4 for description of the actual case outline lead finish.

3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
68994	Xilinx, Incorporated 2100 Logic Drive San Jose, CA 95124