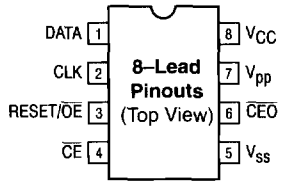
Product Preview

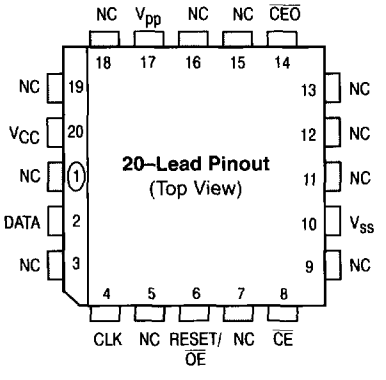
128K Serial EPROM

The MCP17128 serial OTP EPROM is the companion serial EPROM to the MPA1036 Field Programmable Gate Array. When used with the MPA1036, it provides a compact, low pin count, non–volatile configuration code store, with the FPGA automatically configuring on power–up or BFR (Boot From ROM) request.

The MCP17128 can also be cascaded for increased memory storage when needed. It is available in the standard 8–pin plastic DIP (N suffix), 8–pin SOIC (D suffix) and 20–pin PLCC (FN suffix) packages.

- Configuration EPROM for MPA1036 Field Programmable Gate Array
- Voltage Range — 4.5 to 6.0V
- Maximum Read Current of 10mA at 5.0V
- Standby Current of 10μA, Typical
- Industry Standard Synchronous Serial Interface/1 Bit per Rising Edge of Clock
- Full Static Operation
- Sequential Read/Program
- Cascadable Output Enable
- 10MHz Maximum Clock Rate at 5.0Vdc
- Programmable Polarity on Hardware Reset
- Programming With Industry Standard EPROM Programmers
- Electrostatic Discharge Protection > 2000 Volts
- 8–Pin PDIP and SOIC; 20–Pin PLCC Packages
- Commercial (0 to +70°C) and Industrial (–40 to +85°C) Temperature Ranges





MCP17128

128K SERIAL EPROM

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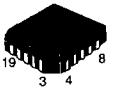
N SUFFIX
PLASTIC PACKAGE
CASE 626–05

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–05



FN SUFFIX
PLCC PACKAGE
CASE 775–02

PIN NAMES

Pins	Function
DATA	Data I/O
CLK	Clock
RESET/$\overline{OE}$	Reset Input and Output Enable
$\overline{CE}$	Chip Enable Input
V_{SS}	Ground
$\overline{CEO}$	Chip Enable Output
V_{PP}	Programming Voltage Supply
V_{CC}	+4.5 to 6.0V Power Supply
NC	Not Connected

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MOTOROLA

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
	V_{CC} and Input Voltages W.R.T. V_{SS}	–6.0 to V_{DD} + 0.6	V
	V_{PP} Voltage W.R.T. V_{SS} During Programming	–0.6 to +14.0	V
	Output Voltage W.R.T. V_{SS}	–0.6 to V_{CC} + 0.6	V
	Storage Temperature Range	–65 to +150	°C
	Ambient Temperature With Power Applied	–65 to +125	°C
	Soldering Temperature of Leads (10 Seconds)	+300	°C
	ESD Protection on All Leads	≥2	kV

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NOTE: Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

DC CHARACTERISTICS (V_{CC} = 4.5 to 6.0V; Commercial (C) T_A = 0 to +70°C; Industrial (I) T_A = –40 to +85°C)

Symbol	Characteristic		Min	Max	Unit	Condition
V_{IH}	Input Voltage High	DATA, $\overline{CE}$, $\overline{CEO}$, Reset	2.0	V_{CC}	V	
V_{IL}	Input Voltage Low	DATA, $\overline{CE}$, $\overline{CEO}$, Reset	–0.3	0.8	V	
V_{OH}	Output Voltage High	DATA, $\overline{CE}$, $\overline{CEO}$, Reset	3.86 2.40		V	I_{OH} = –4mA; V_{CC} ≥ 4.5V
V_{OL}	Output Voltage Low	DATA, $\overline{CE}$, $\overline{CEO}$, Reset		0.32	V	I_{OL} = 4.0mA
I_{LI}	Input Leakage Current		–10	10	µA	V_{IN} = 0.1V to V_{CC}
I_{LO}	Output Leakage Current		–10	10	µA	V_{OUT} = 0.1V to V_{CC}
C_{INT}	Internal Capacitance	(All Inputs/Outputs)		10	pF	V_{CC} = 5.0V (Note 1); T_A = 25°C; f_{clk} = 1MHz
I_{CC} Read	Operating Current			10	mA	V_{CC} = 6.0V; CLK = 10MHz
I_{CCS}	Standby Current			500	µA	V_{CC} = 6.0V

1. This parameter is initially characterized and not 100% tested.

Applications Information

DATA

Three–state DATA output for reading and function as the input during programming.

CLOCK

Clock input. Used to increment the internal address and bit counters for reading and programing.

RESET/$\overline{OE}$

Reset and Output Enable input. A Low level both the $\overline{CE}$ and RESET/$\overline{OE}$ inputs enables the data output driver. A High level on RESET/$\overline{OE}$ resets both the address and bit counters. In the MCP17128, the logic polarity of this input is programmable as either RESET/$\overline{OE}$ or $\overline{OE}$/RESET. This document describes the pin as RESET/$\overline{OE}$ although the opposite polarity is also possible, this option is defined and set at device program time.

$\overline{CE}$

Chip Enable input. Used for device selection. A Low level on both $\overline{CE}$ and $\overline{OE}$ enables the data output driver. A High level on $\overline{CE}$ disables both the address and bit counters and forces the device into a low power mode.

$\overline{CEO}$

Chip Enable Out output. This signal is asserted Low on the clock cycle following the last bit read from the memory. It will stay Low as long as $\overline{CE}$ and $\overline{OE}$ are both Low. It will then follow $\overline{CE}$ until $\overline{OE}$ goes High. Thereafter $\overline{CEO}$ will stay High until the entire PROM is read again. This pin also used to sense the status of RESET polarity when program mode is entered.

V_{PP}

Programming Voltage Supply. Used to enter programming mode (+10V) and to program the memory (+13V) Must be connected directly to V_{CC} for normal Read operation. No overshoot above +15.5V permitted.

CONTROLLING THE MCP17128 SERIAL PROMS

The connections between the FPGA device and the Serial PROM are as follows:

- The DATA output of the MCP17128 drives DO (data in) of the FPGA devices.
- The CLK input of the MCP17128 is driven by the master FPGA DCLK (configuration clock) output.
- The MCP17128 can be cascaded by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the next MCP17128.
- For normal Read operations V_{PP} must be connected to V_{CC}. Do not leave V_{PP} open.

There are two different ways to use the inputs $\overline{CE}$ and $\overline{OE}$:

1. The simplest connection is to have the FPGA $\overline{MEMCE}$ or LDC output drive both $\overline{CE}$ and $\overline{OE}$ in parallel, but it fails when a user applies RESET to the FPGA during the FPGA configuration process. This method must never be used when there is any chance of external reset during configuration. The FPGA will abort the configuration and then restart a new configuration, but the MCP17128 does not reset its address counter, since there was never a High level on the $\overline{OE}$ input. The new configuration reads the remaining data in the PROM and sees it as preamble, length count, etc. Since the FPGA device is the master, it issues the necessary number of CLOCK pulses, up to 16 million (2^{24}) and $\overline{MEMCE}$ goes High. The FPGA configuration will then be wrong, with potential contentions inside the FPGA device and on its output pins.
2. The recommended connection is to have the FPGA $\overline{MEMCE}$ or LDC output drive only the $\overline{CE}$ input of the MCP17128, while the $\overline{OE}$ input is driven by the inverse of the FPGA RESET input. This works under all normal circumstances, even when the configuration is reset before $\overline{MEMCE}$ has gone High. The High level on the $\overline{OE}$ input during RESET clears the PROM internal address pointer, and the reconfiguration starts at the beginning. The polarity of the RESET pin must be programmed to the correct edge.

FPGA MASTER SERIAL MODE SUMMARY

The I/O, logic functions, and associated interconnections of the application FPGA are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the individual configuration of the FPGA. In a Master Serial Mode, the FPGA automatically loads the configuration program from an external memory on power up. The MCP17128 family Serial Configuration PROM has been designed to be compatible with the Master Serial Mode.

Data is read from the Serial Configuration SCPROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal DCLK, which is generated during configuration.

Master Serial Mode provides a simple configuration interface as only a serial data line and two control lines are required to configure an FPGA. Data from the Serial Configuration SCPROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CLK driven by the FPGA DCLK.

Programming the FPGA with Counters Reset Upon Completion

The connections between an FPGA device and its SCPROM are shown in Figure 1. The DATA line from the SCPROM is connected to the CLK input of the SCPROM. At power–up or upon reconfiguration, the $\overline{MEMCE}$ signal goes Low (pulled low by the FPGA device at reset, or by external circuitry for reconfiguration), enabling the SCPROM and its DATA output. During the configuration process, DO reads data from the SCPROM on every rising clock edge. The $\overline{MEMCE}$ signal goes High at the end of configuration and resets the internal address counters of the SCPROM.

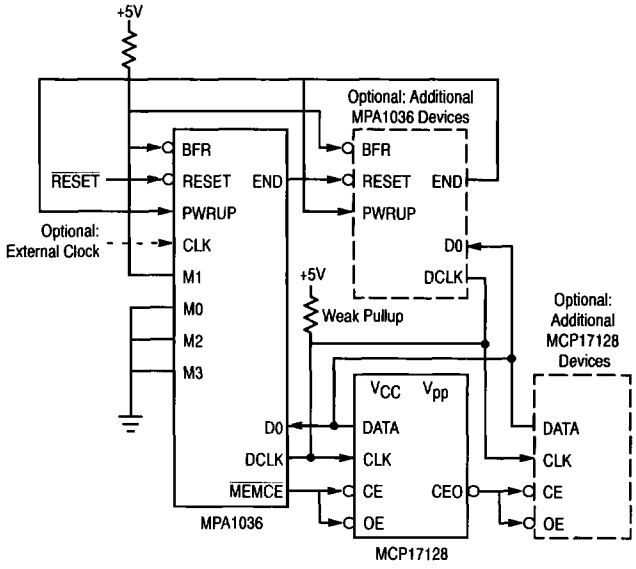


Figure 1. MPA1036 Configuration Using MCP17128 Serial EPROM

Programming the FPGA with Counters Unchanged Upon Completion

The $\overline{OE}$ pin should be tied Low when multiple FPGA configurations for a single FPGA are stored in a Serial Configuration PROM, as shown in Figure 2. The internal address counters are reset upon power–up and configuration begins with the first program stored in memory. Since the $\overline{OE}$ in is held Low, the address counters remain unchanged after configuration is complete. Then to reprogram the FPGA with another program, the $\overline{MEMCE}$ line is pulled Low and configuration begins at the last value of the address counters.

Cascading Serial Configuration PROMs

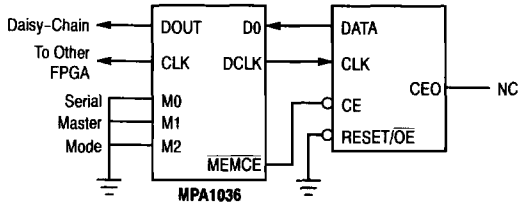
Cascading SCPROMs provide additional memory for multiple FPGAs configured as a daisy–chain, or for future FPGAs requiring larger configuration memories.

When the last bit from the first SCPROM is read, the next clock signal to the SCPROM asserts its $\overline{CEO}$ output Low and disables its DATA line. The second SCPROM recognizes the Low level on its $\overline{CE}$ input and enables its DATA output. (See Figure 1).

When configuration is complete, the address counters of all cascaded SCPROMs are reset if RESET goes Low forcing the RESET/$\overline{OE}$ on each SCPROM to go High.

If the address counters are not to be reset upon completion, then the RESET/$\overline{OE}$ inputs can be tied to ground, as shown in Figure 2. To reprogram the FPGA device with another program, the $\overline{MEMCE}$ line goes Low and configuration begins where the address counters had stopped. In this case, avoid contention between DATA and the configured I/O use of DO if DO was configured as an output.

Additional logic may be required if cascaded memories are so large that the rippled chip enable is not fast enough to activate successive SCPROMs.



Notes:
1. M2 should be programmed as an input during operation if it is tied to Ground.
2. If the FPGA is reset during configuration, it will abort back to initialization state. $\overline{MEMCE}$ will not go High, so an external signal is required to reset the MCP17128 counters.

Figure 2. Address Counters Not Reset

STANDBY MODE

The MCP17128 enters a low power standby mode whenever $\overline{CE}$ is High. In standby mode, the SCPROM consumes less than 500µA of current. The output will remain in a high impedance state regardless of the state of the $\overline{OE}$ input.

PROGRAMMING MODE

Programming mode is entered by holding V_{PP} High for at least two clock edges and is exited by removing power from the device or by a Low on both $\overline{CE}$ and $\overline{OE}$. Figure 5 through Figure 10 shows the programming algorithm.

MCP17128 RESET POLARITY

The MCP17128 lets the user choose the reset polarity as either RESET/$\overline{OE}$ or $\overline{OE}$/RESET. Any third–party commercial programmer should prompt the user for the desired reset polarity.

The programming of the overflow word should be handled transparently by the PROM programmer; it is mentioned here as supplemental information only.

The polarity is programmed into the first overflow word location, max address+1. 00000000 in these locations makes the reset active Low, FFFFFFFF in these locations makes the reset active High. The default condition is RESET active High.

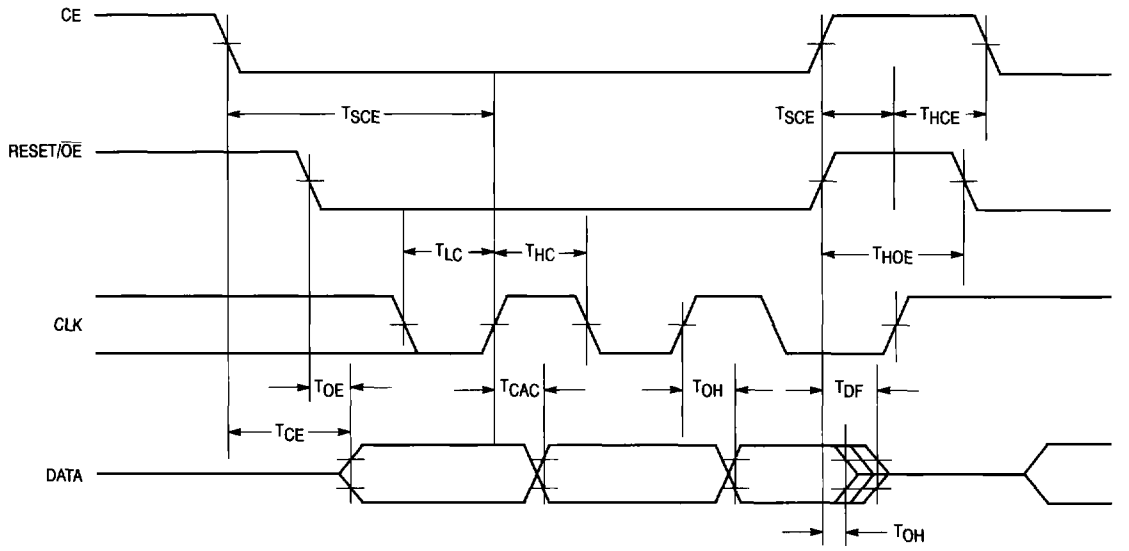


Figure 3. AC Characteristics Over Operating Conditions

AC OPERATING CONDITIONS

Symbol	Parameter	Limit 4.5V ≤ V_{CC} ≤ 6.0V		Unit	Condition
		Min	Max		
T_{OE}	$\overline{OE}$ to Data Delay		45	ns	
T_{CE}	$\overline{CE}$ to Data Delay		50	ns	
T_{CAC}	CLK to Data Delay		60	ns	
T_{OH}	Data Hold From $\overline{OE}$, $\overline{CE}$ or CLK	0		ns	
T_{DF}	$\overline{OE}$ or $\overline{CE}$ to Data Float Delay		50	ns	Note 1
T_{LC}	CLK Low Time	25		ns	Note 2
T_{HC}	CLK High Time	25		ns	Note 2
T_{SCE}	$\overline{CE}$ Setup Time to CLK (To Guarantee Proper Counting)	25		ns	
T_{HCE}	$\overline{CE}$ Hold Time to CLK (To Guarantee Proper Counting)	0		ns	Note 2
T_{HOE}	$\overline{OE}$ High Time (Guarantees Counters are Reset)	20		ns	Note 2
CLK_{max}	Clock Frequency		10	MHz	

1. Float delays are measured with minimum tester AC load and maximum DC load.
2. Guarantee by design, not tested.

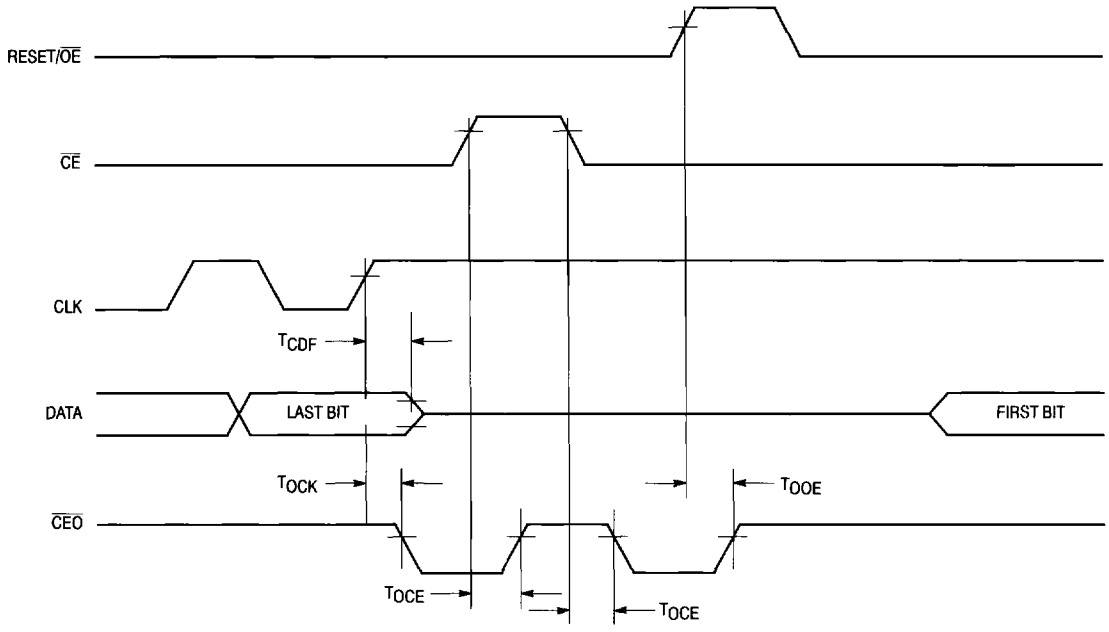


Figure 4.

Symbol	Parameter	Limit 4.5V ≤ V_{CC} ≤ 6.0V		Unit	Condition
		Min	Max		
T_{CDF}	CLK to Data Float Delay		50	ns	
T_{OCK}	CLK to $\overline{CEO}$ Delay		40	ns	
T_{OCE}	$\overline{CE}$ to $\overline{CEO}$ Delay		40	ns	
T_{OOE}	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		40	ns	

PIN ASSIGNMENTS IN THE PROGRAMMING MODE

Pin Name	DIP	PLCC	I/O	Function
DATA	1	2	I/O	The rising edge of the clock shifts a data word in or out of the PROM one bit at a time.
CLK	2	4	I	Clock input. Used to increment the internal address/word counter for reading and programming operation.
RESET/$\overline{OE}$	3	6	I	The rising edge of CLK shifts a data word into the PROM when $\overline{CE}$ and $\overline{OE}$ are High; it shifts a data word out of the PROM when $\overline{CE}$ is Low and $\overline{OE}$ is High. The address/word counter is incremented on the rising edge of CLK while $\overline{CE}$ is held High and $\overline{OE}$ is held Low. Note: Any modified polarity of the RESET/$\overline{OE}$ pin is ignored in the programming mode.
$\overline{CE}$	4	8	I	The rising edge of CLK shifts a data word into the PROM when $\overline{CE}$ and $\overline{OE}$ are High; it shifts a data word out of the PROM when $\overline{CE}$ is Low and $\overline{OE}$ is High. The address/word counter is incremented on the rising edge of CLK while $\overline{CE}$ is held High and $\overline{OE}$ is held Low.
GND	5	10	—	Ground pin.
$\overline{CEO}$	6	14	O	The polarity of the RESET/$\overline{OE}$ pin can be read by sensing the $\overline{CEO}$ pin. Note: The polarity of the RESET/$\overline{OE}$ pin is ignored while in the programming mode. In final verification, this pin must be monitored to go Low one clock cycle after the last data bit has been read.
V_{PP}	7	17	—	Programming Voltage Supply. Programming mode is entered by holding $\overline{CE}$ and $\overline{OE}$ High and V_{PP} at V_{PP1} for two rising clock edges and then lowering V_{PP} to V_{PP2} for one more rising clock edge. A word is programmed by strobing the device with V_{PP} for the duration TPGM V_{PP} must be tied to V_{CC} for normal operation.
V_{CC}	8	20	—	+5 V power supply input.

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DC PROGRAMMING SPECIFICATIONS

Symbol	Parameter	Limit		Unit	Condition
		Min	Max		
V_{CCP}	Supply Voltage During Programming	5.0	6.0	V	
V_{IL}	Input Voltage Low	0	0.5	V	
V_{IH}	Input Voltage High	2.4	V_{CC}	V	
V_{OL}	Output Voltage Low		0.4	V	
V_{OH}	Output Voltage High	3.7		V	
V_{PP1}	Programming Voltage	12.5	13.5	V	Note 1
V_{PP2}	Programming Mode Access Voltage	V_{CCP}	V_{CCP} + 1	V	
I_{PPP}	Supply Current in Programming Mode		100	mA	
I_L	Input or Output Leakage Current	−10	10	µA	
V_{CCL}	First Pass Supply Voltage Low for Final Verification	2.8	3.0	V	
V_{CCH}	Second Pass Supply Voltage High for Final Verification	6.0	6.2	V	

1. No overshoot is permitted on this signal. V_{PP} must not be allowed to exceed V_{PP1} max.

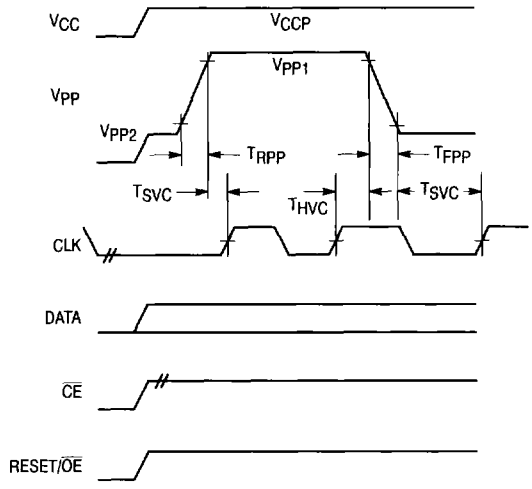

Figure 5. Enter Programming Mode

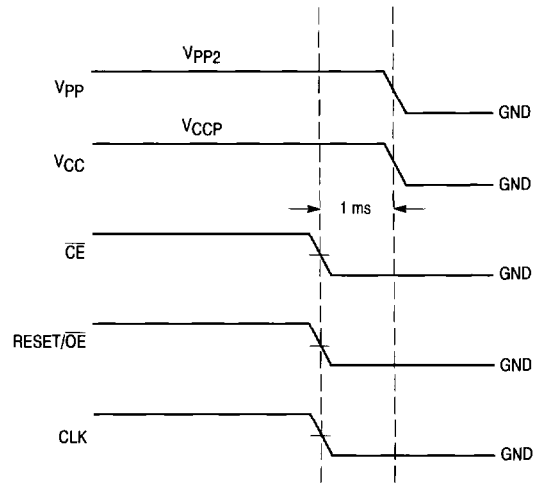

Figure 6. Exit Programming Mode

AC PROGRAMMING SPECIFICATIONS

Symbol	Parameter	Limit		Unit	Condition
		Min	Max		
T_{RPP}	Rise Time of V_{PP} (10 to 90%)	50		ns	
T_{FPP}	Fall Time of V_{PP} (90 to 10%)	50		ns	
T_{PGM}	V_{PP} Programming Pulse Width	0.95	1.05	ms	
T_{SVC}	V_{PP} Setup to CLK for Entering Programming Mode	100		ns	
T_{HVC}	V_{PP} Hold from CLK for Entering Programming Mode	300		ns	
T_{SDP}	Data Setup to CLK for Programming	50		ns	
T_{HDP}	Data Hold from CLK for Programming	0		ns	
T_{SCC}	$\overline{CE}$ Setup to CLK for Programming/Verifying	100		ns	Note 1
T_{HCC}	$\overline{CE}$ Hold from CLK for Programming/Verifying	200		ns	
T_{SCV}	$\overline{CE}$ Setup to V_{PP} for Programming	100		ns	
T_{HCV}	$\overline{CE}$ Hold from V_{PP} for Programming	50		ns	
T_{SIC}	$\overline{OE}$ Setup to CLK for Incrementing Address Counter	100		ns	
T_{HIC}	$\overline{OE}$ Hold from CLK for Incrementing Address Counter	0		ns	
T_{CAC}	CLK to Data Valid		400	ns	
T_{OH}	Data Hold from CLK	0		ns	
T_{CE}	$\overline{CE}$ Low to Data Valid		250	ns	

1. While in programming mode, $\overline{CE}$ should only be changed while CLK is High and has been High for 200ns.

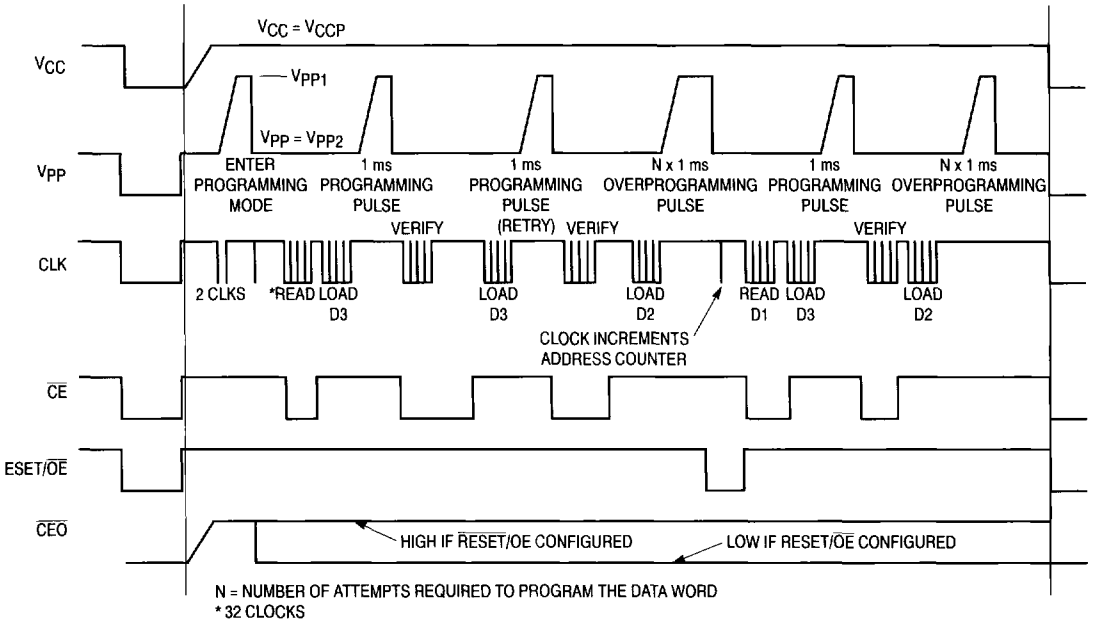

Figure 7. Programming Cycle Overview

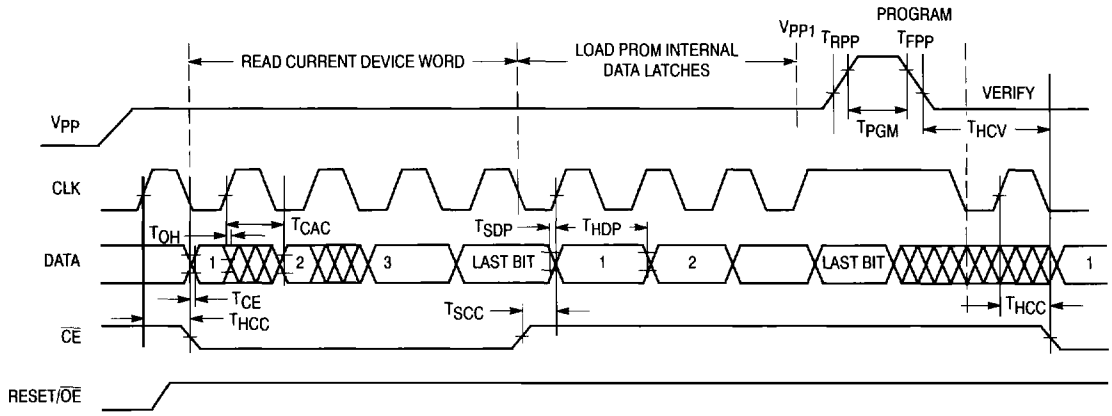

Figure 8. Details of Read/Program/Verify Cycle

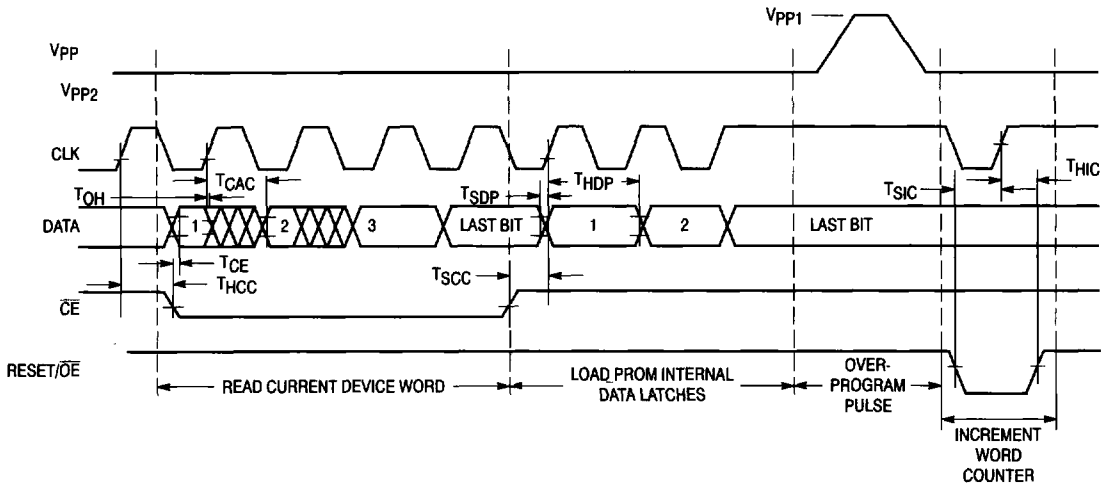

Figure 9. Overprogramming Detail

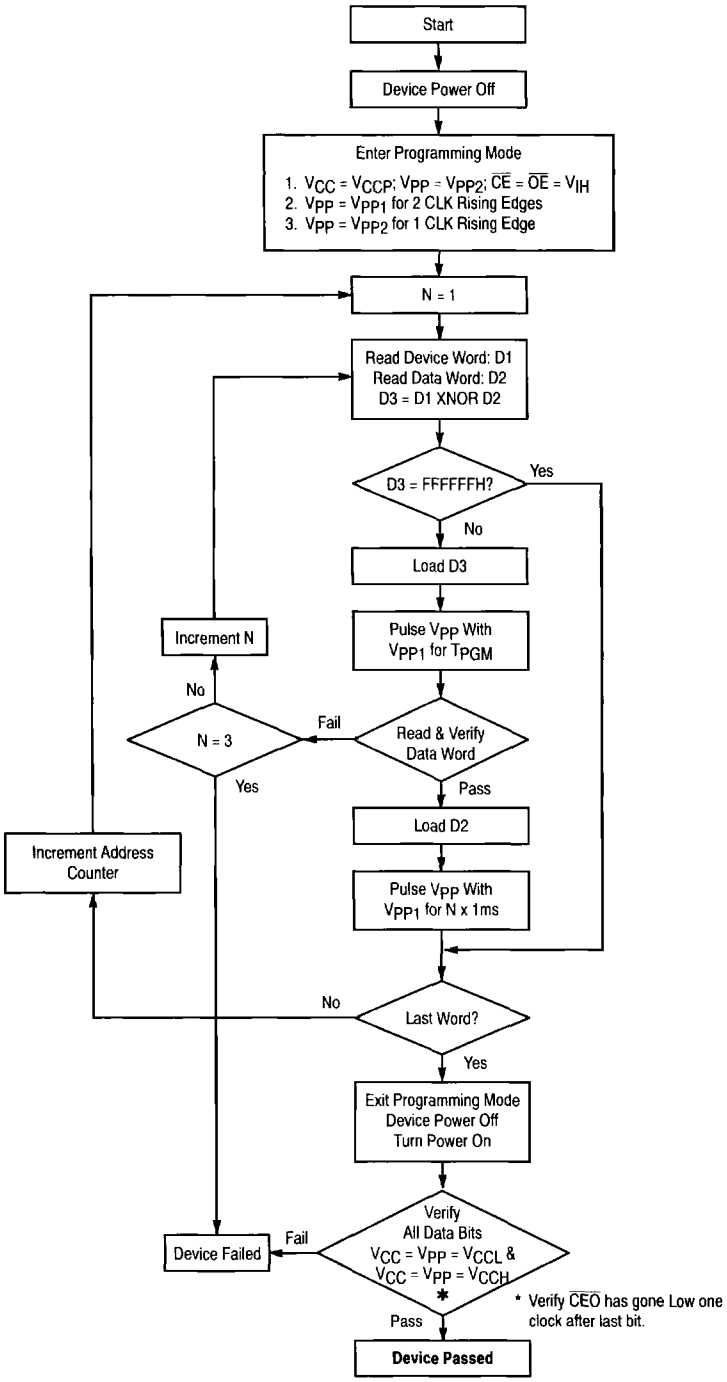

Figure 10. MCP17128 Programming Spec