REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET	35	36	37	38																
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS	REV															
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Rajesh Pithadia

APPROVED BY
Robert M. Heber

DRAWING APPROVAL DATE
07-04-25

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, ELECTRICALLY ALTERABLE (IN-SYSTEM REPROGRAMMABLE), 3M GATES, PROGRAMMABLE LOGIC DEVICE, MONOLITHIC SILICON

REVISION LEVEL	SIZE	CAGE CODE	
	A	67268	**5962-02530**

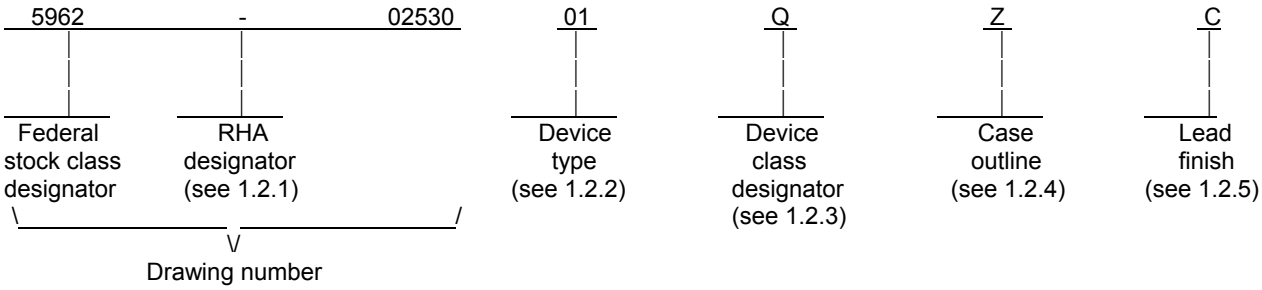
SHEET 1 OF 38

DSCC FORM 2233
APR 97

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting high reliability (device classes Q and M) and space application (device class V. A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	XQ(R)2V3000-4	3M gate programmable array	0.44 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Z	See figure 1 (Reference JEDEC MO-128)	717	Ceramic column grid array CCGA

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range to ground potential (V_{CCINT})	-0.5 V dc to +1.65 V dc
Auxiliary supply voltage range to ground potential (V_{CCAUX})	-0.5 V dc to +4.0 V dc
Output drivers supply voltage range to ground potential (V_{CCO})	-0.5 V dc to +4.0 V dc
Key memory battery backup supply voltage range to ground potential (V_{BATT})	-0.5 V dc to +4.0 V dc
DC input voltage range (user and dedicated I/Os (V_{IN}) 3/	-0.5 V to V_{CCO} + 0.5V
DC input voltage range (V_{REF}) using Ref	-0.5 V to V_{CCO} + 0.5V
Voltage applied to three-state output(V_{TS})	-0.5 V to 4.0V
Lead temperature (soldering, 10 seconds)	+220°C
Power dissipation (P_D)	2.0 W
Thermal resistance, junction-to-case (θ_{JC}):	
Case outlines Z	4.2°C/W 4/
Junction temperature (T_J) for ceramic packages	+145°C 5/
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage relative to ground(V_{CCINT})	+1.425 V dc minimum to +1.575 V dc maximum
Supply voltage relative to ground(V_{CCAUX})	+3.0 V dc minimum to +3.6 V dc maximum
Supply voltage relative to ground(V_{CCO})	+1.2 V dc minimum to +3.6 V dc maximum
Supply voltage relative to ground(V_{BATT})	+1.0 V dc minimum to +3.6 V dc maximum
Data retention V_{CCINT} voltage (V_{DRINT})	+1.2 V minimum
Data retention V_{CCAUX} voltage (V_{DRI})	+2.5 V minimum
V_{REF} current per bank I_{REF}	±10 µA
Input leakage current I_L	±10 µA
Pad pull-up (when selected) @ V_{IN} = 0 V, V_{CCO} = 3.3 V (sample tested) I_{RPU} 6/	250 µA
Pad pull-down (when selected) @ V_{IN} = 3.6 V (sample tested) I_{RPD} 6/	250 µA
Battery supply current I_{BATT}	100 nA
Quiescent V_{CCINT} supply current (I_{CCINTQ}) Typical 0.2 A	1.30 A maximum
Quiescent V_{CCO} supply current 7/ 8/ (I_{CCOQ}) Typical 2.0 mA	6.25 mA maximum
Quiescent V_{CCAUX} supply current 7/ 8/ (I_{CCAUXQ}) Typical 20 mA	95 mA maximum
Input high voltage (V_{IH})	2.0 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum
Maximum input signal transition time (t_{IN})	250 ns
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Radiation features. (RHA marked devices only)

Maximum total dose available (dose rate = 50 – 300 rads(Si)/s) .....200K rads(Si)

1/ All voltage values in this drawing are with respect to V_{SS}

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3/ Inputs configured as PCI are fully PCI compliant. This statement takes precedence over any specification that would imply that the device is not PCI compliant.

4/ When a thermal resistance for this case is specified in MIL-STD-1835, that value shall supersede the value indicated herein.

5/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

6/ Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

7/ With no output current loads and no active input pull-up resistors. All I/O pins are 3-stated and floating.

8/ Data are retained even if V_{CCO} drops to 0 V.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192M-95 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD 78 - IC Latch-Up Test.
JEDEC Publication EIA/JEP 95 - Registered and Standard Outlines for Semiconductor Devices

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics are the preirradiation and postirradiation parameter limits as specified in table IA and shall apply over the full case operating or junction temperature range as applicable.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-PRF-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on three devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is three (3) devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 condition A and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at +25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with method 1020 if MIL-STD-883 and as specified in 1.5 herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and in 1.5 herein.

a. Transient dose rate upset testing for class M devices shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for classes Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on Q and V devices marked as RHA devices, the SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be V_{DD} = 2.5 V dc for the upset measurements and V_{DD} = 2.5 V dc for the latchup measurements.

g. For SEP test limits, see Table IB herein.

TABLE IA. Electrical performance characteristics.

(Pre-irradiation values for RHA marked devices shall also be the post-irradiation values, unless otherwise specified. When performing post-irradiation electrical measurements for any RHA level, T_A = +25°C. Limits shown are guaranteed at T_A = +25°C ±5°C.)

Test	Symbol	Conditions 1.425 V ≤V_{CCINT} ≤1.575 V 3.0 V ≤V_{CCAUX} ≤3.6 V 3.0 V ≤ V_{CCO} ≤ 3.6 V (-55°C ≤ T_C ≤+125°C)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Data retention V_{CCINT} voltage below which configuration may be lost	V_{DRINT}		1, 2, 3	01	1.2		V
Data retention V_{CCAUX} voltage below which configuration may be lost	V_{DRI}		1, 2, 3	01	2.5		V
High-level input voltage	V_{IH}	lvttl	1, 2, 3	01	2.0		V
High-level input voltage	V_{IH}	lvdse	1, 2, 3	01	1.425		V
High-level input voltage LOW	V_{IH}	lvds	1, 2, 3	01	0.25		V
High-level input voltage Med	V_{IH}	lvds	1, 2, 3	01	1.625		V
High-level input voltage High	V_{IH}	lvds	1, 2, 3	01	2.5		V
High-level input voltage	V_{IH}	ldt	1, 2, 3	01	1.425		V
High-level input voltage LOW	V_{IH}	sstl	1, 2, 3	01	0.7		V
High-level input voltage Med	V_{IH}	sstl	1, 2, 3	01	1.2		V
High-level input voltage High	V_{IH}	sstl	1, 2, 3	01	1.7		V
Low-level input voltage	V_{IL}	lvttl	1, 2, 3	01		0.8	V
Low-level input voltage	V_{IL}	lvdse	1, 2, 3	01		1.025	V
Low-level input voltage Low	V_{IL}	lvds	1, 2, 3	01		0.0	V
Low-level input voltage Med	V_{IL}	lvds	1, 2, 3	01		1.375	V
Low-level input voltage High	V_{IL}	lvds	1, 2, 3	01		2.25	V
Low-level input voltage	V_{IL}	ldt	1, 2, 3	01		1.025	V
Low-level input voltage Low	V_{IL}	sstl	1, 2, 3	01		0.5	V
Low-level input voltage Med	V_{IL}	sstl	1, 2, 3	01		1.0	V
Low-level input voltage High	V_{IL}	sstl	1, 2, 3	01		1.5	V
High-level output voltage	V_{OH}	I_{OH} = -1.75,-3.5,-4, -8 or –12 mA (ttl2, ttl4,ttl8,ttl16,ttl24), V_{CCO} = 3.0V,V_{CCINT} = 1.425V	1, 2, 3	01	2.4		V

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1.425 V $\leq V_{CCINT} \leq$1.575 V 3.0 V $\leq V_{CCAUX} \leq$3.6 V 3.0 V $\leq V_{CCO} \leq$ 3.6 V (-55°C $\leq T_C \leq$+125°C)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Low-level output voltage	V_{OL}	I_{OL} = 1.75,3.5, or 4 mA (ttl2, ttl4,ttl8)V_{CCO} = 3.0V, V_{CCINT}=1.425V	1, 2, 3	01		0.4	V
Low-level output voltage		I_{OL} = 8, or 12 mA (ttl16, ttl24) V_{CCO} = 3.0V, V_{CCINT}=1.425V	1, 2, 3	01		0.45	V
Quiescent V_{CCINT} Supply current	I_{CCINTQ} 1/		1, 2, 3	01		1300	mA
Quiescent V_{CCO} Supply current	I_{CCOQ} 1/					6.25	
Quiescent V_{CCAUX} Supply current	I_{CCAUXQ} 1/		1, 2, 3	01		95	mA
Input or output leakage current	I_L		1, 2, 3	01	-10	+10	µA
V_{REF} current per bank	I_{REF}		1, 2, 3	01	-10	+10	µA
Input capacitance (sample tested)	C_{IN}, C_{OUT}	See 4.4.1e, f = 1.0 MHz, V_{OUT} = 0 V	4	01		10	pf
Pad pull-up (when selected)	I_{RPU} 2/	V_{IN} = 0V, V_{CCO} = 3.3 V (sample tested)	1, 2, 3	01		0.25	mA
Pad pull-down (when selected)	I_{RPD} 2/	V_{IN} = 3.6V (sample tested)	1, 2, 3	01		0.25	mA
Battery supply current	I_{BATT}		1, 2, 3	01		100	nA
Functional test	FT	See 4.4.1c	7, 8A, 8B	01			
Power-On Supply Requirements							
Minimum required current supply	$I_{CCINTMIN}$	3/	1, 2, 3	01	1300		mA
Minimum required current supply	$I_{CCAUXMIN}$	3/	1, 2, 3	01	95		mA
Minimum required current supply	I_{CCOMIN}	3/	1, 2, 3	01	6.25		mA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1.425 V $\leq V_{CCINT} \leq$1.575 V 3.0 V $\leq V_{CCAUX} \leq$3.6 V 3.0 V $\leq V_{CCO} \leq$ 3.6 V (-55°C $\leq T_C \leq$+125°C)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
IOB Input Switching Characteristics Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in "IOB Input Switching Characteristics Standard Adjustments" below this section. Input timing for LVTTL is measured at 1.4 V. For other I/O standards are shown in "Input Delay Measurement Methodology" below this section.							
Propagation Delays							
Pad to I output, no delay	T_{IOPI}		9, 10, 11	01		0.88	ns
Pad to I output, with delay	T_{IOPID}					2.49	
Pad to output IQ via transparent latch, no delay	T_{IOPLI}					1.05	
Pad to output IQ via transparent latch, with delay	T_{IOPLID}					4.20	
Sequential Delays							
Clock CLK to output IQ	T_{IOCKIQ}		9, 10, 11	01		0.77	ns
Setup and Hold Times with respect to Clock CLK at IOB input register							
Pad, no delay	T_{IOPICK} / T_{IOICKP}		9, 10, 11	01	1.06/ -0.45		ns
Pad, with delay	$T_{IOPICKD}$/$T_{IOICKPD}$				4.22/ -2.66		
ICE input	T_{IOCECK}/ $T_{IOCKICE}$				0.24/ 0.04		
SR Input (IFF,synchronous)	$T_{IOSRCKI}$				0.34		
IOB Input Switching Characteristics – Continued Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in "IOB Input Switching Characteristics Standard Adjustments" below this section. . Input timing for LVTTL is measured at 1.4 V. For other I/O standards are shown in "Input Delay Measurement Methodology" below this section.							
Set / Reset Delays							
SR input to IQ (asynchronous)	T_{IOSRIQ}		9, 10, 11	01		1.40	ns
GSR to output IQ	T_{GSRQ}					6.88	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1.425 V $\le V_{CCINT} \le$1.575 V 3.0 V $\le V_{CCAUX} \le$3.6 V 3.0 V $\le V_{CCO} \le$ 3.6 V (-55°C $\le T_C \le$+125°C)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Iob Output Switching Characteristics Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in "Lob Output Switching Characteristics Standard Adjustments" below this section.							
Propagation Delays							
O input to Pad	T_{IOOP}		9, 10, 11	01		1.74	ns
O input to Pad via transparent latch	T_{IOOLP}					2.11	
3-State Delays							
T input to Pad high-impedance 4/	T_{IOTHZ}		9, 10, 11	01		0.64	ns
T input to valid data on Pad	T_{IOTON}					1.67	
T input to Pad high-impedance via transparent latch 4/	$T_{IOTLPHZ}$					1.01	
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$					2.04	
GTS to Pad high impedance 4/	T_{GTS}					5.98	
Sequential Delays							
Clock CLK to Pad	T_{IOCKP}		9, 10, 11	01		2.15	ns
Clock CLK to Pad high-impedance (synchronous) 4/	T_{IOCKHZ}					1.2	
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}					2.22	
Setup and Hold Times before/after Clock CLK	Setup Time /Hold Time						
O input	T_{IOOCK} / T_{IOCKO}		9, 10, 11	01	0.39/ -0.11		ns
O OCE input	$T_{IOOCECK}$ / $T_{IOCKOCE}$				0.24/ -0.08		
SR input (OFF)	$T_{IOSRCKO}$ / $T_{IOCKOSR}$				0.34/ -0.07		
3-State Setup Times, T input	T_{IOTCK} / T_{IOCKT}				0.35/ -0.08		
3-State Setup Times, TCE input	$T_{IOTCECK}$ $T_{IOCKTCE}$				0.24/ -0.08		
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}$ $T_{IOCKTSR}$				0.34/ -0.07		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1.425 V $\leq V_{CCINT} \leq$1.575 V 3.0 V $\leq V_{CCAUX} \leq$3.6 V 3.0 V $\leq V_{CCO} \leq$ 3.6 V (-55°C $\leq T_C \leq$+125°C)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Set/Reset Delays							
SR input to Pad (asynchronous)	T_{IOSRP}		9, 10, 11	01		2.98	ns
SR input to Pad high-impedance (asynchronous) 4/	T_{IOSRHZ}					1.92	
SR input to valid data on Pad (asynchronous)	T_{IOSRON}					2.95	
GSR to Pad	T_{IOGSRQ}			01		6.88	
Clock Distribution Switching Characteristics							
Global Clock Buffer I input to O output	T_{GIO}		9,10,11	01		0.59	ns
CLB Switching Characteristics Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.							
Combinatorial Delays							
4-input function: F/G inputs to X/Y outputs	T_{ILO}		9, 10, 11	01		0.44	ns
5-input function: F/G inputs to F5 output	T_{IF5}					0.72	
5-input function: F/G inputs to X output	T_{IF5X}					0.95	
FXINA or FXINB inputs to Y output via MUXFX	T_{IFXY}					0.45	
FXINA input to FX output via MUXFX	T_{INAFX}					0.32	
FXINB input to FX output via MUXFX	T_{INBFX}					0.32	
SOPIN input to SOPOUT output via ORCY	$T_{ISOPSOP}$					0.44	
Incremental delay outing through transparent latch to XQ/YQ outputs	T_{IFNCTL}					0.51	
Sequential Delays							
FF clock CLK to XQ/YQ outputs	T_{CKO}		9, 10, 11	01		0.57	ns
Latch clock CLK to XQ/YQ outputs	T_{CKLO}					0.68	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1.425 V $\leq V_{CCINT} \leq$1.575 V 3.0 V $\leq V_{CCAUX} \leq$3.6 V 3.0 V $\leq V_{CCO} \leq$ 3.6 V (-55°C $\leq T_C \leq$+125°C)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Setup and Hold times before/after Clock CLK					**Setup/Hold**		
BX/BY inputs	T_{DICK}/T_{CKDI}		9, 10, 11	01	0.37/ -0.09		ns
DY inputs	T_{DYCK}/T_{CKDY}				0.37/ -0.09		
DX inputs	T_{DXCK}/T_{CKDX}				0.37/ -0.09		
CE input	T_{CECK}/T_{CKCE}				0.24/ -0.08		
SR/BY inputs (synchronous)	T_{SRCK}/T_{SCKR}				0.26/ -0.03		
CLOCK CLK							
Minimum Pulse Width, High	T_{CH}		9, 10, 11	01	0.77		ns
Minimum Pulse Width, Low	T_{CL}				0.77		
Set/Reset							
Minimum Pulse Width, SR?BY inputs	T_{RPW}		9, 10, 11	01	0.77		ns
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}					1.34	
Toggle Frequency (MHz) (for export control)	F_{TOG}					650	MHz
CLB Distributed RAM Switching Characteristics Sequential Delays							
Clock CLK to X/Y outputs (WE active) in 16 X 1 mode	$T_{SHCKO16}$		9, 10, 11	01		2.05	ns
Clock CLK to X/Y outputs (WE active) in 32 X 1 mode	$T_{SHCKO32}$					2.49	
Clock CLK to F5 output	$T_{SHCKOF5}$					2.23	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1.425 V $\leq V_{CCINT} \leq$1.575 V 3.0 V $\leq V_{CCAUX} \leq$3.6 V 3.0 V $\leq V_{CCO} \leq$ 3.6 V (-55°C $\leq T_C \leq$+125°C)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Setup and Hold Times before/after Clock CLK					**Setup/Hold**		
BX/BY data inputs (DIN)	T_{DS}/T_{DH}		9, 10, 11	01	0.67/-0.11		ns
F/G address inputs	T_{AS}/T_{AH}				0.5/0		
SR input (WS)	T_{WES}/T_{WEH}				0.53/-0.01		
Clock CLK							
Minimum Pulse Width, High	T_{WPH}		9, 10, 11	01	0.72		ns
Minimum Pulse Width, Low	T_{WPL}				0.72		
Minimum clock period to meet address write cycle time	T_{WC}				1.44		
CLB Shift Register Switching Characteristics							
Clock CLK to XY outputs	T_{REG}		9, 10, 11	01		2.92	ns
Clock CLK to XY outputs 32	T_{REG32}					3.35	
Clock CLK to XB output via MC 15 LUT output	T_{REGXB}					2.82	
Clock CLK to YB output via MC 15 LUT output	T_{REGYB}					2.75	
Clock CLK to Shiftout	T_{CKSH}					2.43	
Clock CLK to F5 outputs	T_{REGF5}					3.09	
Setup and Hold Times Before/After Clock CLK							
BX/BY data inputs (DIN)	T_{SRLDS}/T_{SRLDH}		9, 10, 11	01	0.67/-0.09		ns
SR input (WS)	T_{WSS}/T_{WH}				0.24/-0.08		
CLOCK CLK							
Minimum Pulse Width, High	T_{SRPH}		9, 10, 11	01	0.72		ns
Minimum Pulse Width, Low	T_{SRPL}				0.72		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1.425 V $\leq V_{CCINT} \leq$1.575 V 3.0 V $\leq V_{CCAUX} \leq$3.6 V 3.0 V $\leq V_{CCO} \leq$ 3.6 V (-55°C $\leq T_C \leq$+125°C)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Multiplier Switching Characteristics The following provides timing information. **Propagation Delay to Output Pin**							
Input to Pin 35	T_{MULT_P35}		9, 10, 11	01	_	5.91	ns
Input to Pin 34	T_{MULT_P34}		9, 10, 11	01	_	5.79	ns
Input to Pin 33	T_{MULT_P33}		9, 10, 11	01	_	5.66	ns
Input to Pin 32	T_{MULT_P32}		9, 10, 11	01	_	5.54	ns
Input to Pin 31	T_{MULT_P31}		9, 10, 11	01	_	5.42	ns
Input to Pin 30	T_{MULT_P30}		9, 10, 11	01	_	5.29	ns
Input to Pin 29	T_{MULT_P29}		9, 10, 11	01	_	5.17	ns
Input to Pin 28	T_{MULT_P28}		9, 10, 11	01	_	5.05	ns
Input to Pin 27	T_{MULT_P27}		9, 10, 11	01	_	4.92	ns
Multiplier Switching Characteristics The following provides timing information. **Propagation Delay to Output Pin**							
Input to Pin 26	T_{MULT_P26}		9, 10, 11	01	_	4.80	ns
Input to Pin 25	T_{MULT_P25}		9, 10, 11	01	_	4.68	ns
Input to Pin 24	T_{MULT_P24}		9, 10, 11	01	_	4.56	ns
Input to Pin 23	T_{MULT_P23}		9, 10, 11	01	_	4.43	ns
Input to Pin 22	T_{MULT_P22}		9, 10, 11	01	_	4.31	ns
Input to Pin 21	T_{MULT_P21}		9, 10, 11	01	_	4.19	ns
Input to Pin 20	T_{MULT_P20}		9, 10, 11	01	_	4.06	ns
Input to Pin 19	T_{MULT_P19}		9, 10, 11	01	_	3.94	ns
Input to Pin 18	T_{MULT_P18}		9, 10, 11	01	_	3.82	ns
Input to Pin 17	T_{MULT_P17}		9, 10, 11	01	_	3.69	ns
Input to Pin 16	T_{MULT_P16}		9, 10, 11	01	_	3.57	ns
Input to Pin 15	T_{MULT_P15}		9, 10, 11	01	_	3.45	ns
Input to Pin 14	T_{MULT_P14}		9, 10, 11	01	_	3.33	ns
Input to Pin 13	T_{MULT_P13}		9, 10, 11	01	_	3.20	ns
Input to Pin 12	T_{MULT_P12}		9, 10, 11	01	_	3.08	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1.425 V $\leq V_{CCINT} \leq$1.575 V 3.0 V $\leq V_{CCAUX} \leq$3.6 V 3.0 V $\leq V_{CCO} \leq$ 3.6 V (-55°C $\leq T_C \leq$+125°C)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Multiplier Switching Characteristics – Continued. The following provides timing information. **Propagation Delay to Output Pin**							
Input to Pin 11	T_{MULT_P11}		9, 10, 11	01	_	2.96	ns
Input to Pin 10	T_{MULT_P10}		9, 10, 11	01	_	2.83	ns
Input to Pin 9	T_{MULT_P9}		9, 10, 11	01	_	2.71	ns
Input to Pin 8	T_{MULT_P8}		9, 10, 11	01	_	2.59	ns
Input to Pin 7	T_{MULT_P7}		9, 10, 11	01	_	2.46	ns
Input to Pin 6	T_{MULT_P6}		9, 10, 11	01	_	2.34	ns
Input to Pin 5	T_{MULT_P5}		9, 10, 11	01	_	2.22	ns
Input to Pin 4	T_{MULT_P4}		9, 10, 11	01	_	2.10	ns
Input to Pin 3	T_{MULT_P3}		9, 10, 11	01	_	1.97	ns
Input to Pin 2	T_{MULT_P2}		9, 10, 11	01	_	1.95	ns
Input to Pin 1	T_{MULT_P1}		9, 10, 11	01	_	1.73	ns
Input to Pin 0	T_{MULT_P0}		9, 10, 11	01	_	1.60	ns
Setup and Hold Times before/after Clock CLK						**Setup/Hold**	
Data inputs	$T_{MULIDCK}$/ $T_{MULCKID}$		9, 10, 11	01		3.89/ 0	ns
Clock Enable	$T_{MULIDCK\_CE}$/ $T_{MULCKID\_CE}$					0.86 / 0	
Reset	$T_{MULIDCK\_RST}$/ $T_{MULCKID\_RST}$					0.86 / 0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1.425 V $\leq V_{CCINT} \leq$1.575 V 3.0 V $\leq V_{CCAUX} \leq$3.6 V 3.0 V $\leq V_{CCO} \leq$ 3.6 V (-55°C $\leq T_C \leq$+125°C)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Clock to output Pin							
Clock to Pin 35	$T_{MULITCK\_P35}$					3.74	
Clock to Pin 34	$T_{MULITCK\_P34}$					3.61	
Clock to Pin 33	$T_{MULITCK\_P33}$		9, 10, 11	01		3.49	ns
Clock to Pin 32	$T_{MULITCK\_P32}$					3.37	
Clock to Pin 31	$T_{MULITCK\_P31}$					3.25	
Clock to Pin 30	$T_{MULITCK\_P30}$					3.12	
Clock to Pin 29	$T_{MULITCK\_P29}$					3.00	
Clock to Pin 28	$T_{MULITCK\_P28}$					2.88	
Clock to Pin 27	$T_{MULITCK\_P27}$					2.75	
Clock to Pin 26	$T_{MULITCK\_P26}$					2.63	
Clock to Pin 25	$T_{MULITCK\_P25}$					2.51	
Clock to Pin 24	$T_{MULITCK\_P24}$					2.38	
Clock to Pin 23	$T_{MULITCK\_P23}$					2.26	
Clock to Pin 22	$T_{MULITCK\_P22}$					2.14	
Clock to Pin 21	$T_{MULITCK\_P21}$					2.02	
Clock to Pin 20	$T_{MULITCK\_P20}$					1.89	
Clock to Pin 19	$T_{MULITCK\_P19}$					1.77	
Clock to Pin 18	$T_{MULITCK\_P18}$					1.65	
Clock to Pin 17	$T_{MULITCK\_P17}$					1.52	
Clock to Pin 16	$T_{MULITCK\_P16}$					1.40	
Clock to Pin 15	$T_{MULITCK\_P15}$					1.28	
Clock to Pin 14	$T_{MULITCK\_P14}$					1.15	
Clock to Pin 13	$T_{MULITCK\_P13}$					1.15	
Clock to Pin 12	$T_{MULITCK\_P12}$					1.15	
Clock to Pin 11	$T_{MULITCK\_P11}$					1.15	
Clock to Pin 10	$T_{MULITCK\_P10}$					1.15	
Clock to Pin 9	$T_{MULITCK\_P9}$					1.15	
Clock to Pin 8	$T_{MULITCK\_P8}$					1.15	
Clock to Pin 7	$T_{MULITCK\_P7}$					1.15	
Clock to Pin 6	$T_{MULITCK\_P6}$					1.15	
Clock to Pin 5	$T_{MULITCK\_P5}$					1.15	
Clock to Pin 4	$T_{MULITCK\_P4}$					1.15	
Clock to Pin 3	$T_{MULITCK\_P3}$					1.15	
Clock to Pin 2	$T_{MULITCK\_P2}$					1.15	
Clock to Pin 1	$T_{MULITCK\_P1}$					1.15	
Clock to Pin 0	$T_{MULITCK\_P0}$					1.15	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1.425 V $\leq V_{CCINT} \leq$1.575 V 3.0 V $\leq V_{CCAUX} \leq$3.6 V 3.0 V $\leq V_{CCO} \leq$ 3.6 V (-55°C $\leq T_C \leq$+125°C)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Block SelectRAM Switching Characteristics **Sequential Delays**							
Clock CLK to DOUT output	T_{BCKO}		9, 10, 11	01		2.65	ns
Setup and Hold Times before/after Clock CLK					**Setup/Hold**		
ADDR Inputs	T_{BACK}/ T_{BCKA}		9, 10, 11	01	0.36/0		ns
DIN Inputs	T_{BDCK}/ T_{BCKD}				0.36/0		
EN Input	T_{BECK}/ T_{BCKE}				1.20/ -0.58		
RS Input	T_{BRCK}/ T_{BCKR}				1.65/ -0.90		
WEN Input	T_{BWCK}/ T_{BCKW}				0.72/ -0.25		
CLOCK CLK							
Minimum Pulse Width, High	T_{BPWH}		9, 10, 11	01	1.48		ns
Minimum Pulse Width, Low	T_{BPWL}				1.48		
TBUF Switching Characteristics **Combinatorial Delays**							
IN input to OUT output	T_{IO}		9, 10, 11	01	_	0.58	ns
TRI input to OUT high-impedance	T_{OFF}				_	0.55	ns
TRI input to valid data on OUT output	T_{ON}				_	0.55	ns
JTAG Test Access Port Switching Characteristics							
TMS and TDI Setup times before TCK	T_{TAPTK}		9, 10, 11	01	5.5	_	ns
TMS and TDI Hold times after TCK	T_{TCKTAP}				0.0	_	ns
Output delay from clock TCK to output TDO	T_{TCKTDO}				_	10.0	ns
Maximum TCK clock frequency	F_{TCK}				_	33	MHz

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1.425 V $\leq V_{CCINT} \leq$1.575 V 3.0 V $\leq V_{CCAUX} \leq$3.6 V 3.0 V $\leq V_{CCO} \leq$ 3.6 V (-55°C $\leq T_C \leq$+125°C)	Group A Subgroups	Device Types	Limit	Units
Pin-to-Pin Input Parameter Guidelines **Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DCM**					**Value**	**units**
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, with DCM. For data output with different standards, adjust the delays with the values shown in IOB Output Switching Characteristics standard Adjustments. 5/ Global Clock and OFF with DCM	$T_{ICKOFDCM}$		9, 10, 11	01	2.88	ns
Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DCM					**Value**	**units**
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, without DLL. For data output with different standards, adjust the delay with the values shown in IOB Output Switching Characteristics Standard Adjustments. 6/ Global Clock and OFF without DCM	T_{ICKOF}		9, 10, 11	01	6.62	ns
Global Clock Setup and Hold for LVTTL Standard, *with* DCM						
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in Input Switching Characteristics Standard Adjustments. 7/ No Delay Global Clock and IFF with DCM	T_{PSDCM}/ T_{PHDCM}		9, 10, 11	01	1.96/ -0.76	ns
Global Clock Setup and Hold for LVTTL Standard, *without* DCM						
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in Input Switching Characteristics Standard Adjustments. 7/ Full Delay Global Clock and IFF without DCM	T_{PSFD}/ T_{PHFD}		9, 10, 11	01	2.21/ 0.0	ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1.425 V $\leq V_{CCINT} \leq$1.575 V 3.0 V $\leq V_{CCAUX} \leq$3.6 V 3.0 V $\leq V_{CCO} \leq$ 3.6 V (-55°C $\leq T_C \leq$+125°C)	Group A Subgroups	Device Types	Limit	Units
DCM Timing Parameters All devices are 100% functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions. All output jitter and phase specifications are determined through statistical measurement at the package pins						
Operating Frequency Ranges						
OUTPUT Clocks (Low Frequency Mode)					**Constraints Value**	
CLK0, CLK90, CLK190, CLK270	CLKOUT_ FREQ_1X_LF_Min		9, 10, 11	01	24	MHz
CLK0, CLK90, CLK190, CLK270	CLKOUT_ FREQ_1X_LF_Max				180.00	MHz
CLK2X, CLK2X180	CLKOUT_ FREQ_2X_LF_Min				48	MHz
CLK2X, CLK2X180	CLKOUT_FREQ_2X_ LF_Max		9, 10, 11	01	360.00	MHz
CLKDV	CLKOUT_FREQ_DV_ LF_Min				1.5	MHz
CLKDV	CLKOUT_FREQ_DV_ LF_Max				120.00	MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_ LF_Min				24	MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_ LF_Max				210.00	MHz
Input Clocks (Low Frequency Mode)						
CLKIN (using DLL outputs) 8/ 10/	CLKIN_FREQ_DLL_LF_Min		9, 10, 11	01	24	MHz
CLKIN (using DLL outputs) 8/ 10/	CLKIN_FREQ_DLL_LF_Max				180.00	MHz
CLKIN (using CLKFX outputs) 9/ 10/	CLKIN_FREQ_FX_ LF_Min				1.00	MHz
CLKIN (using CLKFX outputs) 9/ 10/	CLKIN_FREQ_FX_ LF_Max				210.00	MHz
PSCLK	PSCLK_FREQ_ LF_Min				0.01	MHz
PSCLK	PSCLK_FREQ_ LF_Max				360.00	MHz
Output Clocks (High Frequency Mode)						
CLKI0, CLK180	CLKOUT_FREQ_1X_HF_Min		9, 10, 11	01	48	MHz
CLKI0, CLK180	CLKOUT_FREQ_1X_HF_Max				360.00	MHz
CLKDV	CLKOUT_FREQ_DV_HF_Min				3.0	MHz
CLKDV	CLKOUT_FREQ_DV_HF_Max				240.00	MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_HF_Min				210.00	MHz
CLKFX, CLKFX180	CLKOUT_FREQ_FX_HF_Max				270.00	MHz

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1.425 V ≤V_{CCINT} ≤1.575 V 3.0 V ≤V_{CCAUX} ≤3.6 V 3.0 V ≤ V_{CCO}≤ 3.6 V (-55°C ≤ T_C ≤+125°C)	Group A Subgroups	Device Types	Limit	Units
Input Clocks (High Frequency Mode)						
CLKIN (using DLL outputs) 8/ 10/	CLKIN_FREQ_DLL_HF_Min			01	48	MHz
CLKIN (using DLL outputs) 8/ 10/	CLKIN_FREQ_DLL_HF_Max				360.00	MHz
CLKIN (using CLKFX outputs) 9/ 10/	CLKIN_FREQ_FX_HF_Min				50.00	MHz
CLKIN (using CLKFX outputs) 9/ 10/	CLKIN_FREQ_FX_HF_Max				270.00	MHz
PSCLK	PSCLK_FREQ_HF_Min				0.01	MHz
PSCLK	PSCLK_FREQ_HF_Max				360.00	MHz

Test	Symbol	Conditions 1.425 V ≤V_{CCINT} ≤1.575 V 3.0 V ≤V_{CCAUX} ≤3.6 V 3.0 V ≤ V_{CCO}≤ 3.6 V (-55°C ≤ T_C ≤+125°C	Group A Subgroups	Device Types	Con-straints F_{CLKIN}	Limits		Units
						Min	Max	
Input Clock Tolerances **Input Clock Low/High Pulse Width**								
PSCLK	PSCLK_PULSE		9, 10, 11	01	< 1MHz	25		ns
PSCLK and CLKIN 11/	PSCLK_PULSE and CLKIN_PULSE		9, 10, 11	01	1-10 MHz	25		ns
					10-25 MHz	10		ns
					25-50 MHz	5		ns
					50-100 MHz	3		ns
					100-150 MHz	2		ns
					150-200 MHz	2		ns
					200-250 MHz	1.8		ns
					250-300 MHz	1.5		ns
					300-350 MHz	1.3		ns
					350-400 MHz	1.15		ns
					>400 MHz	1.05		ns

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1.425 V $\leq V_{CCINT} \leq$1.575 V 3.0 V $\leq V_{CCAUX} \leq$3.6 V 3.0 V $\leq V_{CCO} \leq$ 3.6 V (-55°C $\leq T_C \leq$+125°C)	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Input Clocks Cycle-Cycle Jitter (Low Frequency Mode)							
CLKIN (using DLL outputs) 8/	CLKIN_CYC_JITT_DLL_LF		9, 10, 11	01		+/-300	ps
CLKIN (using CLKFX outputs) 9/	CLKIN_CYC_JITT_FX_LF					+/-300	ps
Input Clocks Cycle-Cycle Jitter (High Frequency Mode)							
CLKIN (using DLL outputs) 8/	CLKIN_CYC_JITT_DLL_HF		9, 10, 11	01		+/-150	ps
CLKIN (using CLKFX outputs) 9/	CLKIN_CYC_JITT_FX_HF					+/-150	ps
Input Clocks Period Jitter (Low Frequency Mode)							
CLKIN (using DLL outputs) 8/	CLKIN_PER_JITT_DLL_LF		9, 10, 11	01		+/-1	ps
CLKIN (using CLKFX outputs) 9/	CLKIN_PER_JITT_FX_LF					+/-1	ps
Input Clocks Period Jitter (High Frequency Mode)							
CLKIN (using DLL outputs) 8/	CLKIN_PER_JITT_DLL_HF		9, 10, 11	01		+/-1	ps
CLKIN (using CLKFX outputs) 9/	CLKIN_PER_JITT_FX_HF					+/-1	ps
Feedback Clock Path Delay Variation							
CLKFB off-chip feedback	CLKFB_DELAY_VAR_EXT		9, 10, 11	01		+/-1	ps

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1.425 V $\leq V_{CCINT} \leq$1.575 V 3.0 V $\leq V_{CCAUX} \leq$3.6 V 3.0 V $\leq V_{CCO} \leq$ 3.6 V (-55°C $\leq T_C \leq$+125°C	Group A Subgroups	Device Types	Limits		Units
					Min	Max	
Output Clock Jitter							
Clock Synthesis Period Jitter						**Value**	
CLK0	CLKOUT_PER_JITT_0		9, 10, 11	01	+/-100		ps
CLK90	CLKOUT_PER_JITT_90				+/-150		ps
CLK180	CLKOUT_PER_JITT_180				+/-150		ps
CLK270	CLKOUT_PER_JITT_270				+/-150		ps
CLK2X, CLK2X180	CLKOUT_PER_JITT_2X				+/-200		ps
CLKDV (integer division)	CLKOUT_PER_JITT_DV1				+/-150		ps
CLKDV (non-integer division)	CLKOUT_PER_JITT_DV2				+/-300		ps
CLKFX, CLKFX180	CLKOUT_PER_JITT_FX				12/		ps
Output Clock Phase Alignment (Specification also applies to PSCLK)							
Phase Offset Between CLKIN and CLKFB						**Value**	
CLKIN/CLKFB	CLKIN_CLKFB_PHASE		9, 10, 11	01	+/-50		ps
Phase Offset Between Any DCM Outputs						**Value**	
All CLK outputs	CLKOUT_PHASE		9, 10, 11	01	+/-140		ps
Duty Cycle Precision						**Value**	
DLL outputs 8/	CLKOUT_DUTY_CYCLE_DLL **13**/		9, 10, 11	01	+/-150		ps
CLKFX outputs	CLKOUT_DUTY_CYCLE_FX		9, 10, 11	01	+/-100		ps

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1.425 V ≤ V_{CCINT} ≤ 1.575 V 3.0 V ≤ V_{CCAUX} ≤ 3.6 V 3.0 V ≤ V_{CCO} ≤ 3.6 V (-55°C ≤ T_C ≤ +125°C)	Group A Subgroups	Device Types	Con-straints F_{CLKIN}	Limits		Units
						Min	Max	
Miscellaneous Timing Parameters **(Specification also applies to PSCLK)**							**Value**	**Units**
Time Required to Achieve LOCK								
Using DLL outputs 8/	LOCK_DLL_60		9, 10, 11	01	>60MHz		20	us
	LOCK_DLL_50_60				50-60 MHz		25	us
	LOCK_DLL_40_50				40-50 MHz		50	us
	LOCK_DLL_30_40				30-40 MHz		90	us
	LOCK_DLL_24_30				24-30 MHz		120	us
Using CLKFX outputs	LOCK_FX_MIN						10	ms
	LOCK_FX_MAX						10	ms
Additional lock time with fine-phase shifting	LOCK_DLL_FINE_SHIFT						50	us
Fine-Phase Shifting							**Value**	
Absolute shifting range	FINE_SHIFT_RANGE		9, 10, 11	01			10	ns
Delay Lines							**Value**	
Tap delay resolution	DCM_TAP_MIN		9, 10, 11	01			30	ps
	DCM_TAP_MAX						60	ps
Source-Synchronous Switching Characteristics The parameters in this section provide the necessary values for calculating timing budgets for source-synchronous transmitter and receiver data-valid windows.								
Duty Cycle Distortion and Clock-Tree Skew							**Value**	
Duty Cycle Distortion 14/	T_{DCD_CLK0}		9, 10, 11	01			140	ps
	T_{DCD_CLK180}						50	ps
Clock Tree Skew 15/	T_{CKSKEW}						110	ps

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1.425 V $\leq V_{CCINT} \leq$1.575 V 3.0 V $\leq V_{CCAUX} \leq$3.6 V 3.0 V $\leq V_{CCO} \leq$ 3.6 V (-55°C $\leq T_C \leq$+125°C)	Group A Subgroups	Device Types	Con-straints F_{CLKIN}	Limits	Units
Sample Window						**Value**	
Sampling Error at Receiver Pins 16/	T_{SAMP}		9, 10, 11	01		550	ps
Pin-to-Pin Setup/Hold: Source-Synchronous Configuration						**Value**	
Data Input Setup and Hold Time Relative to Forwarded Clock Input Pin, Using DCM and Global Clock Buffer. For situations where clock and data inputs confirm to different standards, adjust the setup and hold values accordingly using values shown in IOB Input Switching Characteristics Standard Adjustments. 17/ No Delay Global Clock and IFF with DCM	T_{PSDCM}/ T_{PHDCM}		9, 10, 11	01		0.2/0.5	ns

1/ With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating. If DCI or differential signaling is used, more accurate values can be obtained by using vendor supported software. Data are retained even if $\mathbf{V_{CCO}}$ drops to 0 V.

2/ Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

3/ $\mathbf{I_{CCOMIN}}$ values listed here apply to the entire device (all banks).

4/ 3-state turn-off delays should not be adjusted.

5/ Listed above are representative values where one global clock-input drives one vertical clock line in each accessible column, and where all accessible Lob and CLB flip-flops are clocked by the global clock net. Output timing is measured with 35 pF external capacitive load. The only time it is not 50% of $\mathbf{V_{CC}}$ threshold is with LVCMOS. For other I/O standards and different loads, see “Output Delay Measurement Methodology”. DCM output jitter is included in the measurement.

6/ Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible Lob and CLB flip-flops are clocked by the global clock net. Output timing is measured at 50% Vcc threshold with 35 pF external capacitive load. For other I/O standards and different loads, see “Output Delay Measurement Methodology”.

7/ IFF = Input Flip-Flop or Latch
Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
These values are parametrically.

8/ “DLL outputs” is used here to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.

TABLE IA. Electrical performance characteristics – Continued.

9/ If both DLL and CLKFX outputs are used, follow the more restrictive specification.

10/ If the CLKIN_DIVIDE_BY_2 attribute of the DCM is used, then double these values.

11/ If DCM phase shift feature is used and CLKIN frequency > 200 Mhz, CLKIN duty cycle must be within ±5% (45/55 to 55/45).

12/ Values for this parameter are available from the datasheet accessed at the manufacture's website.

13/ CLKOUT_DUTY_CYCLE_DLL applies to the 1X clock outputs (CLK0, CLK90, CLK180, and CLK270) only if DUTY_CYCLE_CORRECTION = TRUE.

14/ These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times. TDCD_CLK0 applies to cases where local (IOB) inversion is used to provide the negative-edge clock to the DDR element in the I/O. TDCD_CLK180 applies to cases where the CLK180 output of the DCM is used to provide the negative-edge clock to the DDR element in the I/O.

14/ This value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use vendor supported software tools to evaluate clock skew specific to your application.

16/ This parameter indicates the total sampling error of the device input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
- CLK0 and CLK180 DCM jitter
- Worst-case Duty-Cycle Distortion – TDCD_CLK180
- DCM accuracy (phase offset)
- DCM phase shift resolution.

These measurements do not include package or clock tree skew.

17/ IFF = Input Flip-Flop.
The timing values were measured using the fine-phase adjustment feature of the DCM.
The worst-case duty-cycle distortion and DCM jitter on CLK0 and CLK180 is included in these measurements.

TABLE IB. SEP Test Limits. 1/ 2/ 3/

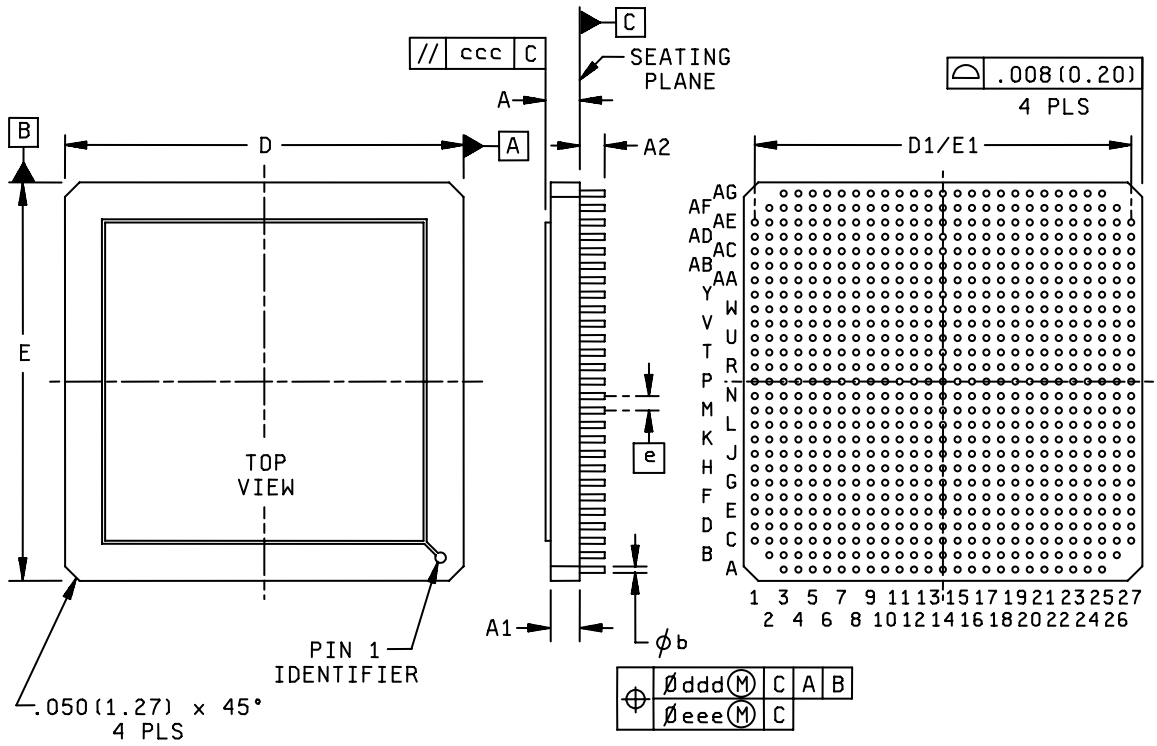
Symbol	Description	Min	Max	Units
TID	Total Ionizing Dose Method 1019, dose rate 50 rads(Si)/sec	200K		Krad(Si)
SEL	Single Event Latch-up Immunity Heavy Ion Linear Energy Transfer (LET)	160		(MeV-m^2/mg)
SEL	Single Event Functional Interrupt GEO 36,000km Typical Day		1.5E-6	Upsets/Device/Day

1/ For SEP test conditions, see 4.4.4.4 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end of line testing. Test plan must be approved by TRB and qualifying activity.

3/ Worst case temperature T_A = +125°C.

Case Z



Symbol	Millimeters		
	Min.	Nom.	Max.
A	-	3.00	3.30
A_1	2.30	2.56	2.82
A_2	2.10	2.20	2.30
D/E		35.00 BSC	
D_1/E_1		33.00 REF	
e		1.27 BSC	
b	0.51	0.54	0.57
ccc	-	-	0.35
ddd	-	-	0.30
eee	-	-	0.15
M		27	

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M-1994.
2. Symbol M is the ball matrix size.
3. Lead finish: High temperature solder Pb(90%)/ Sn(10%)

FIGURE 1. Case outline.

Case Z
See note at end of table.

Bank	Pin Description	Pin Number	Bank	Pin Description	Pin Number
0	IO_L01N_0	B3	0	IO_L73P_0	A11
0	IO_L01P_0	A3	0	IO_L75N_0	H12
0	IO_L02N_0	B4	0	IO_L75P_0/VREF_0	J12
0	IO_L02P_0	A4	0	IO_L76N_0	E12
0	IO_L03N_0/VRP_0	C5	0	IO_L76P_0	D12
0	IO_L03P_0/VRN_0	C6	0	IO_L78N_0	B12
0	IO_L04N_0/VREF_0	B5	0	IO_L78P_0	A12
0	IO_L04P_0	A5	0	IO_L91N_0/VREF_0	J13
0	IO_L05N_0	E6	0	IO_L91P_0	H13
0	IO_L05P_0	D6	0	IO_L92N_0	G13
0	IO_L06N_0	B6	0	IO_L92P_0	F13
0	IO_L06P_0	A6	0	IO_L93N_0	E13
0	IO_L19N_0	E7	0	IO_L93P_0	D13
0	IO_L19P_0	D8	0	IO_L94N_0/VREF_0	B13
0	IO_L21N_0	F8	0	IO_L94P_0	A13
0	IO_L21P_0/VREF_0	E8	0	IO_L95N_0/GCLK7P	C13
0	IO_L22N_0	C7	0	IO_L95P_0/GCLK6S	C14
0	IO_L22P_0	C8	0	IO_L96N_0/GCLK5P	F14
0	IO_L24N_0	B7	0	IO_L96P_0/GCLK4S	E14
0	IO_L24P_0	A7			
0	IO_L25N_0	H9	1	IO_L96N_1/GCLK3P	G14
0	IO_L25P_0	J9	1	IO_L96P_1/GCLK2S	H14
0	IO_L27N_0	F9	1	IO_L95N_1/GCLK1P	A15
0	IO_L27P_0/VREF_0	G9	1	IO_L95P_1/GCLK0S	B15
0	IO_L28N_0	E9	1	IO_L94N_1	C15
0	IO_L28P_0	D9	1	IO_L94P_1/VREF_1	D15
0	IO_L30N_0	C9	1	IO_L93N_1	E15
0	IO_L30P_0	B9	1	IO_L93P_1	F15
0	IO_L49N_0	A8	1	IO_L92N_1	G15
0	IO_L49P_0	A9	1	IO_L92P_1	H15
0	IO_L51N_0	G10	1	IO_L91N_1	J15
0	IO_L51P_0/VREF_0	H10	1	IO_L91P_1/VREF_1	J16
0	IO_L52N_0	F10	1	IO_L78N_1	A16
0	IO_L52P_0	E10	1	IO_L78P_1	B16
0	IO_L54N_0	D10	1	IO_L76N_1	D16
0	IO_L54P_0	C10	1	IO_L76P_1	E16
0	IO_L67N_0	B10	1	IO_L75N_1/VREF_1	F16
0	IO_L67P_0	A10	1	IO_L75P_1	F17
0	IO_L69N_0	G11	1	IO_L73N_1	H16
0	IO_L69P_0/VREF_0	H11	1	IO_L73P_1	H17
0	IO_L70N_0	F11	1	IO_L72N_1	A17
0	IO_L70P_0	F12	1	IO_L72P_1	B17
0	IO_L72N_0	D11	1	IO_L70N_1	C17
0	IO_L72P_0	C11	1	IO_L70P_1	D17
0	IO_L73N_0	B11	1	IO_L69N_1/VREF_1	G18

FIGURE 2. Terminal connections.

Case Z – Continued.

Bank	Pin Description	Pin Number	Bank	Pin Description	Pin Number
1	IO_L69P_1	G17	2	IO_L03P_2/VREF_2	E25
1	IO_L67N_1	A18	2	IO_L04N_2	E26
1	IO_L67P_1	B18	2	IO_L04P_2	E27
1	IO_L54N_1	C18	2	IO_L06N_2	F23
1	IO_L54P_1	D18	2	IO_L06P_2	F24
1	IO_L52N_1	E18	2	IO_L19N_2	F25
1	IO_L52P_1	F18	2	IO_L19P_2	F26
1	IO_L51N_1/VREF_1	H19	2	IO_L21N_2	F27
1	IO_L51P_1	H18	2	IO_L21P_2/VREF_2	G27
1	IO_L49N_1	A19	2	IO_L22N_2	G23
1	IO_L49P_1	A20	2	IO_L22P_2	H23
1	IO_L30N_1	B19	2	IO_L24N_2	G25
1	IO_L30P_1	C19	2	IO_L24P_2	G26
1	IO_L28N_1	D19	2	IO_L25N_2	H21
1	IO_L28P_1	E19	2	IO_L25P_2	J21
1	IO_L27N_1/VREF_1	F19	2	IO_L27N_2	H22
1	IO_L27P_1	G19	2	IO_L27P_2/VREF_2	J22
1	IO_L25N_1	J19	2	IO_L28N_2	H24
1	IO_L25P_1	J20	2	IO_L28P_2	H25
1	IO_L24N_1	C20	2	IO_L30N_2	H27
1	IO_L24P_1	C21	2	IO_L30P_2	J27
1	IO_L22N_1	D20	2	IO_L43N_2	J23
1	IO_L22P_1	E21	2	IO_L43P_2	J24
1	IO_L21N_1/VREF_1	E20	2	IO_L45N_2	J25
1	IO_L21P_1	F20	2	IO_L45P_2/VREF_2	J26
1	IO_L19N_1	A21	2	IO_L46N_2	K20
1	IO_L19P_1	B21	2	IO_L46P_2	K21
1	IO_L06N_1	A22	2	IO_L48N_2	K22
1	IO_L06P_1	B22	2	IO_L48P_2	K23
1	IO_L05N_1	C22	2	IO_L49N_2	K24
1	IO_L05P_1	C23	2	IO_L49P_2	K25
1	IO_L04N_1	D22	2	IO_L51N_2	K26
1	IO_L04P_1/VREF_1	E22	2	IO_L51P_2/VREF_2	K27
1	IO_L03N_1/VRP_1	A23	2	IO_L52N_2	L20
1	IO_L03P_1/VRN_1	B23	2	IO_L52P_2	M20
1	IO_L02N_1	A24	2	IO_L54N_2	L21
1	IO_L02P_1	B24	2	IO_L54P_2	L22
1	IO_L01N_1	A25	2	IO_L67N_2	L24
1	IO_L01P_1	B25	2	IO_L67P_2	L25
			2	IO_L69N_2	L26
2	IO_L01N_2	C27	2	IO_L69P_2/VREF_2	L27
2	IO_L01P_2	D27	2	IO_L70N_2	M19
2	IO_L02N_2/VRP_2	D25	2	IO_L70P_2	N19
2	IO_L02P_2/VRN_2	D26	2	IO_L72N_2	M22
2	IO_L03N_2	E24	2	IO_L72P_2	M23

FIGURE 2. Terminal connections – Continued.

Bank	Pin Description	Pin Number	Bank	Pin Description	Pin Number
2	IO_L73N_2	M24	3	IO_L51N_3/VREF_3	V22
2	IO_L73P_2	N24	3	IO_L51P_3	W22
2	IO_L75N_2	M26	3	IO_L49N_3	V21
2	IO_L75P_2/VREF_2	M27	3	IO_L49P_3	V20
2	IO_L76N_2	N20	3	IO_L48N_3	W27
2	IO_L76P_2	N21	3	IO_L48P_3	Y27
2	IO_L78N_2	N22	3	IO_L46N_3	W26
2	IO_L78P_2	N23	3	IO_L46P_3	W25
2	IO_L91N_2	N25	3	IO_L45N_3/VREF_3	W24
2	IO_L91P_2	P25	3	IO_L45P_3	W23
2	IO_L93N_2	N26	3	IO_L43N_3	W21
2	IO_L93P_2/VREF_2	N27	3	IO_L43P_3	W20
2	IO_L94N_2	P20	3	IO_L28N_3	W19
2	IO_L94P_2	P21	3	IO_L28P_3	Y19
2	IO_L96N_2	P22	3	IO_L27N_3/VREF_3	Y25
2	IO_L96P_2	P23	3	IO_L27P_3	Y24
			3	IO_L25N_3	Y23
3	IO_L96N_3	R27	3	IO_L25P_3	AA23
3	IO_L96P_3	R26	3	IO_L24N_3	Y22
3	IO_L94N_3	R25	3	IO_L24P_3	Y21
3	IO_L94P_3	R24	3	IO_L22N_3	AA27
3	IO_L93N_3/VREF_3	R23	3	IO_L22P_3	AB27
3	IO_L93P_3	T23	3	IO_L21N_3/VREF_3	AA26
3	IO_L91N_3	R22	3	IO_L21P_3	AA25
3	IO_L91P_3	R21	3	IO_L19N_3	AB26
3	IO_L78N_3	R20	3	IO_L19P_3	AB25
3	IO_L78P_3	R19	3	IO_L06N_3	AB24
3	IO_L76N_3	T27	3	IO_L06P_3	AB23
3	IO_L76P_3	T26	3	IO_L04N_3	AC27
3	IO_L75N_3/VREF_3	T24	3	IO_L04P_3	AC26
3	IO_L75P_3	U24	3	IO_L03N_3/VREF_3	AC25
3	IO_L73N_3	T22	3	IO_L03P_3	AC24
3	IO_L73P_3	U22	3	IO_L02N_3/VRP_3	AD27
3	IO_L72N_3	T20	3	IO_L02P_3/VRN_3	AE27
3	IO_L72P_3	T19	3	IO_L01N_3	AD26
3	IO_L70N_3	U27	3	IO_L01P_3	AD25
3	IO_L70P_3	U26			
3	IO_L69N_3/VREF_3	U25	4	IO_L01N_4/DOUT	AF25
3	IO_L69P_3	V25	4	IO_L01P_4/INIT_B	AG25
3	IO_L67N_3	U21	4	IO_L02N_4/D0	AF24
3	IO_L67P_3	U20	4	IO_L02P_4/D1	AG24
3	IO_L54N_3	V27	4	IO_L03N_4/D2/ALT_VRP_4	AD23
3	IO_L54P_3	V26	4	IO_L03P_4/D3/ALT_VRN_4	AE23
3	IO_L52N_3	V24	4	IO_L04N_4/VREF_4	AF23
3	IO_L52P_3	V23	4	IO_L04P_4	AG23

FIGURE 2. Terminal connections – Continued.

Case Z – Continued.

Bank	Pin Description	Pin Number	Bank	Pin Description	Pin Number
4	IO_L05N_4/VRP_4	AD22	4	IO_L91P_4	Y15
4	IO_L05P_4/VRN_4	AE22	4	IO_L92N_4	AB15
4	IO_L06N_4	AF22	4	IO_L92P_4	AA15
4	IO_L06P_4	AG22	4	IO_L93N_4	AC15
4	IO_L19N_4	AC21	4	IO_L93P_4	AD15
4	IO_L19P_4	AB21	4	IO_L94N_4/VREF_4	AE15
4	IO_L21N_4	AE21	4	IO_L94P_4	AE14
4	IO_L21P_4/VREF_4	AE20	4	IO_L95N_4/GCLK3S	AF15
4	IO_L22N_4	AF21	4	IO_L95P_4/GCLK2P	AG15
4	IO_L22P_4	AG21	4	IO_L96N_4/GCLK1S	Y14
4	IO_L24N_4	AB20	4	IO_L96P_4/GCLK0P	AA14
4	IO_L24P_4	AA20			
4	IO_L25N_4	AC20	5	IO_L96N_5/GCLK7S	AC14
4	IO_L25P_4	AD20	5	IO_L96P_5/GCLK6P	AB14
4	IO_L27N_4	AG20	5	IO_L95N_5/GCLK5S	AG13
4	IO_L27P_4/VREF_4	AG19	5	IO_L95P_5/GCLK4P	AF13
4	IO_L28N_4	AB19	5	IO_L94N_5	AE13
4	IO_L28P_4	AA19	5	IO_L94P_5/VREF_5	AD13
4	IO_L30N_4	AC19	5	IO_L93N_5	AC13
4	IO_L30P_4	AD19	5	IO_L93P_5	AB13
4	IO_L49N_4	AE19	5	IO_L92N_5	AA13
4	IO_L49P_4	AF19	5	IO_L92P_5	Y13
4	IO_L51N_4	AA18	5	IO_L91N_5	W13
4	IO_L51P_4/VREF_4	Y18	5	IO_L91P_5/VREF_5	W12
4	IO_L52N_4	AB18	5	IO_L78N_5	AG12
4	IO_L52P_4	AC18	5	IO_L78P_5	AF12
4	IO_L54N_4	AD18	5	IO_L76N_5	AD12
4	IO_L54P_4	AE18	5	IO_L76P_5	AC12
4	IO_L67N_4	AF18	5	IO_L75N_5/VREF_5	AB12
4	IO_L67P_4	AG18	5	IO_L75P_5	AB11
4	IO_L69N_4	AA17	5	IO_L73N_5	Y12
4	IO_L69P_4/VREF_4	Y17	5	IO_L73P_5	Y11
4	IO_L70N_4	AB17	5	IO_L72N_5	AG11
4	IO_L70P_4	AB16	5	IO_L72P_5	AF11
4	IO_L72N_4	AD17	5	IO_L70N_5	AE11
4	IO_L72P_4	AE17	5	IO_L70P_5	AD11
4	IO_L73N_4	AF17	5	IO_L69N_5/VREF_5	AA10
4	IO_L73P_4	AG17	5	IO_L69P_5	AA11
4	IO_L75N_4	Y16	5	IO_L67N_5	AG10
4	IO_L75P_4/VREF_4	W16	5	IO_L67P_5	AF10
4	IO_L76N_4	AC16	5	IO_L54N_5	AE10
4	IO_L76P_4	AD16	5	IO_L54P_5	AD10
4	IO_L78N_4	AF16	5	IO_L52N_5	AC10
4	IO_L78P_4	AG16	5	IO_L52P_5	AB10
4	IO_L91N_4/VREF_4	W15	5	IO_L51N_5/VREF_5	Y9

FIGURE 2. Terminal connections – Continued.

Case Z – Continued.

Bank	Pin Description	Pin Number	Bank	Pin Description	Pin Number
5	IO_L51P_5	Y10	6	IO_L21N_6/VREF_6	AA1
5	IO_L49N_5	AG9	6	IO_L22P_6	AA5
5	IO_L49P_5	AG8	6	IO_L22N_6	AA6
5	IO_L30N_5	AF9	6	IO_L24P_6	AA3
5	IO_L30P_5	AE9	6	IO_L24N_6	AA2
5	IO_L28N_5	AD9	6	IO_L25P_6	Y5
5	IO_L28P_5	AC9	6	IO_L25N_6	Y6
5	IO_L27N_5/VREF_5	AB9	6	IO_L27P_6	Y4
5	IO_L27P_5	AA9	6	IO_L27N_6/VREF_6	Y3
5	IO_L25N_5	AE8	6	IO_L28P_6	Y1
5	IO_L25P_5	AE7	6	IO_L28N_6	W1
5	IO_L24N_5	AD8	6	IO_L43P_6	W8
5	IO_L24P_5	AC8	6	IO_L43N_6	W9
5	IO_L22N_5	AB8	6	IO_L45P_6	W6
5	IO_L22P_5	AA8	6	IO_L45N_6/VREF_6	W7
5	IO_L21N_5/VREF_5	AG7	6	IO_L46P_6	W5
5	IO_L21P_5	AF7	6	IO_L46N_6	W4
5	IO_L19N_5	AC7	6	IO_L48P_6	W3
5	IO_L19P_5	AB7	6	IO_L48N_6	W2
5	IO_L06N_5	AG6	6	IO_L49P_6	V7
5	IO_L06P_5	AF6	6	IO_L49N_6	V8
5	IO_L05N_5/VRP_5	AE6	6	IO_L51P_6	V5
5	IO_L05P_5/VRN_5	AD6	6	IO_L51N_6/VREF_6	V6
5	IO_L04N_5	AG5	6	IO_L52P_6	V4
5	IO_L04P_5/VREF_5	AF5	6	IO_L52N_6	V3
5	IO_L03N_5/D4/ALT_VRP_5	AE5	6	IO_L54P_6	V2
5	IO_L03P_5/D5/ALT_VRN_5	AD5	6	IO_L54N_6	V1
5	IO_L02N_5/D6	AG4	6	IO_L67P_6	U8
5	IO_L02P_5/D7	AF4	6	IO_L67N_6	T8
5	IO_L01N_5/RDWR_B	AG3	6	IO_L69P_6	U6
5	IO_L01P_5/CS_B	AF3	6	IO_L69N_6/VREF_6	U7
			6	IO_L70P_6	U4
6	IO_L01P_6	AE1	6	IO_L70N_6	U3
6	IO_L01N_6	AD1	6	IO_L72P_6	U2
6	IO_L02P_6/VRN_6	AD3	6	IO_L72N_6	U1
6	IO_L02N_6/VRP_6	AD2	6	IO_L73P_6	T9
6	IO_L03P_6	AC4	6	IO_L73N_6	R9
6	IO_L03N_6/VREF_6	AC3	6	IO_L75P_6	T5
6	IO_L04P_6	AC2	6	IO_L75N_6/VREF_6	T6
6	IO_L04N_6	AC1	6	IO_L76P_6	T4
6	IO_L06P_6	AB5	6	IO_L76N_6	R4
6	IO_L06N_6	AB4	6	IO_L78P_6	T2
6	IO_L19P_6	AB3	6	IO_L78N_6	T1
6	IO_L19N_6	AB2	6	IO_L91P_6	R7
6	IO_L21P_6	AB1	6	IO_L91N_6	R8

FIGURE 2. Terminal connections – Continued.

Case Z – Continued.

Bank	Pin Description	Pin Number	Bank	Pin Description	Pin Number
6	IO_L93P_6	R5	7	IO_L43P_7	K3
6	IO_L93N_6/VREF_6	R6	7	IO_L43N_7	J4
6	IO_L94P_6	R3	7	IO_L30P_7	H3
6	IO_L94N_6	P3	7	IO_L30N_7	H4
6	IO_L96P_6	R2	7	IO_L28P_7	J5
6	IO_L96N_6	R1	7	IO_L28N_7	J6
			7	IO_L27P_7/VREF_7	H5
7	IO_L96P_7	P5	7	IO_L27N_7	H6
7	IO_L96N_7	P6	7	IO_L25P_7	J7
7	IO_L94P_7	P7	7	IO_L25N_7	J8
7	IO_L94N_7	P8	7	IO_L24P_7	G1
7	IO_L93P_7/VREF_7	N1	7	IO_L24N_7	F1
7	IO_L93N_7	N2	7	IO_L22P_7	G2
7	IO_L91P_7	N3	7	IO_L22N_7	G3
7	IO_L91N_7	N4	7	IO_L21P_7/VREF_7	F2
7	IO_L78P_7	N6	7	IO_L21N_7	F3
7	IO_L78N_7	N7	7	IO_L19P_7	G5
7	IO_L76P_7	N9	7	IO_L19N_7	G6
7	IO_L76N_7	N8	7	IO_L06P_7	F4
7	IO_L75P_7/VREF_7	N5	7	IO_L06N_7	F5
7	IO_L75N_7	M6	7	IO_L04P_7	E1
7	IO_L73P_7	M1	7	IO_L04N_7	E2
7	IO_L73N_7	M2	7	IO_L03P_7/VREF_7	D1
7	IO_L72P_7	M4	7	IO_L03N_7	C1
7	IO_L72N_7	M5	7	IO_L02P_7/VRN_7	E3
7	IO_L70P_7	M8	7	IO_L02N_7/VRP_7	E4
7	IO_L70N_7	M9	7	IO_L01P_7	D2
7	IO_L69P_7/VREF_7	L1	7	IO_L01N_7	D3
7	IO_L69N_7	L2			
7	IO_L67P_7	L3	0	VCCO_0	K13
7	IO_L67N_7	L4	0	VCCO_0	K12
7	IO_L54P_7	K1	0	VCCO_0	K11
7	IO_L54N_7	K2	0	VCCO_0	J11
7	IO_L52P_7	K4	0	VCCO_0	J10
7	IO_L52N_7	K5	0	VCCO_0	G12
7	IO_L51P_7/VREF_7	L6	0	VCCO_0	D7
7	IO_L51N_7	L7	0	VCCO_0	C12
7	IO_L49P_7	K6	1	VCCO_1	K17
7	IO_L49N_7	K7	1	VCCO_1	K16
7	IO_L48P_7	L8	1	VCCO_1	K15
7	IO_L48N_7	K8	1	VCCO_1	J18
7	IO_L46P_7	J1	1	VCCO_1	J17
7	IO_L46N_7	H1	1	VCCO_1	G16
7	IO_L45P_7/VREF_7	J2	1	VCCO_1	D21
7	IO_L45N_7	J3	1	VCCO_1	C16

FIGURE 2. Terminal connections – Continued.

Case Z – Continued.

Bank	Pin Description	Pin Number	Bank	Pin Description	Pin Number
2	VCCO_2	N18	7	VCCO_7	K9
2	VCCO_2	M25	7	VCCO_7	G4
2	VCCO_2	M21	7	VCCO_7	N10
2	VCCO_2	M18			
2	VCCO_2	L19	NA	CCLK	AA22
2	VCCO_2	L18	NA	PROG_B	C4
2	VCCO_2	K19	NA	DONE	AC22
2	VCCO_2	G24	NA	M0	AC6
3	VCCO_3	AA24	NA	M1	Y7
3	VCCO_3	V19	NA	M2	AE4
3	VCCO_3	U19	NA	HSWAP_EN	D5
3	VCCO_3	U18	NA	TCK	G20
3	VCCO_3	T25	NA	TDI	H7
3	VCCO_3	T21	NA	TDO	G22
3	VCCO_3	T18	NA	TMS	F21
3	VCCO_3	R18	NA	PWRDWN_B	AE24
4	VCCO_4	AE16	NA	DXN	G8
4	VCCO_4	AD21	NA	DXP	F7
4	VCCO_4	AA16	NA	VBATT	D23
4	VCCO_4	W18	NA	RSVD	C24
4	VCCO_4	W17			
4	VCCO_4	V17	NA	VCCAUX	AF14
4	VCCO_4	V16	NA	VCCAUX	AE26
4	VCCO_4	V15	NA	VCCAUX	AE2
5	VCCO_5	AE12	NA	VCCAUX	P26
5	VCCO_5	AD7	NA	VCCAUX	P2
5	VCCO_5	AA12	NA	VCCAUX	C26
5	VCCO_5	W11	NA	VCCAUX	C2
5	VCCO_5	W10	NA	VCCAUX	B14
5	VCCO_5	V13	NA	VCCINT	V18
5	VCCO_5	V12	NA	VCCINT	V14
5	VCCO_5	V11	NA	VCCINT	V10
6	VCCO_6	AA4	NA	VCCINT	U17
6	VCCO_6	V9	NA	VCCINT	U16
6	VCCO_6	U10	NA	VCCINT	U15
6	VCCO_6	U9	NA	VCCINT	U14
6	VCCO_6	T10	NA	VCCINT	U13
6	VCCO_6	T7	NA	VCCINT	U12
6	VCCO_6	T3	NA	VCCINT	U11
6	VCCO_6	R10	NA	VCCINT	T17
7	VCCO_7	M10	NA	VCCINT	T11
7	VCCO_7	M7	NA	VCCINT	R17
7	VCCO_7	M3	NA	VCCINT	R11
7	VCCO_7	L10	NA	VCCINT	P18
7	VCCO_7	L9	NA	VCCINT	P17

FIGURE 2. Terminal connections – Continued.

Case Z – Continued.

Bank	Pin Description	Pin Number	Bank	Pin Description	Pin Number
NA	VCCINT	P11	NA	GND	U23
NA	VCCINT	P10	NA	GND	U5
NA	VCCINT	N17	NA	GND	T16
NA	VCCINT	N11	NA	GND	T15
NA	VCCINT	M17	NA	GND	T14
NA	VCCINT	M11	NA	GND	T13
NA	VCCINT	L17	NA	GND	T12
NA	VCCINT	L16	NA	GND	R16
NA	VCCINT	L15	NA	GND	R15
NA	VCCINT	L14	NA	GND	R14
NA	VCCINT	L13	NA	GND	R13
NA	VCCINT	L12	NA	GND	R12
NA	VCCINT	L11	NA	GND	P27
NA	VCCINT	K18	NA	GND	P24
NA	VCCINT	K14	NA	GND	P19
NA	VCCINT	K10	NA	GND	P16
NA	GND	AG271	NA	GND	P15
NA	GND	AG261	NA	GND	P14
NA	GND	AG14	NA	GND	P13
NA	GND	AG21	NA	GND	P12
NA	GND	AG11	NA	GND	P9
NA	GND	AF271	NA	GND	P4
NA	GND	AF26	NA	GND	P1
NA	GND	AF20	NA	GND	N16
NA	GND	AF8	NA	GND	N15
NA	GND	AF2	NA	GND	N14
NA	GND	AF11	NA	GND	N13
NA	GND	AE25	NA	GND	N12
NA	GND	AE3	NA	GND	M16
NA	GND	AD24	NA	GND	M15
NA	GND	AD14	NA	GND	M14
NA	GND	AD4	NA	GND	M13
NA	GND	AC23	NA	GND	M12
NA	GND	AC17	NA	GND	L23
NA	GND	AC11	NA	GND	L5
NA	GND	AC5	NA	GND	J14
NA	GND	AB22	NA	GND	H26
NA	GND	AB6	NA	GND	H20
NA	GND	AA21	NA	GND	H8
NA	GND	AA7	NA	GND	H2
NA	GND	Y26	NA	GND	G21
NA	GND	Y20	NA	GND	G7
NA	GND	Y8	NA	GND	F22
NA	GND	Y2	NA	GND	F6
NA	GND	W14	NA	GND	E23

FIGURE 2. Terminal connections – Continued.

Case Z – Continued.

Bank	Pin Description	Pin Number
NA	GND	E17
NA	GND	E11
NA	GND	E5
NA	GND	D24
NA	GND	D14
NA	GND	D4
NA	GND	C25
NA	GND	C3
NA	GND	B271
NA	GND	B26
NA	GND	B20
NA	GND	B8
NA	GND	B2
NA	GND	B11
NA	GND	A271
NA	GND	A261
NA	GND	A14
NA	GND	A2

FIGURE 2. Terminal connections – Continued.

TABLE IIA. Electrical test requirements 1/, 2/, 3/, 4/, 5/, 6/, 7/.

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
		Device class M	Device class N	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)				1, 7, 9
2	Static burn-in I and II (method 1015)	Required	Not Required	Required	Required
3	Same as line 1				1*, 7* Δ
4	Dynamic burn-in (method 1015)	Not Required	Not Required	Not Required	Required
5	Same as line 1				1*, 7* Δ
6	Final electrical parameters	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	2, 8A, 10	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test parameters	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	2, 8A, 10	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7 and 8 functional tests shall verify the truth table.

4/ * indicates PDA applies to subgroup 1 and 7.

5/ ** see 4.4.1e.

6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

7/ See 4.4.1d.

TABLE IIB Delta limits at +25

Parameter 1/	Device types
	All
I_{CCOQ} standby	± 300μA of specified limit in table IA.
I_{CCINQ} standby	± 300μA of specified limit in table IA.
I_{CCAUXQ} standby	± 300μA of specified limit in table IA.
I_L	± 2 nA of specified limit in table IA.

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and vendors data book.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: FINAL PRELIMINARY AS OF 07-04-25

Approved sources of supply for SMD 5962-02530 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0253001QZC	68994	XQ2V3000-4CG717

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
68994	Xilinx, Incorporated 2100 Logic Drive San Jose, CA 95124