REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R010-97.	96-10-04	Ray Monnin
B	Update boilerplate to meet current MIL-PRF-38535 requirements. - glg.	14-03-24	Charles Saffle

REV																				
SHEET																				
REV	B	B	B	B	B	B	B	B	B	B	B									
SHEET	15	16	17	18	19	20	21	22	23	24	25									

REV STATUS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

PREPARED BY
Kenneth Rice

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Jeff Bowling

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
96-03-12

REVISION LEVEL
B

MICROCIRCUIT, MEMORY, DIGITAL, CMOS 4200 GATE PROGRAMMABLE LOGIC ARRAY,MONOLITHIC SILICON

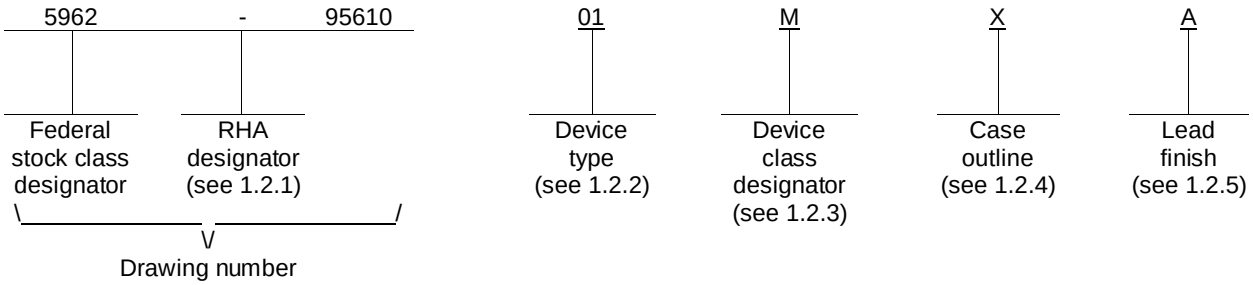
SIZE	CAGE CODE	
A	**67268**	**5962-95610**

SHEET 1 OF 25

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Toggle Speed
01	3142A-05	4200 gate programmable array	4.1 ns
02	3142A-04	4200 gate programmable array	3.3 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA15-84	84 1/	Pin grid array package
Y	See figure 1	100	Quad flat package
Z	See figure 1	100	Quad flat package
U	CMGA6-132	132 2/	Pin grid array package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ 84 = actual number of pins used, not maximum listed in MIL-STD-1835.
2/ 132 = actual number of pins used, not maximum listed in MIL-STD-1835.

1.3 Absolute maximum ratings. 3/

Supply voltage range to ground potential (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range	-0.5 V dc to V_{CC} +0.5 V dc
Voltage applied to three-state output(V_{TS})	-0.5 V dc to V_{CC} +0.5 V dc
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case outline X, U	See MIL-STD-1835
Case outlines Y, Z	20°C/W 4/
Junction temperature (T_J)	+150°C 5/
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions. 6/

Case operating temperature Range(T_C)	-55°C to +125°C
Supply voltage relative to ground(V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Ground voltage (GND)	0 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD 78 - IC Latch-Up Test.

(Copies of these documents are available online at http://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
4/ When a thermal resistance for this case is specified in MIL-STD-1835 that value shall supersede the value indicated herein.
5/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
6/ All voltage values in this drawing are with respect to V_{SS}.

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Logic block diagram. The logic block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.11 Operational notes. Additional information shall be provided by the device manufacturer (see 6.7 herein).

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7, 8A, and 8B tests shall consist of verifying the functionality of the device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
High Level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IL} = 0.8V I_{OH} = -8.0 mA, V_{IH} = 2.0 V	1, 2, 3	All	3.7		V
Low level output voltage	V_{OL}	V_{CC} = 5.5 V, I_{OL} = 8.0V V_{IL} = 0.8 V, V_{IH} = 2.0 V	1, 2, 3	All		0.4	V
Quiescent power supply current	I_{CCO}	CMOS inputs, $V_{CC} = V_{IN}$ = 5.5 V	1, 2, 3	All		8	mA
Quiescent power supply current	I_{CCO}	TTL inputs, $V_{CC} = V_{IN}$ = 5.5 V	1, 2, 3	All		14	mA
Input leakage current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = 0 V and 5.5 V	1, 2, 3	All	-20	20	µA
Horizontal long line, pull-up current	I_{RLL}	V_{CC} = 5.5 V, V_{IN} = 0 V and 5.5 V	1, 2, 3	All	0.20	4.20	mA
High level input voltage	V_{IHT}	TTL inputs	1, 2, 3	All	2.0		V
Low level input voltage	V_{ILT}	TTL inputs	1, 2, 3	All		0.8	V
High level input voltage	V_{IHC}	CMOS inputs	1, 2, 3	All	0.7 V_{CC}		V
Low level input voltage	V_{ILC}	CMOS inputs	1, 2, 3	All		0.2 V_{CC}	V
Power down ($\overline{PWR}$ $\overline{DWN}$) voltage 2/	V_{PD}	PWR DWN = 0.0 V	1, 2, 3	All	3.5		V
Input capacitance except XTL1 AND XTL2	C_{IN}	See 4.4.1e	4	All		16	pF
Input capacitance XTL1 and XTL2	C_{IN}	See 4.4.1e	4	All		20	pF
Output capacitance	C_{OUT}	See 4.4.1e	4	All		16	pF
Functional test		See 4.4.1c	7, 8A, 8B	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Interconnect + t_{PID} + 144(t_{ILO}) + t_{OPF}	t_{B1}		9, 10, 11	01		669.8	ns
				02		553.9	
t_{PID} + 144(t_{CKO}) + t_{OPF} + interconnect	t_{B2}		9, 10, 11	01		665.9	ns
				02		562.6	
t_{PID} + 144t_{QLO} + t_{OPF} + interconnect	t_{B3}		9, 10, 11	01		1126.7	ns
				02		951.4	
t_{PID} + 24t_{PUS} + t_{OPF} + interconnect	t_{B4}		9, 10, 11	01		436	ns
				02		380.1	
t_{PID} + 24t_{PUF} + t_{OPF} + interconnect	t_{B5}		9, 10, 11	01		340	ns
				02		308.1	
t_{PID} + 24t_{ON1} + t_{OPF} + interconnect	t_{B6}		9, 10, 11	01		198.4	ns
				02		173.7	
t_{PID} + 24t_{ON2} + t_{OPF} + interconnect	t_{B7}		9, 10, 11	01		234.4	ns
				02		209.7	

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
Logic input to output (combinational)	t_{ILO}	See figures 4 and 5 as applicable	3/	01		4.1	ns
				02		3.3	
Reset input to output	t_{RIO}		3/	01		4.4	ns
				02		3.7	
Reset direct width	t_{RPW}		3/	01	3.8		ns
				02	3.2		
Master reset pin to CLB output (X, Y)	t_{MRQ}		3/	01		17	ns
				02		14	
K clock input to CLB output	t_{CKO}		3/	01		3.1	ns
				02		2.5	
Clock K to the outputs X or Y when Q is return through function generators to drive X or Y	t_{QLO}		3/	01		6.3	ns
				02		5.2	
K clock logic-input setup	t_{ICK}		3/	01	3.1		ns
				02	2.5		
K clock logic-input hold	t_{CKI}		3/	All	0		ns
Logic input setup to K clock	t_{DICK}		3/	01	2.0		ns
				02	1.6		
Logic input hold from K clock	t_{CKDI}		3/	01	1.2		ns
				02	1.0		
Logic input setup to enable clock	t_{ECCK}		3/	01	3.8		ns
				02	3.2		
Logic input hold to enable clock	t_{CKEC}		3/	All	1.0		ns
Pad (package pin) to input direct t_{CCKIN}, t_{BCCKIN}	t_{PID}		3/	01		1.5	ns
				02		1.3	
I/O clock to I/O RI input (FF)	t_{IKRI}		3/	01		2.8	ns
				02		2.5	
I/O clock to pad-input setup	t_{PICK}		3/	01	15		ns
				02	14		
I/O clock to pad-input hold	t_{IKPI}		3/	All	0		ns

See footnotes at end of table

TABLE I. Electrical performance characteristics - Continued.

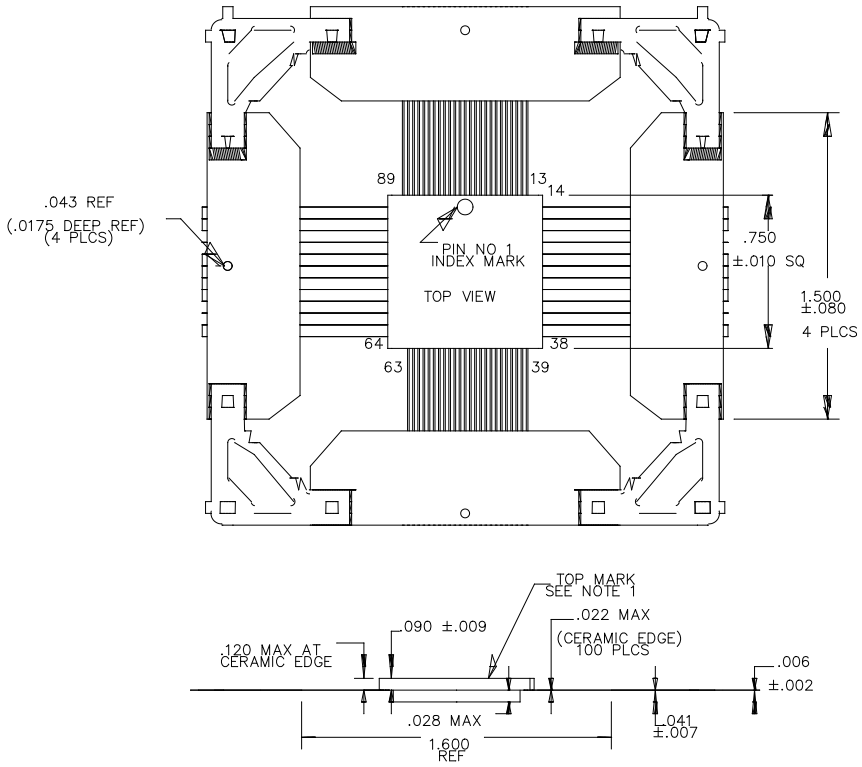
Test	Symbol	Conditions $4.5\ V \le V_{CC} \le 5.5\ V$ $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
I/O propagation delay clock (OK) to pad (fast)	t_{OKPOF}	See figures 4 and 5 as applicable	3/	01		5.5	ns
				02		5	
I/O clock to pad-output setup	t_{OOK}		3/	01	6.2		ns
				02	5.6		
I/O clock to pad-output hold	t_{OKO}		3/	All	0		ns
Output (enabled fast) to pad	t_{OPF}		3/	01		4.1	ns
				02		3.7	
Output (enabled slow) to pad	t_{OPS}		3/	01		13	ns
				02		11	
Master RESET to input RI	t_{RRI}		3/	01		20.1	ns
				02		17.1	
Master RESET to output (FF)	t_{RPO}		3/	01		24	ns
				02		20	
Bidirectional buffer delay	t_{BIDI}		3/	01		1.4	ns
				02		1.2	
TBUF data input to output	t_{IO}		3/	01		4.1	ns
				02		3.8	
TBUF three-state to output active and valid (single pull-up)	t_{ON1}		3/	01		5.7	ns
				02		4.9	
TBUF three-state to output active and valid (double pull-up)	t_{ON2}		3/	01		7.2	ns
				02		6.4	
TBUF three-state to output inactive (single pull-up)	t_{PUS}		3/	01		15.6	ns
				02		13.5	
TBUF three-state to output inactive (pair of pull-ups)	t_{PUF}		3/	01		11.6	ns
				02		10.5	

1/ Tested initially and after any design or process change that may affect this parameter and guaranteed to the limits specified in table I with the following conditions:
Global clock at 16MHz for device 01, and 25 MHz for devices 02.
20 outputs at 5 MHz
50 outputs at 1 MHz
Alternate clock at 10 MHz
100 configurable logic blocks (CLB) at 5 MHz
150 CLBs at 1 MHz
20 horizontal long lines at 5 MHz
30 vertical long lines at 1 MHz
50 inputs at 5 MHz
10 inputs at 10 MHz

2/ $\overline{\text{PWRDWN}}$ transitions must occur during operational V_{CC} levels.

3/ Parameter is not directly tested. Devices are first 100 percent functionally tested. Benchmark patterns (t_{B1-7}) are then used to determine the compliance of this parameter. Characterization data is taken initially and after any design or process change which may affect this parameter.

Case Y

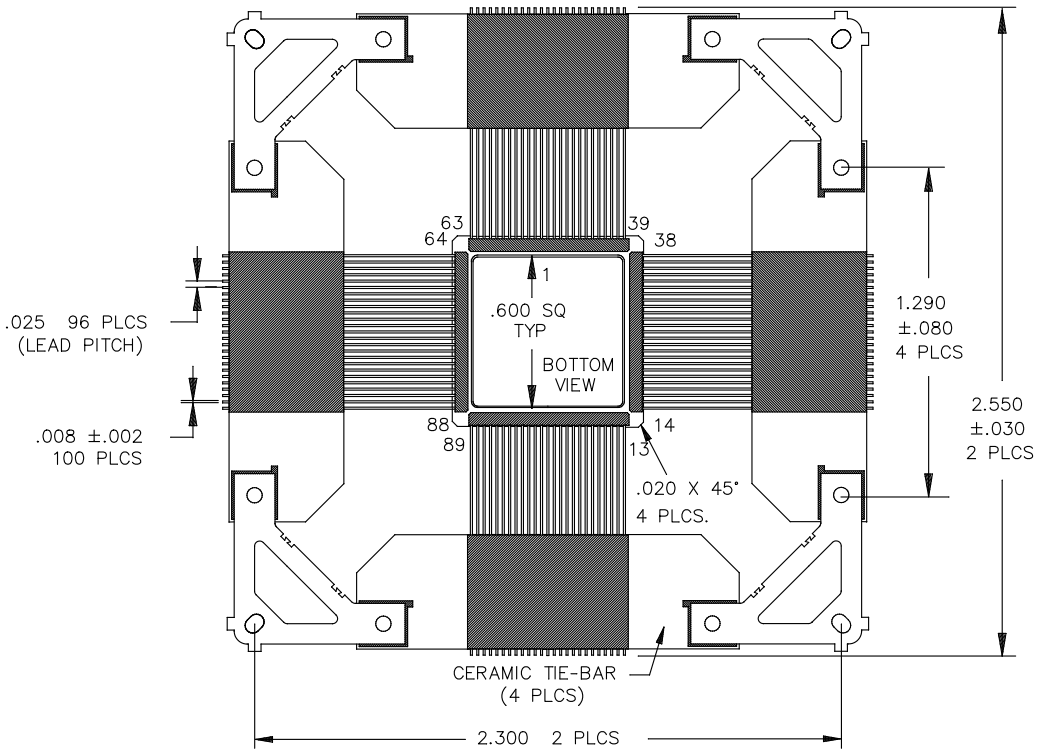


NOTES:

1. Top side mark location, product mark is located on the lid side of package; i.e., lid side facing up. When mounted in this position, the pin out is clockwise.
2. Dimensions are in inches.
3. The US government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch- pound units, the inch-pound units shall take precedence.
4. Pin 1 identifier location. Pin 1 is the middle pin on the side with center justified identifier mark. Identifier mark may be a notch, dot, or triangle.
5. The leads of this package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true positions" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete. Package lead protection mechanisms (tie bars) are shown on the drawing for reference only. When microcircuit devices contained in this package style are shipped for use in Government equipment, or shipped directly to the Government as spare parts or mechanical qualification samples, lead "true position" and "coplanarity" protection shall be in place.

FIGURE 1. Case outline.

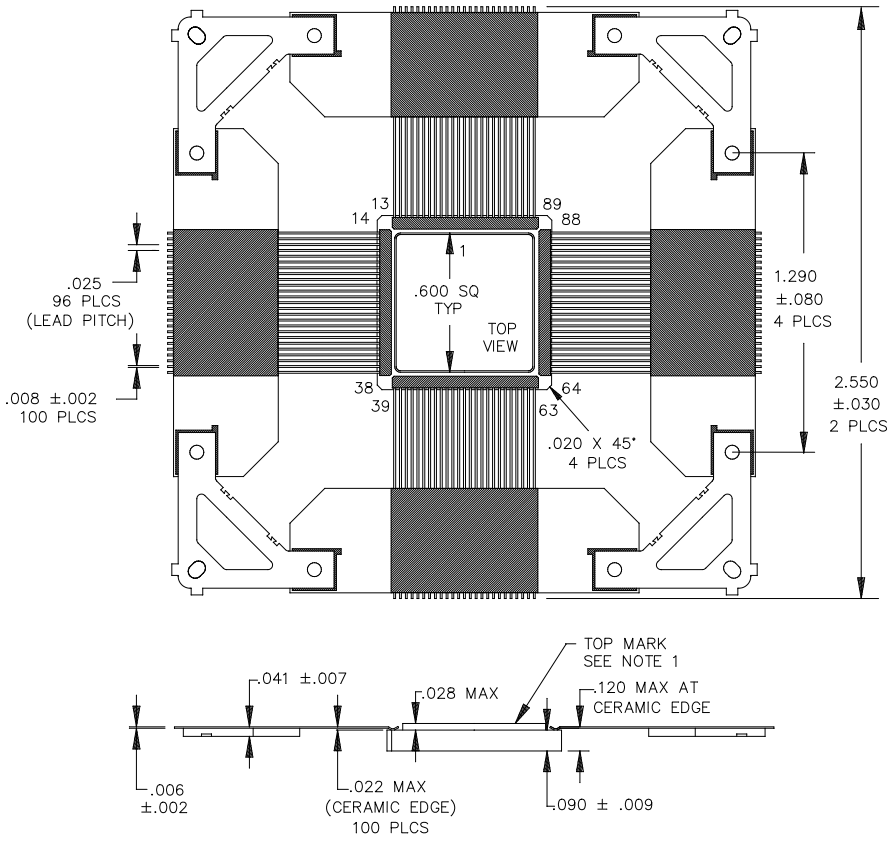
Case Y – continued.



Inches	Mm	Inches	mm
.002	0.05	.025	0.64
.006	0.15	.028	0.71
.008	0.20	.030	0.76
.009	0.23	.090	2.29
.010	0.25	.120	3.05
.020	0.51	.600	15.24
.022	0.56	.750	19.05
		2.550	64.77

FIGURE 1. Case outline - Continued.

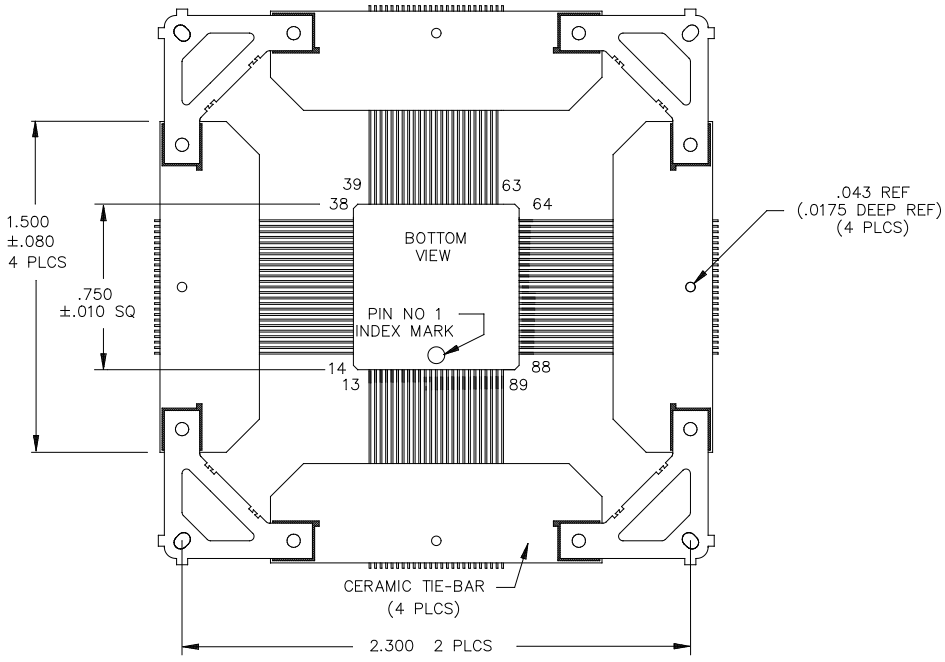
Case Z



NOTES:

1. Top side mark location, product mark is located on the lid side of package; i.e., lid side facing up. When mounted in this position, the pin out is clockwise.
2. Dimensions are in inches.
3. The US government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
4. Pin 1 identifier location. Pin 1 is the middle pin on the side with center justified identifier mark. Identifier mark may be a notch, dot, or triangle.
5. The leads of this package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true positions" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete. Package lead protection mechanisms (tie bars) are shown on the drawing for reference only. When microcircuit devices contained in this package style are shipped for use in Government equipment, or shipped directly to the Government as spare parts or mechanical qualification samples, lead "true position" and "coplanarity" protection shall be in place.

FIGURE 1. Case outline - Continued.



Inches	Mm	Inches	mm
.002	0.05	.025	0.64
.006	0.15	.028	0.71
.008	0.20	.030	0.76
.009	0.23	.090	2.29
.010	0.25	.120	3.05
.020	0.51	.600	15.24
.022	0.56	.750	19.05
		2.550	64.77

FIGURE 1. Case outline - Continued.

Case outline X

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
A1	A9-I/O		D10	WRT-D1-I/O		K2	M2-I/O
A2	A8-I/O		D11	I/O		K3	HDC-I/O
A3	A11-I/O		E1	I/O		K4	I/O
A4	I/O		E2	I/O		K5	$\overline{\text{I/O}}$
A5	A6-I/O		E3	I/O		K6	INIT-I/O
A6	A13-I/O		E9	I/O		K7	I/O
A7	A14-I/O		E10	$\overline{\text{D2}}$-I/O		K8	I/O
A8	I/O		E11	CS1-I/O		K9	$\overline{\text{I/O}}$
A9	A3-I/O		F1	I/O		K10	MASTER RESET
A10	A2-I/O		F2	I/O		K11	D7-I/O
A11	CCLK		F3	V_{CC}		L1	MO-RTRIG
B1	$\overline{\text{I/O}}$		F9	V_{CC}		L2	$\overline{\text{I/O}}$
B2	PWRDN		F10	D5-I/O		L3	LDC-I/O
B3	A10-I/O		F11	D3-I/O		L4	I/O
B4	I/O		G1	M2-I/O		L5	I/O
B5	A12-I/O		G2	I/O		L6	I/O
B6	A15-I/O		G3	I/O		L7	I/O
B7	A4-I/O		G9	I/O		L8	I/O
B8	I/O		G10	I/O		L9	I/O
B9	$\overline{\text{CS}}$2-A1-I/O		G11	D4-I/O		L10	I/O
B10	WS-A0-I/O		H1	I/O		L11	XT2-I/O
B11	DIN-D0-I/O		H2	I/O			
C1	I/O		H10	D6-I/O			
C2	TCLKIN-I/O		H11	I/O			
C3	INDEX PIN		J1	I/O $\overline{\text{\quad\quad}}$			
C5	A7-I/O		J2	M1-RDATA			
C6	GND		J5	I/O			
C7	A5-I/O		J6	GND			
C10	$\overline{\text{DOUT}}$-I/O		J7	I/O $\overline{\text{\quad}}$			
C11	RCLK-I/O		J10	DONE-PG			
D1	I/O		J11	XTL1-I/O-CLKIN			
D2	I/O		K1	I/O			

NC = no connect

FIGURE 2. Terminal connections.

Case outlines Y and Z.

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
1	GND		35	I/O		68	D6-I/O
2	A13		36	I/O		69	I/O
3	A6		37	M1-RDATA		70	I/O
4	A12		38	GND		71	I/O
5	A7		39	MO-TRIG		72	D5-I/O
6	I/O		40	V_{CC}		73	CSO
7	I/O		41	M2		74	D4-I/O
8	A11		42	HDC		75	I/O
9	A8		43	I/O		76	V_{CC}
10	A10		44	LDC		77	D3-I/O
11	A9		45	I/O		78	CS1
12	V_{CC}		46	I/O		79	D2-I/O
13	GND		47	I/O		80	I/O
14	PWRDWN		48	I/O		81	I/O
15	TCLKIN-I/O		49	I/O		82	I/O
16	I/O		50	INIT		83	D1-I/O
17	I/O		51	GND		84	RCLK-RDY/BUSY
18	I/O		52	I/O		85	DIN-DO-I/O
19	I/O		53	I/O		86	DOUT-I/O
20	I/O		54	I/O		87	CCLK
21	I/O		55	I/O		88	V_{CC}
22	I/O		56	I/O		89	GND
23	I/O		57	I/O		90	WS-A0
24	I/O		58	I/O		91	CS2-A1
25	I/O		59	I/O		92	I/O
26	V_{CC}		60	I/O		93	A2
27	I/O		61	XTL2-I/O		94	A3
28	I/O		62	GND		95	I/O
29	I/O		63	RESET		96	I/O
30	I/O		64	V_{CC}		97	A15
31	I/O		65	DONE-PG		98	A4
32	I/O		66	D7-I/O		99	A14
33	I/O		67	BCLKIN-XTL1-I/O		100	A5
34	I/O						

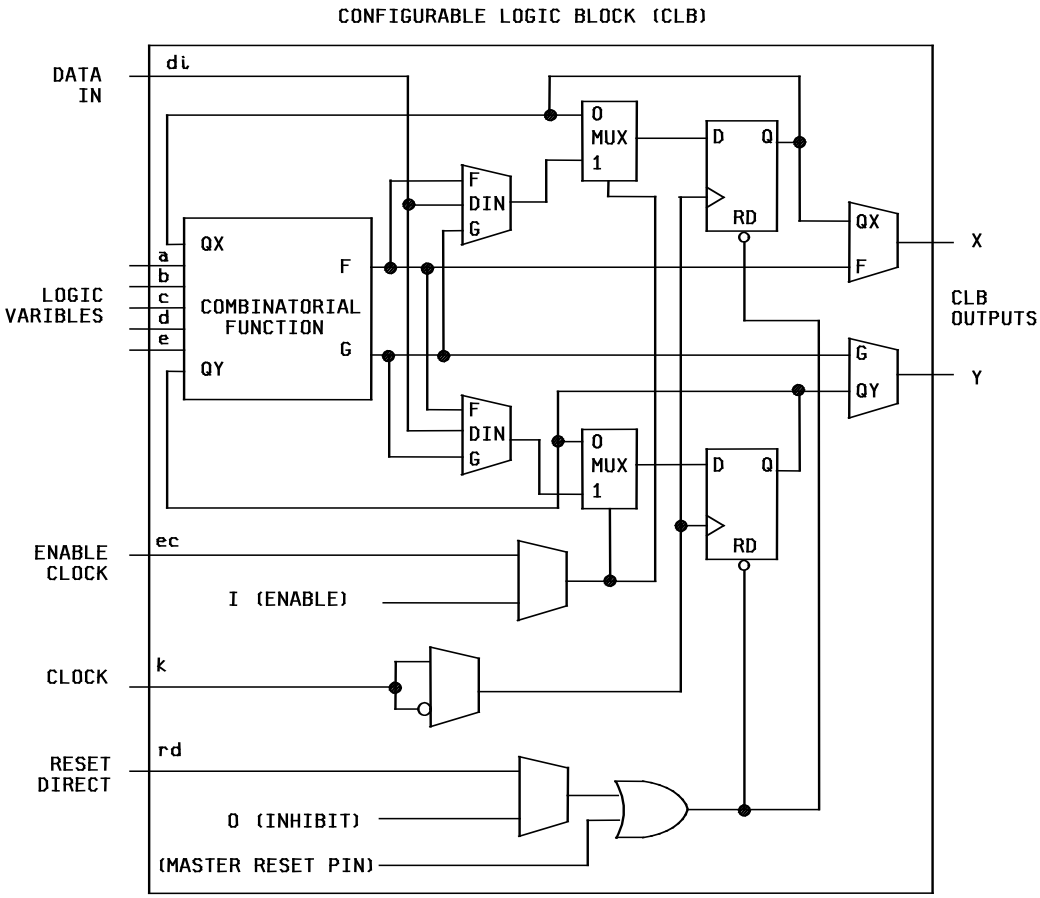
NC = no connect

FIGURE 2. Terminal connections - Continued.

Case outlines U

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
A1	$\overline{\text{PWRDWN}}$		D3	V_{CC}		L13	I/O
A2	NC		D12	V_{CC}		L14	NC
A3	NC		D13	I/O		M1	I/O
A4	I/O		D14	LDC-I/O		M2	A0-W5-I/O
A5	I/O		E1	A7-I/O		M3	DOUT-I/O
A6	I/O		E2	I/O		M4	V_{CC}
A7	I/O		E3	I/O		M5	D1-I/O
A8	I/O		E12	I/O		M6	D2-I/O
A9	I/O		E13	NC		M7	GND
A10	I/O		E14	I/O		M8	V_{CC}
A11	NC		F1	NC		M9	D2-I/O
A12	NC		F2	A12-I/O		M10	I/O
A13	NC		F3	I/O		M11	V_{CC}
A14	MO-RT		F12	I/O		M12	D7-I/O
B1	A10-I/O		F13	I/O		M13	XTAL2-I/O
B2	I/O		F14	I/O		M14	I/O
B3	I/O		G1	A6-I/O		N1	A1-CS2-I/O
B4	I/O		G2	A13-I/O		N2	DIN-D0-I/O
B5	I/O		G3	V_{CC}		N3	I/O
B6	I/O		G12	V_{CC}		N4	$\overline{\text{RCLK}}$-BUSY/RDY-I/O
B7	I/O		G13	I/O		N5	I/O
B8	I/O		G14	INIT-I/O		N6	NC
B9	I/O		H1	A14-I/O		N7	D3-I/O
B10	I/O		H2	A5-I/O		N8	D4-I/O
B11	I/O		H3	GND		N9	$\overline{\text{CSO}}$-I/O
B12	I/O		H12	GND		N10	I/O
B13	M1-$\overline{\text{RD}}$		H13	I/O		N11	D6-I/O
B14	HDC-I/O		H14	I/O		N12	I/O
C1	I/O		J1	NC		N13	DONE-PG
C2	A9-I/O		J2	A4-I/O		N14	I/O
C3	I/O		J3	I/O		P1	CCLK
C4	GND		J12	I/O		P2	I/O
C5	I/O		J13	I/O		P3	I/O
C6	I/O		J14	I/O		P4	I/O
C7	GND		K1	A15-I/O		P5	NC
C8	V_{CC}		K2	I/O		P6	CS1- I/O
C9	I/O		K3	I/O		P7	I/O
C10	I/O		K12	I/O		P8	NC
C11	GND		K13	I/O		P9	NC
C12	I/O		K14	I/O		P10	I/O
C13	M2-I/O		L1	A3-I/O		P11	NC
C14	I/O		L2	A2-I/O		P12	I/O
D1	A11-I/O		L3	GND		P13	XTAL1- I/O
D2	A8-I/O		L12	GND		P14	$\overline{\text{RESET}}$

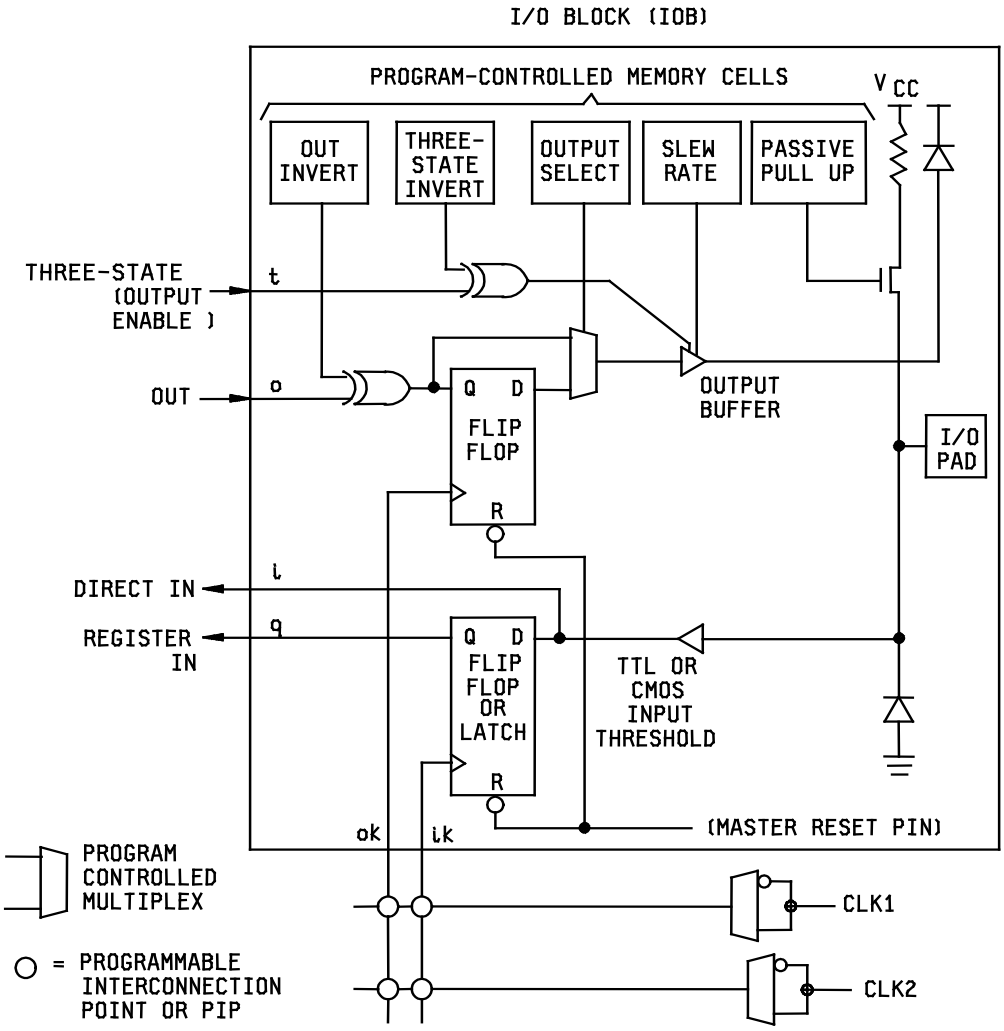
FIGURE 2. Terminal connections - Continued.



NOTE: Each configurable logic block includes a combinatorial logic section, two flip-flops, and program memory controlled multiplexer selection of function.

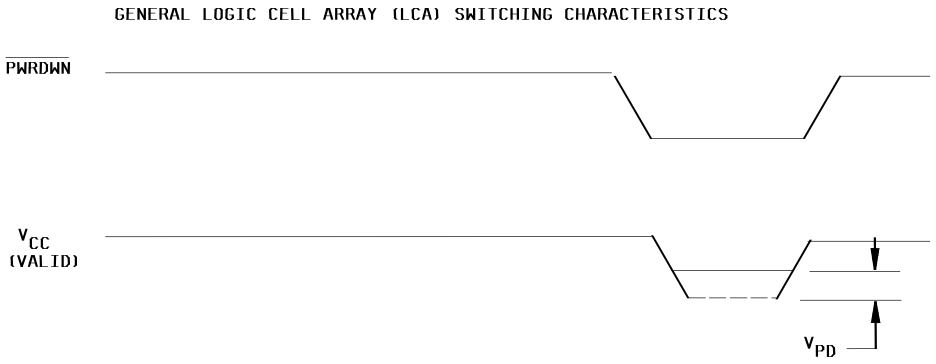
It has: Five logic variable inputs: a, b, c, d, and e.
a direct data input: di
an enable clock: ec
a clock (invertible): k
an asynchronous reset: rd
two outputs: x and y

FIGURE 3. Logic block diagram.



NOTE: The input/output block includes input and output storage elements and I/O options selected by configuration memory cells. A choice of two clocks is available on each die edge. The polarity of each clock line (not each flip-flop or latch) is programmable. A clock line that triggers the flip-flop on the rising edge is an active low latch enable (latch transparent) signal and vice versa. Passive pull-up can only be enable on inputs, not on outputs. All user inputs are programmed for TTL or CMOS thresholds.

FIGURE 3. Logic block diagram - Continued.



NOTE: All timings except t_{TSHZ} and t_{TSON} are measured at 1.5 V levels with 50 pF minimum output load. For input signals, rise and fall times are less than 6.0 ns, with low amplitude = 0.0 V, and high amplitude = 3.0 V.

FIGURE 4. Timing diagrams and switching characteristics.

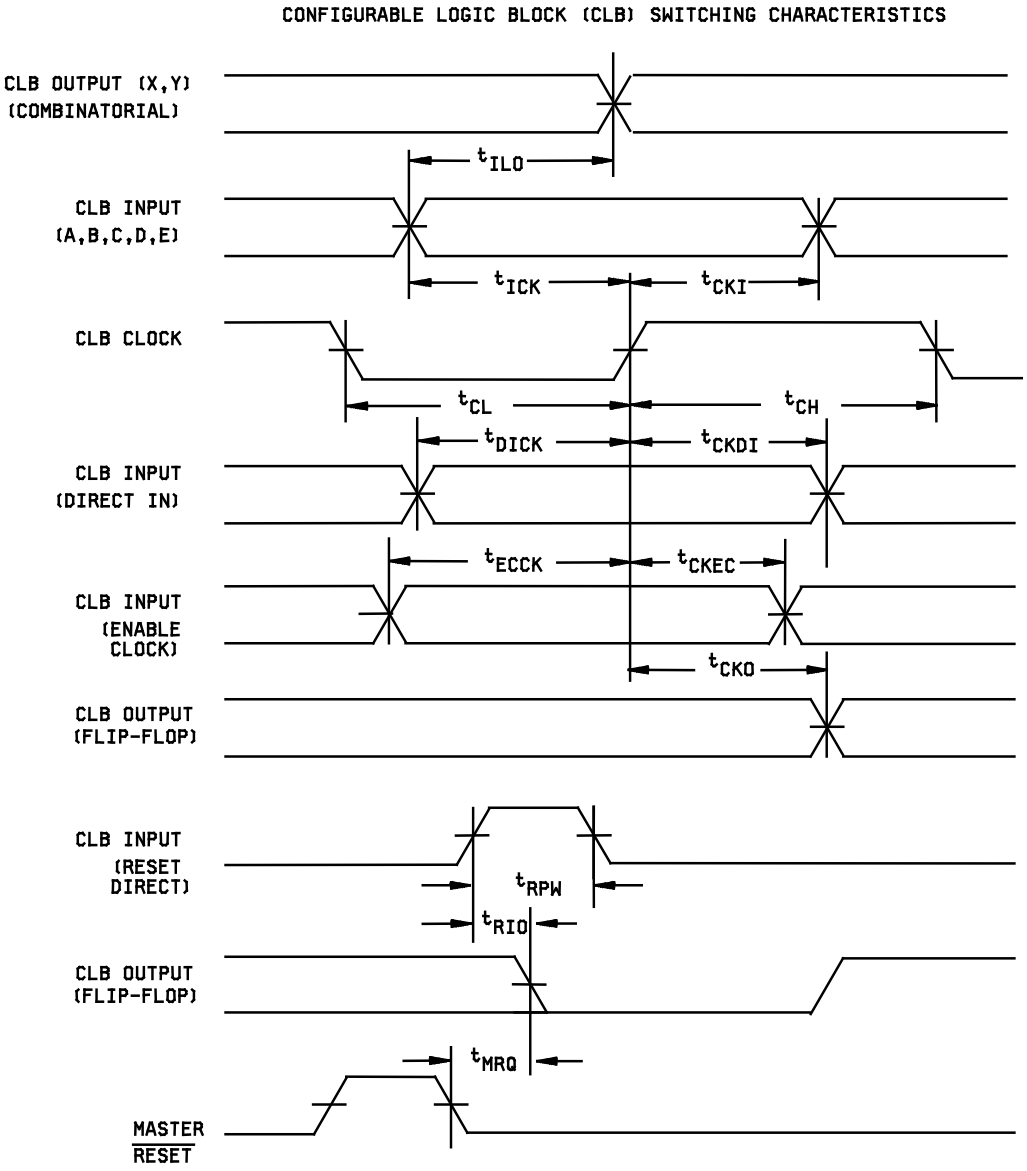
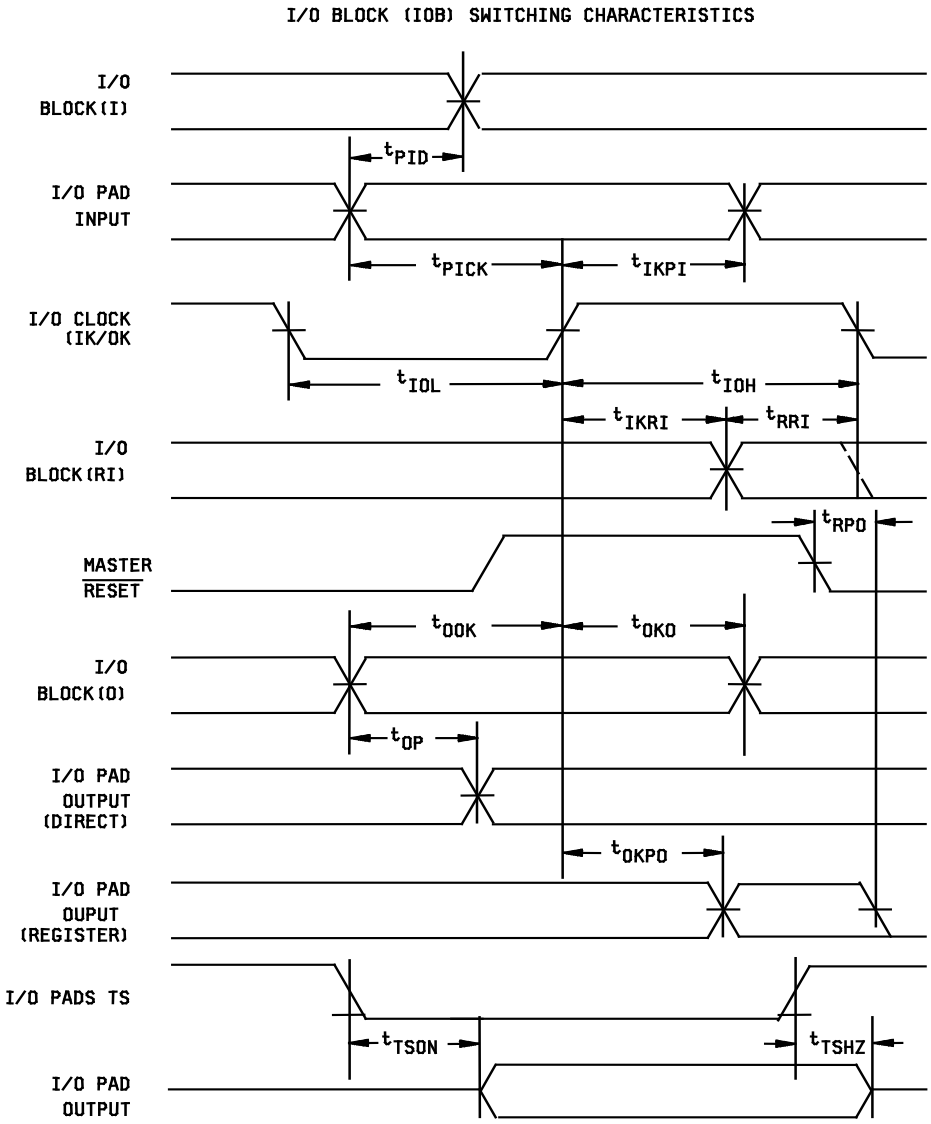
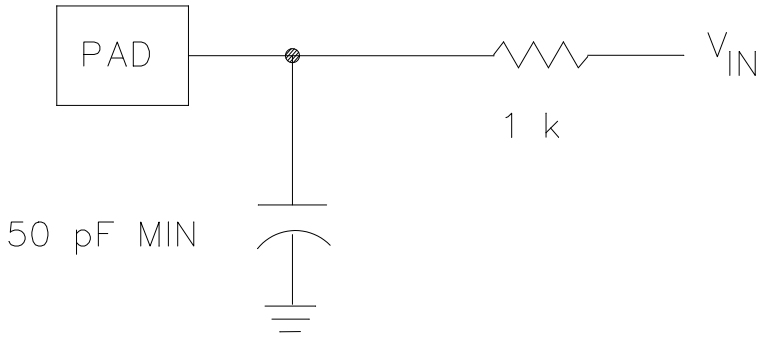


FIGURE 4. Timing diagrams and switching characteristics - Continued.

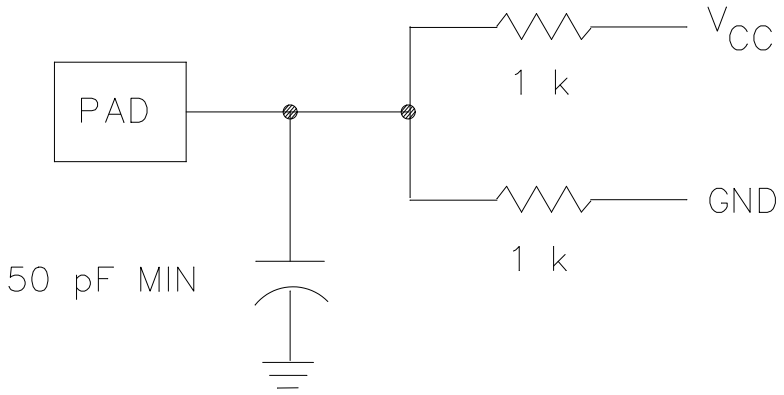


NOTE: All timings except t_{TSHZ} and t_{TSON} are measured at 1.5 V with 50 pF minimum load output. For input signals, rise and fall times are ≤ 6ns, low amplitude = 0 V and high = 3 V. t_{TSHZ} is determined when the output shifts 10 percent (of the output voltage swing) from V_{OL} level or V_{OH} level. See figure 5, circuit A herein for circuit used. t_{TSON} is measured at 0.5 V_{CC} level with V_{IN} = 0.0 for three-state to active high, and V_{IN} = V_{CC} for three-state to active low. See figure 5, circuit B herein for circuit used.

FIGURE 4. Timing diagrams and switching characteristics - Continued.



CIRCUIT A



CIRCUIT B

FIGURE 5. Load circuit.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1, 7, 9	1, 7, 9
2	Static burn-in (method 1015)	Required	Required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Not required	Not required	Not required
5	Final electrical parameters	1*, 2, 3, 7*, 8A, 8B, 9, 10,11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10 11
6	Group A test requirements	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
7	Group C end-point electrical parameters	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B Δ	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
8	Group D end-point electrical parameters	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
9	Group E end-point electrical parameters	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{CCO} standby	± 300 μA
I_{IL}, I_{OL}	± 2 nA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.5 Delta measurements for device class Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

6.7 Additional operating data.

a. Power on delay is 2^{14} cycles from the non-master mode. This provides 11 to 33 ms of wait time.

b. Power on delay is 2^{16} cycles for the master mode. This provides 43 to 130 ms of wait time.

c. Clear is 375 cycles ±25 cycles and may take as long as 250 to 750 ms.

d. During normal power up, V_{CC} must rise from 2.0 V to V_{CC} minimum in less than 10 ms. If this does not occur, configuration must be delayed by using RESET.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 14-03-24

Approved sources of supply for SMD 5962-95610 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9561001MXC	3/	XC3142A-5PG84B
5962-9561001MUC	3/	XC3142A-5PG132B
5962-9561001MYC	3/	XC3142A-5CB100B
5962-9561001MZC	3/	XC3142A-5CB100B
5962-9561002MXC	3/	XC3142A-4PG84B
5962-9561002MUC	3/	XC3142A-4PG132B
5962-9561002MYC	3/	XC3142A-4CB100B
5962-9561002MZC	3/	XC3142A-4CB100B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply. The last known supplier is listed below.

Vendor CAGE number	Vendor name and address
68994	Xilinx, Incorporated 2100 Logic Drive San Jose, CA 95124