REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Table IA, Capacitance test - moved packages to show correct capacitance. Added conversion table for Y and Z package. Redrew case U figure 1 to correct row names. Made changes to Table IIA. ksr	99-04-09	Raymond Monnin
B	Boilerplate update, part of 5 year review. ksr	07-06-12	Robert M. Heber
C	Update drawing to reflect current MIL-PRF-38535 requirements. llb	16-05-16	Charles F. Saffle

REV	C	C	C	C	C															
SHEET	35	36	37	38	39															
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

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CHECKED BY
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APPROVED BY
Raymond Monnin

DRAWING APPROVAL DATE
96-06-24

REVISION LEVEL
C

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990
http://www.landandmaritime.dla.mil

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, 36000 GATE PROGRAMMABLE LOGIC ARRAY MONOLITHIC SILICON

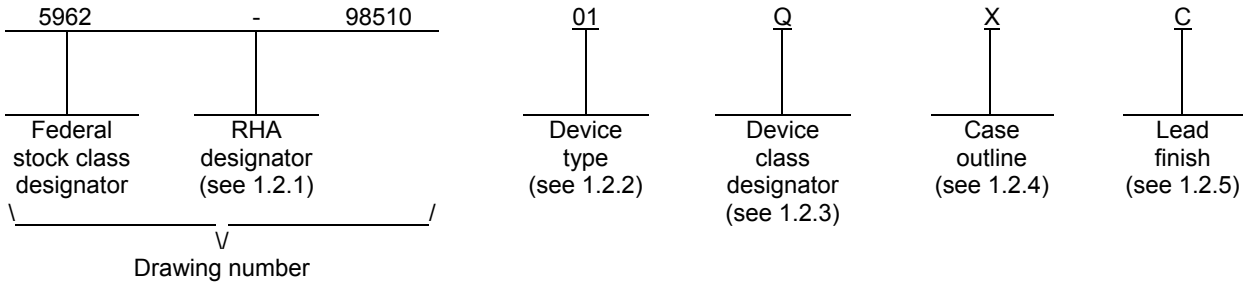
SIZE	CAGE CODE	
A	**67268**	**5962-98510**

SHEET 1 OF 39

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of space application (device class V), high reliability (device class Q), and nontraditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN. For device class N, the user is cautioned to assure that the device is appropriate for the application environment.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes N, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type. The device type identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	XQ4036XL-3	36,000 gate programmable array	3.0 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
N	Certification and qualification to MIL-PRF-38535 with a nontraditional performance environment (encapsulated in plastic)
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outlines. The case outlines are as designated in MIL-STD-1835, JEP 95, and as follows:

Outline letter	Descriptive designator	Terminals	Package style	Document
X	CMGA36-P411	411	Pin grid array package	MIL-STD-883
Y	See figure 1	228	Quad flat package	
Z	See figure 1	228	Quad flat package	
U	LBGA-B-352 (JEDEC MO-192-BAR-2)	352	Plastic, Ball grid array with four rows on each side	JEP 95
T	PQFP-G-240 (JEDEC MS-029-GA)	240	Plastic, Quad flat package with heat sink molded in the package	JEP 95

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q, and V.

1.3 Absolute maximum ratings. 1/ 2/

Supply voltage range to ground potential (V_{CC})	-0.5 V dc to +4.0 V dc
DC input voltage range (V_{IN})	-0.5 V to 5.5 V
Voltage applied to three-state output (V_{TS})	-0.5 V to 5.5 V
Lead temperature (soldering, 10 seconds)	+260°C
Power dissipation (P_D)	2.0 W
Thermal resistance, junction-to-case (θ_{JC}):	
Case outline X	See MIL-STD-1835
Case outline Y, Z	20°C/W 3/
Case outline U	0.8°C/W 3/
Case outline T	1.5°C/W 3/
Junction temperature (T_J) for ceramic packages	+150°C 4/
Junction temperature (T_J) for plastic packages	+125°C 4/
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage relative to ground (V_{CC})	+3.0 V dc minimum to +3.6 V dc maximum
Input high voltage (V_{IH})	50% of V_{CC} to 5.5 V
Input low voltage (V_{IL})	0V to 30% of V_{CC}
Maximum input signal transition time (t_{IN})	250 ns
Case operating temperature range (T_C)	-55°C to +125°C
Junction operating temperature range (T_J)	-55°C to +125° for Plastic packages

1.5 Digital logic testing for device classes N, Q, and V.

Fault coverage measurement of manufacturing logic tests (Method 5012 of MIL-STD-883)	99.9 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ All voltage values in this drawing are with respect to V_{SS}.
2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ When a thermal resistance for this case is specified in MIL-STD-1835 that value shall supersede the value indicated herein.
4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with Method 5004 of MIL-STD-883.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation *or contract*.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP 95 - Registered and Standard Outlines for Semiconductor Devices

(Copies of this document are available online at www.jedec.org/ or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions for device classes N, Q, and V shall be as specified in MIL-PRF-38535 and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Logic block diagram. The logic block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. A certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $3.0 \le Vcc \le 3.6V$ ($-55°C \le T_C \le +125°C$ for ceramic packages) ($-55°C \le T_J \le +125°C$ for plastic packages)	Group A subgroups	Device type	Limits		Unit
					Min	Max	
High-level output voltage	VOH	I_{OH} = -4 mA, V_{CC}=min (LVTTL)	1, 2, 3	01	2.4		V
High-level output voltage		I_{OH} = -500 µA, V_{CC}= min (LVCMOS)	1, 2, 3	01	90% V_{CC}		V
Low-level output voltage	VOL	I_{OL} = 12 mA, V_{CC}=min (LVTTL) 1/	1, 2, 3	01		0.4	V
Low-level output voltage		I_{OL} = 1500 µA, V_{CC}=min (LVCMOS)	1, 2, 3	01		10% V_{CC}	V
Data Retention Supply Voltage (below which configuration data may be lost)	VDR	(Read back mode only)	1, 2, 3	01	2.5		V
Quiescent FPGA Supply current 2/	ICCO		1, 2, 3	01		15	mA
Input or output leakage current	IL		1, 2, 3	01	-10	+10	µA
Input capacitance (sample tested) U and T case outlines	CIN, COUT	See 4.4.1e, f = 1.0 Mhz, V_{OUT} = 0 V	4	01		10	pF
Input capacitance (sample tested) X, Y, and Z case outline						6	pF
Pad pull-up (when selected)	IRPU	V_{IN} = 0V (sample tested)	1, 2, 3	01	0.02	0.25	mA
Pad pull-down (when selected)	IRPD	V_{IN} = 3.6V (sample tested)	1, 2, 3	01	0.02	0.15	mA
Horizontal Longline pull-up (when selected) @ logic Low	IRLL		1, 2, 3	01	03	2.0	mA
Functional test	FT	See 4.4.1c	7, 8A, 8B	01			

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $3.0 \le Vcc \le 3.6V$ ($-55°C \le T_C \le +125°C$ for ceramic packages) ($-55°C \le T_J \le +125°C$ for plastic packages)	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Wide Decoder Switching Characteristic Guidelines							
Full length, two pull-ups, inputs from IOB I-pins 3/	TWAF2	See figure 4 as applicable 4/ 5/	9, 10, 11	01		11.6	ns
Half length, two pull-ups, inputs from IOB I-pins 3/	TWAO2					8.0	
CLB Switching Characteristic Guidelines							
Combinatorial Delays							
F/G inputs to X/Y outputs	TILO	See figures 3 and 4 as applicable 4/ 5/	9, 10, 11	01		1.6	ns
F/G inputs via H' to X/Y outputs	TIHO					2.7	
F/G inputs via transparent latch to Q outputs	TITO	See figures 3 and 4 as applicable 6/				2.9	
C inputs via SR/HO via H to X/Y outputs	THH0O	See figures 3 and 4 as applicable 4/ 5/				2.5	
C inputs via HI via H to X/Y outputs	THH1O					2.4	
C inputs via DIN/H2 via H to X/Y outputs	THH2O					2.5	
C inputs via EC, DIN/H2 to YQ, XQ output (bypass)	TCBYP					1.5	
CLB Fast Carry Logic							
Operand inputs (F1, F2, G1, G4) to C_{OUT}	TOPCY	See figure 3 as applicable 6/	9, 10, 11	01		2.7	ns
Add/Subtract input (F3) to C_{OUT}	TASCY	See figure 3 as applicable 6/				3.3	
Initialization inputs (F1, F3) to C_{OUT}	TINCY	See figure 3 as applicable 4/ 5/				2.0	
C_{IN} through function generators to X/Y outputs	TSUM	See figure 3 as applicable 4/ 5/				2.8	
C_{IN} to C_{OUT}, bypass function generations	TBYP	See figure 3 as applicable 6/				0.3	
Sequential Delays							
Clock K to Flip-Flop outputs Q	TCKO	See figures 3 and 4 as applicable 4/ 5/	9, 10, 11	01		2.1	ns
Clock K to Latch outputs Q	TCKLO	See figure 3 6/				2.1	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $3.0 \le Vcc \le 3.6V$ ($-55°C \le T_C \le +125°C$ for ceramic packages) ($-55°C \le T_J \le +125°C$ for plastic packages)	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Setup Time before Clock K							
F/G inputs	TICK	See figure 3 6/	9, 10, 11	01	1.1		ns
F/G inputs via H	TIHCK				2.2		
C inputs via H0 through H	THH0CK				2		
C inputs via H1 through H	THH1CK				1.9		
C inputs via H2 through H	THH2CK				2		
C inputs Via DIN	TDICK				0.9		
C inputs via EC	TECCK				1		
C inputs via S/R, going Low (inactive)	TRCK				0.6		
C_{IN} input via F/G	TCCK				2.3		
C_{IN} input via F/G and H	TCHCK				3.4		
Hold Time after Clock K							
F/G inputs	TCKI	See figure 3 6/	9, 10, 11	01	0		ns
F/G inputs via H	TCKIH				0		
C inputs via SR/HO through H	TCKHH0				0		
C inputs via H1 through H	TCKHH1				0		
C inputs via DIN/H2 through H	TCKHH2				0		
C inputs via DIN/H2	TCKDI				0		
C inputs via EC	TCKEC				0		
C inputs via SR, going Low (inactive)	TCKR				0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $3.0 \le Vcc \le 3.6V$ $(-55°C \le T_C \le +125°C$ for ceramic packages) $(-55°C \le T_J \le +125°C$ for plastic packages)	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock							
Clock High time	TCH	See figure 3 6/	9, 10, 11	01	3		ns
Clock Low time	TCL						
Set/Reset Direct							
Width (High)	TRPW	See figure 3 6/	9, 10, 11	01	3		ns
Delay from C inputs via S/R, going High to Q	TRIO					3.7	
Global Set/Reset							
Minimum GSR Pulse Width	TMRW	See figure 3 6/	9, 10, 11	01	19.8		ns
Delay from GSR input to any Q	TMRQ					22.5	
Delay from GSR input to any Pad	TRPO					27.1	
Toggle Frequency (MHz) 7/	FTOG					166	MHz
Propagation Delays							
Clock (OK) to Pad	TOKPOF	See figure 3 6/	9, 10, 11	01		5	ns
Output (O) to Pad	TOPF					4.1	
3 state to Pad hi-Z (slew-rate independent)	TTSHZ					4.4	
3-state to Pad active and valid	TTSONF					4.1	
Output (O) to Pad via Fast Output MUX	TOFPF					5.5	
Setup and Hold Times							
Output (O) to clock (OK) setup time	TOOK	See figure 3 6/ 8/	9, 10, 11	01	0.5		ns
Output (O) to clock (OK) hold time	TOKO				0		
Clock Enable (EC) to clock (OK) setup	TECOK				0		
Clock Enable (EC) to clock (OK) hold	TOKEC				0.3		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 3.0 ≤ Vcc ≤ 3.6V (-55°C ≤ T_C ≤ +125°C for ceramic packages) (-55°C ≤ T_J ≤ +125°C for plastic packages)	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Slew Rate Adjustment							
for output SLOW option add	TSLOW	6/	9, 10, 11	01		3	ns
BENCHMARK PATTERNS (100% Tested) Conditions							
Core + TILO+TIHO	TILHO1	See figure 4 as applicable 4/ 5/ 9/	9, 10, 11	01		50.9	ns
Core + TILO+TIHO	TILHO2					51.6	
Core + TILO+TIHO	TILHO3					51.0	
Core + TILO+TIHO	TILHO4					51.0	
Core + TILO+TIHO	TILHO5					51.9	
Core + THH0O +THECQO	THH0O					80.9	
Core + THH10 + THH2QO	THH10					84.7	
Core + THH20 + THELQO	THH20					80.7	
Core + TINCY + TSUM	CRY1					52.9	
Local Line Patterns							
Core + Local Line 1	LOCAL 1	See figure 4 as applicable 4/ 5/ 9/	9, 10, 11	01		92.8	ns
Core + Local Line 2	LOCAL 2					102.0	
Core + Local Line 3	LOCAL 3					104.4	
Core + Local Line 4	LOCAL 4					106.5	
Core + Local Line 5	LOCAL 5					113.4	
Core + Local Line 6	LOCAL 6					104.7	
Core + Local Line 7	LOCAL 7					109.3	
Core + Local Line 8	LOCAL 8					101.7	
Core + Local Double Line 1	DBL 1					81.4	
Core + Local Double Line 2	DBL 2					81.6	
Core + Horizontal Quad A	QHA					128.6	
Core + Horizontal Quad B	QHB					137.4	
Core + Horizontal Quad C	QHC					135.0	
Core + Vertical Quad A	QVA					135.0	
Core + Vertical Quad B	QVB					137.7	
Core + Vertical Quad C	QVC					135.1	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $3.0 \le Vcc \le 3.6V$ ($-55°C \le T_C \le +125°C$ for ceramic packages) ($-55°C \le T_J \le +125°C$ for plastic packages)	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Long-Line patterns							
Core + Horizontal Long Line 1	HLL1	See figure 4 as applicable 4/ 5/ 9/	9, 10, 11	01		92.2	ns
Core + Horizontal Long Line 2	HLL2					127.5	
Core + Horizontal Long Line 3	HLL3					124.2	
Core + Horizontal Long Line 4	HLL4					100.7	
Core + Horizontal Long Line 5	HLL5					130.6	
Core + Horizontal Long Line 6	HLL6					130.0	
Core + Vertical Long Line 1	VLL1					66.3	
Core + Vertical Long Line 2	VLL2					68.6	
Core + Vertical Long Line 3	VLL3					72.2	
Core + Vertical Long Line 4	VLL4					71.5	
Core + Vertical Long Line 5	VLL5					70.4	
Core + Vertical Long Line 6	VLL6					69.6	
Core + Vertical Long Line 7	VLL7					72.7	
Core + Vertical Long Line 8	VLL8					74.3	
Core + Vertical Long Line 9	VLL9					74.6	
Core + Vertical Long Line 10	VLL10					74.1	
Core + Horizontal Long Line 1 (Loaded)	HLL1_L					148.9	
Core + Horizontal Long Line 2 (Loaded)	HLL2_L					203.0	
Core + Horizontal Long Line 3 (Loaded)	HLL3_L					190.8	
Core + Horizontal Long Line 4 (Loaded)	HLL4_L					159.4	
Core + Horizontal Long Line 5 (Loaded)	HLL5_L					207.7	
Core + Horizontal Long Line 6 (Loaded)	HLL6_L					214.1	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $3.0 \le Vcc \le 3.6V$ ($-55°C \le T_C \le +125°C$ for ceramic packages) ($-55°C \le T_J \le +125°C$ for plastic packages)	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Core + Vertical Long Line 1 (Loaded)	VLL1_L	See figure 4 as applicable 4/ 5/	9, 10, 11	01		107.8	ns
Core + Vertical Long Line 2 (Loaded)	VLL2_L					96.8	
Core + Vertical Long Line 3 (Loaded)	VLL3_L					99.0	
Core + Vertical Long Line 4 (Loaded)	VLL4_L					103.2	
Core + Vertical Long Line 5 (Loaded)	VLL5_L					96.7	
Core + Vertical Long Line 6 (Loaded)	VLL6_L					103.0	
Core + Vertical Long Line 7 (Loaded)	VLL7_L					103.6	
Core + Vertical Long Line 8 (Loaded)	VLL8_L					99.2	
Core + Vertical Long Line 9 (Loaded)	VLL9_L					89.0	
Core + Vertical Long Line 10 (Loaded)	VLL10_L					103.6	
Clock Patterns							
Global Low Skew Clock	GLS	See figure 4 as applicable 4/ 5/	9, 10, 11	01		57.4	ns
Global Early Clock	GE					142.3	
KX Clock Line	KX_K					127.0	
Edge Line Patterns							
Core + Edge Long Line	EDGELL	See figure 4 as applicable. 4/ 5/ and (9/ where applicable)	9, 10, 11	01		151.8	ns
Octal 1	OCTAL 1					79.4	
Core + Top Edge Double Line	T_EDBL					56.2	
Core + Left Edge Double Line	L_EDBL					51.1	
Core + Bottom Edge Double Line	B_EDBL					55.6	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 3.0 ≤ Vcc ≤ 3.6V (-55°C ≤ T_C ≤ +125°C for ceramic packages) (-55°C ≤ T_J ≤ +125°C for plastic packages)	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Edge Line Patterns – Continued.							
Core + Right Edge Double Line	R_EDBL	See figure 4 as applicable 4/ 5/ and (9/ where applicable)	9, 10, 11	01		53.3	ns
Top Left Half Wide Decoder	TL_HWD2					59.5	
Top Right Half Wide Decoder	TR_HWD2					138.7	
Full Wide Decoder	R_WD2					100.3	
Buffer Patterns							
Full Length Tbuf at HLL3	F_TBUF3	See figure 4 as applicable 4/ 5/	9, 10, 11	01		358.9	ns
Full Length Tbuf at HLL4	F_TBUF4					356.2	
Left Half Length Tbuf at HLL3 with 4 Pullup	L_TBUF3_4					106.7	
Left Half Length Tbuf at HLL4 with 4 Pullup	L_TBUF4_4					109.3	
Left Half Length Tbuf at HLL3 with 1 Pullup	L_TBUF3_1					598.3	
Left Half Length Tbuf at HLL4 with 1 Pullup	L_TBUF4_1					597.8	
Right Half Length Tbuf at HLL3 with 4 Pullup	R_TBUF3_4					105.7	
Right Half Length Tbuf at HLL4 with 4 Pullup	R_TBUF4_4					106.9	
Right Half Length Tbuf at HLL3 with 1 Pullup	R_TBUF3_1					596.4	
Right Half Length Tbuf at HLL4 with 1 Pullup	R_TBUF4_1					598.7	
Clock/Setup/Hold Patterns							
GLS Clock Setup	SETUP_GLS	See figure 4 as applicable 4/ 5/	9, 10, 11	01	6.6		ns
GE Clock Setup	SETUP_ GE				7.0		
GLS Clock Hold	HOLD_GLS				0		
GE Clock Hold	HOLD_GE				0.8		
GE Clock Hold	TCKO_GLS_POS					9.7	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $3.0 \le Vcc \le 3.6V$ ($-55°C \le T_C \le +125°C$ for ceramic packages) ($-55°C \le T_J \le +125°C$ for plastic packages)	Group A subgroups	Device type	Limits		Unit
					Min	Max	
GLS Clock To Out (rise)	TCKO_GLS_NEG	See figure 4 as applicable 4/ 5/	9, 10, 11	01		9.7	ns
GLS Clock To Out (fall)	TCKO_GE_POS					9.4	
GE Clock To Out (fall)	TCKO_GE_NEG					9.4	
IOB Patterns (CMOS)							
TPPLI To TOPS	TPPLI_TOPS	See figure 4 as applicable 4/ 5/ and (10 where applicable)	9, 10, 11	01		16.7	ns
TPID To Out Thru MUX1	TPID_TMUX1					7.3	
TPID to TOPF Thru Wide Decoder	TPID_WDEC_TOPF					36.8	
TPLI To Out Thru EC	TPLI_TECI					8.7	
TPPLI To Out Thru EC	TPPLI_TEC					15.2	
TPDLI To TOPF	TPDLI_TOPF					16.9	
TPFLI to TOPF	TPFLI_TOPF					8.8	
TPID To Out Thru MUX0	TPID_TMUXO					7.9	
TPPFLI To TOPF	TPPFLI_TOPF					14.4	
TPID To TOPF	TPID_TOPF					5.8	
TBUF driving half a Horizontal Longline (Horizontal Longline Switching Characteristics Guidelines)							
I going High or Low to half of a Horizontal Longline going High or Low, while T is Low. Buffer is constantly active.	T HIO1	See figure 4 as applicable 4/ 5/ 11/	9, 10, 11	01		4.8	ns
T going Low to half of a Horizontal Longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low	T HON					5.4	
T going High to half of a Horizontal Longline going from Low to High, pulled up by four resistors. 12/	T HPU4					5.3	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $3.0 \le Vcc \le 3.6V$ ($-55°C \le T_C \le +125°C$ for ceramic packages) ($-55°C \le T_J \le +125°C$ for plastic packages)	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TBUF driving a Horizontal Longline							
I going High or Low to Horizontal Longline going High or Low, while T is Low. Buffer is constantly active.	T IOI	See figure 4 as applicable 4/ 5/	9, 10, 11	01		11.6	ns
T going Low to Horizontal Longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	T ON					12.3	
T going High to Horizontal Longline going from Low to High, pulled up by two resistors. 13/	T PU2					14.4	
Setup Times (IOB Input Switching Characteristic Guidelines)							
Pad to Clock (IK), no delay	TPICK	See figure 3 as applicable 6/	9, 10, 11	01	1.7		ns
Pad to Clock (IK), partial delay	TPICKP				8.4		
Pad to Clock (IK), full delay	TPICKD				10.5		
Pad to Clock (IK), via transparent Fast Capture Latch, no delay	TPICKF				2.4		
Pad to Clock (IK), via transparent Fast Capture Latch, partial delay	TPICKFP				9.0		
Pad to Fast Capture Latch Enable (OK), no delay	TPOCK 8/				0.7		
Clock Enable (EC) to Clock (IK)	TECIK 8/				0.3		
Hold Times							
All Hold times	8/	See figure 3 as applicable 6/	9, 10, 11	01	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $3.0 \le Vcc \le 3.6V$ ($-55°C \le T_C \le +125°C$ for ceramic packages) ($-55°C \le T_J \le +125°C$ for plastic packages)	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Propagation Delays							
Pad to I1, 12 via transparent FCL and input latch, no delay 14/	TPFLI	See figures 3 and 4 as applicable 4/ 5/	9, 10, 11	01		3.1	ns
Pad to I1, 12 via transparent FCL and input latch, partial delay 14/	TPPFLI					9.8	
Clock (IK) to I1, 12 (flip flop)	TIKRI	See figures 3 and 4 as applicable 6/				1.8	
Clock (IK) to I1, 12 (latch enable, active Low)	TIKLI					1.9	
FCL Enable (OK) active edge to I1, 12 (via transparent standard input latch) 14/	TOKLI					3.6	
Minimum GSR Pulse Width	TMRW				19.8		
Delay from GSR input to any Q	TRRI					22.5	
Delay from FCL enable (OK) active edge to IFF clock (IK) active edge 15/	TOKIK				1.7		
Pad to I1, 12	TPID	See figures 3 and 4 as applicable 4/ 5/				1.6	
Pad to I1, 12 via transparent latch, no delay	TPLI					2.6	
Pad to I1, 12 via transparent input latch, partial delay	TPPLI					9.8	
Pad to I1, 12 via transparent input latch, full delay	TPDLI					11.9	

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 3.0 ≤ Vcc ≤ 3.6V (-55°C ≤ T_C ≤ +125°C for ceramic packages) (-55°C ≤ T_J ≤ +125°C for plastic packages)	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output Flip-Flop, Clock to Out (Pin to Pin Output parametrics Guidelines)							
Global Low Skew Clock to Output using OFF 16/	TICKOF	See figures 3 and 4 as applicable 4/ 5/ 17	9, 10, 11	01		9.8	ns
Global Early Clock to Output using OFF Values are for BUFGE #s 1, 2, 5 and 6. Add 1.4 ns for BUFGE #s 3, 4, 7 and 8 16/ 18/	TICKEOF					8.1	
For output SLOW option add	TSLOW					3.0	
Output/Output Mux/Clock to out							
Global Low Skew Clock to Output using OMUX 19/	TPFPF	See figure 3 as applicable 6/ 17/	9, 10, 11	01		10.0	ns
Global Early Clock to Output using OMUX Values are for BUFGE #s 1, 2, 5 and 6. Add 1.4 ns for BUFGE #s 3, 4, 7 and 8 18/ 19/	TPEFPF					8.2	
For output SLOW option add	TSLOW					3.0	
Global Low Skew Clock, Set-Up and Hold							
Input Setup Time, using Global Low Skew clock and IFF (full delay) 15/	TPSD	See figure 3 as applicable 6/ 9/ 20/	9, 10, 11	01	6.6		ns
Input Hold Time, using Global Low Skew clock and IFF (full delay) 15/	TPHD				0		
Global Buffers Switching Characteristic Guidelines							
From pad through Global Low Skew buffer, to any clock K	TGLS	See figure 4 as applicable 4/ 5/ 21/	9, 10, 11	01		4.8	ns
From pad through Global Early buffer, to any clock K in same quadrant	TGE						

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

1/ With up to 64 pins simultaneously sinking 12 mA.

2/ With no output current loads, no active input or Longline pull-up resistors, all I/O pins tri-stated and floating.

3/ These delays are specified from the decoder input to the decoder output. Fewer than the specified number of pull up resistors can be used, if desired. Using fewer pull ups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pull ups are used.

4/ Parameter is not directly tested. Devices are first 100 percent functionally tested. Benchmark timing patterns are then used to determine the compliance of this parameter. Characterization data is taken at initial device introduction, and after any design or process changes which may affect this parameter.

5/ Benchmark patterns are used to determine compliance to this parameter.

6/ Parameter is not tested but is guaranteed by design through simulation.

7/ Maximum flip-flop toggle rate for export control purposes.

8/ Input pad setup times and hold times are specified with respect to the internal clock (IK). To calculate setup time, Subtract clock delay (clock pad to IK) from the specified input pad setup time value, but do not subtract below zero, "Negative" hold time means that the delay in the input data is adequate for the external system hold time to be zero, provided the input clock uses the global signal distribution from pad to IK.

9/ Core = TILO + TCKO

10/ These delays are specified from the decoder input to the decoder output. For pad-to-pad delays, add the input delay (TPID) output delay (TOPF or TOPS) .

11/ These values include a minimum load of one output, spaced a far as possible from the active pullup(s). Use the static timing analyzer to determine the delay for each destination.

12/ Fewer than the specified number of pullup resistors can be used, if desired. Using fewer pullups reduces the power consumption but increases delays. Use the static analyzer to determine delays if fewer pullups are used.

13/ These values are for a minimum load with the driver paced as far as possible from the active pull up(s). Fewer than the specified number of pull up resistors can be used, if desired. Using fewer pull ups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pull ups are used.

14/ FCL = Fast Capture Latch

15/ IFF = Input Flip-Flop or Latch

16/ OFF = Output Flip Flop

17/ These are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net. Output timing is measured at ~50% V_{CC} threshold with 35 pF external capacitive load.

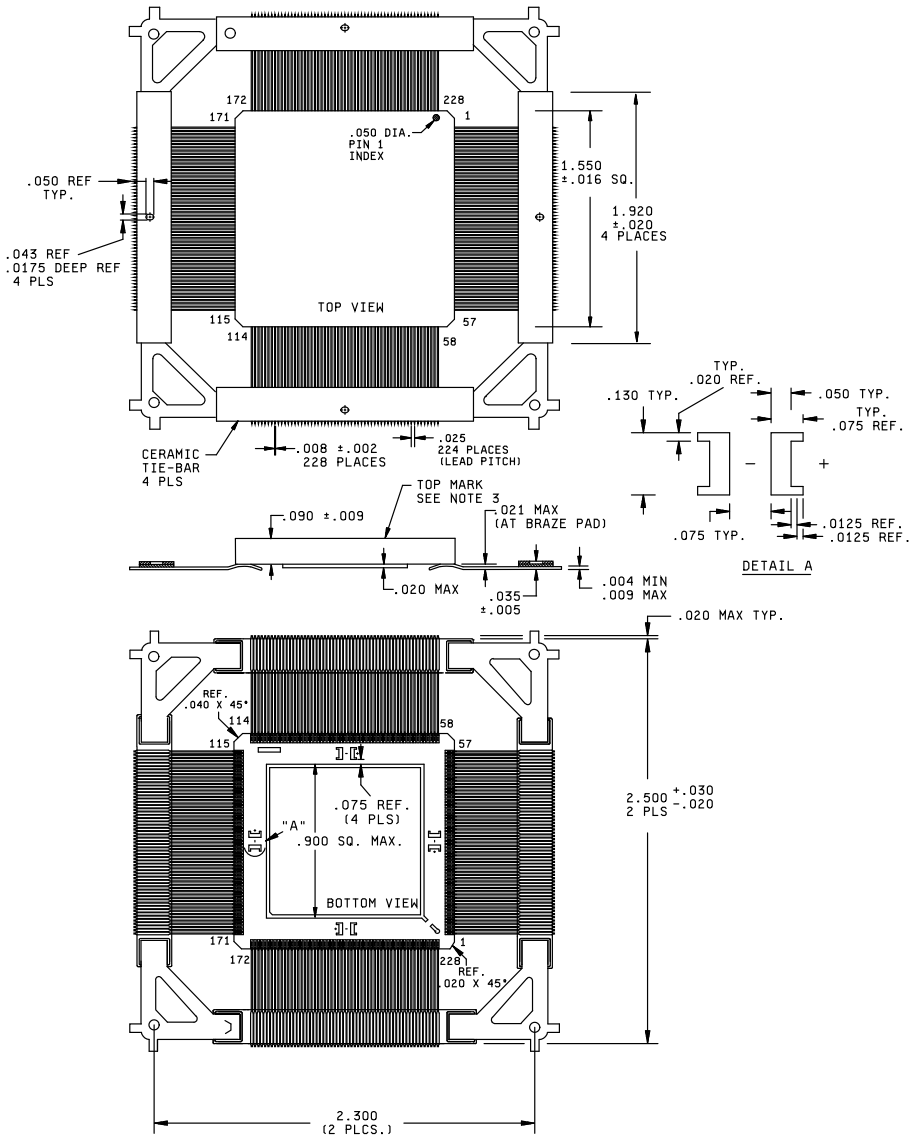
18/ BUFGE = Global Early Buffers

19/ OMUX = Output MUX

20/ Setup time is measured with the fastest route and the lightest load. Use the static timing analyzer to determine the setup time under given design conditions. Hold time is measured using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer to determine the setup and hold time under given design conditions.

21/ Parameters are for BUFGE # 1, 2, 5 and 6. Add 1.4 ns for BUFGE # 3, 4, 7 and 8.

Cases Y and Z



NOTES:

1. Dimensions are in inches.
2. Packages are shipped flat as depicted
3. Lead dimensions call out includes lead finish.
4. The leads of this package style shall be protected from mechanical distortion and damage such that dimensions pertaining to relative lead/body "true positions" and lead "coplanarity" are always maintained until the next higher level package attachment process is complete. Package lead protection mechanisms (tie bars) are shown on the drawing for reference only. When microcircuit devices contained in this package style are shipped for use in Government equipment, or shipped directly to the Government as spare parts or mechanical qualification samples, lead "true position" and "coplanarity" protection shall be in place.
5. Case Y represents marking the device on the nonlid side of device, i.e., lid side facing down. When mounted in this position, the pin out is clockwise. Case Z represents marking the device on the lid side of the device i.e., lid side facing up. When mounted in this position, the pin out is counterclockwise.

FIGURE 1. Case outline.

Inch to metric conversion table for convenience only.

Inches	Metric mm
2.500	63.50
2.300	58.42
1.920	48.77
1.550	39.37
.900	22.86
.130	3.30
.125	3.18
.090	2.29
.075	1.91
.050	1.27
.043	1.09
.040	1.02
.035	.89
.030	.76
.025	.64
.021	.53
.020	.51
.0175	.44
.016	.41
.0125	.32
.009	.23
.008	.20
.005	.13
.004	.10
.002	.05

FIGURE 1. Case outline - Continued.

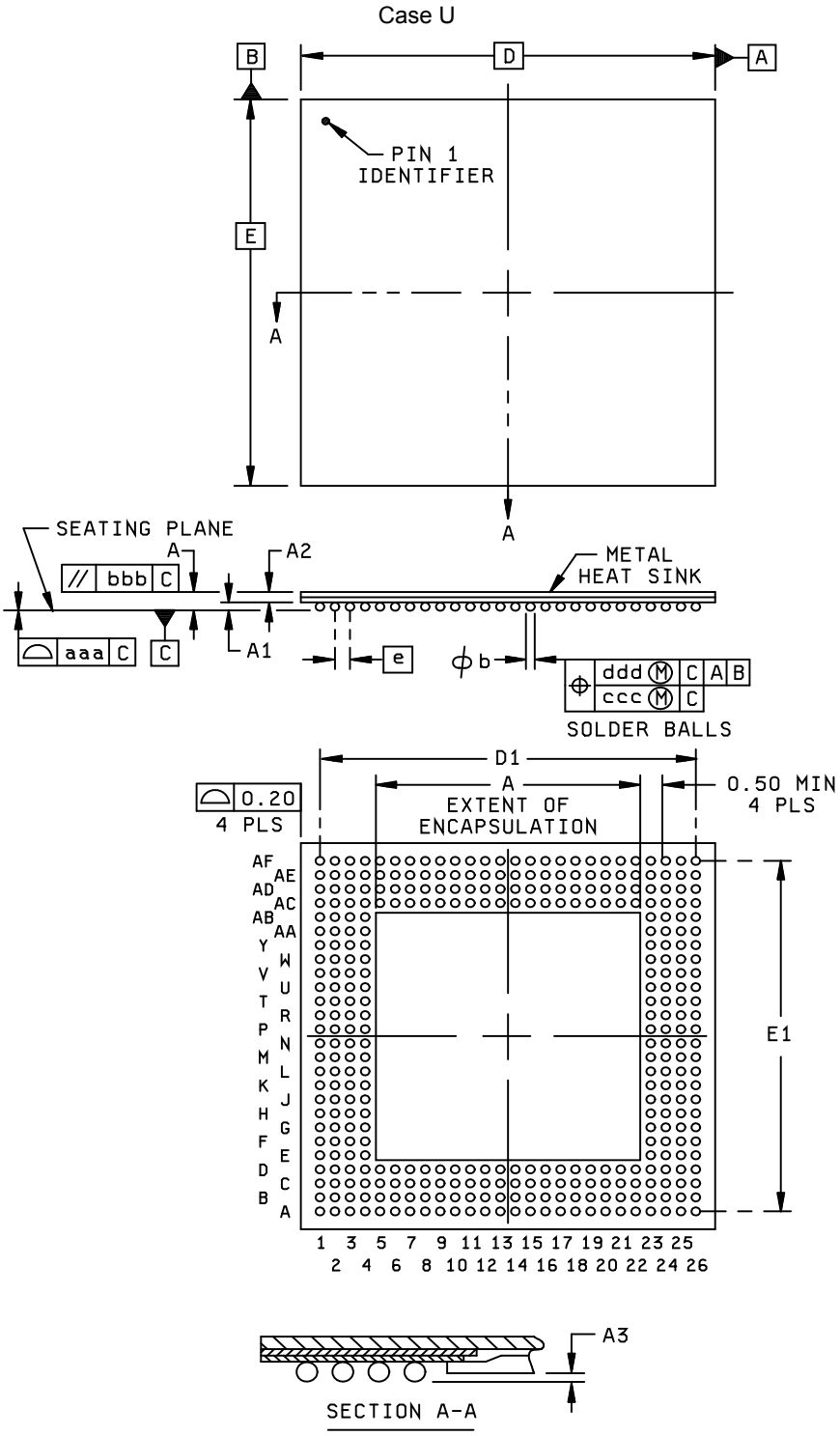


FIGURE 1. Case outline - Continued.

BG352			
Symbol	Millimeters		
	Min.	Nom.	Max.
A	1.10	1.40	1.70
A1	0.50	0.60	0.70
A2	0.60	---	1.00
A3	0.20	---	---
D/E	35.00 BSC		
D1/E1	31.75 REF		
e	1.27 BSC		
∅b	0.60	0.75	0.90
aaa	---	---	0.20
bbb	---	---	0.25
ccc	---	---	0.15
ddd	---	---	0.30
M	26		
REF	JEDEC MO-192-BAR-2		

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M-1994.
2. Symbol "M" is the pin matrix size.
3. Conforms to JEDEC MO-192 (Depopulated).

FIGURE 1. Case outline - Continued.

Device type	All	Device type	All	Device type	All
Case outline	X	Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A3	VCC	C19	I/O	E35	M0
A5	I/O	C21	I/O	E37	NC
A7	I/O	C23	NC	E39	I/O
A9	GND	C25	NC	F2	NC
A11	VCC	C27	I/O	F4	GND
A13	NC	C29	I/O_FCLK2	F6	A17_I/O
A15	I/O	C31	I/O	F8	I/O
A17	I/O	C33	NC	F10	I/O
A19	GND	C35	I/O	F12	I/O
A21	VCC	C37	HDC_I/O	F14	I/O
A23	I/O	C39	VCC	F16	I/O
A25	I/O	D2	I/O	F18	NC
A27	I/O	D4	I/O	F20	I/O
A29	GND	D6	VCC	F22	NC
A31	VCC	D8	NC	F24	I/O
A33	I/O	D10	I/O	F26	I/O
A35	I/O	D12	NC	F28	I/O
A37	GND	D14	GND	F30	I/O
A39	M1	D16	I/O	F32	I/O
B2	TDI_I/O	D18	I/O	F34	I/O
B4	I/O	D20	GND	F36	VCC
B6	NC	D22	I/O	F38	I/O
B8	I/O	D24	I/O	G1	I/O
B10	I/O	D26	GND	G3	A13_I/O
B12	I/O	D28	I/O	G5	NC
B14	I/O	D30	NC	G7	BUFGS_TL_GCK8_
B16	I/O	D32	NC		A15_I/O
B18	I/O	D34	GND	G9	TCK_I/O
B20	I/O	D36	BUFGP_BL_	G31	I/O
B22	I/O		GCK3_I/O	G33	M2
B24	I/O	D38	I/O	G35	LDC_I/O
B26	I/O	E1	I/O	G37	I/O
B28	I/O	E3	I/O	G39	I/O
B30	I/O	E5	A14_I/O	H2	I/O
B32	I/O	E7	NC	H4	A12_I/O
B34	NC	E9	I/O	H6	I/O
B36	BUFGS_BL_	E11	TMS_I/O	H8	BUFGP_TL_A16_
	GCK2_I/O	E13	I/O		GCK1_I/O
B38	I/O	E15	I/O	H32	I/O
C1	GND	E17	I/O	H34	NC
C3	I/O	E19	I/O	H36	I/O
C5	I/O	E21	I/O	H38	I/O
C7	NC	E23	NC	J1	VCC
C9	I/O	E25	I/O	J3	I/O
C11	I/O_FCLK1	E27	I/O	J5	NC
C13	I/O	E29	I/O	J7	I/O
C15	NC	E31	I/O	J33	I/O
C17	I/O	E33	I/O	J35	I/O
				J37	I/O
				J39	GND

FIGURE 2. Terminal connections.

Device type	All	Device type	All	Device type	All
Case outline	X	Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
K2	I/O	V2	NC	AF2	NC
K4	I/O	V4	A19_I/O	AF4	GND
K6	I/O	V6	I/O	AF6	I/O
K34	I/O	V34	I/O	AF34	I/O
K36	NC	V36	I/O	AF36	GND
K38	NC	V38	I/O	AF38	NC
L1	GND	W1	VCC	AG1	I/O
L3	I/O	W3	A8_I/O	AG3	I/O
L5	NC	W5	NC	AG5	I/O
L35	NC	W35	NC	AG35	I/O
L37	I/O	W37	$\overline{\text{INIT}}$ _I/O	AG37	I/O
L39	VCC	W39	GND	AG39	I/O
M2	I/O	Y2	A9_I/O	AH2	I/O
M4	I/O	Y4	GND	AH4	I/O
M6	I/O	Y6	A7_I/O	AH6	I/O
M34	I/O	Y34	I/O	AH34	I/O
M36	I/O	Y36	GND	AH36	I/O
M38	I/O	Y38	NC	AH38	I/O
N1	I/O	AA1	GND	AJ1	VCC
N3	NC	AA3	A6_I/O	AJ3	I/O
N5	I/O	AA5	A20_I/O	AJ5	NC
N35	I/O	AA35	I/O	AJ35	I/O
N37	I/O	AA37	NC	AJ37	I/O
N39	I/O	AA39	VCC	AJ39	GND
P2	I/O	AB2	NC	AK2	NC
P4	GND	AB4	A5_I/O	AK4	I/O
P6	I/O	AB6	I/O	AK6	CSI_A2_I/O
P34	I/O	AB34	I/O	AK34	I/O
P36	GND	AB36	I/O	AK36	I/O
P38	NC	AB38	I/O	AK38	NC
R1	A11_I/O	AC1	I/O	AL1	GND
R3	NC	AC3	NC	AL3	I/O
R5	I/O	AC5	I/O	AL5	I/O
R35	I/O	AC35	I/O	AL7	I/O
R37	I/O	AC37	I/O	AL33	I/O
R39	I/O	AC39	NC	AL35	NC
T2	A18_I/O	AD2	A4_I/O	AL37	I/O
T4	I/O	AD4	A21_I/O	AL39	VCC
T6	I/O	AD6	I/O	AM2	I/O
T34	I/O	AD34	I/O	AM4	I/O
T36	I/O	AD36	I/O	AM6	I/O
T38	I/O	AD38	I/O	AM8	I/O
U1	I/O	AE1	I/O	AM32	D7_I/O
U3	A10_I/O	AE3	I/O	AM34	I/O
U5	I/O	AE5	I/O	AM36	I/O
U35	I/O	AE35	I/O	AM38	I/O
U37	I/O	AE37	I/O		
U39	I/O	AE39	I/O		

FIGURE 2. Terminal connections - Continued.

Device type	All	Device type	All	Device type	All
Case outline	X	Case outline	X	Case outline	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
AN1	NC	AR27	I/O	AU33	I/O
AN3	A3_I/O	AR29	I/O	AU35	I/O
AN5	NC	AR31	I/O	AU37	NC
AN7	TDO	AR33	I/O	AU39	GND
AN9	I/O	AR35	DONE	AV2	BUFGP_TR_ GCK7_A1_I/O
AN31	I/O	AR37	NC		
AN33	$\overline{\text{PROG}}$	AR39	I/O	AV4	I/O
AN35	I/O	AT2	NC	AV6	I/O
AN37	I/O	AT4	A0_$\overline{\text{WS}}$_I/O	AV8	NC
AN39	I/O	AT6	GND	AV10	I/O
AP2	I/O	AT8	I/O	AV12	I/O
AP4	VCC	AT10	I/O	AV14	I/O
AP6	DO_DIN_I/O	AT12	I/O	AV16	I/O
AP8	NC	AT14	GND	AV18	I/O
AP10	I/O	AT16	I/O	AV20	$\overline{\text{RS}}$_I/O
AP12	I/O	AT18	I/O	AV22	I/O
AP14	I/O	AT20	GND	AV24	I/O
AP16	I/O	AT22	I/O	AV26	NC
AP18	I/O	AT24	I/O	AV28	I/O
AP20	D4_I/O	AT26	GND	AV30	I/O
AP22	I/O	AT28	I/O_FCLK3	AV32	D6_I/O
AP24	D5_I/O	AT30	NC	AV34	NC
AP26	I/O	AT32	I/O	AV36	I/O
AP28	I/O	AT34	VCC	AV38	I/O
AP30	NC	AT36	BUFGS_BR_ GCK4_I/O	AW1	I/O
AP32	I/O	AT38	I/O	AW3	I/O
AP34	BUFGP_BR_ GCK5_I/O	AU1	VCC	AW5	GND
AP36	GND	AU3	BUFGS_TR_ GCK6_DOUT_I/O	AW7	I/O
AP38	NC	AU5	NC	AW9	$\overline{\text{RDY}}$_$\overline{\text{BUSY}}$_ $\overline{\text{RCLK}}$_I/O
AR1	I/O	AU7	D1_I/O	AW11	VCC
AR3	I/O	AU9	NC	AW13	GND
AR5	CCLK	AU11	I/O	AW15	I/O
AR7	I/O	AU13	NC	AW17	NC
AR9	I/O	AU15	NC	AW19	I/O
AR11	I/O	AU17	NC	AW21	VCC
AR13	I/O_FCLK4	AU19	D3_I/O	AW23	GND
AR15	D2_I/O	AU21	I/O	AW25	NC
AR17	I/O	AU23	I/O	AW27	NC
AR19	I/O	AU25	NC	AW29	I/O
AR21	I/O	AU27	$\overline{\text{CS0}}$_I/O	AW31	VCC
AR23	I/O	AU29	I/O	AW33	GND
AR25	I/O	AU31	I/O	AW35	I/O
				AW37	NC
				AW39	VCC
					I/O

FIGURE 2. Terminal connections - Continued.

Case outlines Y and Z

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
1	VSS		51	I/O		101	I/O
2	BUFGP_TL_A16_GCK1_I/O		52	I/O		102	I/O
3	A17_I/O		53	I/O		103	I/O
4	I/O		54	BUFGS_BL_GCK2_I/O		104	I/O
5	I/O		55	M1		105	I/O
6	TDI_I/O		56	VSS		106	I/O
7	TCK_I/O		57	M0		107	I/O
8	I/O		58	VCC		108	I/O
9	I/O		59	M2		109	I/O
10	I/O		60	BUFGP_BL_GCK3_I/O		110	I/O
11	I/O		61	HDC_I/O		111	I/O
12	I/O		62	I/O		112	BUFGS_BR_GCK4_I/O
13	I/O		63	I/O		113	VSS
14	VSS		64	I/O		114	DONE
15	I/O_FCLK1		65	$\overline{\text{LDC}}$ _I/O		115	VCC
16	I/O		66	I/O		116	$\overline{\text{PROG}}$
17	TMS_I/O		67	I/O		117	D7_I/O
18	I/O		68	I/O		118	BUFGP_BR_GCK5_I/O
19	I/O		69	I/O		119	I/O
20	I/O		70	I/O		120	I/O
21	I/O		71	I/O		121	I/O
22	I/O		72	VSS		122	I/O
23	I/O		73	I/O		123	D6_I/O
24	I/O		74	I/O		124	I/O
25	I/O		75	I/O		125	I/O
26	I/O		76	I/O		126	I/O
27	VSS		77	I/O		127	I/O
28	VCC		78	I/O		128	I/O
29	I/O		79	I/O		129	VSS
30	I/O		80	I/O		130	I/O
31	I/O		81	I/O		131	I/O
32	I/O		82	I/O		132	I/O_FCLK3
33	I/O		83	I/O		133	I/O
34	I/O		84	$\overline{\text{INIT}}$ _I/O		134	D5_I/O
35	I/O		85	VCC		135	$\overline{\text{CS0}}$ _I/O
36	I/O		86	VSS		136	I/O
37	VCC		87	I/O		137	I/O
38	I/O		88	I/O		138	I/O
39	I/O		89	I/O		139	I/O
40	I/O		90	I/O		140	D4_I/O
41	I/O_FCLK2		91	I/O		141	I/O
42	VSS		92	I/O		142	VCC
43	I/O		93	I/O		143	VSS
44	I/O		94	I/O		144	D3_I/O
45	I/O		95	VCC		145	$\overline{\text{RS}}$ _I/O
46	I/O		96	I/O		146	I/O
47	I/O		97	IO		147	I/O
48	I/O		98	I/O		148	I/O
49	I/O		99	I/O		149	I/O
50	I/O		100	VSS		150	D2_I/O

FIGURE 2. Terminal connections - Continued.

Device type	All		Device type	All		Device type	All
Terminal number	Terminal symbol		Terminal number	Terminal symbol		Terminal number	Terminal symbol
151	I/O		177	I/O		203	A9_I/O
152	VCC		178	CSI_A2_I/O		204	A19_I/O
153	I/O		179	A3_I/O		205	A18_I/O
154	I/O_FCLK4		180	I/O		206	I/O
155	I/O		181	I/O		207	I/O
156	I/O		182	I/O		208	A10_I/O
157	VSS		183	I/O		209	A11_I/O
158	I/O		184	I/O		210	VCC
159	I/O		185	I/O		211	I/O
160	I/O		186	VSS		212	I/O
161	I/O		187	I/O		213	I/O
162	I/O		188	I/O		214	I/O
163	I/O		189	I/O		215	VSS
164	D1_I/O		190	I/O		216	I/O
165	RDY_$\overline{\text{BUSY}}$_$\overline{\text{RCLK}}$_I/O		191	VCC		217	I/O
166	I/O		192	A4_I/O		218	I/O
167	I/O		193	A5_I/O		219	I/O
168	D0_DIN_I/O		194	I/O		220	A12_I/O
169	BUFGS_TR_GCK6_DOUT_I/O		195	I/O		221	A13_I/O
170	CCLK		196	A21_I/O		222	I/O
171	VCC		197	A20_I/O		223	I/O
172	TDO		198	A6_I/O		224	I/O
173	VSS		199	A7_I/O		225	I/O
174	A0_/WS_I/O		200	VSS		226	A14_I/O
175	BUFGP_TR_GCK7_A1_I/O		201	VCC		227	BUFGS_TL_GCK8_A15_I/O
176	I/O		202	A8_I/O		228	VCC

FIGURE 2. Terminal connections - Continued.

Device type	All	Device type	All	Device type	All
Case outline	U	Case outline	U	Case outline	U
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	GND	C4	BUFGP_TR_GCK7_A1_I/O	E4	BUFGS_TR_GCK6_DOUT_I/O
A2	GND				
A3	I/O	C5	I/O	E23	I/O
A4	I/O	C6	A3_I/O	E24	TCK_I/O
A5	GND	C7	I/O	E25	I/O
A6	I/O	C8	NC	E26	GND
A7	I/O	C9	I/O	F1	I/O
A8	GND	C10	I/O	F2	I/O
A9	I/O	C11	I/O	F3	D1_I/O
A10	VCC	C12	A5_I/O	F4	I/O
A11	I/O	C13	A21_I/O	F23	I/O
A12	I/O	C14	A9_I/O	F24	I/O
A13	A6_I/O	C15	I/O	F25	I/O
A14	GND	C16	I/O	F26	I/O
A15	A19_I/O	C17	I/O	G1	I/O
A16	A10_I/O	C18	I/O	G2	I/O
A17	VCC	C19	I/O	G3	I/O
A18	I/O	C20	I/O	G4	$\overline{RDY}_\overline{BUSY}_\overline{RCLK}$_I/O
A19	GND	C21	A13_I/O		
A20	I/O	C22	I/O		
A21	I/O	C23	I/O	G23	VCC
A22	GND	C24	BUFGS_TL_GCK8_A15_I/O	G24	I/O
A23	I/O			G25	I/O
A24	I/O	C25	A17_I/O	G26	I/O
A25	GND	C26	TDI_I/O	H1	GND
A26	GND	D1	I/O	H2	I/O
B1	GND	D2	I/O	H3	I/O
B2	VCC	D3	D0_DIN_I/O	H4	VCC
B3	A0_$\overline{WS}$_I/O	D4	TDO	H23	I/O
B4	I/O	D5	I/O	H24	I/O
B5	I/O	D6	CSI_A2_I/O	H25	TMS_I/O
B6	I/O	D7	VCC	H26	GND
B7	I/O	D8	I/O	J1	D2_I/O
B8	I/O	D9	I/O	J2	I/O
B9	I/O	D10	I/O	J3	I/O_FCLK4
B10	I/O	D11	I/O	J4	I/O
B11	I/O	D12	A4_I/O	J23	I/O_FCLK1
B12	I/O	D13	VCC	J24	I/O
B13	A20_I/O	D14	A8_I/O	J25	I/O
B14	A7_I/O	D15	I/O	J26	I/O
B15	A18_I/O	D16	I/O	K1	VCC
B16	A11_I/O	D17	I/O	K2	I/O
B17	I/O	D18	I/O	K3	I/O
B18	I/O	D19	VCC	K4	I/O
B19	I/O	D20	I/O	K23	I/O
B20	I/O	D21	I/O	K24	I/O
B21	I/O	D22	A14_I/O	K25	I/O
B22	A12_I/O	D23	BUFGP_TL_A16_GCK1_I/O	K26	VCC
B23	I/O			L1	I/O
B24	I/O	D24	I/O	L2	I/O
B25	VCC	D25	I/O	L3	I/O
B26	GND	D26	I/O	L4	I/O
C1	I/O	E1	GND	L23	I/O
C2	I/O	E2	I/O	L24	I/O
C3	CCLK	E3	I/O	L25	I/O
				L26	I/O

FIGURE 2. Terminal connections - Continued.

Device type	All	Device type	All	Device type	All
Case outline	U	Case outline	U	Case outline	U
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
M1	I/O	W1	GND	AC24	BUFGS_BL_GCK2_I/O
M2	I/O	W2	I/O		
M3	I/O	W3	I/O	AC25	I/O
M4	I/O	W4	I/O	AC26	I/O
M23	I/O	W23	VCC	AD1	I/O
M24	I/O	W24	I/O	AD2	D7_I/O
M25	I/O	W25	I/O	AD3	DONE
M26	I/O	W26	GND	AD4	I/O
N1	GND	Y1	I/O	AD5	I/O
N2	D3_I/O	Y2	I/O	AD6	I/O
N3	I/O	Y3	D6_I/O	AD7	I/O
N4	$\overline{RS}$_I/O	Y4	VCC	AD8	I/O
N23	VCC	Y23	I/O	AD9	I/O
N24	I/O	Y24	I/O	AD10	I/O
N25	I/O	Y25	I/O	AD11	I/O
N26	I/O	Y26	I/O	AD12	I/O
P1	I/O	AA1	I/O	AD13	I/O
P2	D4_I/O	AA2	I/O	AD14	I/O
P3	I/O	AA3	I/O	AD15	I/O
P4	VCC	AA4	I/O	AD16	I/O
P23	I/O	AA23	I/O	AD17	I/O
P24	I/O	AA24	I/O	AD18	I/O
P25	I/O	AA25	I/O	AD19	I/O
P26	GND	AA26	I/O	AD20	I/O
R1	I/O	AB1	GND	AD21	I/O
R2	I/O	AB2	I/O	AD22	I/O
R3	I/O	AB3	I/O	AD23	HDC_I/O
R4	I/O	AB4	I/O	AD24	M0
R23	I/O	AB23	M1	AD25	I/O
R24	I/O	AB24	I/O	AD26	I/O
R25	I/O	AB25	I/O	AE1	GND
R26	I/O	AB26	GND	AE2	VCC
T1	I/O	AC1	I/O	AE3	I/O
T2	I/O	AC2	I/O	AE4	I/O
T3	I/O	AC3	BUFGP_BR_GCK5_I/O	AE5	I/O
T4	I/O			AE6	I/O
T23	I/O	AC4	$\overline{PROG}$	AE7	I/O
T24	I/O	AC5	BUFGS_BR_GCK4_I/O	AE8	I/O
T25	I/O			AE9	I/O
T26	I/O	AC6	I/O	AE10	I/O
U1	VCC	AC7	I/O	AE11	I/O
U2	I/O	AC8	VCC	AE12	I/O
U3	I/O	AC9	I/O	AE13	I/O
U4	I/O_FCLK3	AC10	I/O	AE14	I/O
U23	I/O_FCLK2	AC11	I/O	AE15	I/O
U24	I/O	AC12	I/O	AE16	I/O
U25	I/O	AC13	I/O	AE17	I/O
U26	VCC	AC14	VCC	AE18	I/O
V1	$\overline{CS0}$_I/O	AC15	I/O	AE19	I/O
V2	D5_I/O	AC16	I/O	AE20	I/O
V3	I/O	AC17	I/O	AE21	I/O
V4	I/O	AC18	I/O	AE22	I/O
V23	I/O	AC19	I/O	AE23	$\overline{LDC}$_I/O
V24	I/O	AC20	VCC	AE24	BUFGP_BL_GCK3_I/O
V25	I/O	AC21	I/O		
V26	I/O	AC22	I/O	AE25	VCC
		AC23	M2	AE26	GND

FIGURE 2. Terminal connections - Continued.

Device type	All	Device type	All	Device type	All
Case outline	U	Case outline	U	Case outline	U
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
AF1	GND	AF10	VCC	AF18	I/O
AF2	GND	AF11	I/O	AF19	GND
AF3	I/O	AF12	I/O	AF20	I/O
AF4	I/O	AF13	GND	AF21	I/O
AF5	GND	AF14	$\overline{\text{INIT}}$_I/O	AF22	GND
AF6	I/O	AF15	I/O	AF23	I/O
AF7	I/O	AF16	I/O	AF24	I/O
AF8	GND	AF17	VCC	AF25	GND
AF9	I/O			AF26	GND

THE END OF CASE (U) IS ABOVE - THE START OF CASE (T) IS BELOW

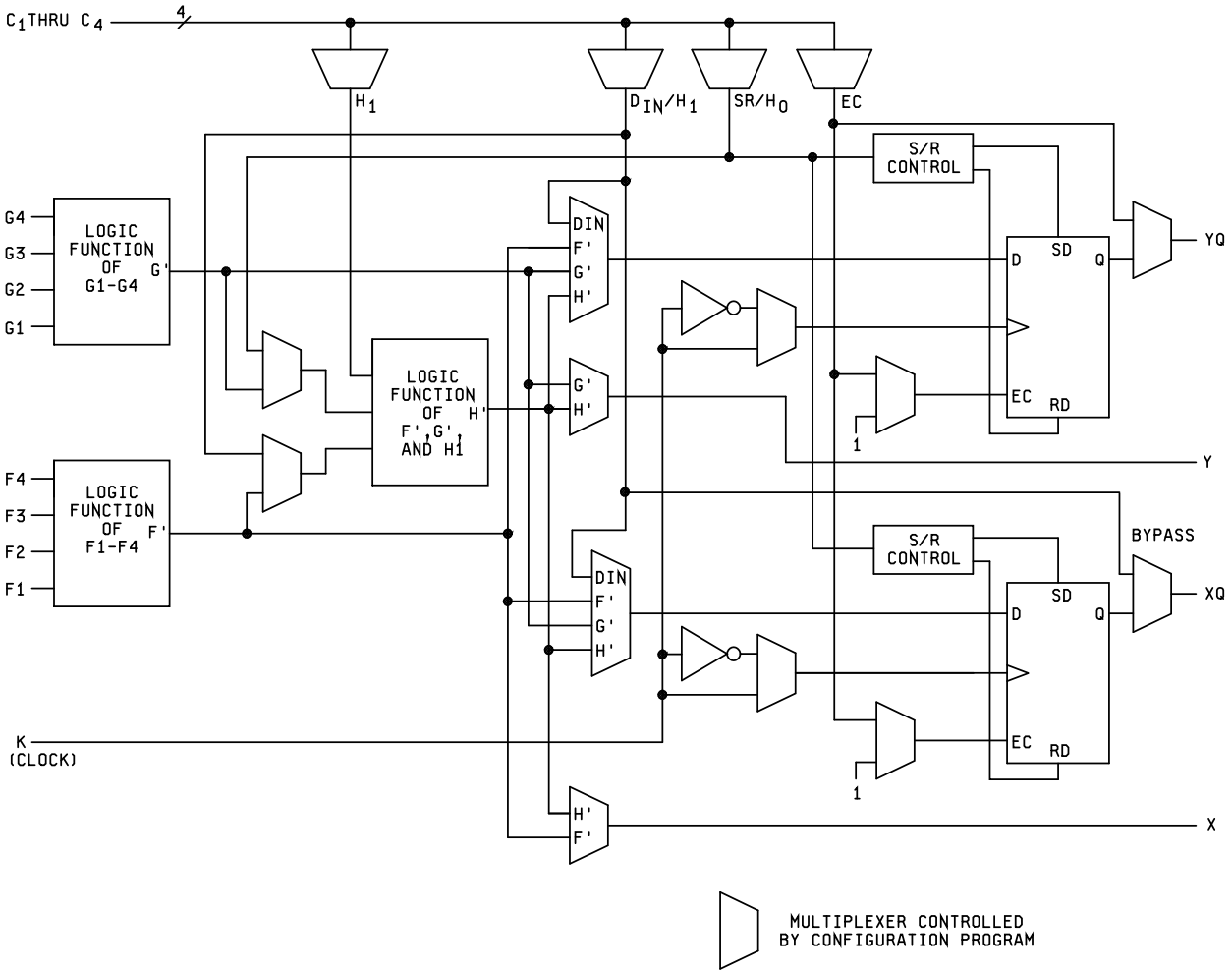
Device type	All	Device type	All	Device type	All
Case outline	T	Case outline	T	Case outline	T
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
P1	VSS	P36	I/O	P70	I/O
P2	BUFGP_TL_A16_$\overline{\text{GCK1}}$_I/O	P37	VSS	P71	I/O
		P38	I/O	P72	I/O
P3	A17_I/O	P39	I/O	P73	I/O
P4	I/O	P40	VCC	P74	I/O
P5	I/O	P41	I/O	P75	VSS
P6	TDI_I/O	P42	I/O	P76	I/O
P7	TCK_I/O	P43	I/O	P77	I/O
P8	I/O	P44	I/O_FCLK2	P78	I/O
P9	I/O	P45	VSS	P79	I/O
P10	I/O	P46	I/O	P80	VCC
P11	I/O	P47	I/O	P81	I/O
P12	I/O	P48	I/O	P82	I/O
P13	I/O	P49	I/O	P83	VSS
P14	VSS	P50	I/O	P84	I/O
P15	I/O_FCLK1	P51	I/O	P85	I/O
P16	I/O	P52	I/O	P86	I/O
P17	TMS_I/O	P53	I/O	P87	I/O
P18	I/O	P54	I/O	P88	I/O
P19	VCC	P55	I/O	P89	$\overline{\text{INIT}}$_I/O
P20	I/O	P56	I/O	P90	VCC
P21	I/O	P57	BUFGS_BL_GCK2_I/O	P91	VSS
P22	VSS			P92	I/O
P23	I/O	P58	M1	P93	I/O
P24	I/O	P59	VSS	P94	I/O
P25	I/O	P60	M0	P95	I/O
P26	I/O	P61	VCC	P96	I/O
P27	I/O	P62	M2	P97	I/O
P28	I/O	P63	BUFGP_BL_GCK3_I/O	P98	VSS
P29	VSS			P99	I/O
P30	VCC	P64	HDC_I/O	P100	I/O
P31	I/O	P65	I/O	P101	VCC
P32	I/O	P66	I/O	P102	I/O
P33	I/O	P67	I/O	P103	I/O
P34	I/O	P68	$\overline{\text{LDC}}$_I/O	P104	I/O
P35	I/O	P69	I/O	P105	I/O

FIGURE 2. Terminal connections - Continued.

Device type	All	Device type	All	Device type	All
Case outline	T	Case outline	T	Case outline	T
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
P106	VSS	P151	VSS	P195	I/O
P107	I/O	P152	D3_I/O	P196	VSS
P108	I/O	P153	$\overline{RS}$ _I/O	P197	I/O
P109	I/O	P154	I/O	P198	I/O
P110	I/O	P155	I/O	P199	I/O
P111	I/O	P156	I/O	P200	I/O
P112	I/O	P157	I/O	P201	VCC
P113	I/O	P158	VSS	P202	A4_I/O
P114	I/O	P159	D2_I/O	P203	A5_I/O
P115	I/O	P160	I/O	P204	GND
P116	I/O	P161	VCC	P205	I/O
P117	I/O	P162	I/O	P206	I/O
P118	BUFGS_BR_GCK4_I/O	P163	I/O_FCLK4	P207	A21_I/O
P119	VSS	P164	I/O	P208	A20_I/O
P120	DONE	P165	I/O	P209	A6_I/O
P121	VCC	P166	VSS	P210	A7_I/O
P122	$\overline{PROG}$	P167	I/O	P211	VSS
P123	D7_I/O	P168	I/O	P212	VCC
P124	BUFGP_BR_GCK5_I/O	P169	I/O	P213	A8_I/O
P125	I/O	P170	I/O	P214	A9_I/O
P126	I/O	P171	I/O	P215	A19_I/O
P127	I/O	P172	I/O	P216	A18_I/O
P128	I/O	P173	D1_I/O	P217	I/O
P129	D6_I/O	P174	$\overline{RDY}$_$\overline{BUSY}$_$\overline{RCLK}$_I/O	P218	I/O
P130	I/O	P175	I/O	P219	GND
P131	I/O	P176	I/O	P220	A10_I/O
P132	I/O	P177	D0_DIN_I/O	P221	A11_I/O
P133	I/O	P178	BUFGS_TR_GCK6_DOUT_I/O	P222	VCC
P134	I/O	P179	CCLK	P223	I/O
P135	VSS	P180	VCC	P224	I/O
P136	I/O	P181	TDO	P225	I/O
P137	I/O	P182	VSS	P226	I/O
P138	I/O_FCLK3	P183	$\overline{A0}$_$\overline{WS}$_I/O	P227	VSS
P139	I/O	P184	BUFGP_TR_GCK7_A1_I/O	P228	I/O
P140	VCC	P185	I/O	P229	I/O
P141	D5_I/O	P186	I/O	P230	I/O
P142	$\overline{CS0}$_I/O	P187	CSI_A2_I/O	P231	I/O
P143	VSS	P188	A3_I/O	P232	A12_I/O
P144	I/O	P189	I/O	P233	A13_I/O
P145	I/O	P190	I/O	P234	I/O
P146	I/O	P191	I/O	P235	I/O
P147	I/O	P192	I/O	P236	I/O
P148	D4_I/O	P193	I/O	P237	I/O
P149	I/O	P194	I/O	P238	A14_I/O
P150	VCC			P239	BUFGS_TL_GCK8_A15_I/O
				P240	VCC

FIGURE 2. Terminal connections - Continued.

Simplified block diagram of CLB



Note: The CLB storage elements can also be configured as latches. The two latches have common clock (CK) and clock enable (EC) inputs. (RAM and Carry logic functions not shown)

FIGURE 3. Logic block diagrams.

Fast Carry Logic

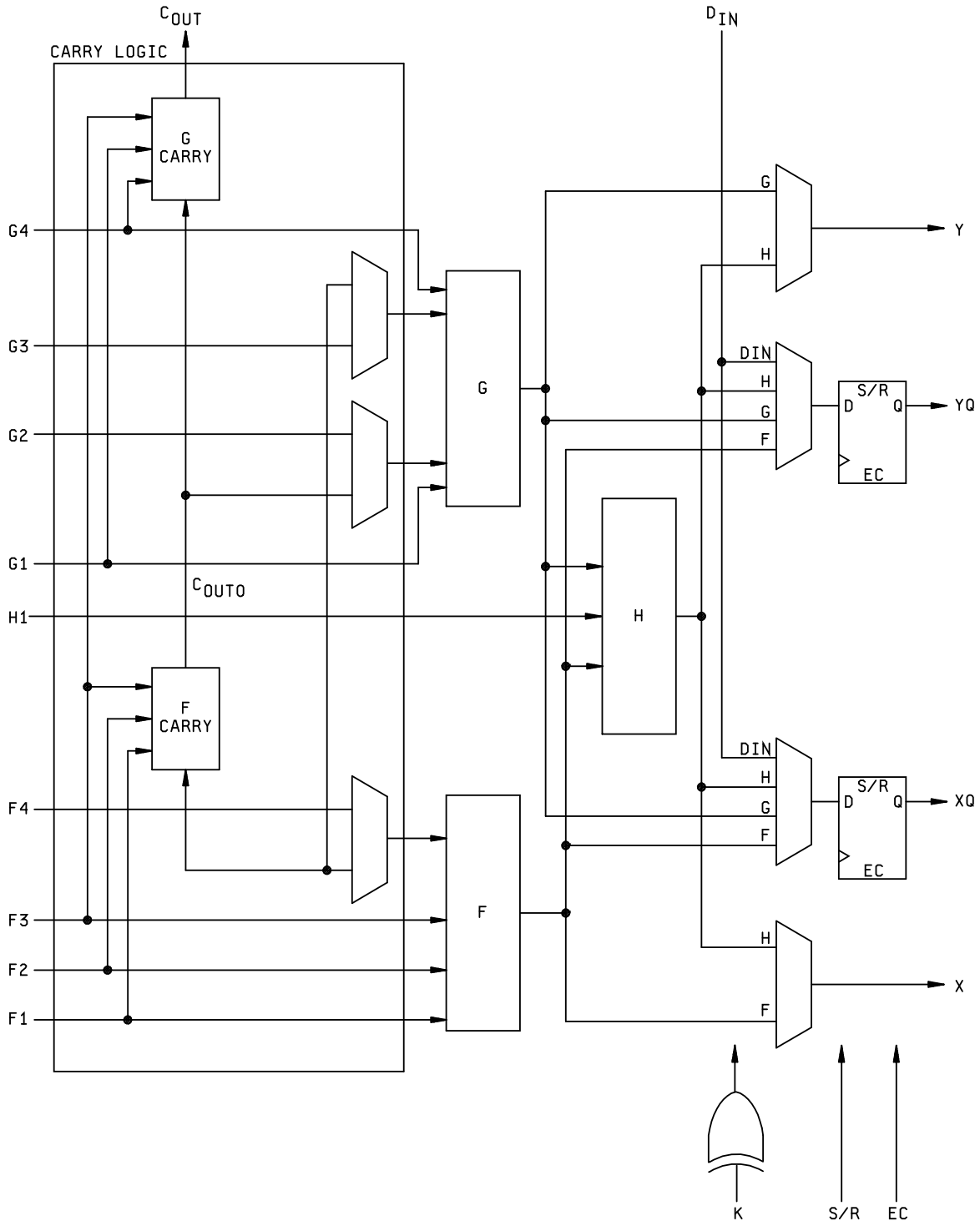


FIGURE 3. Logic block diagrams - Continued.

Simplified block diagram of IOB

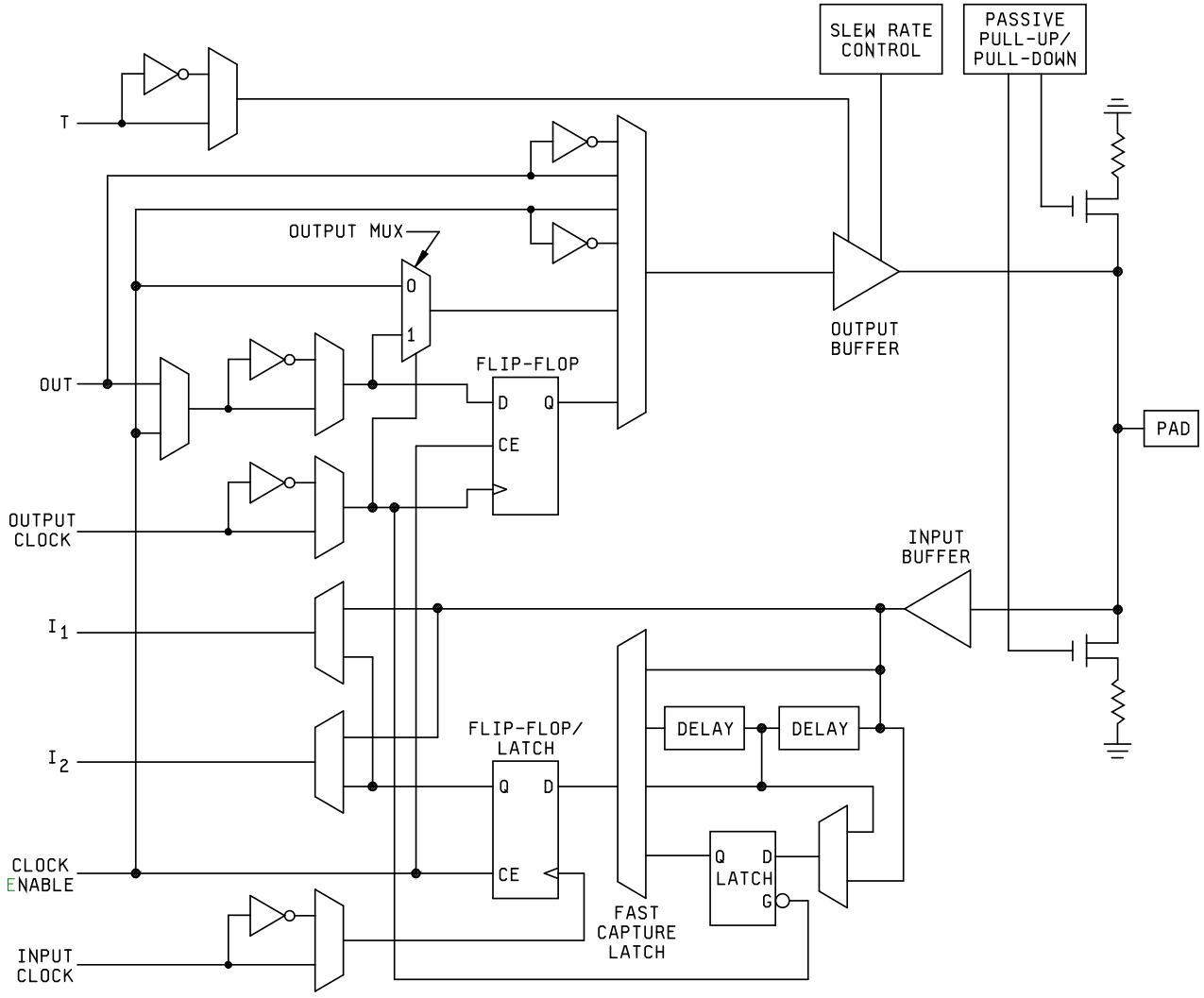
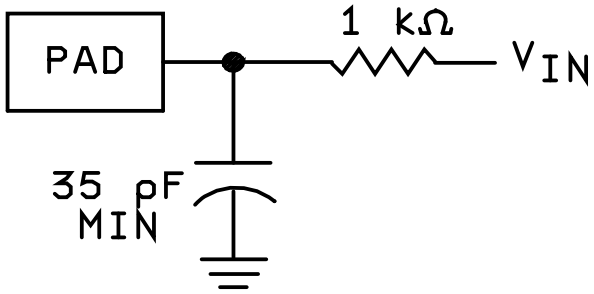
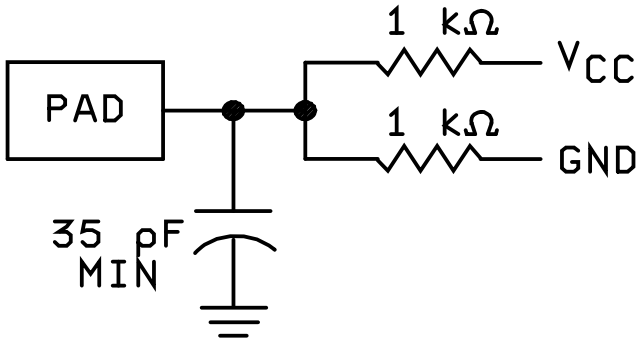


FIGURE 3. Logic block diagrams.



CIRCUIT A



CIRCUIT B

FIGURE 4. Load circuits.

4. VERIFICATION

4.1 Sampling and inspection. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device classes N, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with method 5012 of MIL-STD-883 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device classes N, Q, and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

(1) The following shall apply to device class N only. Sample size is five devices with no failures. For C_{IN} and C_{OUT}, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types that by design, will yield the same capacitance values when tested in accordance with table I herein. The device manufacturer shall set a functional group limit for the C_{IN} and C_{OUT} tests. The device manufacturer may then test one device function from a functional group to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I herein. The device manufacturer shall submit to DLA Land and Maritime-VA the device functions listed in each functional group and the test results for each device tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. The devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

TABLE II. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line No.	Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)		
		Device class N	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1, 7, 9
2	Static burn-in I and II (method 1015)	Not Required	Required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Not Required	Not Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters	2, 8A, 10	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test parameters	2, 8A, 10	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters		2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters		1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB Delta limits at +25

Parameter 1/	Device types
	All
ICCO standby	± 1 mA of specified limit in table I.
IL	± 1 µA of specified limit in table I.

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging for device classes N, Q, and V shall be in accordance with MIL-PRF-38535.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

V_{CC}	SUPPLY VOLTAGE.
GND	GROUND
CCLK	CONFIGURATION CLOCK
DONE	DONE
PROGRAM	PROGRAM
RCLK	READ CLOCK.
M0	MODE 0
M1	MODE 1
M2	MODE 2
TDO	TEST DATA OUTPUT
TDI	TEST DATA IN
TCK	TEST CLOCK
TMS	TEST MODE SELECT
HDC	HIGH DURING CONFIGURATION
LDC	LOW DURING CONFIGURATION
RTRIG	READ TRIGGER.
INIT	INIT
GCK1-GCK8	GLOBALLow-Skew buffer
CSO	CHIP SELECT, WRITE
CS1	CHIP SELECT, WRITE
WS	WRITE STROBE
RS	READ STROBE
A0-A21	ADDRESS
D0-D7	DATA
DIN	DATA INPUT
DOUT	DATA OUTPUT
I/O	INPUT/OUTPUT
RDY/BUSY	During peripheral parallel mode configuration, this pin indicates when the chip is ready for another byte of data to be written into it. After configuration is complete, this pin becomes a user programmed I/O pin.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.6 Sources of supply. Sources of supply for device classes N, Q, and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional operating data.

a. Power on delay is 2^{14} cycles from the non-master mode. This provides 11 to 33 ms of wait time.

b. Power on delay is 2^{16} cycles for the master mode. This provides 43 to 130 ms of wait time.

c. Clear is 375 cycles ±25 cycles and may take as long as 250 to 750 µs.

d. During normal power up, V_{CC} must rise from 2.0 V to V_{CC} minimum in less than 10 ms. If this does not occur, configuration must be delayed by using RESET.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-05-16

Approved sources of supply for SMD 5962-98510 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9851001QXC	3/	XQ4036XL-3BPG411
5962-9851001QYC	3/	XQ4036XL-3BCB228
5962-9851001QZC	3/	XQ4036XL-3BCB228
5962-9851001NUA	3/	XQ4036XL-3NBG352
5962-9851001NTB	3/	XQ4036XL-3NHQ240

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply. Last source of supply is listed below.

Vendor CAGE number	Vendor name and address
68994	Xilinx, Incorporated 2100 Logic Drive San Jose, CA 95124