1K X25010 128 x 8 Bit

SPI Serial E²PROM

FEATURES

- 1MHz Clock Rate
- 128 X 8 Bits
  - —4 Byte Page Mode
- Low Power CMOS
  - —150µA Standby Current
  - —3mA Active Write Current
- 3V To 5.5V Power Supply
- Block Write Protection
  - —Protect 1/4, 1/2 or all of E²PROM Array
- Built-in Inadvertent Write Protection
  - —Power-Up/Power-Down Protection Circuitry
  - —Write Latch
  - —Write Protect Pin
- Self-Timed Write Cycle
  - —5mS Write Cycle Time (Typical)
- High Reliability
  - —Endurance: 100,000 Cycles per byte
  - —Data Retention: 100 Years
  - —ESD Protection: 2000V on all Pins
- 8-Pin Mini-DIP Package
- 8-Pin SOIC Package

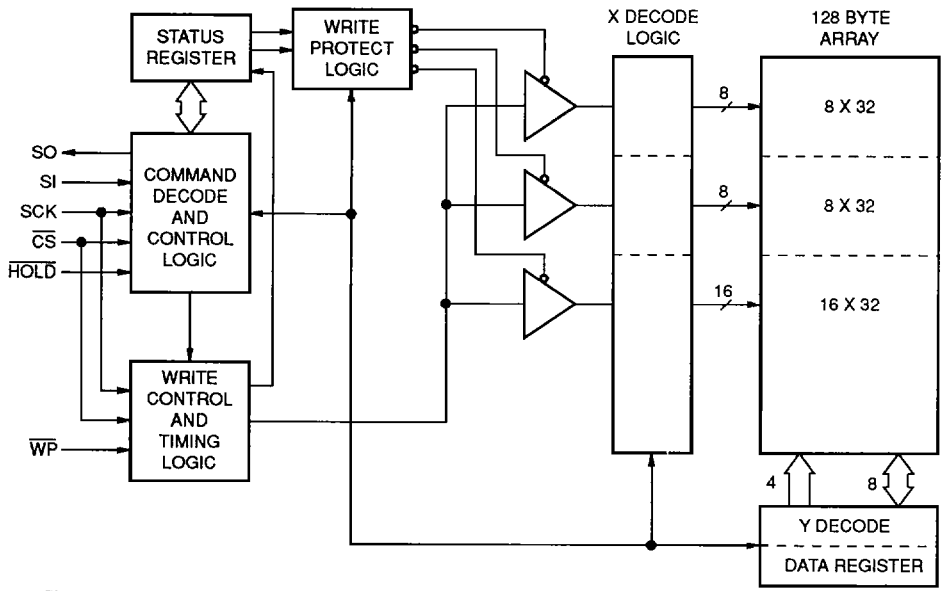
DESCRIPTION

The X25010 is a CMOS 1024 bit serial E²PROM, internally organized as 128 x 8. The X25010 features a serial interface and software protocol allowing operation on a simple three wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

The X25010 also features two additional inputs that provide the end user with added flexibility. By asserting the $\overline{HOLD}$ input, the X25010 will ignore transitions on its inputs, thus allowing the host to service higher priority interrupts. The $\overline{WP}$ input can be used as a hardwire input to the X25010 disabling all write attempts; thus providing a mechanism for limiting end user capability of altering the memory.

The X25010 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles per byte and a minimum data retention of 100 years.

FUNCTIONAL DIAGRAM



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PIN DESCRIPTIONS

Serial Output (SO)

SO is a push-pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is the serial data input pin. All data, opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are sampled or latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is high, the X25010 is deselected and the SO output pin is at high impedance and unless an internal write operation is underway the X25010 will be in the standby power mode. $\overline{CS}$ low enables the X25010, placing it in the active power mode. It should be noted that after power-on, a high to low transition on $\overline{CS}$ is required prior to the start of any operation.

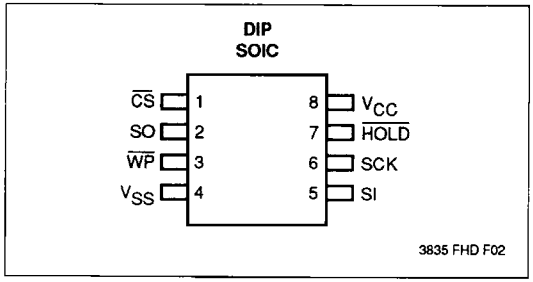
Write Protect ($\overline{WP}$)

When $\overline{WP}$ is low, nonvolatile writes to the X25010 are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held high, all functions, including nonvolatile writes operate normally. WP going low while $\overline{CS}$ is still low will interrupt a write to the X25010. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no affect on write.

Hold ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought low while SCK is Low. To resume communication, $\overline{HOLD}$ is brought high, again while SCK is low. If the pause feature is not used, $\overline{HOLD}$ should be held high at all times.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
$\overline{HOLD}$	Hold Input

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PRINCIPLES OF OPERATION

The X25010 is a 128 x 8 E^2PROM designed to interface directly with the synchronous serial peripheral interface (SPI) of the popular 6805 and 68HC11 microcontroller families.

The X25010 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising SCK. $\overline{CS}$ must be low and the $\overline{HOLD}$ and $\overline{WP}$ inputs must be high during the entire operation.

Table 1 contains a list of the instructions and their operation codes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. SCK is static, allowing the user to stop the clock and then resume operations. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input to place the X25010 into a "PAUSE" condition. After releasing $\overline{HOLD}$, the X25010 will resume operation from the point when $\overline{HOLD}$ was first asserted.

Write Enable (WREN) and Write Disable (WRDI)

The X25010 contains a write enable latch. This latch must be SET before a write operation will be completed internally. The WREN instruction will set the latch and the WRDI instruction will reset the latch. This latch is automatically reset upon a power-on condition and after the completion of a byte or page write cycle. The latch is also reset if $\overline{WP}$ is brought low.

Read Status Register (RDSR)

The RDSR instruction provides access to the status register. The status register may be read at any time, even during a write cycle. The status register is formatted as follows:

7	6	5	4	3	2	1	0
X	X	X	X	BP1	BP0	WEL	WIP

The **Write-In-Process (WIP)** bit indicates whether the X25010 is busy with a write operation. When set to a "1" a write is in progress, when set to a "0" no write is in progress. During a write all other bits are set to "1".

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch. When set to a "1" the latch is set, when set to a "0" the latch is reset.

The **Block Protect (BP0 and BP1)** bits indicate the extent of protection employed. These bits are set by the user issuing the WRSR instruction.

Write Status Register (WRSR)

The write status register instruction allows the user to select one of four levels of protection. The X25010 is divided into four 128-bit segments. One, two or all four of the segments may be protected. That is, the user may read the segment but will be unable to alter (write) data within the selected segments. The partitioning is controlled as illustrated below.

Status Register Bits		Array Addresses
BP1	BP0	Protected
0	0	NONE
0	1	$60–$7F (1/4)
1	0	$40–$7F (1/2)
1	1	$00–$7F (All)

Table 1. Instruction Set

Instruction Name	Instruction Format*	Operation
WREN	0000 0110	Set the Write Enable Latch (Enable Write Operations)
WRDI	0000 0100	Reset the Write Enable Latch (Disable Write Operations)
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register (Block Protect Bits)
READ	0000 0011	Read Data from Memory Array beginning at Selected Address
WRITE	0000 0010	Write Data to Memory Array beginning at Selected Address (1 to 4 Bytes)

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*Instructions are shown MSB in leftmost position. Instructions are transferred MSB first.

DEVICE OPERATION

Clock and Data Timing

Data input on the SI line is sampled and latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

Read Sequence

The $\overline{CS}$ line is first pulled low to select the device. The 8 bit read opcode is transmitted to the X25010, followed by the 8 bit byte address. After the read opcode and byte address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The byte address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached ($7F) the address counter rolls over to address $00 allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ high. Refer to the read operation sequence illustrated in Figure 1.

Write Sequence

Prior to any attempt to write data into the X25010 the write enable latch must first be set by issuing the WREN instruction. (See Fig. 2) $\overline{CS}$ is first taken low, then the instruction is clocked into the X25010. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken high. If the user continues the write operation without taking $\overline{CS}$ high after issuing the WREN instruction the write operation will be ignored.

Once the write enable latch is set, the user may proceed by issuing the write instruction, followed by the address and then the data to be written. This is minimally a twenty-four clock operation. $\overline{CS}$ must go low and remain low for the duration of the operation. The host may continue to write up to four bytes of data to the X25010. The only restriction is the four bytes must reside on the same page. A page address begins with address XXXX XX00 and ends with XXXX XX11. If the byte address counter reaches XXXX XX11 and the clock continues the counter will roll back to the first address of the page and overwrite any data that may have been written.

For the write operation (byte or page write) to be completed, $\overline{CS}$ can only be brought high after the twenty-fourth, thirty-second, fourtieth or fourtyeighth clock. If it is brought high at any other time the write operation will not be completed. Refer to Figure 4 below for a detailed illustration of the page write sequence and time frames in which $\overline{CS}$ going high are valid.

While the write is in progress the stats register may be read to check the WIP bit. During this time the WIP bit will be high and all other bits in the status register will be high.

Hold Operation

The $\overline{HOLD}$ input should be high (at V_{IH}) under normal operation. If a data transfer is to be interrupted $\overline{HOLD}$ can be pulled low to suspend the transfer until it can be resumed. The only restriction is the SCK input must be low when $\overline{HOLD}$ is first pulled low and SCK must also be low when $\overline{HOLD}$ is released.

The $\overline{HOLD}$ input may be tied high either directly to V_{CC} or tied to V_{CC} through a resistor.

Operational Notes

The X25010 powers-on in the following state:

- The device is in the low power standby state.
- A high to low transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is high impedance.
- The write enable latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

- The write enable latch is reset upon power-up.
- A write enable instruction must be issued to set the write enable latch.
- $\overline{CS}$ must come high at the proper clock count in order to start a write cycle.

The write enable latch is reset when $\overline{WP}$ is brought low.

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Figure 1. Read Operation Sequence

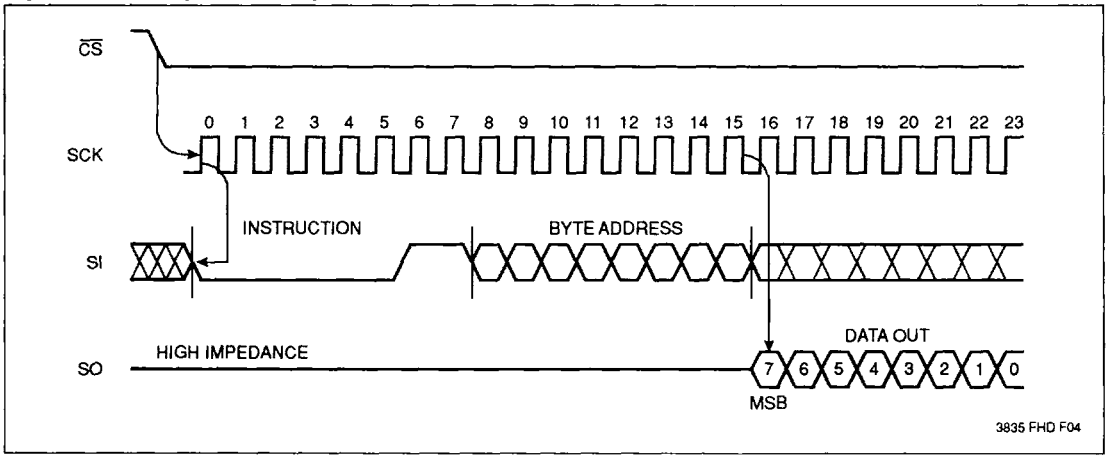


Figure 2. Write Enable Latch

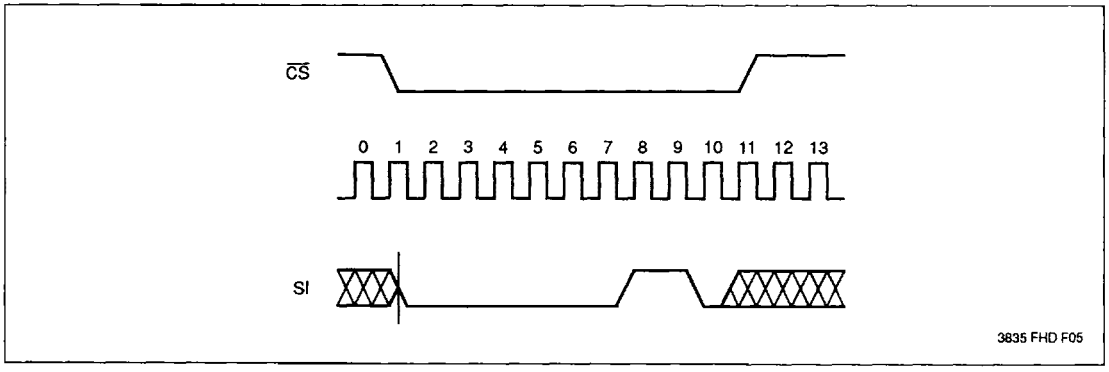


Figure 3. Write Operation Sequence

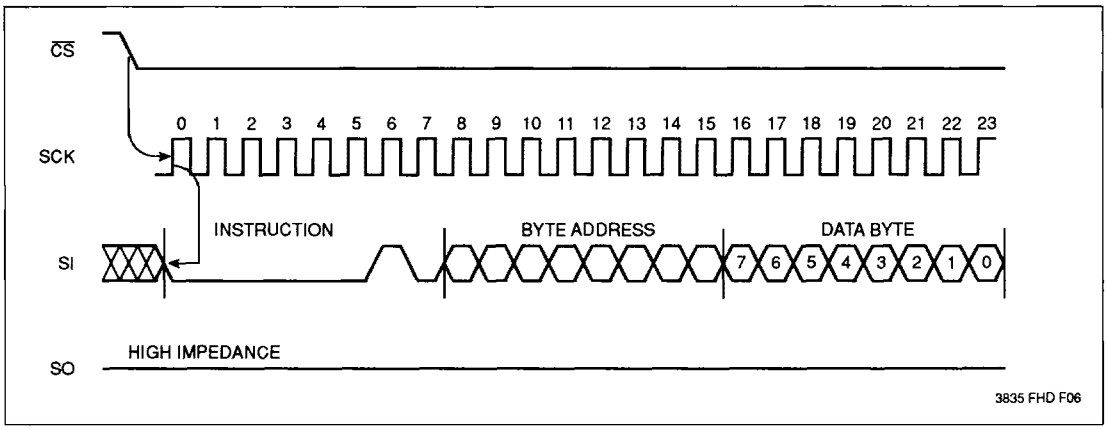
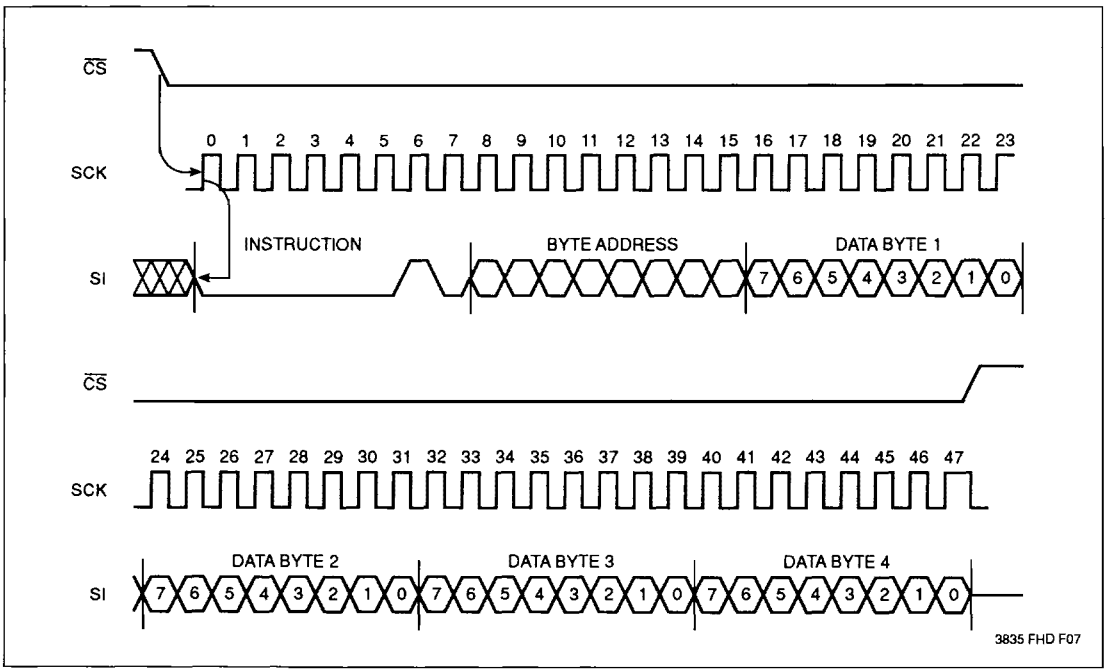


Figure 4. Page Write Operation Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .....–65°C to +135°C
Storage Temperature .....–65°C to +150°C
Voltage on any Pin with Respect to Ground –1.0V to +7V
D.C. Output Current 5mA
Lead Temperature
(Soldering, 10 Seconds) .....300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

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Supply Voltage	Limits
X25010	5V ± 10%
X25010-3	3V to 5.5V

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D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Supply Current (Active)		3	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 1MHz, SO = OPEN
I_{SB}	V_{CC} Supply Current (Standby)		150	µA	$\overline{CS}$ = V_{CC}, V_{IN} = Gnd or V_{CC} – 0.3V
I_{LI}	Input Leakage Current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = GND to V_{CC}
V_{IL}(1)	Input Low Voltage	–1.0	V_{CC} x 0.3	V	
V_{IH}(1)	Input High Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	V_{CC}–0.8		V	I_{OH} = –1.0mA

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POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_{PUR}(2)	Power-up to Read Operation		1	ms
t_{PUW}(2)	Power-up to Write Operation		5	ms

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CAPACITANCE T_A = 25°C, f = 1.0MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
C_{OUT}(2)	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

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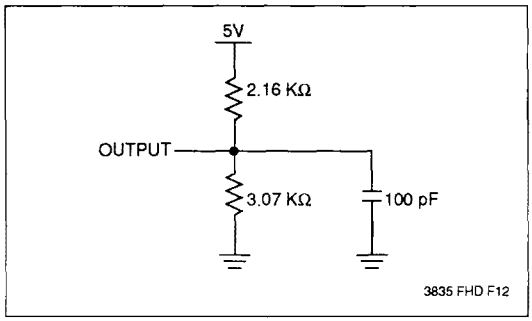
Notes: (1) V_{IL} Min and V_{IH} Max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} x 0.5

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A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{CYC}	Cycle Time	1000		ns
t_{LEAD}	$\overline{CS}$ Lead Time	500		ns
t_{LAG}	$\overline{CS}$ Lag Time	500		ns
t_{WH}	Clock High Time	400		ns
t_{WL}	Clock Low Time	400		ns
t_{SU}	Data Setup Time	100		ns
t_H	Data Hold Time	100		ns
t_{RI}	Data In Rise Time		2.0	µs
t_{FI}	Data In Fall Time		2.0	µs
t_{HD}	$\overline{HOLD}$ Setup Time	200		ns
t_{CD}	$\overline{HOLD}$ Hold Time	200		ns
t_{CS}	$\overline{CS}$ Deselect Time	500		ns
t_{WC}(3)	Write Cycle Time		10	ms

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Data Output Timing

Symbol	Parameter	Min.	Max.	Units
f_{SCK}	Clock Frequency	0	1	MHz
t_{DIS}	Output Disable Time		500	ns
t_V	Output Valid from clock Low		360	ns
t_{HO}	Output Hold Time	0		ns
t_{RO}(1)	Output Rise Time		300	ns
t_{FO}(1)	Output Fall Time		300	ns
t_{LZ}	$\overline{HOLD}$ High to Output in Low Z	100		ns
t_{HZ}	$\overline{HOLD}$ Low to Output in High Z	100		ns

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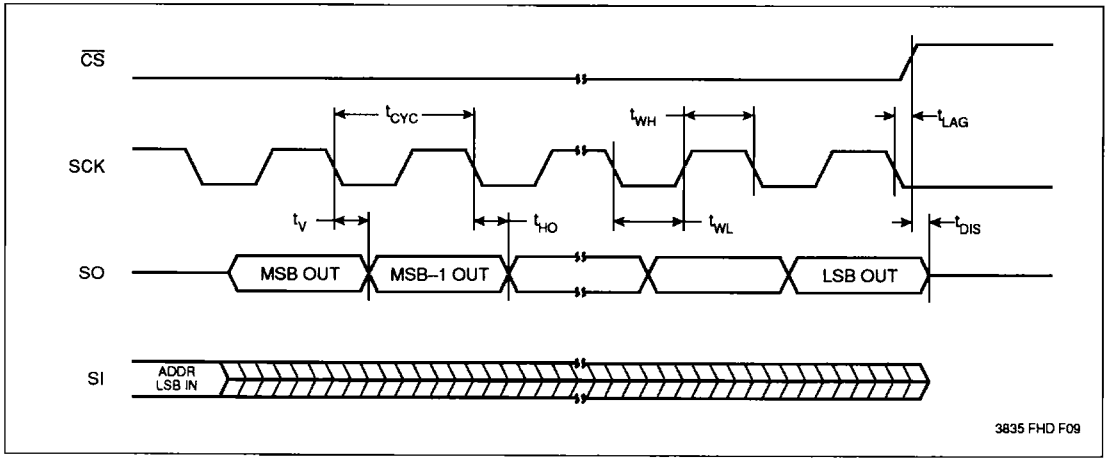
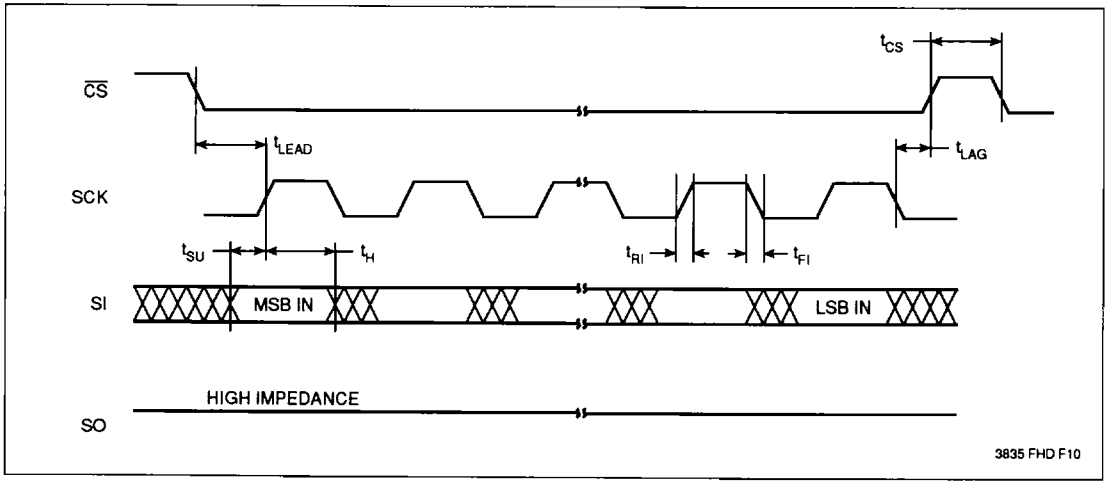
Notes: (3) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

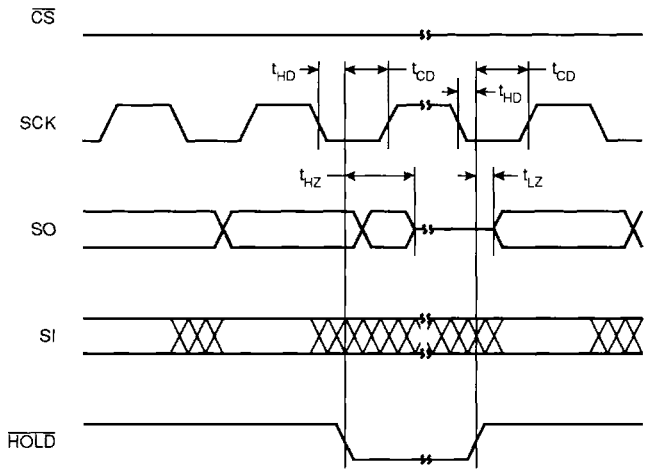
Serial Output Timing



Serial Input Timing



Hold Timing



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