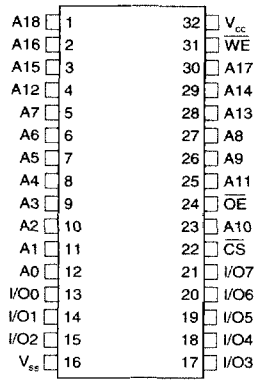
512Kx8 CMOS EEPROM, WE512K8-XCX, SMD 5962-93091

FIG. 1

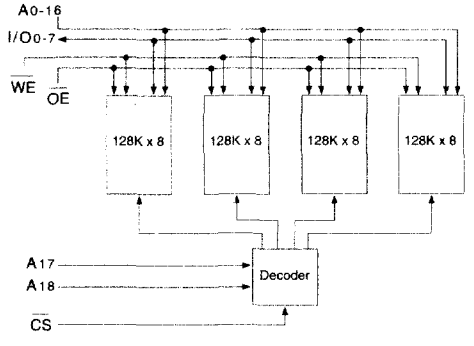
PIN CONFIGURATION TOP VIEW



PIN DESCRIPTION

A_{0-18}	Address Inputs
I/O_{0-7}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5.0V Power
V_{SS}	Ground

BLOCK DIAGRAM



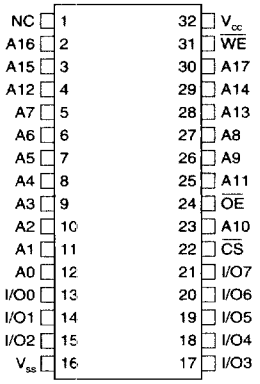
512Kx8 BIT CMOS EEPROM MODULE FEATURES

- Read Access Times of 150, 200, 250, 300ns
- JEDEC Standard 32 Pin, Hermetic Ceramic DIP (Package 300)
- Commercial, Industrial and Military Temperature Ranges
- MIL-STD-883 Compliant Devices Available
- Write Endurance 10,000 Cycles
- Data Retention at 25°C, 10 Years
- Low Power CMOS Operation:
  3mA Standby Typical/100mA Operating Maximum
- Automatic Page Write Operation
  Internal Address and Data Latches for
  512 Bytes, 1 to 128 Bytes/Row, Four Pages
- Page Write Cycle Time 10ms Max.
- Data Polling for End of Write Detection
- Hardware and Software Data Protection
- TTL Compatible Inputs and Outputs

256KX8 CMOS EEPROM, WE256K8-XCX, SMD 5962-93155

FIG.2

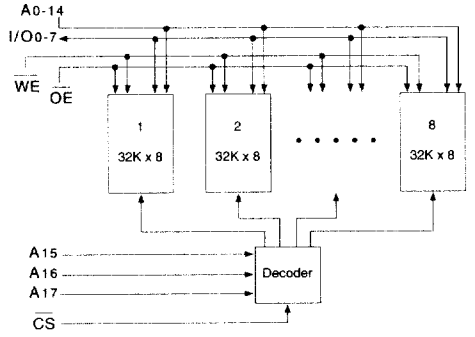
PIN CONFIGURATION TOP VIEW



PIN DESCRIPTION

A_{0-17}	Address Inputs
I/O_{0-7}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
Vcc	+5.0V Power
Vss	Ground

BLOCK DIAGRAM



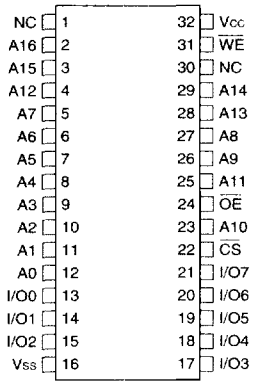
256Kx8 BIT CMOS EEPROM MODULE FEATURES

- Read Access Times of 150, 200ns
- JEDEC Standard 32 Pin, Hermetic Ceramic DIP (Package 302)
- Commercial, Industrial and Military Temperature Ranges
- MIL-STD-883 Compliant Devices Available
- Write Endurance 10,000 Cycles
- Data Retention at 25°C, 10 Years
- Low Power CMOS Operation:
  2mA Standby Typical/90mA Operating Maximum
- Automatic Page Write Operation
  Internal Address and Data Latches for
  512 Bytes, 1 to 64 Bytes/Row, Eight Pages
- Page Write Cycle Time 10mS Max.
- Data Polling for End of Write Detection
- Hardware and Software Data Protection
- TTL Compatible Inputs and Outputs

128KX8 CMOS EEPROM, WE128K8-XCX, SMD 5962-93154

FIG. 3

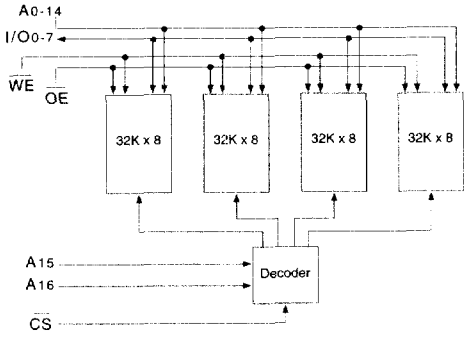
PIN CONFIGURATION TOP VIEW



PIN DESCRIPTION

A_{0-16}	Address Inputs
I/O_{0-7}	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5.0V Power
V_{SS}	Ground

BLOCK DIAGRAM



128Kx8 BIT CMOS EEPROM MODULE FEATURES

- Read Access Times of 150, 200ns
- JEDEC Standard 32 Pin, Hermetic Ceramic DIP (Package 300)
- Commercial, Industrial and Military Temperature Ranges
- MIL-STD-883 Compliant Devices Available
- Write Endurance 10,000 Cycles
- Data Retention at 25°C, 10 Years
- Low Power CMOS Operation:
  1mA Standby Typical/70mA Operating
- Automatic Page Write Operation
  Internal Address and Data Latches for
  256 Bytes, 1 to 64 Bytes/Row, Four Pages
- Page Write Cycle Time 10mS Max.
- Data Polling for End of Write Detection
- Hardware and Software Data Protection
- TTL Compatible Inputs and Outputs

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol		Unit
Operating Temperature	T_A	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Signal Voltage Any Pin	V_G	-0.6 to + 6.25	V
Voltage on $\overline{OE}$ and A9		-0.6 to +13.5	V
Thermal Resistance junction to case	θ_{JC}	28	°C/W
Lead Temperature (soldering -10 secs)		+300	°C

NOTE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O
H	X	X	Standby	High Z
L	L	H	Read	Data Out
L	H	L	Write	Data In
X	H	X	Out Disable	High Z/Data Out
X	X	H	Write	
X	L	X	Inhibit	

CAPACITANCE

(T_A = +25°C)

Parameter	Sym	Condition	512Kx8 Max	256Kx8 Max	128Kx8 Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1MHz	45	80	45	pF
Output Capacitance	C_{OUT}	$V_{I/O}$ = 0V, f = 1MHz	60	80	60	pF

This parameter is guaranteed by design but not tested.

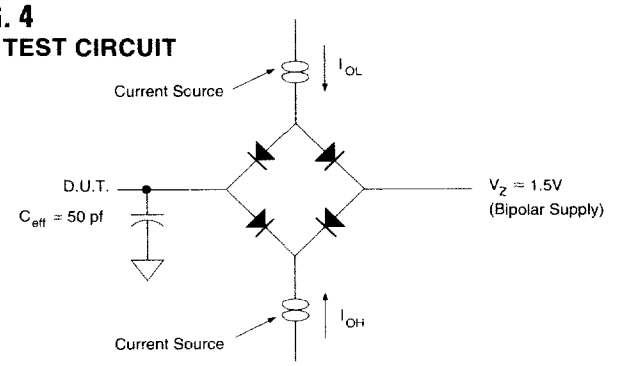
DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	512K x 8			256K x 8			128K x 8			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}			10			10			10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}			10			10			10	µA
Dynamic Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		80	100		60	90		50	70	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		3	8		2	6		1	4	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA, Vcc = 4.5V			0.45			0.45			0.45	V
Output High Voltage	V_{OH}	I_{OH} = -400µA, Vcc = 4.5V	2.4			2.4			2.4			V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

FIG. 4
AC TEST CIRCUIT



AC TEST CONDITIONS

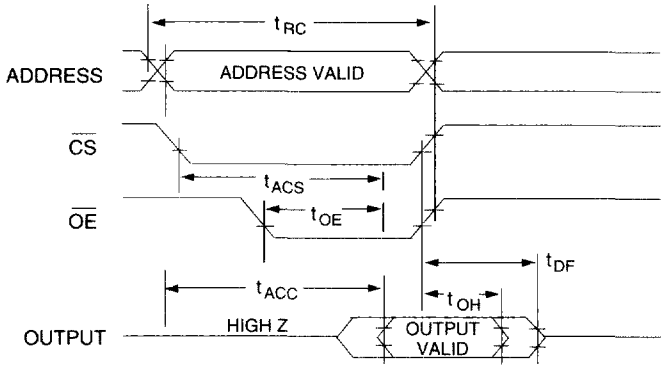
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

READ

Figure 5 shows Read cycle waveforms. A read cycle begins with selection address, chip select and output enable. Chip select is accomplished by placing the $\overline{CS}$ line low. Output enable is done by placing the $\overline{OE}$ line low. The memory places the selected data byte on I/O0 through I/O7 after the access time. The output of the memory is placed in a high impedance state shortly after either the $\overline{OE}$ line or $\overline{CS}$ line is returned to a high level.

FIG. 5
READ WAVEFORMS



NOTE:
$\overline{OE}$ may be delayed up to t_{ACS}-t_{OE} after the falling edge of $\overline{CS}$ without impact on t_{OE} or by t_{ACC}-t_{OE} after an address change without impact on t_{ACC}.

AC READ CHARACTERISTICS (SEE FIGURE 5) FOR WE512K8-XCX

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-150		-200		-250		-300		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		250		300		ns
Address Access Time	t_{ACC}		150		200		250		300	ns
Chip Select Access Time	t_{ACS}		150		200		250		300	ns
Output Hold from Address Change, $\overline{OE}$ or $\overline{CS}$	t_{OH}	0		0		0		0		ns
Output Enable to Output Valid	t_{OE}		85		85		100		125	ns
Chip Select or Output Enable to High Z Output	t_{DF}		70		70		70		70	ns

FOR WE256K8-XCX AND WE128K8-XCX

Parameter	Symbol	-150		-200		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	150		200		ns
Address Access Time	t_{ACC}		150		200	ns
Chip Select Access Time	t_{ACS}		150		200	ns
Output Hold from Address Change, $\overline{OE}$ or $\overline{CS}$	t_{OH}	10		10		ns
Output Enable to Output Valid	t_{OE}		85		100	ns
Chip Select or Output Enable to High Z Output	t_{DF}		70		70	ns

WRITE

Write operations are initiated when both $\overline{CS}$ and $\overline{WE}$ are low and $\overline{OE}$ is high. The EEPROM devices support both a $\overline{CS}$ and $\overline{WE}$ controlled write cycle. The address is latched by the falling edge of either $\overline{CS}$ or $\overline{WE}$, whichever occurs last.

The data is latched internally by the rising edge of either $\overline{CS}$ or $\overline{WE}$, whichever occurs first. A byte write operation will automatically continue to completion.

WRITE CYCLE TIMING

Figures 6 and 7 show the write cycle timing relationships. A write cycle begins with address application, write enable and chip select. Chip select is accomplished by placing the $\overline{CS}$ line low. Write enable consists of setting the $\overline{WE}$ line low. The write cycle begins when the last of either $\overline{CS}$ or $\overline{WE}$ goes low.

The $\overline{WE}$ line transition from high to low also initiates an internal 150µsec delay timer to permit page mode operation. Each subsequent $\overline{WE}$ transition from high to low that occurs before the completion of the 150µsec time out will restart the timer from zero. The operation of the timer is the same as a retriggerable one-shot.

AC WRITE CHARACTERISTICS

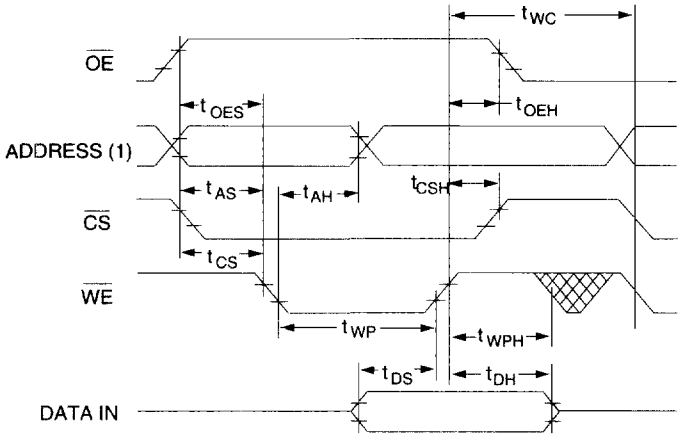
(VCC = 5.0V, VSS = 0V, TA = -55°C to +125°C)

Parameter	Symbol	512K x 8		256K x 8		128K x 8		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time, TYP = 6mS	t_{WC}		10		10		10	ms
Address Set-up Time	t_{AS}	10		30		30		ns
Write Pulse Width ($\overline{WE}$ or $\overline{CS}$)	t_{WP}	150		150		150		ns
Chip Select Set-up Time	t_{CS}	0		0		0		ns
Address Hold Time (1)	t_{AH}	125		50		50		ns
Data Hold Time	t_{DH}	10		0		0		ns
Chip Select Hold Time	t_{CH}	0		0		0		ns
Data Set-up Time	t_{DS}	100		100		100		ns
Output Enable Set-up Time	t_{OES}	10		30		30		ns
Output Enable Hold Time	t_{OEH}	10		0		0		ns
Write Pulse Width High	t_{WPH}	50		50		50		ns

NOTES:

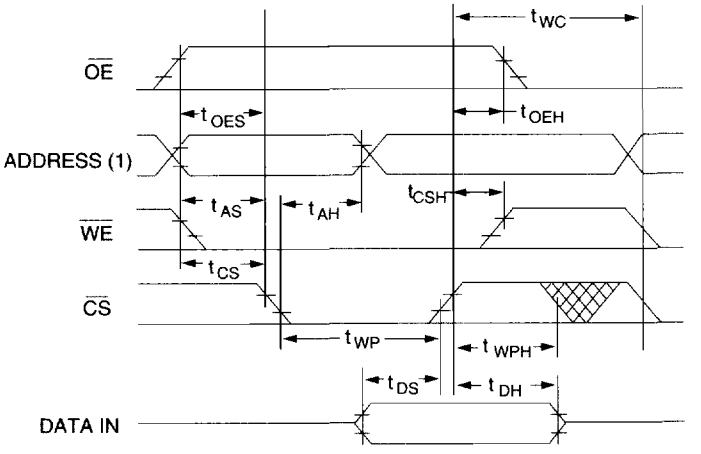
1. A_{17} and A_{18} must remain valid through $\overline{WE}$ and $\overline{CS}$ low pulse, for 512K x 8.
   A_{15}, A_{16}, and A_{17} must remain valid through $\overline{WE}$ and $\overline{CS}$ low pulse, for 256K x 8.
   A_{15} and A_{16} must remain valid through $\overline{WE}$ and $\overline{CS}$ low pulse, for 128K x 8.

FIG. 6
WRITE WAVEFORMS
WE CONTROLLED



NOTE:
1. Decoded Address Lines must be valid for the duration of the write.

FIG. 7
WRITE WAVEFORMS
CS CONTROLLED



NOTE:
1. Decoded Address Lines must be valid for the duration of the write.

DATA POLLING

Operation with data polling permits a faster method of writing to the EEPROM. The actual time to complete the memory programming cycle is faster than the guaranteed maximum.

The EEPROM features a method to determine when the internal programming cycle is completed. After a write cycle is initiated, the EEPROM will respond to read cycles to provide the microprocessor with the status of the programming cycle. The status consists of the last data byte written being returned with data bit I/O_7 complemented during the programming cycle, and I/O_7 true after completion.

Data polling allows a simple bit test operation to determine the status of the EEPROM. During the internal programming cycle, a read of the last byte written will produce the complement of the data on I/O_7. For example, if the data written consisted of I/O_7 = HIGH, then the data read back would consist of I/O_7 = LOW.

A polled byte write sequence would consist of the following steps:

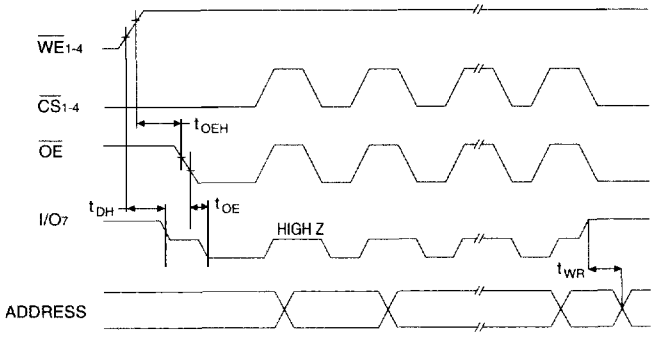
1. write byte to EEPROM
2. store last byte and last address written
3. release a time slice to other tasks
4. read byte from EEPROM - last address
5. compare I/O_7 to stored value
   - **a)** If different, write cycle is not completed, go to step 3.
   - **b)** If same, write cycle is completed, go to step 1 or step 3.

DATA POLLING AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	512Kx8		256Kx8		128Kx8		Unit
		Min	Max	Min	Max	Min	Max	
Data Hold Time	t_{DH}	10		0		0		ns
Output Enable Hold Time	t_{OEH}	10		0		0		ns
Output Enable To Output Delay	t_{OE}		100		100		100	ns
Write Recovery Time	t_{WR}	0		0		0		ns

FIG. 8
DATA POLLING WAVEFORMS



PAGE WRITE OPERATION

These devices have a page write operation that allows one to 64 bytes of data (one to 128 bytes for the WE512K8) to be written into the device and then simultaneously written during the internal programming period. Successive bytes may be loaded in the same manner after the first data byte has been loaded. An internal timer begins a time out operation at each write cycle. If another write cycle is completed within 150µs or less, a new time out period begins. Each write cycle restarts the delay period. The write cycles can be continued as long as the interval is less than the time out period.

The usual procedure is to increment the least significant address lines from A_0 through A_5 (A_0 through A_6 for the WE512K8) at each write cycle. In this manner a page of up to 64 bytes (128 bytes for the WE512K8) can be loaded into the EEPROM in a burst mode before beginning the relatively long interval programming cycle.

After the 150µs time out is completed, the EEPROM begins an internal write cycle. During this cycle the entire page of bytes will be written at the same time. The internal programming cycle is the same regardless of the number of bytes accessed.

The page address must be the same for each byte load and must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CS}$). The block address also must be the same for each byte load and must remain valid throughout the $\overline{WE}$ (or $\overline{CS}$) low pulse. The page and block address lines are summarized below:

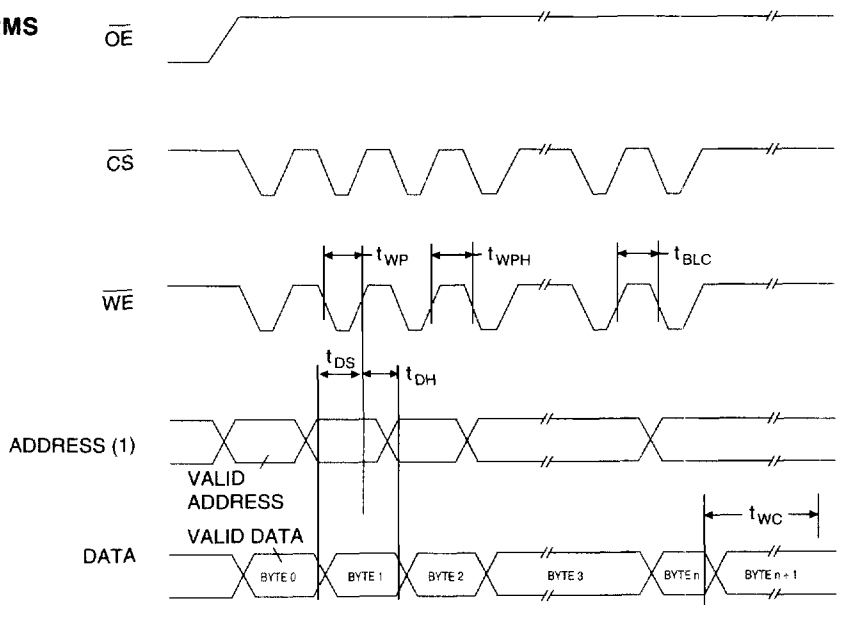
PAGE MODE CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Min	Max	Unit
Write Cycle Time, TYP = 6mS	t_{WC}		10	ms
Data Set-up Time	t_{DS}	100		ns
Data Hold Time	t_{DH}	10		ns
Write Pulse Width	t_{WP}	150		ns
Byte Load Cycle Time	t_{BLC}		150	µs
Write Pulse Width High	t_{WPH}	50		ns

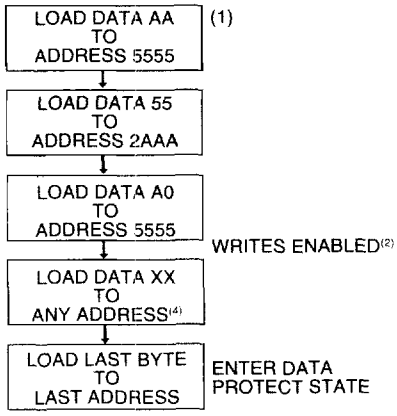
Device	Block Address	Page Address
WE512K8-XCX	A_{17}-A_{18}	A_7-A_{16}
WE256K8-XCX	A_{15}-A_{17}	A_6-A_{14}
WE128K8-XCX	A_{15}-A_{16}	A_6-A_{14}

FIG. 9
PAGE WRITE WAVEFORMS



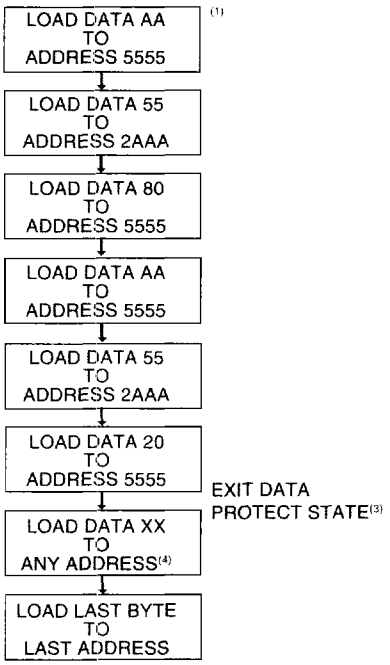
NOTE:
1. Decoded Address Lines must be valid for the duration of the write.

FIG. 10
SOFTWARE BLOCK DATA PROTECTION ENABLE ALGORITHM



NOTES:
1. Data Format: I/O7-0 (Hex);
   Address Format: A14 -A0 (Hex).
   A17 and A18 control selection of one of four blocks in the 512Kx8.
   A15, A16, and A17 control selection of one of 8 pages in the 256Kx8.
   A15 and A16 control one of the four blocks in the 128Kx8.
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data at each of 4 blocks may be loaded in the 512Kx8. 1 to 64 bytes of data at each of 8 blocks may be loaded in the 256Kx8 and 1 to 64 bytes on 4 blocks in the 128Kx8.

FIG. 11
SOFTWARE BLOCK DATA PROTECTION DISABLE ALGORITHM



NOTES:
1. Data Format: I/O7-0 (Hex);
   Address Format: A14 -A0 (Hex).
   A17 and A18 control selection of one of four blocks in the 512Kx8.
   A15, A16, and A17 control selection of one of 8 pages in the 256Kx8.
   A15 and A16 control one of the four blocks in the 128Kx8.
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data at each of 4 blocks may be loaded in the 512Kx8. 1 to 64 bytes of data at each of 8 blocks may be loaded in the 256Kx8 and 1 to 64 bytes on 4 blocks in the 128Kx8.

SOFTWARE DATA PROTECTION

A software write protection feature may be enabled or disabled by the user. When shipped by White Microelectronics, the devices have the feature disabled. Write access to the device is unrestricted.

To enable software write protection, the user writes three access code bytes to three special internal locations. Once write protection has been enabled, each write to the EEPROM must use the same three byte write sequence to permit writing. After setting software data protection, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device, however, for the duration of twc. The write protection feature can be disabled by a six byte write sequence of specific data to specific locations. Power transitions will not reset the software write protection.

Each 32K byte block (128K bytes for the WE512K8) of EEPROM has independent write protection. One or more blocks may be enabled and the rest disabled in any combination. The software write protection guards against inadvertent writes during power transitions or unauthorized modification using a PROM programmer. The block selection is controlled by the upper most address lines (A17 through A18 for the WE512K8, A15 through A17 for the WE256K8, or A15 and A16 for the WE128K8).

HARDWARE DATA PROTECTION

Several methods of hardware data protection have been implemented in the White Microelectronics EEPROM. These are included to improve reliability during normal operations.

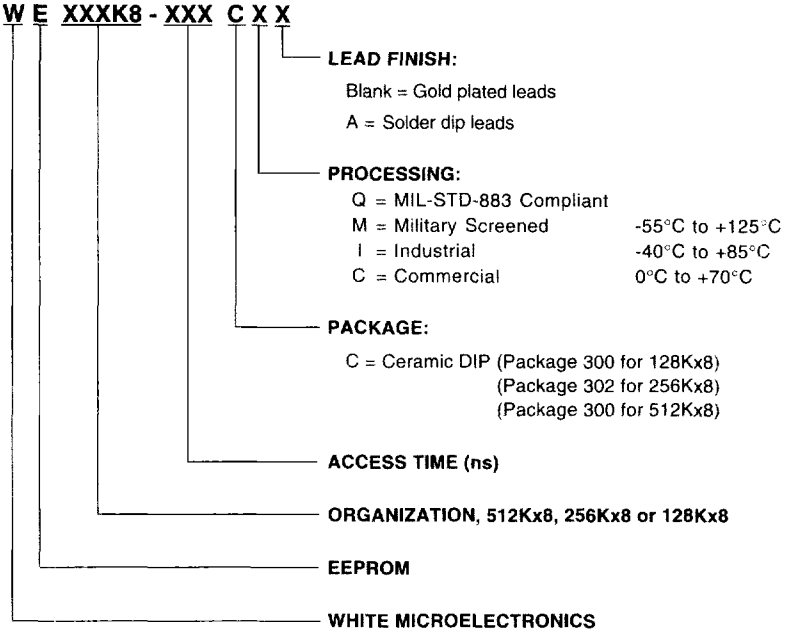
a) Vcc power on delay
As Vcc climbs past 3.8V typical the device will wait 5mSec typical before allowing write cycles.

b) Vcc sense
While below 3.8V typical write cycles are inhibited.

c) Write inhibiting
Holding $\overline{OE}$ low and either $\overline{CS}$ or $\overline{WE}$ high inhibits write cycles.

d) Noise filter
Pulses of <8ns (typ) on $\overline{WE}$ or $\overline{CS}$ will not initiate a write cycle.

ORDERING INFORMATION



DEVICE TYPE	SPEED	PACKAGE	WM PART NO.	SMD NO.
512K x 8 EEPROM	150ns	32 pin DIP (C)	WE512K8-150CQ	5962-93091 01HYX
512K x 8 EEPROM	300ns	32 pin DIP (C)	WE512K8-300CQ	5962-93091 02HYX
512K x 8 EEPROM	250ns	32 pin DIP (C)	WE512K8-250CQ	5962-93091 03HYX
512K x 8 EEPROM	200ns	32 pin DIP (C)	WE512K8-200CQ	5962-93091 04HYX
256K x 8 EEPROM	200ns	32 pin DIP (C)	WE256K8-200CQ	5962-93155 01HXX
256K x 8 EEPROM	150ns	32 pin DIP (C)	WE256K8-150CQ	5962-93155 02HXX
128K x 8 EEPROM	200ns	32 pin DIP (C)	WE128K8-200CQ	5962-93154 01HXX
128K x 8 EEPROM	150ns	32 pin DIP (C)	WE128K8-150CQ	5962-93154 02HXX