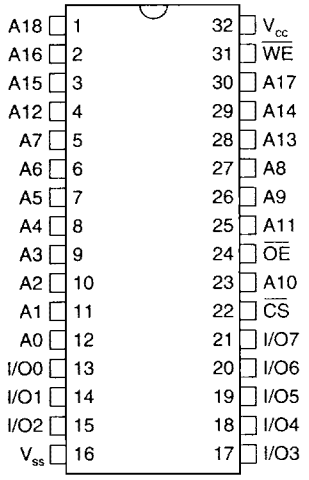


FIGURE 1 — Pin Configuration

A0 - A18	Address Inputs
I/O0 - I/O7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	+5.0V Power
V_{SS}	Ground

Pin Description

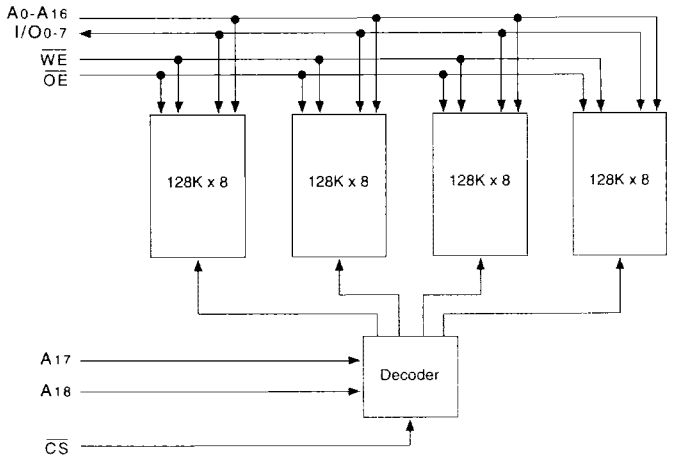


FIGURE 2 — Block Diagram

WE-512K8-150CX

512K x 8 CMOS EEPROM Module

SMD 5962-93091

FEATURES

- **Read Access Time: 150nS**
- **JEDEC Standard 32 Pin DIP, Hermetic Ceramic Package**
- **Full Military and Industrial Temperature Ranges**
- **MIL-STD-883D Compliant Devices Available**
- **Low Power CMOS Operation:**
  3mA Standby Typical
  80mA Operating Maximum
- **Automatic Page Write Operation**
  Internal Address and Data Latches for 512 Bytes, 1 to 128 Bytes/Page, Four Pages
- **Page Write Cycle Time: 10mS Max.**
- **Data Polling for End of Write Detection**
- **Hardware and Software Data Protection**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Write Endurance 10,000 Cycles**
- **Data Retention at 25°C, 10 Years**

DESCRIPTION

The White Technology WE-512K8-150CX is a CMOS EEPROM housed in an hermetically sealed ceramic 32 pin package. Featuring industry standard pinouts for EEPROMs, the device provides 512K bytes of non-volatile low power memory. The device is well suited for program storage and data logging applications. The device retains data for ten years after writing.

Designed for use in hostile environments, the memory packaging and construction is well matched to military and severe industrial applications. Screening and burn in to military standards are available options.

Inputs and outputs are CMOS and TTL compatible. The logic levels and drive capabilities permit the memory to interface with most digital logic systems. Since the device is all CMOS, low power operation for standby applications such as battery operated systems is simple. The normal operating range for V_{CC} includes standard TTL levels. Programming is also accomplished using the standard five-volt supply.

The memory features low power consumption. Typical values for operating current are 50mA at 25°C while being read at 5MHz. In standby, the memory has a typical current of 3mA at 25°C. In systems where multiple modules are operating using chip select to activate each device, the overall current requirement is only slightly above that required for one unit. Those units not selected require only standby current.

Several alternate methods of writing data may be used. Data may be written one byte at a time or from 1 to 4 pages of up to 64 bytes each in bursts. Either of these methods may be used with fixed time out of 10mSec or a variable minimum time out using data polling techniques.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Commercial	Military	Unit
Operating Temperature	T_A	-40 to +85	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +125	-65 to +150	°C
Signal Voltage Any Pin	V_G	-0.6 to +6.25	-0.6 to +6.25	V
Voltage on $\overline{OE}$ and A9		-0.6 to +13.5	-0.6 to +13.5	V

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	A0-A16	Mode	Data I/O	Device Current
H	X	X	X	Standby	High Z	Standby
L	L	H	Stable	Read	Data Out	Active
L	H	L	Stable	Write	Data In	Active
X	H	X	X	Out Disable	High Z	Active
X	X	H	X	Write Inhibit		Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.0	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C

CAPACITANCE

Parameter	Symbol	Condition	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1MHz, T_A = 25°C	40	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V, f = 1MHz, T_A = 25°C	40	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = Max, V_{IN} = GND or V_{CC}		20	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		20	µA
Dynamic Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		80	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{CC}, $\overline{OE}$ = V_{IH}, Duty Cycle = Max		8	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA		0.45	V
Output High Voltage	V_{OH}	I_{OH} = -400µA	2.4		V

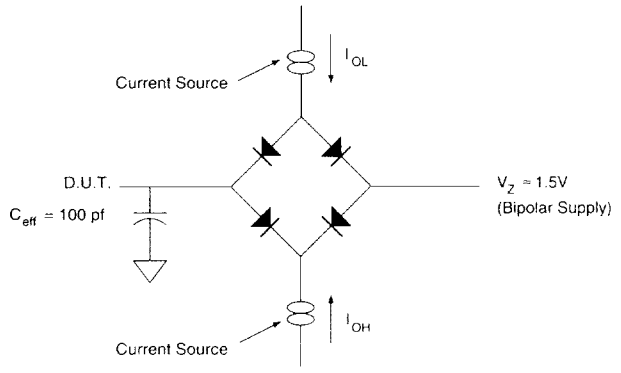


FIGURE 3 — AC Test Circuit

AC TEST CONDITIONS

Parameter	Sym.	Typ.	Unit
Input Pulse Level		0 to 3.0	V
Input Rise and Fall		5	nS
Input and Output Reference Level		1.5	V
Output Load Capacitance	CL	100	pF

Notes:
V_Z is programmable from -2V to +7V
I_{OL} & I_{OH} programmable from 0 to 16mA
Tester Impedance Z_0 = 75 Ω
V_Z is typically the midpoint of V_{OH} and V_{OL} (i.e. (2.4 + 0.4)/2 = 1.4V)
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE Tester Includes Jig Capacitance

WRITE

Write operations are initiated when both $\overline{CS}$ and $\overline{WE}$ are low and $\overline{OE}$ is high. The WE-512K8-150CX supports both a $\overline{CS}$ and $\overline{WE}$ controlled write cycle. The address is latched by the falling edge of either $\overline{CS}$ or $\overline{WE}$, whichever occurs last.

The data is latched internally by the rising edge of either $\overline{CS}$ or $\overline{WE}$, whichever occurs first. A byte write operation will automatically continue to completion.

WRITE CYCLE TIMING

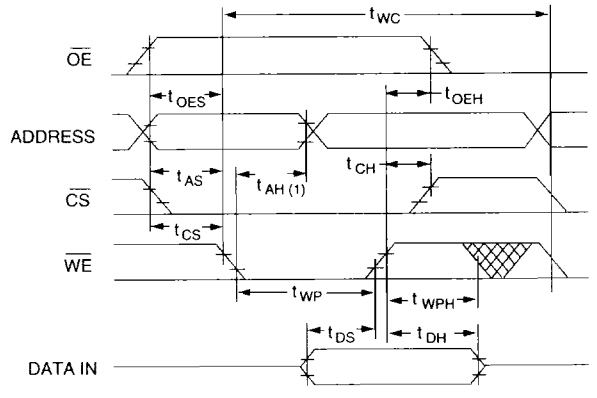
Figures 4 and 5 show the write cycle timing relationships. A write cycle begins with address application, write enable and chip select. Chip select is accomplished by placing the $\overline{CS}$ line low. Write enable consists of setting the $\overline{WE}$ line low. The write cycle begins when the last of either $\overline{CS}$ or $\overline{WE}$ goes low.

The $\overline{WE}$ line transition from high to low also initiates an internal 150µSec delay timer to permit page mode operation. Each subsequent $\overline{WE}$ transition from high to low that occurs before the completion of the 150µSec time out will restart the timer from zero. The operation of the timer is the same as a retriggerable one-shot.

AC WRITE CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol	Min.	Max.	Unit
WRITE CYCLE				
Write Cycle Time, TYP = 6mS	t_{WC}		10	mS
Address Set-up Time	t_{AS}	10		nS
Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	t_{WP}	150		nS
Chip Select Set-up Time	t_{CS}	0		nS
Address Hold Time (1)	t_{AH}	100		nS
Data, Hold Time	t_{DH}	10		nS
Chip Select Hold Time	t_{CH}	0		nS
Data Set-up Time	t_{DS}	100		nS
Output Enable Set-up Time	t_{OES}	10		nS
Output Enable Hold Time	t_{OEH}	10		nS



1) A17 and A18 must remain valid for the duration of the write cycle.

FIGURE 4 – Write Waveforms – $\overline{WE}$ Controlled

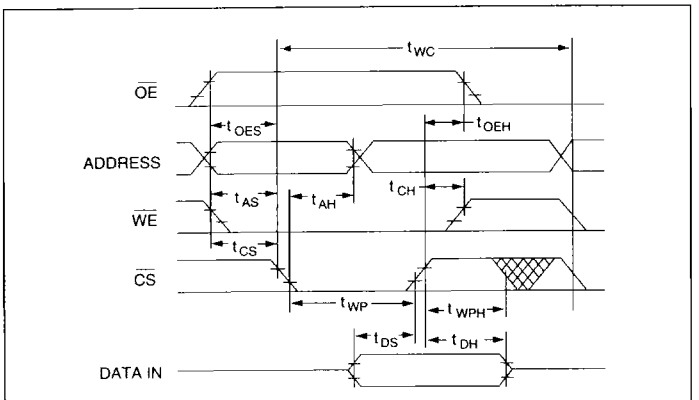


FIGURE 5 – Write Waveforms – $\overline{CS}$ Controlled

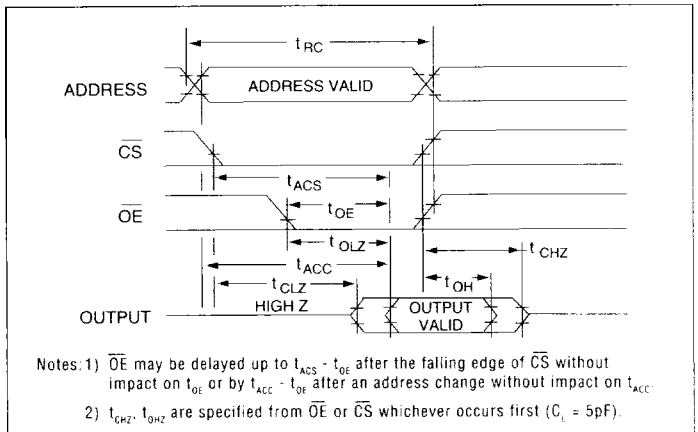
READ

Figure 6 shows Read cycle waveforms. A read cycle begins with selection address, chip select and output enable. Chip select is accomplished by placing the $\overline{CS}$ line low. Output enable is done by placing the $\overline{OE}$ line low. The memory places the selected data byte on I/O0 through I/O7 after the access time. The output of the memory is placed in a high impedance state shortly after either the $\overline{OE}$ line or $\overline{CS}$ line is returned to a high level.

AC READ CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol	Min.	Max.	Unit
READ CYCLE				
Read Cycle Time	t_{RC}	150		nS
Address Access Time	t_{ACC}		150	nS
$\overline{CS}$ Access Time	t_{ACS}		150	nS
Output Hold from Add. Change, $\overline{OE}$ or $\overline{CS}$	t_{OH}	0		nS
Output Enable to Output Valid	t_{OE}	0	85	nS
Chip Select to Output in Low Z	t_{CLZ}	0		nS
Chip Select to Output in High Z	t_{CHZ}		70	nS
Output Enable to Output in Low Z	t_{OLZ}	0		nS



Notes: 1) $\overline{OE}$ may be delayed up to t_{ACS} - t_{OE} after the falling edge of $\overline{CS}$ without impact on t_{OE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.

2) t_{OHZ}, t_{OHZ} are specified from $\overline{OE}$ or $\overline{CS}$ whichever occurs first (C_L = 5pF).

3) All I/O transitions are measured ±200mV from steady state with loading as specified in "Load Test Circuits."

FIGURE 6 – Read Waveforms

DATA POLLING

Operation with data polling permits a faster method of writing to the EEPROM. The actual time to complete the memory programming cycle is faster than the guaranteed maximum.

The EEPROM features a method to determine when the internal programming cycle is completed. After a write cycle is initiated, the WE-512K8-150CX will respond to read cycles to provide the microprocessor with the status of the programming cycle. The status consists of the last data byte written being returned with data bit I/O7 complemented during the programming cycle, and I/O7 true after completion.

DATA POLLING CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol	Min.	Max.	Unit
DATA POLLING CHARACTERISTICS				
Data Hold Time	t_{DH}	10		nS
$\overline{OE}$ Hold Time	t_{OEH}	10		nS
$\overline{OE}$ To Output Delay	t_{OE}		150	nS
Write Recovery Time	t_{WR}	0		nS

Data polling allows a simple bit test operation to determine the status of the WE-512K8-150CX. During the internal programming cycle, a read of the last byte written will produce the complement of the data on I/O7. For example, if the data written consisted of I/O7 = HIGH, then the data read back would consist of I/O7 = LOW.

A polled byte write sequence would consist of the following steps:

1) write byte to EEPROM
2) store last byte and last address written
3) release a time slice to other tasks
4) read byte from EEPROM - last address
5) compare I/O7 to stored value
   A) If different, write cycle is not completed, go to step 3.
   B) If same, write cycle is completed, go to step 1 or step 3.

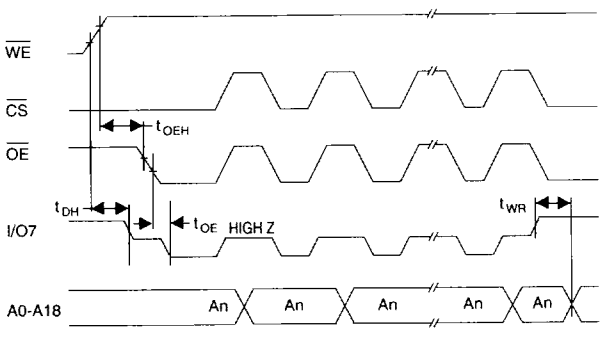


FIGURE 7 – Data Polling Waveforms

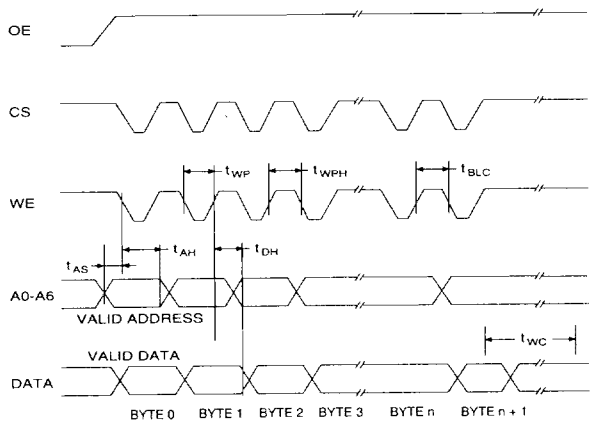
PAGE WRITE OPERATION

The WE-512K8-150CX features page write operation. A page is actually a 128 byte internal buffer that can be written to at normal SRAM speeds. The host can write from one to 128 bytes during such a burst. For each byte the lower address lines A0 - A6 would be used to select a location in the page. Address lines A7 - A16 select the page in a block. Address lines A17 and A18 select one of four blocks of memory.

An internal timer begins a time out operation at each write cycle. If another write cycle is completed within 150µSec or less, a new time out period begins. Each write cycle restarts the delay period. The write cycles can be continued as long as the interval is less than the time out period.

The usual procedure is to increment the least significant address lines from A0 - A6 at each write cycle. In this manner a page of up to 128 bytes can be loaded into the EEPROM in a burst mode before beginning the relatively long interval programming cycle.

After the 150µSec time out is completed, the EEPROM begins an internal write cycle. During this cycle the entire page of bytes will be written at the same time. The internal programming cycle is the same whether one, five, ten, or sixty-four bytes are accessed.



Note: A7 through A18 must specify the page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
$\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
A17, 18 must remain valid for duration of write cycle.

FIGURE 8 – Page Mode Write Waveforms

PAGE MODE CHARACTERISTICS

(V_{CC} = 5V, V_{SS} = 0V, T_A = -55°C TO 125°C)

Parameter	Symbol	Min.	Max.	Unit
PAGE MODE WRITE CHARACTERISTICS				
Write Cycle Time, TYP = 6mS	t_{WC}		10	mS
Address Set-up Time	t_{AS}	10		nS
Address Hold Time (1)	t_{AH}	100		nS
Data Set-up Time	t_{DS}	100		nS
Data Hold Time	t_{DH}	10		nS
Write Pulse Width	t_{WP}	150		nS
Byte Load Cycle Time	t_{BLC}		150	µS
Write Pulse Width High	t_{WPH}	50		nS

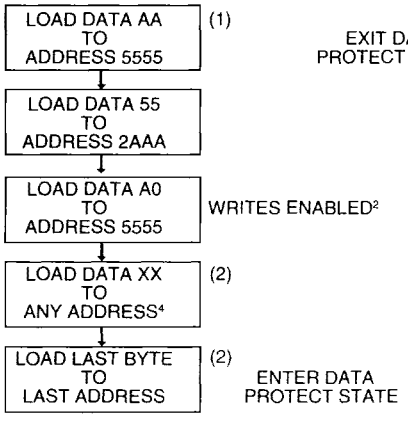
(1) A17 and A18 must remain valid for duration of write cycle.

SOFTWARE DATA PROTECTION

A software write protection feature may be enabled or disabled by the user. When shipped by White Technology, the WE-512K8-150CX has the feature disabled. Write access to the device is unrestricted.

To enable software write protection, the user writes three access code bytes to three special internal locations. Once write protection has been enabled, each write to the EEPROM must use the same three byte write sequence to permit writing. The write protection feature can be disabled by a six byte write sequence of specific data to specific locations. Power transitions will not reset the software write protection.

Each 128K byte block of the EEPROM has independent write protection. One or more blocks may be enabled and the rest disabled in any combination. The software write protection guards against inadvertent writes during power transitions, or unauthorized modification using a PROM programmer. The block section is controlled by address lines A17 and A18.



Notes:
1. Data Format: I/O7 - I/O0 (Hex); Address Format: A14 - A0 (Hex). A17 and A18 control selection of one of four blocks.
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 128 bytes of data may be loaded.

FIGURE 9 – Software Block Data Protection Enable Algorithm

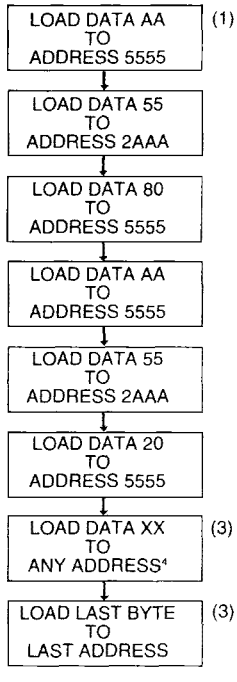


FIGURE 10 – Software Block Data Protection Disable Algorithm

HARDWARE DATA PROTECTION

Several methods of hardware data protection have been implemented in the White Technology WE-512K8-150CX EEPROM. These are included to improve reliability during normal operations.

a) Vcc power on delay - As Vcc climbs past 3.8V the device will wait 5mSec before allowing write cycles.
b) Vcc sense - While below 3.8V write cycles are inhibited.
c) Write inhibiting - Holding $\overline{OE}$ low and either $\overline{CS}$ or $\overline{WE}$ high inhibits write cycles.

ORDERING INFORMATION

PACKAGE OPTIONS

C	Ceramic DIP

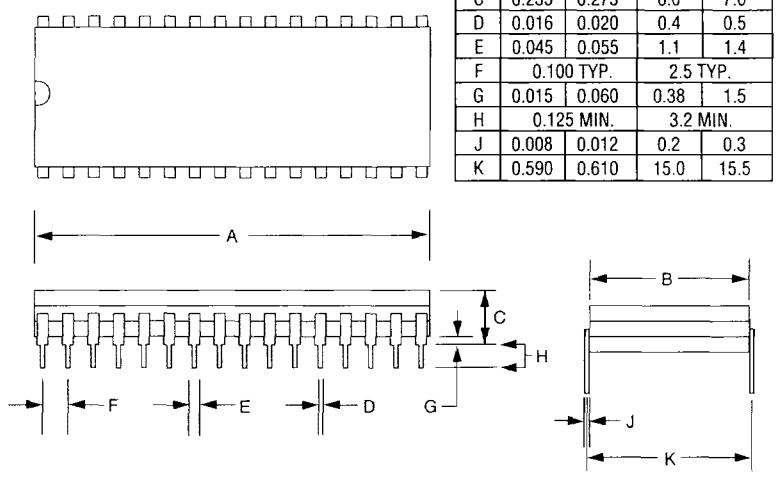
TEMPERATURE RANGE OPTIONS

M	Military	-55°C to +125°C
I	Industrial	-40°C to +85°C
C	Commercial	0°C to +70°C

W E - 512K 8 - 150 C X

- **PROCESSING:**
  - Q = MIL-STD-883 Compliant
  - M = Military
  - I = Industrial
  - C = Commercial
- **PACKAGE:**
  - C = Ceramic Side Brazed
- **ACCESS/CYCLE TIME**
- **BITS PER WORD**
- **NUMBER OF WORDS**
- **EEPROM**
- **WHITE TECHNOLOGY**

PACKAGE OUTLINE



DIM.	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.654	1.686	42.0	42.8
B	0.580	0.600	14.7	15.2
C	0.235	0.275	6.0	7.0
D	0.016	0.020	0.4	0.5
E	0.045	0.055	1.1	1.4
F	0.100 TYP.		2.5 TYP.	
G	0.015	0.060	0.38	1.5
H	0.125 MIN.		3.2 MIN.	
J	0.008	0.012	0.2	0.3
K	0.590	0.610	15.0	15.5

White Technology, Inc.
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1292 2nd Printing 2.5 PG 18369 (Supersedes 0192/17461)

NOTES:

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Application Specific Multichip Modules for Military, Industrial and Commercial Applications

- Customer specified processors, coprocessors, memory, temperature ranges, packaging and other application specific requirements.
- Engineering support from circuit design through final package assembly.
- Facility certified to MIL-STD-1772.
- Military screening available to meet requirements of MIL-H-38534 and Test Method 5008 of MIL-STD-883.

Custom Memory Modules

- **MCMMs** with customer defined memory capacities and packaging. Our customers can specify the amount and organizations needed for unique applications.

Standard SRAM Modules

- 25 to 120 nS speeds
- 512K x 8, 256K x 8, 128K x 8, 128K x 32, 512K x 32 MCMMs
- 32 pin JEDEC DIP pinouts (DESC qualified, QML-38534 per EQC-92-138)
- Hex-in-line 66 pin PGA-type modules, configurable as 128K x 32, 256K x 16 or 512K x 8
- 64M SRAM configurable to 8M x 8, 4M x 16 or 2M x 32
- Military, Industrial and Commercial grade devices
- Military screening available
- Low power CMOS

Standard EEPROM Modules

- 512K x 8, 256K x 8, 128K x 8 DIP modules
- 150 nS access time
- Low power CMOS
- 32 pin JEDEC DIP pinouts (DESC qualified, QML-38534 per EQC-92-070)
- Hex-in-line 66 pin PGA-type modules, configurable as 128K x 32, 256K x 16 or 512K x 8
- Military, Industrial and Commercial temperatures
- Military screening available

Standard Flash Modules

- 1024K x 8, 200nS, 34 pin DIP module
- Hex-in-line 66 pin PGA-type modules, configurable as 128K x 32, 256K x 16 or 512K x 8
- 128M Flash PROM configurable to 16M x 8, 8M x 16 or 4M x 32

Standard Microcontroller Modules

- 80C31 based with 64Kbytes Flash and 8Kbytes SRAM
- 80C88 based with 16K x 8 SRAM and 16K x 8 EEPROM
- 68020 based with 32K x 32 SRAM, 32K x 32 EEPROM, optional 68881FPC, RS232/422/485
- i486™ based with 512K x 32 SRAM, 1M x 32 EEPROM; advanced info

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