X9111

Single Supply/Low Power/1024-Tap/SPI Bus/Single Digitally-Controlled (XDCP™) Potentiometer

FN8159
Rev 5.00
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The X9111 integrates a single, digitally controlled potentiometer (XDCP) on a monolithic CMOS integrated circuit.

The digital controlled potentiometer is implemented using 1023 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the SPI bus interface. The potentiometer has associated with it a volatile Wiper Counter Register (WCR) and four nonvolatile Data Registers that can be directly written to and read by the user. The contents of the WCR control the position of the wiper on the resistor array through the switches. Power-up recalls the contents of the default data register (DR0) to the WCR.

The XDCP can be used as a 3-terminal potentiometer or as a 2-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

Features

- 1024 resistor taps – 10-bit resolution
- SPI serial interface for write, read, and transfer operations of the potentiometer
- Wiper resistance, 40Ω typical at 5V
- Four nonvolatile Data Registers
- Nonvolatile storage of multiple wiper positions
- Power-on recall, loads saved wiper position on power-up
- Standby current <3µA maximum
- V_{CC}: 2.7V to 5.5V operation
- 100kΩ end-to-end resistance
- 100-year data retention
- Endurance: 100,000 data changes per bit per register
- 14 Ld TSSOP
- Low-power CMOS
- Single supply version of the X9110
- Pb-Free (RoHS compliant)

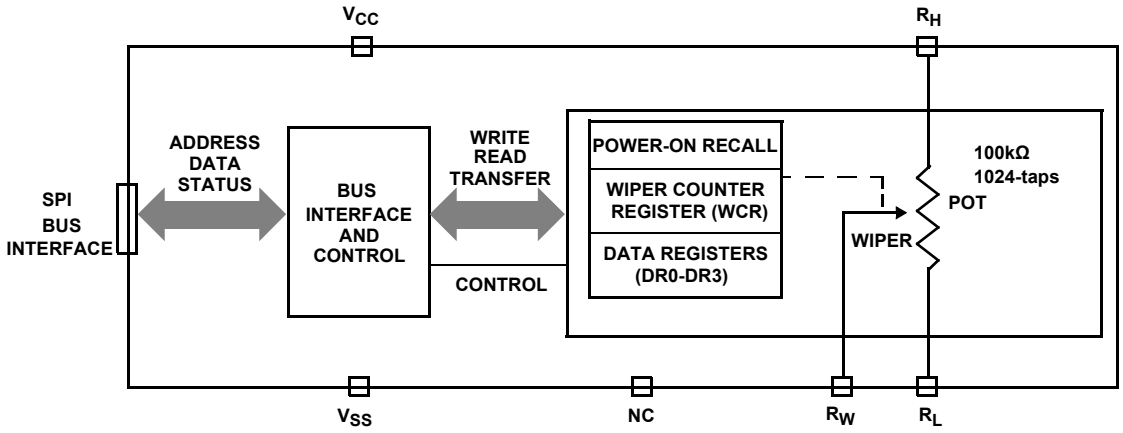


FIGURE 1. FUNCTIONAL DIAGRAM

Circuit Level Applications

- Vary the gain of a voltage amplifier
- Provide programmable DC reference voltages for comparators and detectors
- Control the volume in audio circuits
- Trim out the offset voltage error in a voltage amplifier circuit
- Set the output voltage of a voltage regulator
- Trim the resistance in Wheatstone bridge circuits
- Control the gain, characteristic frequency, and Q-factor in filter circuits
- Set the scale factor and zero point in sensor signal conditioning circuits
- Vary the frequency and duty cycle of timer ICs
- Vary the DC biasing of a pin diode attenuator in RF circuits
- Provide a control variable (I, V, or R) in feedback circuits

System Level Applications

- Adjust the contrast in LCD displays
- Control the power level of LED transmitters in communication systems
- Set and regulate the DC biasing point in an RF power amplifier in wireless systems
- Control the gain in audio and home entertainment systems
- Provide the variable DC bias for tuners in RF wireless systems
- Set the operating points in temperature control systems
- Control the operating point for sensors in industrial systems
- Trim offset and gain errors in artificial intelligent systems

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	V_{CC} LIMITS (V)	POTENTIOMETER ORGANIZATION (kΩ)	TEMP RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
X9111TV14IZ	X9111TV ZI	5 ±10%	100	-40 to +85	14 Ld TSSOP (4.4mm)	M14.173
X9111TV14Z	X9111TV Z			0 to +70	14 Ld TSSOP (4.4mm)	M14.173
X9111TV14Z-2.7	X9111TV ZF	2.7 to 5.5		0 to +70	14 Ld TSSOP (4.4mm)	M14.173
X9111TV14IZ-2.7 (Note 1)	X9111TV ZG			-40 to +85	14 Ld TSSOP (4.4mm)	M14.173

NOTES:

1. Add “T1” suffix for 2.5k unit tape and reel option.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see product information page for X9111. For more information on MSL, see tech brief TB363.

Detailed Functional Diagram

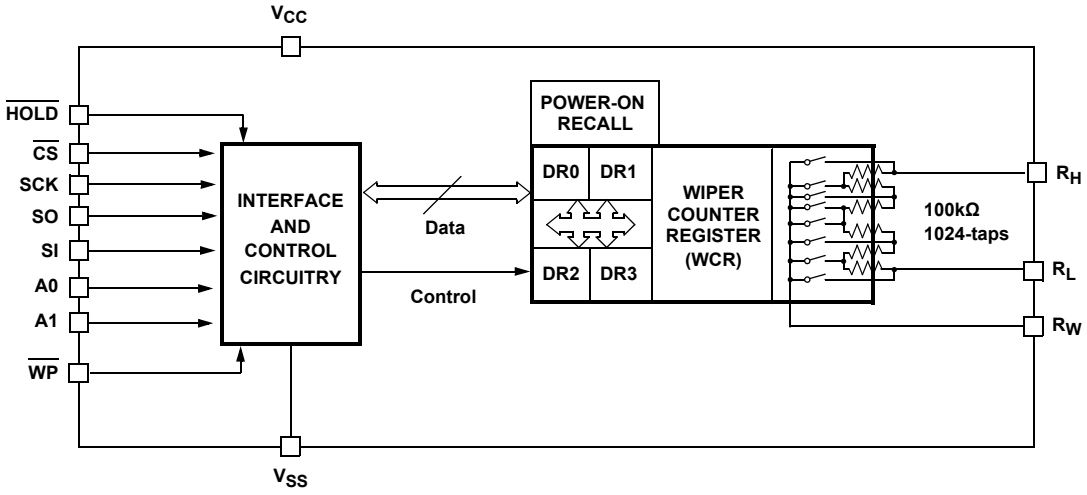
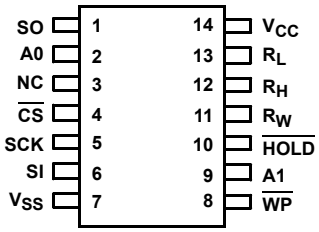


FIGURE 2. DETAILED FUNCTIONAL DIAGRAM

Pin Configuration

X9111
(14 LD TSSOP)
TOP VIEW



Pin Descriptions

PIN (TSSOP)	SYMBOL	FUNCTION
1	SO	Serial Data Output
2	A0	Device Address
3	NC	No Connect
4	$\overline{CS}$	Chip Select
5	SCK	Serial Clock
6	SI	Serial Data Input
7	V_{SS}	System Ground
8	$\overline{WP}$	Hardware Write Protect
9	A1	Device Address
10	$\overline{HOLD}$	Device Select. Pause the Serial Bus
11	R_W	Wiper Terminal of the Potentiometer
12	R_H	High Terminal of the Potentiometer
13	R_L	Low Terminal of the Potentiometer
14	V_{CC}	System Supply Voltage

Bus Interface Pins

SERIAL OUTPUT (SO)

SO is a serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

SERIAL INPUT (SI)

SI is the serial data input pin. All opcodes, byte addresses and data to be written to the pots and pot registers are input on this pin. Data is latched by the rising edge of the serial clock.

SERIAL CLOCK (SCK)

The SCK input is used to clock data into and out of the X9111.

HOLD ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

DEVICE ADDRESS (A_0, A_1)

The address inputs are used to set the 8-bit slave address. A match in the slave address serial data stream must be made with the address input (A1–A0) in order to initiate communication with the X9111.

CHIP SELECT ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X9111 is deselected and the SO pin is at high impedance, and (unless an internal write cycle is underway) the device will be in the standby state. $\overline{CS}$ LOW enables the X9111, placing it in the active power mode. It should be noted that after a power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

HARDWARE WRITE PROTECT INPUT ($\overline{WP}$)

The $\overline{WP}$ pin when LOW prevents nonvolatile writes to the Data Registers.

Potentiometer Pins

R_H, R_L

The R_H and R_L pins are equivalent to the terminal connections on a mechanical potentiometer.

R_W

The wiper pin is equivalent to the wiper terminal of a mechanical potentiometer.

Bias Supply Pins

SYSTEM SUPPLY VOLTAGE (V_{CC}) AND SUPPLY GROUND (V_{SS})

The V_{CC} pin is the system supply voltage. The V_{SS} pin is the system ground.

Other Pins

NO CONNECT (NC)

Pin should be left open. This pin is used for Intersil manufacturing and test purposes.

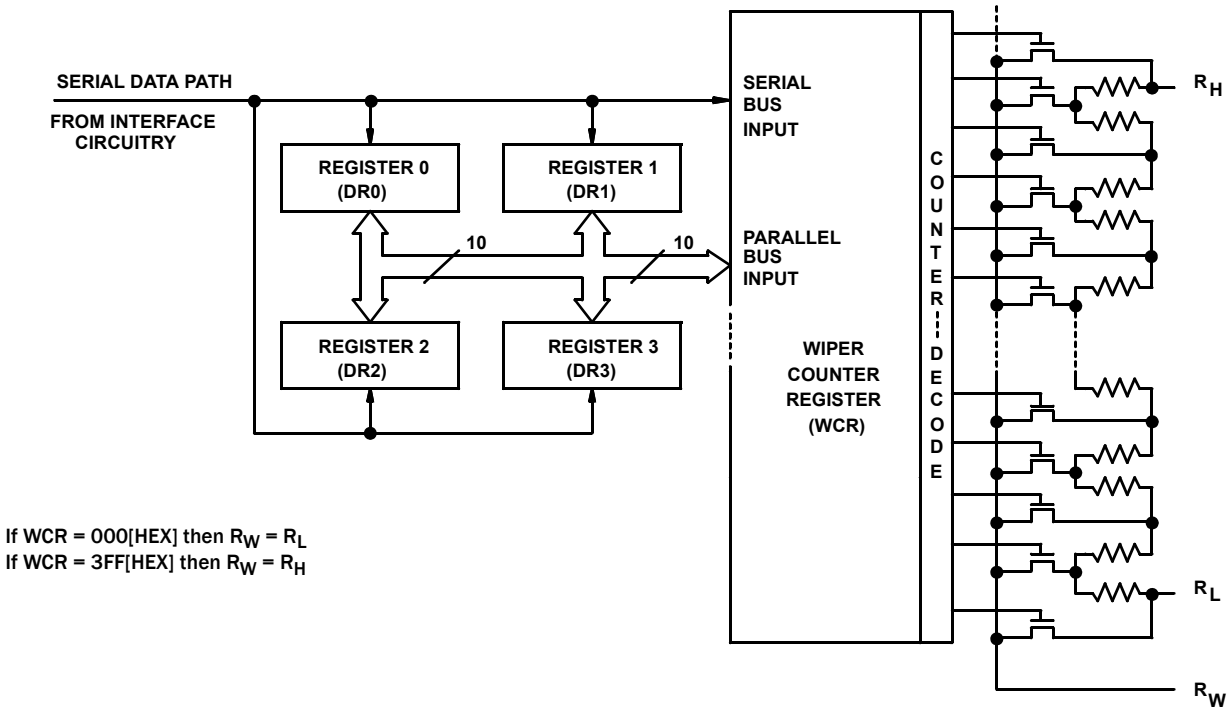


FIGURE 3. DETAILED POTENTIOMETER BLOCK DIAGRAM

Principles of Operation

Device Description

SERIAL INTERFACE

The X9111 supports the SPI interface hardware conventions. The device is accessed via the SI input with data clocked-in on the rising SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{WP}$ pins must be HIGH during the entire operation.

The SO and SI pins can be connected together, since they have three state outputs. This can help to reduce system pin count.

ARRAY DESCRIPTION

The X9111 is comprised of a resistor array (see Figure 3). The array contains the equivalent of 1,023 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L inputs).

At both ends of each array and between each resistor segment is a CMOS switch connected to the wiper (R_W) output. Within the individual array, only one switch may be turned on at a time.

These switches are controlled by a Wiper Counter Register (WCR). The 10-bits of the WCR (WCR[9:0]) are decoded to select, and enable, one of 1024 switches.

WIPER COUNTER REGISTER (WCR)

The X9111 contains a Wiper Counter Register (see Table 1 on page 5) for the XDCP potentiometer. The WCR is equivalent to a serial-in, parallel-out register/counter with its outputs decoded to select one of 1024 switches along its resistor array. The contents of the WCR can be altered in one of three ways:

1. It may be written directly by the host via the write Wiper Counter Register instruction (serial load).
2. It may be written indirectly by transferring the contents of one of four associated Data Registers via the XFR Data Register.
3. It is loaded with the contents of its Data Register zero (DR0) upon power-up.

The Wiper Counter Register is a volatile register, meaning its contents are lost when the X9111 is powered-down. Although the register is automatically loaded with the value in R0 upon power-up, this may be different from the value present at power-down. Power-up guidelines are recommended to ensure proper loadings of the R0 value into the WCR.

DATA REGISTERS (DR3 TO DR0)

The potentiometer has four 10-bit nonvolatile Data Registers. These can be read or written directly by the host. Data can also be transferred between any of the four Data Registers and the Wiper Counter Register. All operations changing data in one of the Data Registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as regular memory locations for system parameters or user preference data.

A DR[9:0] is used to store one of the 1024 wiper positions (0 ~1023). See Table 2 on page 5

STATUS REGISTER (SR)

This 1-bit status register is used to store the system status (see Table 4).

WIP: Write In Progress status bit, read only.

- When WIP = 1, indicates that high-voltage write cycle is in progress.
- When WIP = 0, indicates that no high-voltage write cycle is in progress.

Device Instructions

Identification Byte (ID and A)

The first byte sent to the X9111 from the host, following a $\overline{CS}$ going HIGH to LOW, is called the Identification Byte. The most significant four bits of the slave address are a device type identifier. The ID[3:0] bits is the device ID for the X9111; this is fixed as 0101[B] (refer to Table 5 on page 6).

The A1–A0 bits in the ID byte are the internal slave address. The physical device address is defined by the state of the A1–A0 input pins. The slave address is externally specified by the user. The X9111 compares the serial data stream with the address input state; a successful compare of the address bits is required for the X9111 to successfully continue the command sequence. Only the device whose slave address matches the incoming device address sent by the master executes the instruction. The A1–A0 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}. The R/$\overline{W}$ bit is used to set the device to either read or write mode.

Instruction Byte and Register Selection

The next byte sent to the X9111 contains the instruction and register pointer information. The three most significant bits are used provide the instruction opcode (I[2:0]). The RB and RA bits point to one of the four registers. The format is shown in Table 5.

TABLE 1. WIPER LATCH, WL (10-BIT), WCR9–WCR0: USED TO STORE THE CURRENT WIPER POSITION (VOLATILE, V)

WCR9	WCR8	WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0
V	V	V	V	V	V	V	V	V	V
(MSB)									(LSB)

TABLE 2. DATA REGISTER, DR (10-BIT), BIT 9–BIT 0: USED TO STORE WIPER POSITIONS OR DATA (NONVOLATILE, NV)

BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NV	NV	NV	NV	NV	NV	NV	NV	NV	NV
MSB									LSB

TABLE 3. STATUS REGISTER, SR (1-BIT)

WIP
(LSB)

TABLE 4. IDENTIFICATION BYTE FORMAT

	DEVICE TYPE IDENTIFIER				INTERNAL SLAVE ADDRESS		READ OR WRITE BIT
ID3	ID2	ID1	ID0	0	A1	A0	R/$\overline{W}$
0	1	0	1				
(MSB)							(LSB)

TABLE 5. INSTRUCTION BYTE FORMAT

INSTRUCTION OPCODE				REGISTER SELECTION			
I2	I1	I0	0	RB	RA	0	0
(MSB)							(LSB)

RB	RA	REGISTER
0	0	DR0
0	1	DR1
1	0	DR2
1	1	DR3

Five of the seven instructions are four bytes in length. These instructions are:

- **Read Wiper Counter Register** – read the current wiper position of the selected pot.
- **Write Wiper Counter Register** – change current wiper position of the selected pot.
- **Read Data Register** – read the contents of the selected data register.
- **Write Data Register** – write a new value to the selected data register.
- **Read Status** – This command returns the contents of the WIP bit, which indicates if the internal write cycle is in progress.

The basic sequence of the four byte instructions is illustrated in Figure 5 on page 7. These four-byte instructions exchange data between the WCR and one of the Data Registers. A transfer from a Data Register to a WCR is essentially a write to a static RAM, with the static RAM controlling the wiper position. The response of the wiper to this action will be delayed by tWRL. A transfer from the WCR (current wiper position), to a Data Register is a write to nonvolatile memory and takes a minimum of tWR to complete. The transfer can occur between the potentiometer and one of its associated registers. The Read Status Register instruction is the only unique format (see Figure 6 on page 7).

Two instructions require a two-byte sequence to complete (see Figure 4 on page 7). These instructions transfer data between the host and the X9111, either between the host and one of the Data Registers, or directly between the host and the Wiper Counter Register. These instructions are:

- **XFR Data Register to Wiper Counter Register** – This transfers the contents of one specified Data Register to the associated Wiper Counter Register.
- **XFR Wiper Counter Register to Data Register** – This transfers the contents of the specified Wiper Counter Register to the specified associated Data Register.

See Instruction format for more details.

Write in Process (WIP bit)

The contents of the Data Registers are saved to nonvolatile memory when the $\overline{CS}$ pin goes from LOW to HIGH after a complete write sequence is received by the device. The progress of this internal write operation can be monitored by a Write In Process bit (WIP). The WIP bit is read with a Read Status command (see Figure 6 on page 7).

Power-Up and Power-Down Requirements

There are no restrictions on the power-up condition of V_{CC} and the voltages applied to the potentiometer pins provided that the V_{CC} is always more positive than or equal to the voltages at R_H, R_L, and R_W, i.e., $V_{CC} \geq R_H, R_L, R_W$. There are no restrictions on the power-down condition. However, the datasheet parameters for the DCP do not apply until 1 millisecond after V_{CC} reaches its final value.

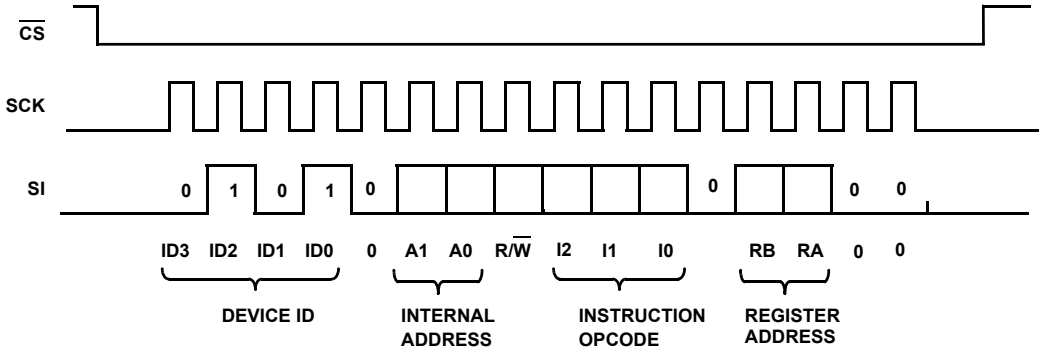


FIGURE 4. TWO-BYTE INSTRUCTION SEQUENCE

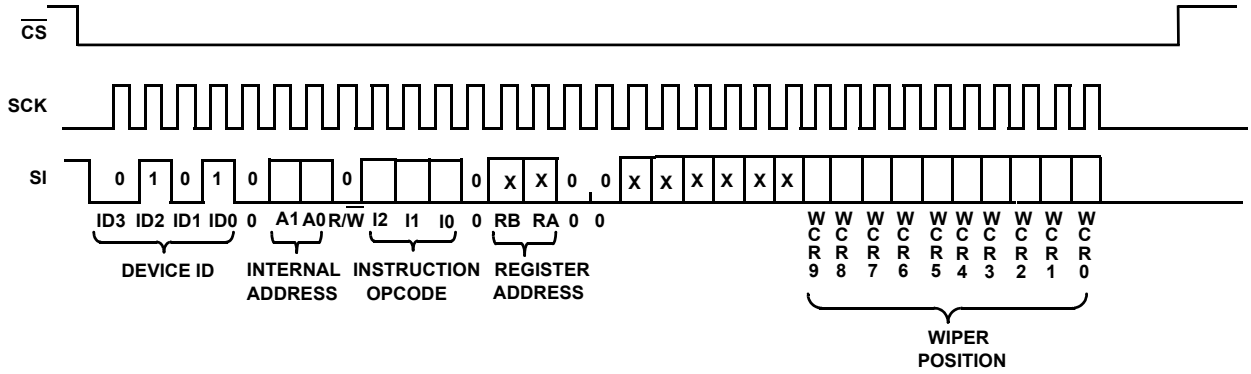


FIGURE 5. FOUR-BYTE INSTRUCTION SEQUENCE (WRITE OR READ FOR WCR OR DATA REGISTERS)

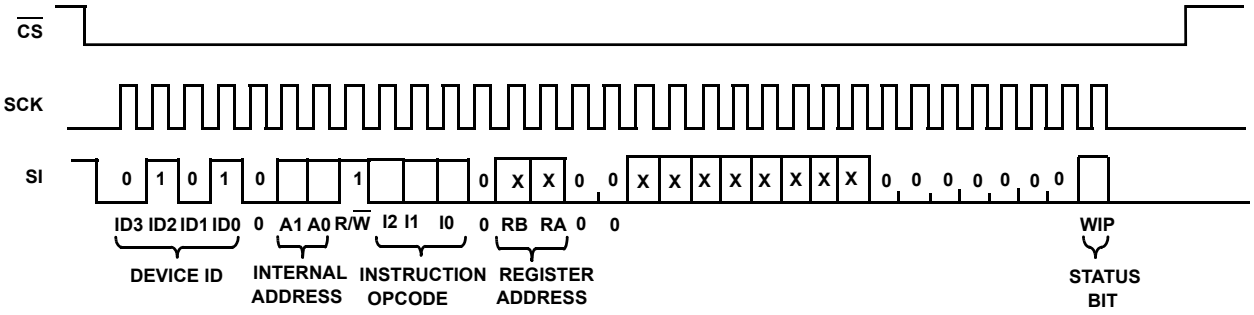


FIGURE 6. FOUR-BYTE INSTRUCTION SEQUENCE (READ STATUS REGISTERS)

TABLE 6. INSTRUCTION SET

INSTRUCTION		INSTRUCTION SET								OPERATION
	R/$\overline{W}$	I_3	I_2	I_1	0	RB	RA	0	0	
Read Wiper Counter Register	1	1	0	0	0	0	0	0	0	Read the contents of the Wiper Counter Register
Write Wiper Counter Register	0	1	0	1	0	0	0	0	0	Write new value to the Wiper Counter Register
Read Data Register	1	1	0	1	0	1/0	1/0	0	0	Read the contents of the Data Register pointed to RB-RA
Write Data Register	0	1	1	0	0	1/0	1/0	0	0	Write new value to the Data Register pointed to RB-RA
XFR Data Register to Wiper Counter Register	1	1	1	0	0	1/0	1/0	0	0	Transfer the contents of the Data Register pointed to by RB-RA to the Wiper Counter Register
XFR Wiper Counter Register to Data Register	0	1	1	1	0	1/0	1/0	0	0	Transfer the contents of the Wiper Counter Register to the Data Register pointed to by RB-RA
Read Status (WIP Bit)	1	0	1	0	0	0	0	0	1	Read the status of the internal write cycle, by checking the WIP bit (read status register).

NOTE: 1/0 = data is one or zero

Instruction Format

Read Wiper Counter Register (WCR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				Register Addresses				Wiper Position (Sent by X9111 on SO)								Wiper Position (sent by X9111 on SO)								$\overline{CS}$ Rising Edge
	0	1	0	1	0	A1	A0	R/$\overline{W}$ = 1	1	0	0	0	0	0	0	0	X	X	X	X	X	X	WCR9	WCR8	WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0	

Write Wiper Counter Register (WCR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				Register Addresses				Wiper Position (Sent by Master on SI)								Wiper Position (Sent by Master on SI)								$\overline{CS}$ Rising Edge
	0	1	0	1	0	A1	A0	R/$\overline{W}$ = 0	1	0	1	0	0	0	0	0	X	X	X	X	X	X	WCR9	WCR8	WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0	

Read Data Register (DR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				Register Addresses				Wiper Position (Sent by X9111 on SO)								Wiper Position (sent by X9111 on SO)								$\overline{CS}$ Rising Edge
	0	1	0	1	0	A1	A0	R/$\overline{W}$ = 1	1	0	1	0	RB	RA	0	0	X	X	X	X	X	X	WCR9	WCR8	WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0	

Write Data Register (DR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				Register Addresses				Wiper Position or Data (Sent by Master on SI)								Wiper Position or Data (Sent by Master on SI)								$\overline{CS}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	A1	A0	R/$\overline{W}$ = 0	1	1	0	0	RB	RA	0	0	X	X	X	X	X	X	WCR9	WCR8	WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0		

Transfer Data Register (DR) to Wiper Counter Register (WCR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				Register Addresses				$\overline{CS}$ Rising Edge
	0	1	0	1	0	A1	A0	R/$\overline{W}$ = 1	1	1	0	0	RB	RA	0	0	

Transfer Wiper Counter Register (WCR) to Data Register (DR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				Register Addresses				$\overline{CS}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	A1	A0	R/$\overline{W}$ = 0	1	1	1	0	RB	RA	0	0		

Read Status Register (SR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				Register Addresses				Status Data (Sent by Slave on SO)								Status Data (Sent by Slave on SO)								$\overline{CS}$ Rising Edge
	0	1	0	1	0	A1	A0	R/$\overline{W}$ = 1	0	1	0	0	0	0	0	1	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	WIP	

NOTES:

4. “A0 and A1”: stand for the device address sent by the master.
5. WCRx refers to wiper position data in the Wiper Counter Register.
6. “X”: Don’t Care.

Absolute Maximum Ratings

Temperature under bias . . . . . -65°C to +135°C
Storage temperature . . . . . -65°C to +150°C
Voltage on SCK any address input
with respect to V_{SS} . . . . . -1V to +7V
$\Delta V = | (VH–VL) |$ . . . . . 0V to V_{CC}
Pb-Free Reflow Profile . . . . . see TB493
I_W (10s) . . . . . ±6mA

Recommended Operating Conditions

Temperature Range
Commercial . . . . . 0°C to +70°C
Industrial . . . . . -40°C to +85°C
Supply Voltage (V_{CC}) Limits
X9111 . . . . . 5V ±10%
X9111-2.7 . . . . . 2.7V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Analog Characteristics

Over recommended industrial operation conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{TOTAL}	End to End Resistance			100		kΩ
	End to End Resistance Tolerance				±20	%
	Power Rating	+25°C, each pot			50	mW
I_W	Wiper Current				±3	mA
R_W	Wiper Resistance	Wiper Current = ±50µA, V_{CC} = 5V		40	110	Ω
		Wiper Current = ±50µA, V_{CC} = 3V		150	300	Ω
V_{TERM}	Voltage on any R_H or R_L Pin	V_{SS} = 0V	V_{SS}		V_{CC}	V
	Noise	Ref: 1V		-120		dBV
	Resolution			1.6		%
	Absolute Linearity (Note 7)	$R_{w(n)(actual)} - R_{w(n)(expected)}$, where n = 8 to 1006			±1	MI (Note 9)
		$R_{w(n)(actual)} - R_{w(n)(expected)}$ (Note 10)		±1.5	±2.0	MI (Note 9)
	Relative Linearity (Note 8)	$R_{w(m+1)} - [R_{w(m)} + MI]$, where m = 8 to 1006			±0.5	MI (Note 9)
		$R_{w(m+1)} - [R_{w(m)} + MI]$ (Note 10)		±0.5	±1.0	MI (Note 9)
	Temperature Coefficient of R_{TOTAL}			±300		ppm/°C
	Ratiometric Temperature Coefficient				20	ppm/°C
$C_H/C_L/C_W$	Potentiometer Capacitancies	See Macro model		10/10/25		pF

NOTES:

7. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
8. Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
9. MI = RTOT/1023 or $(R_H - R_L)/1023$, single pot
10. n = 0, 1, 2, ...,1023; m =0, 1, 2, ..., 1022.
11. ESD Rating on RH, RL, RW pins is 1.5kV (HBM, 1.0µA leakage maximum), ESD rating on all other pins is 2.0kV.

DC Operating Characteristics

Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CC1}	V_{CC} Supply Current (Active)	f_{SCK} = 2.5 MHz, SO = Open, V_{CC} = 5.5V Other inputs = V_{SS}			400	µA
I_{CC2}	V_{CC} Supply Current (Nonvolatile Write)	f_{SCK} = 2.5MHz, SO = Open, V_{CC} = 5.5V Other inputs = V_{SS}		1	5	mA
I_{SB}	V_{CC} Current (Standby)	SCK = SI = V_{SS}, Address = V_{SS}, $\overline{CS}$ = V_{CC} = 5.5V			3	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{SS} to V_{CC}			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}			10	µA
V_{IH}	Input HIGH Voltage		V_{CC} x 0.7		V_{CC} + 1	V
V_{IL}	Input LOW Voltage		-1		V_{CC} x 0.3	V
V_{OL}	Output LOW Voltage	I_{OL} = 3mA			0.4	V
V_{OL}	Output LOW Voltage	I_{OH} = -1mA, V_{CC} ≥ +3V	V_{CC} - 0.8			V
V_{OL}	Output LOW Voltage	I_{OH} = -0.4mA, V_{CC} ≤ +3V	V_{CC} - 0.4			V

Endurance And Data Retention

PARAMETER	MIN	UNITS
Minimum Endurance	100,000	Data changes per bit per register
Data Retention	100	Years

Capacitance

SYMBOL	TEST	TEST CONDITIONS	MAX	UNIT
$C_{IN/OUT}$ (Note 12)	Input/Output Capacitance (SI)	V_{OUT} = 0V	8	pF
C_{OUT} (Note 12)	Output Capacitance (SO)	V_{OUT} = 0V	8	pF
C_{IN} (Note 12)	Input Capacitance (A0, $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$, and SCK)	V_{IN} = 0V	6	pF

Power-Up Timing

SYMBOL	PARAMETER	MIN	MAX	UNIT
$t_r V_{CC}$ (Note 12)	V_{CC} Power-Up Rate	0.2	50	V/ms
t_{PUR} (Note 13)	Power-Up to Initiation of Read Operation		1	ms
t_{PUW} (Note 13)	Power-Up to Initiation of Write Operation		50	ms

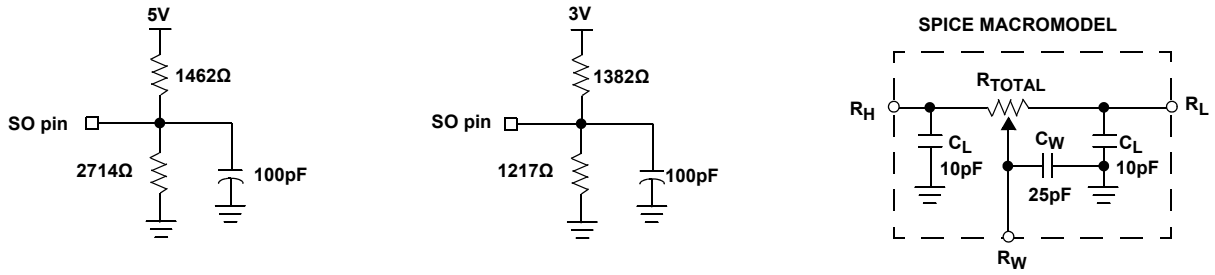
NOTES:

12. This parameter is not 100% tested.
13. t_{PUR} and t_{PUW} are the delays required from the time the (last) power supply (V_{CC}-) is stable until the specific instruction can be issued. These parameters are not 100% tested.

AC Test Conditions

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing level	V_{CC} x 0.5

Equivalent AC Load Circuit



AC Timing

SYMBOL	PARAMETER	MIN	MAX	UNIT
f_{SCK}	SSI/SPI Clock Frequency		2.5	MHz
t_{CYC}	SSI/SPI Clock Cycle Time	400		ns
t_{WH}	SSI/SPI Clock High Time	150		ns
t_{WL}	SSI/SPI Clock Low Time	150		ns
t_{LEAD}	Lead Time	150		ns
t_{LAG}	Lag Time	150		ns
t_{SU}	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ Input Set-Up Time	50		ns
t_H	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ Input Hold Time	50		ns
t_{RI}	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ Input Rise Time		50	ns
t_{FI}	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ Input Fall Time		50	ns
t_{DIS}	SO Output Disable Time	0	500	ns
t_V	SO Output Valid Time		100	ns
t_{HO}	SO Output Hold Time	0		ns
t_{RO}	SO Output Rise Time		50	ns
t_{FO}	SO Output Fall Time		50	ns
t_{HOLD}	$\overline{HOLD}$ Time	400		ns
t_{HSU}	$\overline{HOLD}$ Set-Up Time	50		ns
t_{HH}	$\overline{HOLD}$ Hold Time	50		ns
t_{HZ}	$\overline{HOLD}$ Low to Output in High-Z		100	ns
t_{LZ}	$\overline{HOLD}$ High to Output in Low-Z		100	ns
T_I	Noise Suppression Time Constant at SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ Inputs		20	ns
t_{CS}	$\overline{CS}$ Deselect Time	100		ns
t_{WPASU}	$\overline{WP}$, A0, A1 Set-Up Time	0		ns
t_{WPAH}	$\overline{WP}$, A0, A1 Hold Time	0		ns

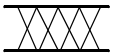
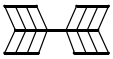
High-Voltage Write Cycle Timing

SYMBOL	PARAMETER	TYP	MAX	UNIT
t_{WR}	High-Voltage Write Cycle Time (Store Instructions)	5	10	ms

XDCP Timing

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{WRPO}	Wiper Response Time after the Third (Last) Power Supply is Stable	5	10	µs
t_{WRL}	Wiper Response Time after Instruction Issued (All Load Instructions)	5	10	µs

Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Timing Diagrams

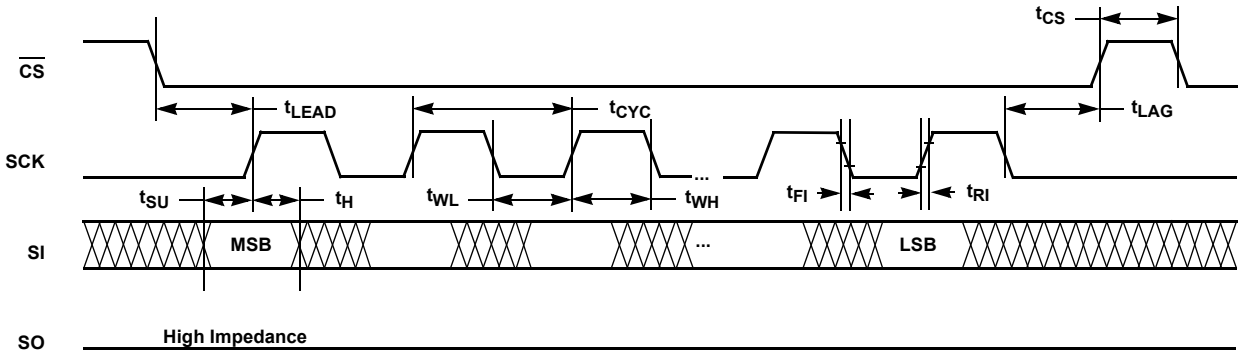


FIGURE 7. INPUT TIMING

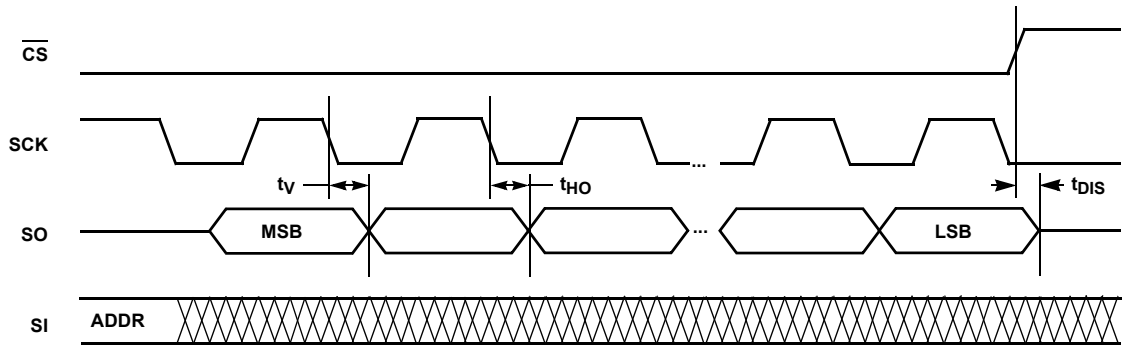


FIGURE 8. OUTPUT TIMING

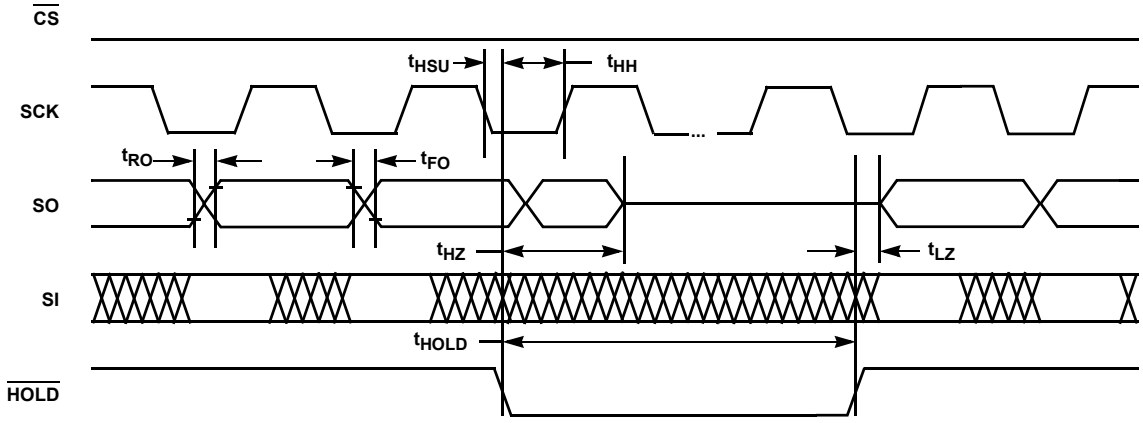


FIGURE 9. HOLD TIMING

Timing Diagrams (Continued)

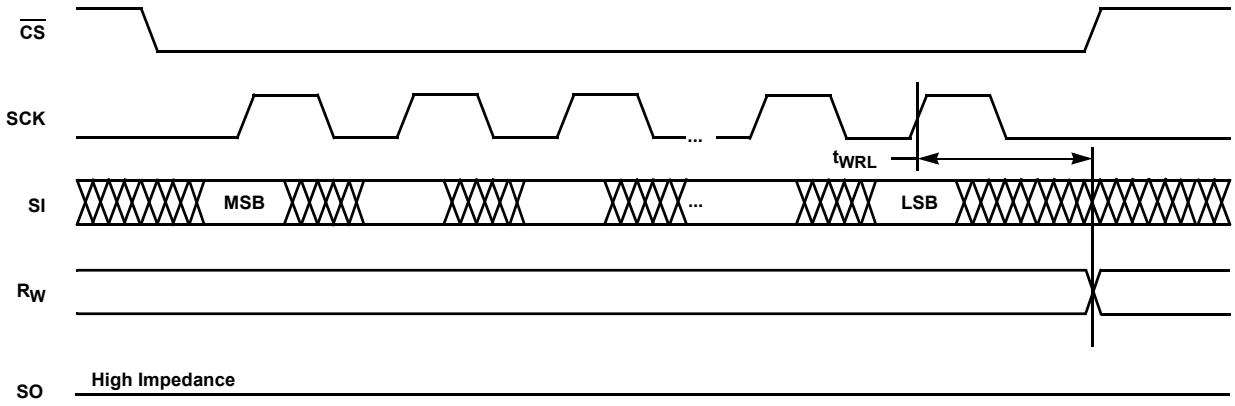


FIGURE 10. XDCP TIMING (FOR ALL LOAD INSTRUCTIONS)

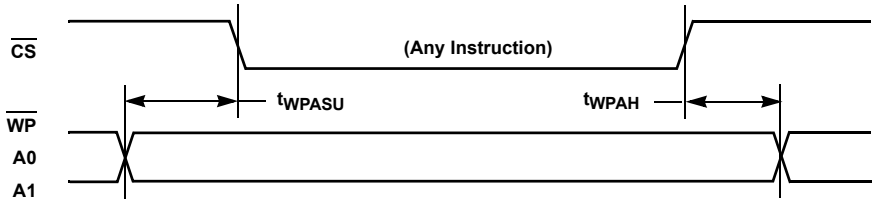


FIGURE 11. WRITE PROTECT AND DEVICE ADDRESS PINS TIMING

Applications information

Basic Configurations of Electronic Potentiometers

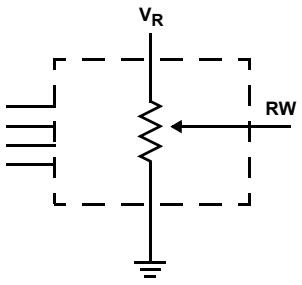


FIGURE 12. THREE-TERMINAL POTENTIOMETER; VARIABLE VOLTAGE DIVIDER

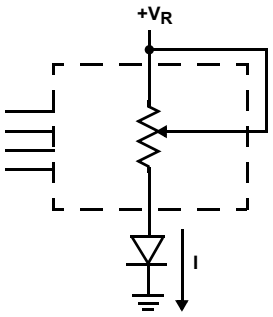
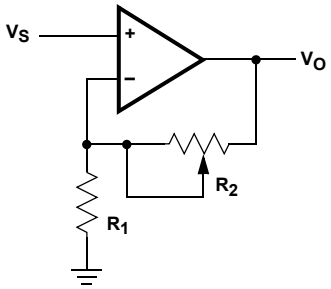


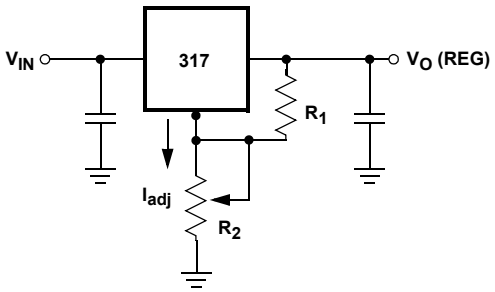
FIGURE 13. TWO-TERMINAL VARIABLE RESISTOR; VARIABLE CURRENT

Application Circuits



$V_O = (1+R_2/R_1)V_S$

FIGURE 14. NONINVERTING AMPLIFIER



V_O (REG) = 1.25V $(1+R_2/R_1)+I_{adj}$ R_2

FIGURE 15. VOLTAGE REGULATOR

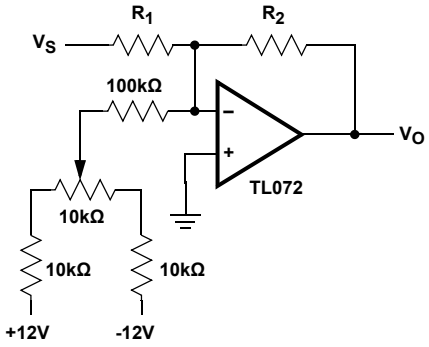
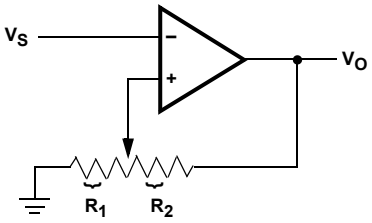
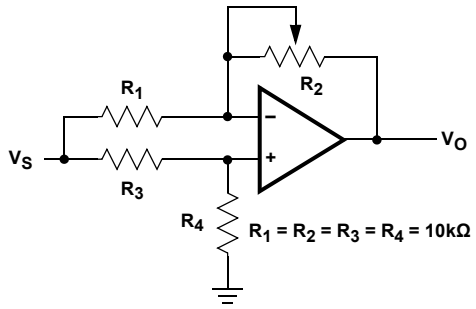


FIGURE 16. OFFSET VOLTAGE ADJUSTMENT



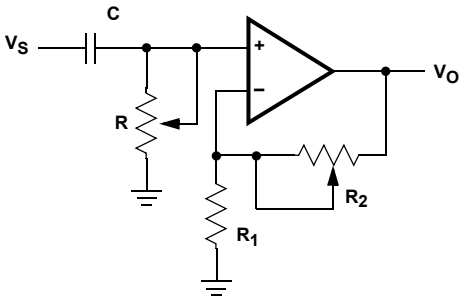
$V_{UL} = \{R_1/(R_1+R_2)\}\ V_O(max)$
$R_{LL} = \{R_1/(R_1+R_2)\}\ V_O(min)$

FIGURE 17. COMPARATOR WITH HYSTERISIS



$V_O = G\ V_S$
$-1/2 \leq G \leq +1/2$

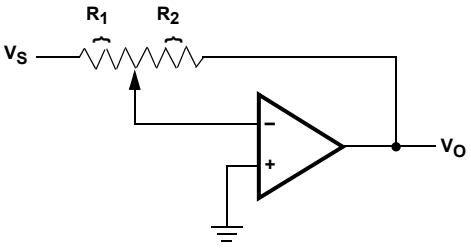
FIGURE 18. ATTENUATOR



$GO = 1 + R_2/R_1$
$fc = 1/(2\pi RC)$

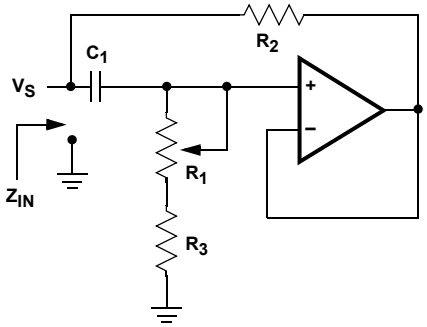
FIGURE 19. FILTER

Application Circuits (Continued)



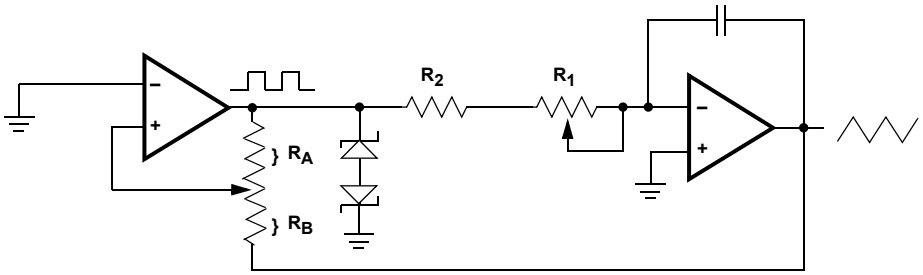
$V_O = G\ V_S$
$G = - R_2/R_1$

FIGURE 20. INVERTING AMPLIFIER



$Z_{IN} = R_2 + s\ R_2\ (R_1 + R_3)\ C_1 = R_2 + s\ Leq$
$(R_1 + R_3) >> R_2$

FIGURE 21. EQUIVALENT L-R CIRCUIT



FREQUENCY $\propto R_1, R_2, C$
AMPLITUDE $\propto R_A, R_B$

FIGURE 22. FUNCTION GENERATOR

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
October 13, 2016	FN8159.5	Updated entire datasheet applying Intersil's new standards. Updated the Ordering Information table on page 2. Updated Notes 1 and 2. Added Note 3. In "AC Timing" on page 12, changed f_{SCK} maximum specification from "2.0" to "2.5". Added Revision History and About Intersil sections. Updated Package Outline Drawing M14.173 to the latest revision changes are as follows: -Updated drawing to remove table and added land pattern

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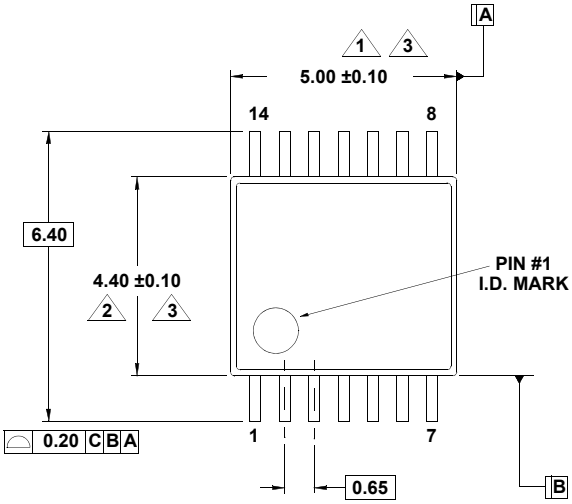
Package Outline Drawing

For the most recent package outline drawing, see M14.173.

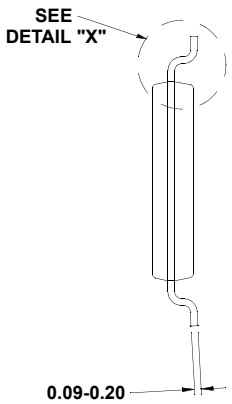
M14.173

14 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)

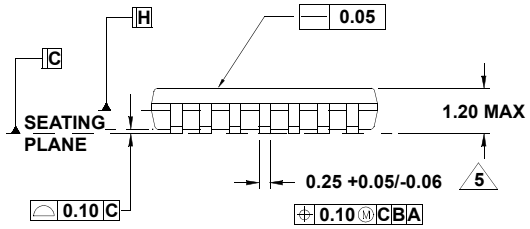
Rev 3, 10/09



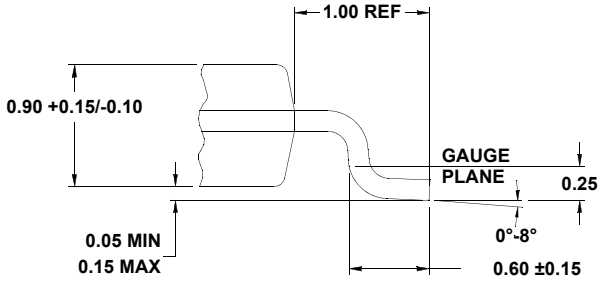
TOP VIEW



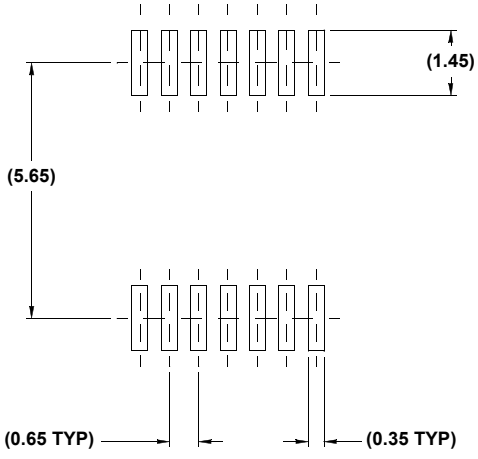
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153, variation AB-1.