Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

XC17V00 Series Configuration PROMs

DS073 (v1.11) June 7, 2007 **Product Specification**

Features

- One-time programmable (OTP) read-only memory designed to store configuration bitstreams of Xilinx FPGA devices
- Simple interface to the FPGA
- Cascadable for storing longer or multiple bitstreams
- Programmable reset polarity (active High or active Low) for compatibility with different FPGA solutions
- Low-power CMOS floating-gate process
- 3.3V supply voltage
- Guaranteed 20 year life data retention
- Available in compact plastic packages: VQ44, PC44, PC20, VO8, and SO20
- Programming support by leading programmer manufacturers.
- Design support using the ISE™ Foundation™ and ISE WebPACK™ software.
- Dual configuration modes for the XC17V16 and XC17V08 devices
  - Serial slow/fast configuration (up to 20 Mb/s)
  - Parallel (up to 160 Mb/s at 20 MHz)

Description

Xilinx introduces the high-density XC17V00 family of configuration PROMs which provide an easy-to-use, cost-effective method for storing large Xilinx FPGA configuration bitstreams. Initial devices in the 3.3V family are available in 16 Mb, 8 Mb, 4 Mb, 2 Mb, and 1 Mb densities. See Figure 1 and Figure 2 for simplified block diagrams of the XC17V00 family.

The XC17V00 PROM can configure a Xilinx FPGA using the FPGA serial configuration mode interface. When the FPGA is in Master Serial mode, it generates a configuration clock that drives the PROM. A short access time after the rising clock edge, data appears on the PROM DATA output pin that is connected to the FPGA DIN pin. The FPGA generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the PROM. When the FPGA is in Slave Serial mode, the PROM and the FPGA must both be clocked by an incoming signal.

The XC17V08 and XC17V16 PROM can optionally configure a Xilinx FPGA using the FPGA Parallel (SelectMAP) configuration mode interface. When the FPGA is in Master SelectMAP mode, the FPGA generates the configuration clock that drives the PROM.

When the FPGA is in Slave SelectMAP mode, an external, free-running oscillator generates the configuration clock that drives the PROM and the FPGA. After the rising configuration clock (CCLK) edge, data is available on the PROMs DATA (D0-D7) pins. The data is clocked into the FPGA on the following rising edge of the CCLK (Figure 3).

Multiple PROMs can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the DATA outputs of all PROMs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family.

For device programming, either the Xilinx ISE Foundation or ISE WebPACK software compiles the FPGA design file into a standard Hex format, which is then transferred to most commercial PROM programmers.

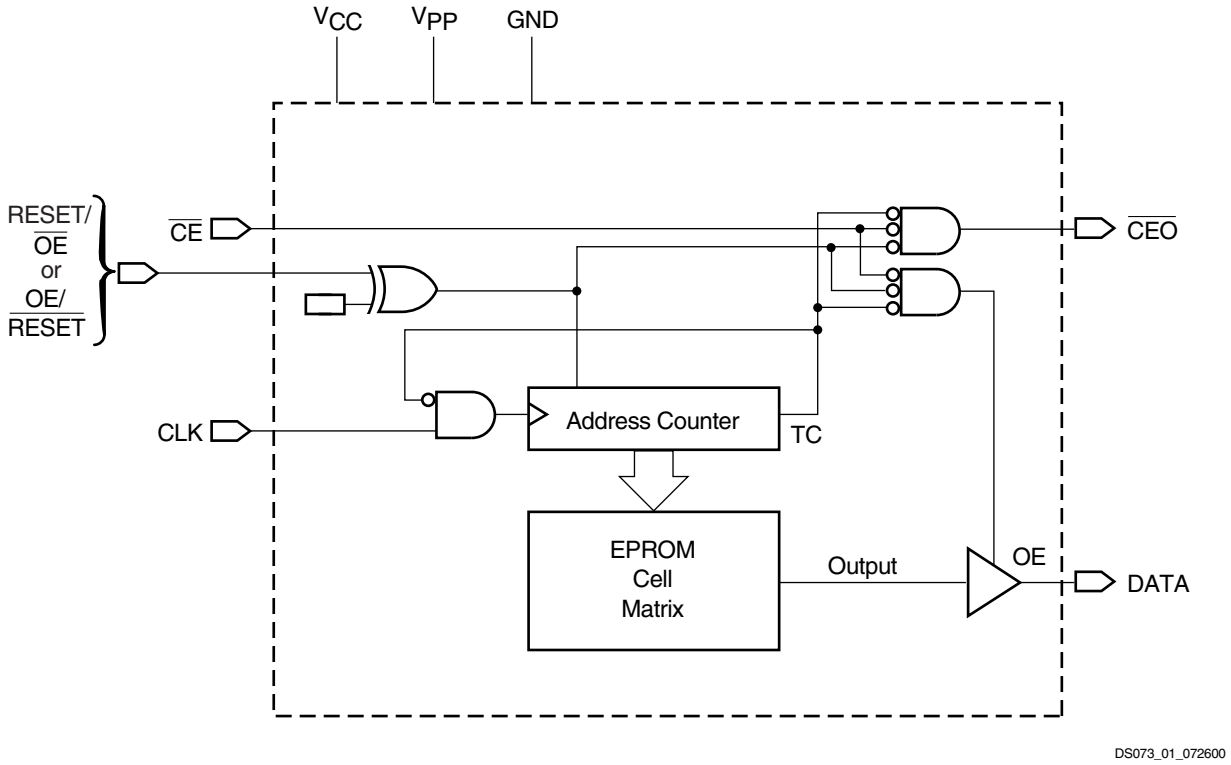


Figure 1: **Simplified Block Diagram for XC17V04, XC17V02, and XC17V01 (does not show programming circuit)**

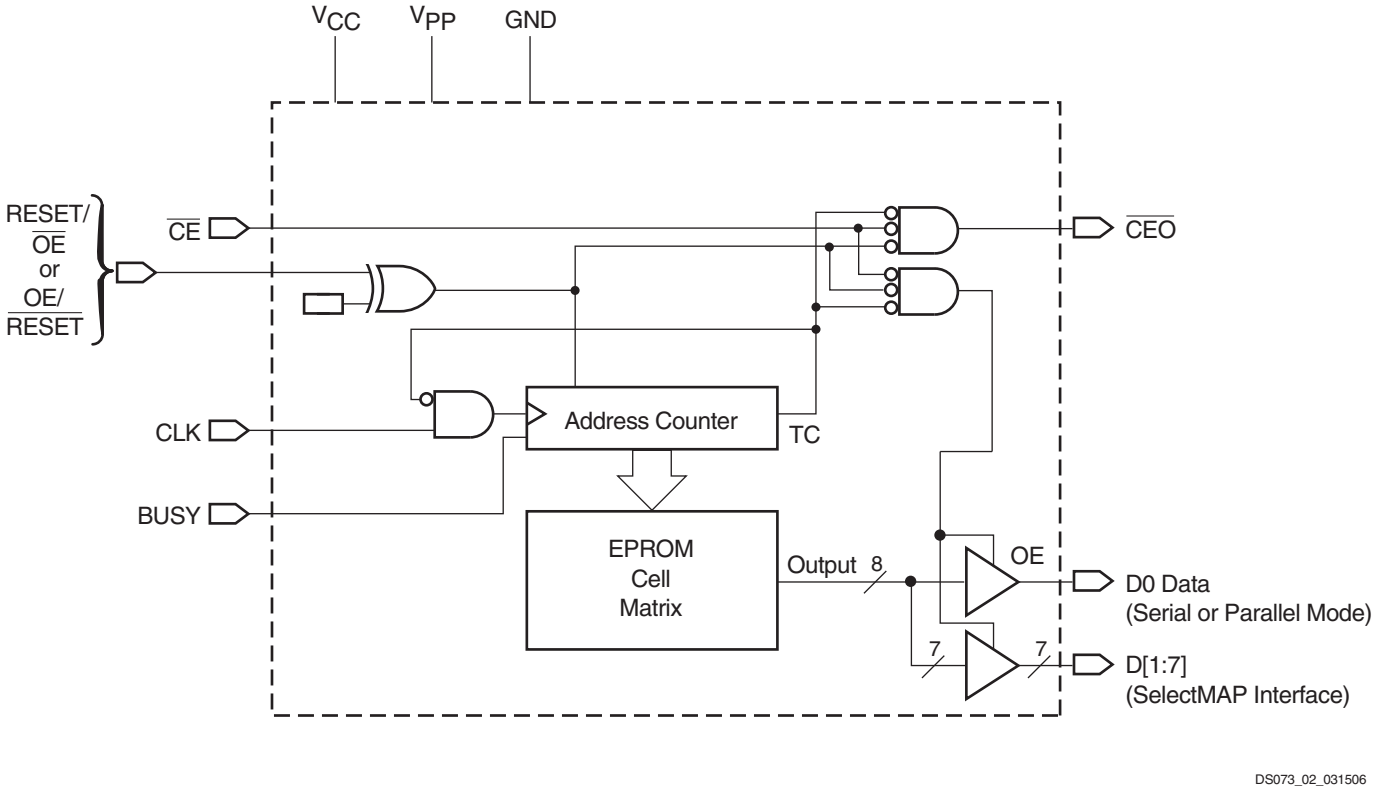


Figure 2: **Simplified Block Diagram for XC17V16 and XC17V08 (does not show programming circuit)**

Pin Description

DATA[0:7]

The array data value corresponding to the internal address counter location is output on enabled DATA[0-7] output pin(s) when $\overline{CE}$ is active, $\overline{OE}$ is active, and the internal address counter has not incremented beyond its Terminal Count (TC) value. Otherwise, all data pins are in a high impedance state when $\overline{CE}$ is inactive, $\overline{OE}$ is inactive, or the internal address counter has incremented beyond its Terminal Count (TC) value.

The XC17V01, XC17V02, and XC17V04 have only the single DATA output pin for connection to the FPGA serial configuration data input pin.

The XC17V08 and XC17V16 have the D[0-7] output pins. During device programming, the XC17V08 and XC17V16 must be programmed for use in either serial output mode or parallel output mode. For XC17V08 and XC17V16 devices programmed to serial output mode, only the D0 pin is enabled for data output to the Virtex series FPGA serial configuration data input pin. In serial mode, the D[1-7] output pins remain in high impedance state and may be unconnected. For XC17V08 and XC17V16 devices programmed to parallel output mode, all D[0-7] output pins are enabled for byte-wide data output to the FPGA SelectMAP configuration data input pins.

The DATA/D0 pin is a bidirectional I/O during device programming.

CLK

Each rising edge on the CLK input increments the internal address counter, when $\overline{CE}$ is active, $\overline{OE}$ is active, the internal address counter has not incremented past its Terminal Count (TC) value, and BUSY is Low.

Note: The BUSY condition applies to only the XC17V08 and XC17V16.

RESET/$\overline{OE}$

The polarity of this input pin is programmable as either RESET/$\overline{OE}$ or OE/$\overline{RESET}$. The polarity is set at the time of device programming. The device default is active-High RESET, but compatibility with Xilinx FPGAs requires the polarity to be programmed with an active-Low RESET.

When RESET is active, the address counter is held at “0”, and puts the DATA output in a high-impedance state.

$\overline{CE}$

When High, this pin holds the internal address counter in reset, puts the DATA output in a high-impedance state, and forces the device into low-I_{CC} standby mode.

$\overline{CEO}$

Chip Enable Output is connected to the $\overline{CE}$ input of the next PROM in the daisy chain. This output is Low when the $\overline{CE}$ and $\overline{OE}$ inputs are both active AND the internal address counter has been incremented beyond its Terminal Count (TC) value. $\overline{CEO}$ returns to High when $\overline{OE}$ goes inactive or $\overline{CE}$ goes High.

BUSY (XC17V16 and XC17V08 Only)

Asserting the BUSY input High prevents rising edges on CLK from incrementing the internal address counter and maintains current data on the data pins.

Note: If the BUSY pin is floating, then the programmable option to internally tie BUSY to an internal pull-down resistor must be set during device programming.

V_{PP}

Programming voltage. No overshoot above the specified maximum voltage is permitted on this pin. For normal read operation, this pin must be connected to V_{CC}. Failure to do so may lead to unpredictable, temperature-dependent operation and severe problems in circuit debugging.

Caution! Do not leave V_{PP} floating!

V_{CC} and GND

Positive supply and ground pins.

PROM Pinouts for XC17V16 and XC17V08

Pins not listed in Table 1 are “no connect.”

Table 1: **Pinouts for XC17V16 and XC17V08**

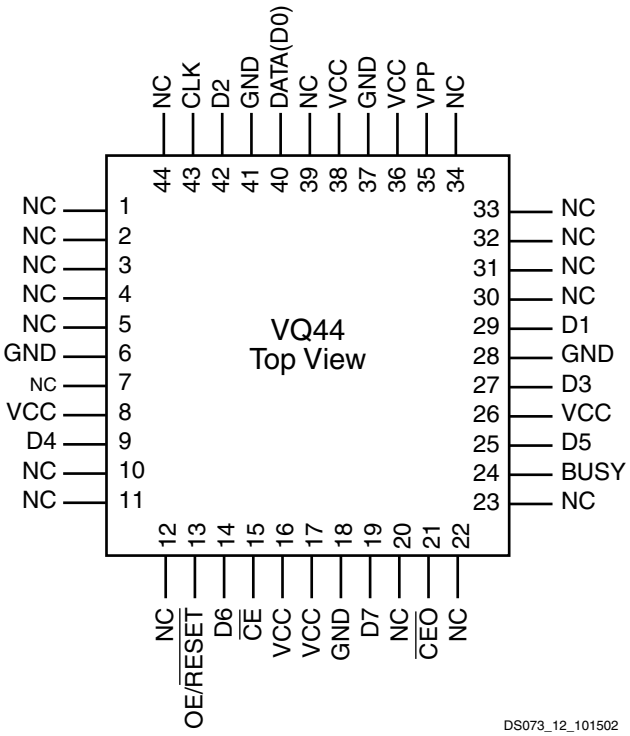
Pin Name	44-pin VQFP (VQ44)	44-pin PLCC (PC44)
BUSY	24	30
D0	40	2
D1	29	35
D2	42	4
D3	27	33
D4	9	15
D5	25	31
D6	14	20
D7	19	25
CLK	43	5
RESET/$\overline{OE}$ (OE/$\overline{RESET}$)	13	19
$\overline{CE}$	15	21
GND	6, 18, 28, 37, 41	3, 12, 24, 34, 43
$\overline{CEO}$	21	27
V_{PP}	35	41
V_{CC}	8, 16, 17, 26, 36, 38	14, 22, 23, 32, 42, 44

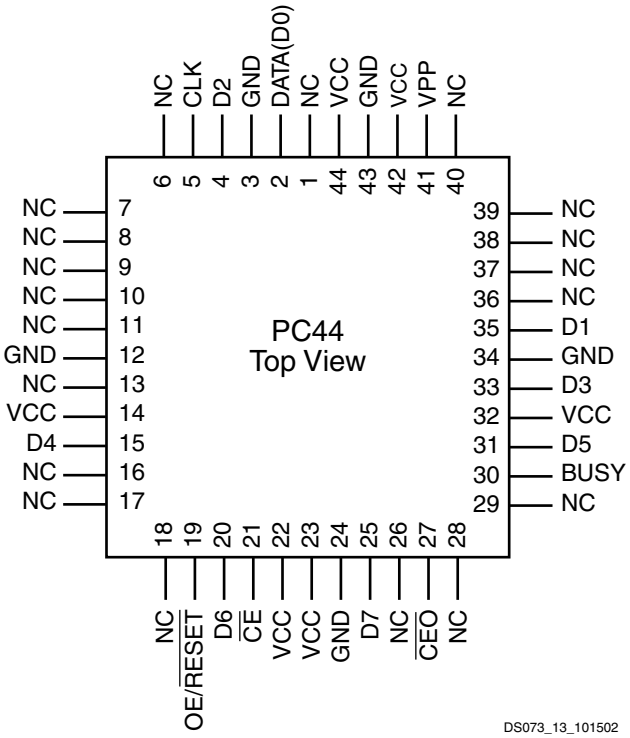
Capacity

Table 2: **Device Capacities**

Devices	Configuration Bits
XC17V16	16,777,216
XC17V08	8,388,608

Pinout Diagrams for XC17V16 and XC17V08





PROM Pinouts for XC17V04, XC17V02, and XC17V01

Pins not listed in Table 3 are “no connect.”

Table 3: **Pinouts for XC17V04, XC17V02, and XC17V01**

Pin Name	8-pin VOIC (V08) (1)	20-pin SOIC (SO20) (1)	20-pin PLCC (PC20) (1,2)	44-pin VQFP (VQ44) (2)	44-pin PLCC (PC44) (2)
DATA	1	1	1	40	2
CLK	2	3	3	43	5
RESET/$\overline{OE}$ (OE/$\overline{RESET}$)	3	8	8	13	19
CE	4	10	10	15	21
GND	5	11	11	18, 41	24, 3
CEO	6	13	13	21	27
V_{PP}	7	18	18	35	41
V_{CC}	8	20	20	38	44

Notes:

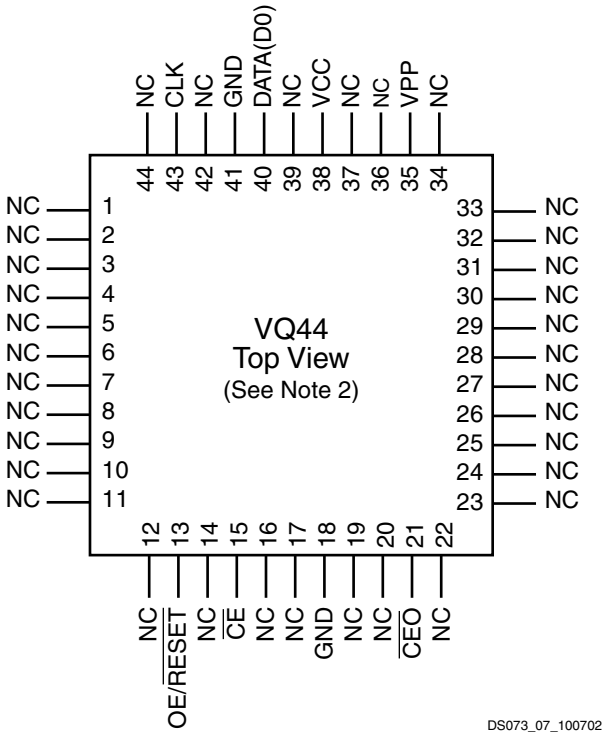
1. XC17V01 available in these packages.
2. XC17V02 and XC17V04 available in these packages.

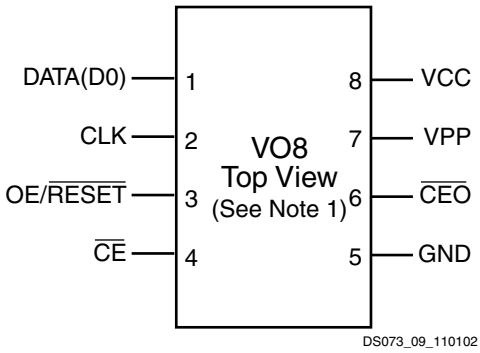
Capacity

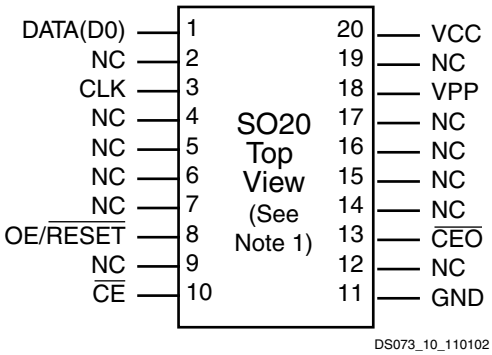
Table 4: **Device Capacities**

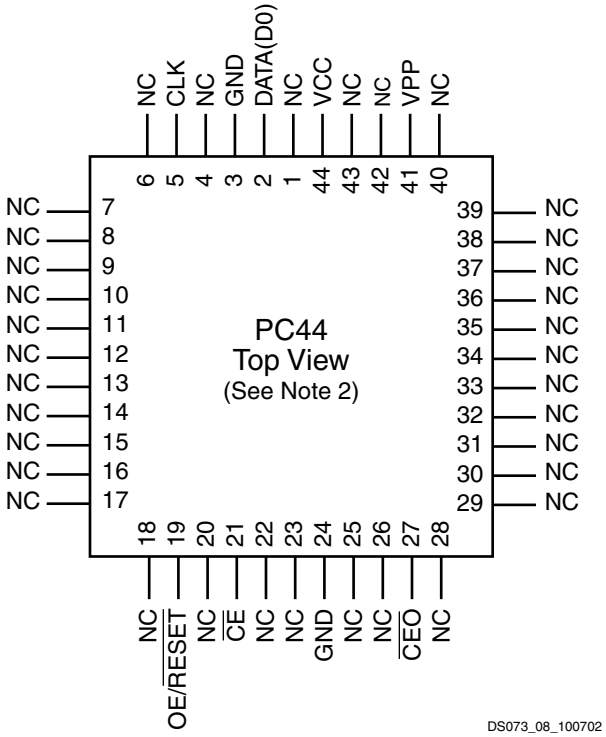
Devices	Configuration Bits
XC17V04	4,194,304
XC17V02	2,097,152
XC17V01	1,679,360

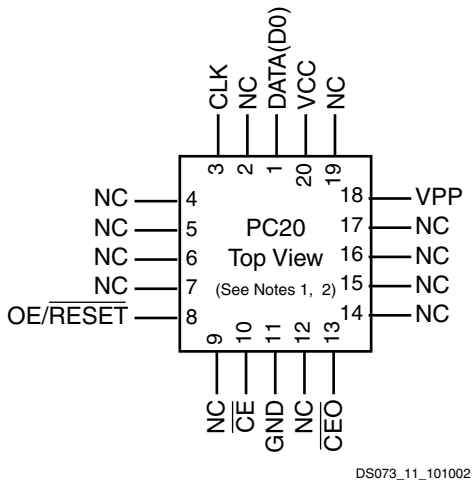
Pinout Diagrams for XC17V04, XC17V02, and XC17V01











Notes:

1. XC1701 is available in these packages.
2. XC1702 and XC1704 are available in these packages.

Xilinx FPGAs and Compatible PROMs

Table 5: **Xilinx FPGAs and Compatible PROMs**

Device	Configuration Bits	PROM
XC2V40	360,096	XC17V01
XC2V80	635,296	XC17V01
XC2V250	1,697,184	XC17V02
XC2V500	2,761,888	XC17V04
XC2V1000	4,082,592	XC17V04
XC2V1500	5,659,296	XC17V08
XC2V2000	7,492,000	XC17V08
XC2V3000	10,494,368	XC17V16
XC2V4000	15,659,936	XC17V16
XC2V6000	21,849, 504	XC17V16 + XC17V08
XC2V8000	29,063,072	2 of XC17V16
XCV50	559,200	XC17V01
XCV100	781,216	XC17V01
XCV150	1,040,096	XC17V01
XCV200	1,335,840	XC17V01
XCV300	1,751,808	XC17V02
XCV400	2,546,048	XC17V04
XCV600	3,607,968	XC17V04
XCV800	4,715,616	XC17V08
XCV1000	6,127,744	XC17V08
XCV50E	630,048	XC17V01
XCV100E	863,840	XC17V01
XCV200E	1,442,016	XC17V01
XCV300E	1,875,648	XC17V02
XCV400E	2,693,440	XC17V04
XCV405E	3,430,400	XC17V04
XCV600E	3,961,632	XC17V04
XCV812E	6,519,648	XC17V08
XCV1000E	6,587,520	XC17V08
XCV1600E	8,308,992	XC17V08
XCV2000E	10,159,648	XC17V16
XCV2600E	12,922,336	XC17V16
XCV3200E	16,283,712	XC17V16
XC3S50	439,264	XC17V01
XC3S200	1,047,616	XC17V01
XC3S400	1,699,136	XC17V02
XC3S1000	3,223,488	XC17V04
XC3S1500	5,214,784	XC17V08
XC3S2000	7,673,024	XC17V08
XC3S4000	11,316,864	XC17V16
XC3S5000	13,271,936	XC17V16

Controlling PROMs

Connecting the FPGA device with the PROM.

- The DATA output(s) of the PROM(s) drives the configuration data input(s) of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s).
- The $\overline{CEO}$ output of a PROM drives the $\overline{CE}$ input of the next PROM in a daisy chain (if any).
- The $\overline{RESET}$/OE input of all PROMs is best driven by the $\overline{INIT}$ output of the lead FPGA device. This connection assures that the PROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V_{CC} glitch.
- The PROM $\overline{CE}$ input is best connected to the FPGA DONE pin(s) and a pullup resistor. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 15 mA maximum.
- SelectMAP mode is similar to Slave Serial mode. The DATA is clocked out of the PROM one byte per CCLK instead of one bit per CCLK cycle. See FPGA data sheets for special configuration requirements.

FPGA Master Serial Mode Summary

The I/O and logic functions of the Configurable Logic Block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Serial mode, the FPGA automatically loads the configuration program from an external memory. The Xilinx PROMs have been designed for compatibility with the Master Serial mode.

Upon power-up or reconfiguration, an FPGA enters the Master Serial mode whenever all three of the FPGA mode-select pins are Low (M0=0, M1=0, M2=0). Data is read from the PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial Mode provides a simple configuration interface. Only one serial data line, two control lines, and one clock line are required to configure an FPGA. Data from the PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function DIN pin on the FPGA is used only for configuration, it must still be held at a defined level during normal operation. The Xilinx FPGA families take care of this automatically with an on-chip default pull-up/down resistor or keeper circuit.

Cascading Configuration PROMs

For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded PROMs provide additional memory. After the last bit from the first PROM is read, the next clock signal to the PROM asserts its $\overline{CEO}$ output Low and disables its DATA line. The second PROM recognizes the Low level on its $\overline{CE}$ input and enables its DATA output. See Figure 3.

After configuration is complete, the address counters of all cascaded PROMs are reset if the FPGA $\overline{PROGRAM}$ pin goes Low, assuming the PROM reset polarity option has been inverted.

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{CE}$ is asserted High. The output remains in a high impedance state regardless of the state of the $\overline{OE}$ input.

Programming

The devices can be programmed on programmers supplied by Xilinx or qualified third-party vendors. The user must ensure that the appropriate programming algorithm and the latest version of the programmer software are used. The wrong choice can permanently damage the device.

Selecting Reset Polarity and Configuration Modes

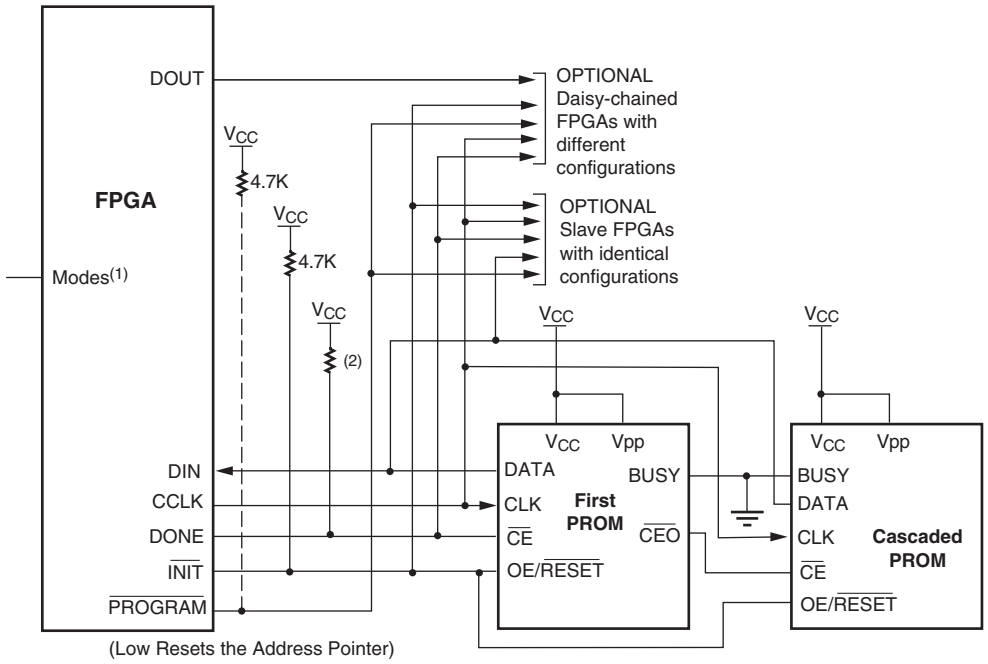
The OE/$\overline{RESET}$ input polarity is programmable on all XC17V00 PROMs. In addition, the XC17V08 and XC17V16 can accommodate either serial or parallel configuration mode. The reset polarity and configuration mode are selectable through the programmer software. For compatibility with Xilinx FPGAs, the OE/$\overline{RESET}$ polarity must be programmed with $\overline{RESET}$ active-Low.

Table 6: **Truth Table for XC17V00 Control Inputs**

Control Inputs		Internal Address	Outputs		
RESET(1)	**$\overline{CE}$**		**DATA**	**$\overline{CEO}$**	**I_{CC}**
Inactive	Low	If address ≤ TC(2): increment If address > TC(2): don't change	Active High-Z	High Low	Active Reduced
Active	Low	Held reset	High-Z	High	Active
Inactive	High	Not changing	High-Z	High	Standby
Active	High	Held reset	High-Z	High	Standby

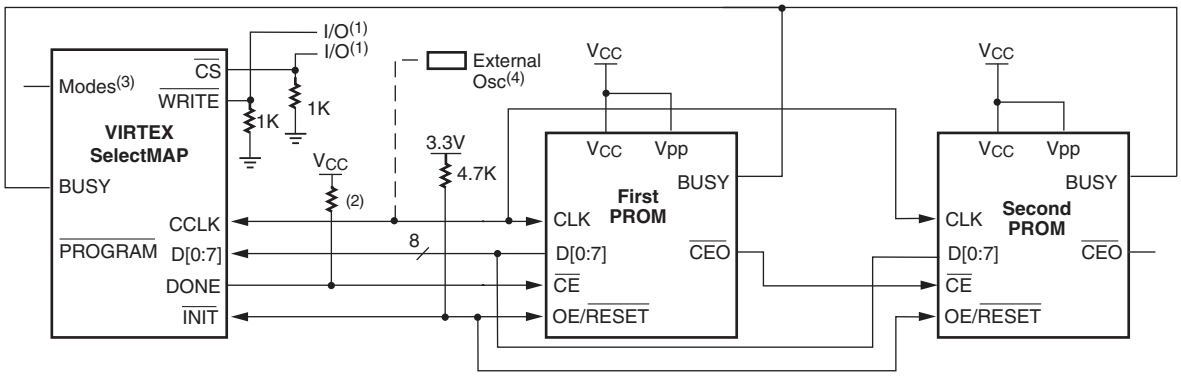
Notes:

1. The XC17V00 RESET input has programmable polarity
2. TC = terminal count, highest address value.



(1) For Mode pin connections, refer to the appropriate FPGA data sheet or user guide.
(2) For specific DONE resistor recommendations, refer to the appropriate FPGA data sheet or user guide.

Master Serial Mode



(1) $\overline{CS}$ and $\overline{WRITE}$ must be pulled down to be used as I/O. One option is shown.
(2) For specific DONE resistor recommendations, refer to the appropriate FPGA data sheet or user guide.
(3) For Mode pin connections, refer to the appropriate FPGA data sheet or user guide.
(4) External oscillator required for FPGA slave SelectMAP modes.

Virtex SelectMAP Mode, XC17V16 and XC17V08 only.

DS073_03_033106

Figure 3: **(a) Master Serial Mode (b) Virtex SelectMAP Mode (dotted lines indicates optional connection)**

Absolute Maximum Ratings(1)

Symbol	Description	Conditions	Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{PP}	Supply voltage relative to GND	–0.5 to +12.5	V
V_{IN}	Input voltage relative to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to High-Z output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions (3V Supply)

Symbol	Description		Min	Max	Units
V_{CC}(1)	Supply voltage relative to GND (T_A = 0° C to +70° C)	Commercial	3.0	3.6	V
	Supply voltage relative to GND (T_A = –40° C to +85° C)	Industrial	3.0	3.6	V
T_{VCC}(2)	V_{CC} rise time from 0V to nominal voltage		1.0	50	ms

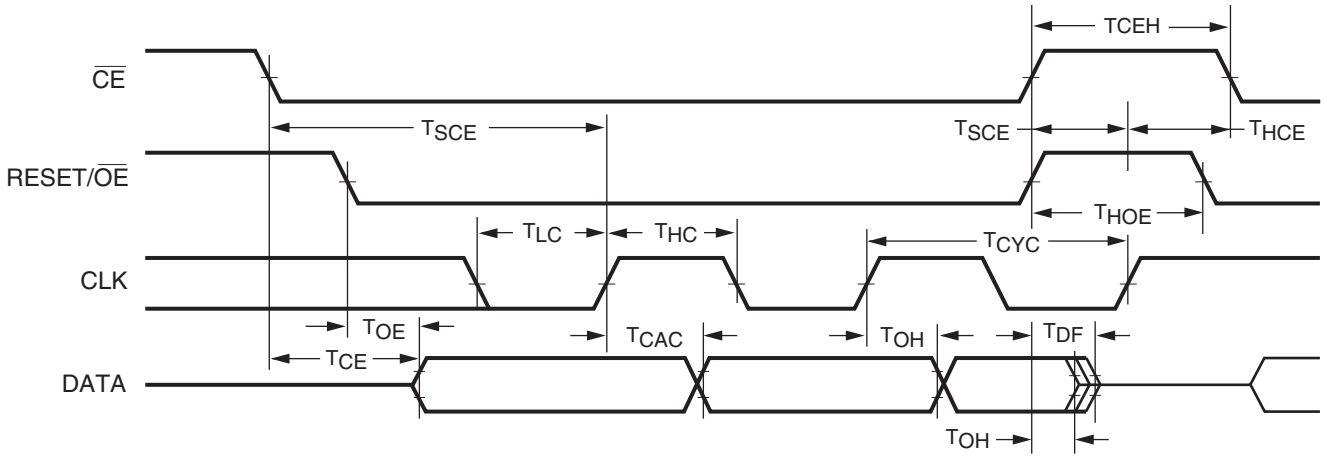
Notes:

1. During normal read operation V_{PP} ***must*** be connected to V_{CC}.
2. At power up, the device requires the V_{CC} power supply to monotonically rise from 0V to nominal voltage within the specified V_{CC} rise time. If the power supply cannot meet this requirement, then the device may not power-on-reset properly.

DC Characteristics Over Operating Condition

Symbol	Description	Min	Max	Units
V_{IH}	High-level input voltage	2	V_{CC}	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = –3 mA)	2.4	–	V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)	–	0.4	V
I_{CCA}	Supply current, active mode (at maximum frequency) (XC17V16 and XC17V08 only)	–	100	mA
I_{CCA}	Supply current, active mode (at maximum frequency) (XC17V04, XC17V02, and XC17V01 only)	–	15	mA
I_{CCS}	Supply current, standby mode	–	1	mA
I_L	Input or output leakage current	–10	10	µA
C_{IN}	Input capacitance (V_{IN} = GND, f = 1.0 MHz)	–	15	pF
C_{OUT}	Output capacitance (V_{IN} = GND, f = 1.0 MHz)	–	15	pF

AC Characteristics Over Operating Condition for XC17V04, XC17V02, and XC17V01



Notes:
1 The XC17V00 RESET/OE input polarity is programmable. The RESET/OE input is shown in the timing diagram with active-high RESET polarity. Timing specifications are identical for both polarity settings.
2 The diagram shows timing relationships. The diagram is not reflective of actual FPGA signal sequences. See the appropriate FPGA data sheet or user guide for actual configuration signal sequences.

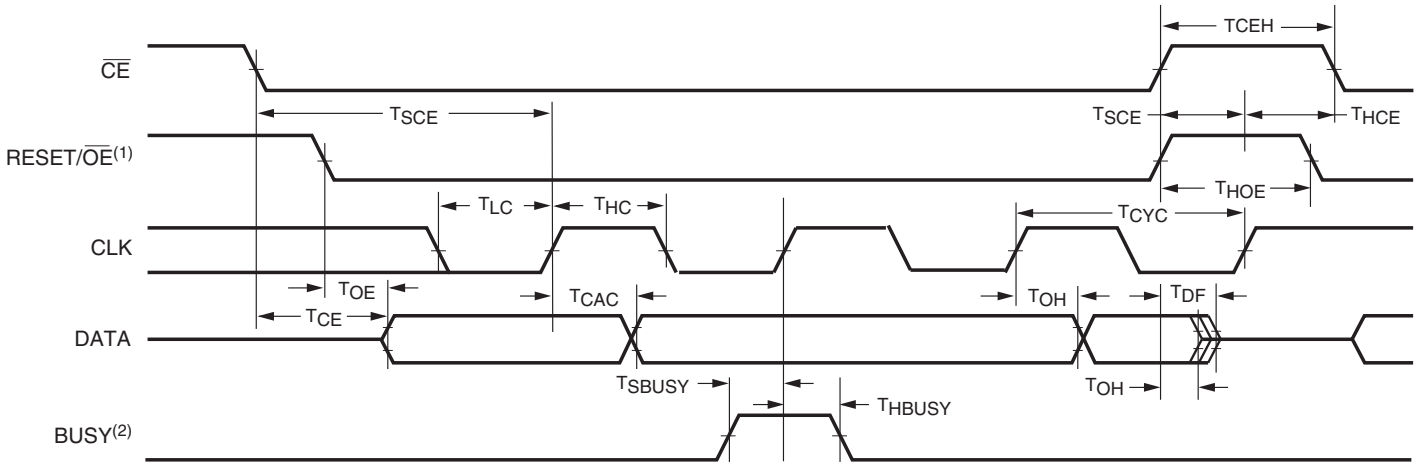
DS073_04_14102005

Symbol	Description	Min	Max	Units
T_{OE}	$\overline{OE}$ to data delay	–	30	ns
T_{CE}	$\overline{CE}$ to data delay	–	45	ns
T_{CAC}	CLK to data delay	–	45	ns
T_{DF}	$\overline{CE}$ or $\overline{OE}$ to data float delay(2,3)	–	50	ns
T_{OH}	Data hold from $\overline{CE}$, $\overline{OE}$, or CLK(3)	0	–	ns
T_{CYC}	Clock periods	67	–	ns
T_{LC}	CLK Low time(3)	25	–	ns
T_{HC}	CLK High time(3)	25	–	ns
T_{SCE}	$\overline{CE}$ setup time to CLK (to guarantee proper counting)	25	–	ns
T_{HCE}	$\overline{CE}$ hold time to CLK (to guarantee proper counting)	0	–	ns
T_{HOE}	$\overline{OE}$ hold time (guarantees counters are reset)	25	–	ns
T_{CEH}	$\overline{CE}$ High time (guarantees counters are reset)	20	–	ns

Notes:

1. AC test load = 50 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
5. If T_{CEH} High, 2 µs, T_{CE} = 2 µs.
6. If T_{HOE} High, 2 µs, T_{OE} = 2 µs.

AC Characteristics Over Operating Condition for XC17V16 and XC17V08



Note:
1 The XC17V00 RESET/OE input polarity is programmable. The RESET/OE input is shown in the timing diagram with active-high RESET polarity. Timing specifications are identical for both polarity settings.
2. If BUSY is inactive (Low) during a rising CLK edge, then new DATA appears at time T_{CAC} after the rising CLK edge. If BUSY is active (High) during a rising CLK edge, then there is no corresponding change to DATA.

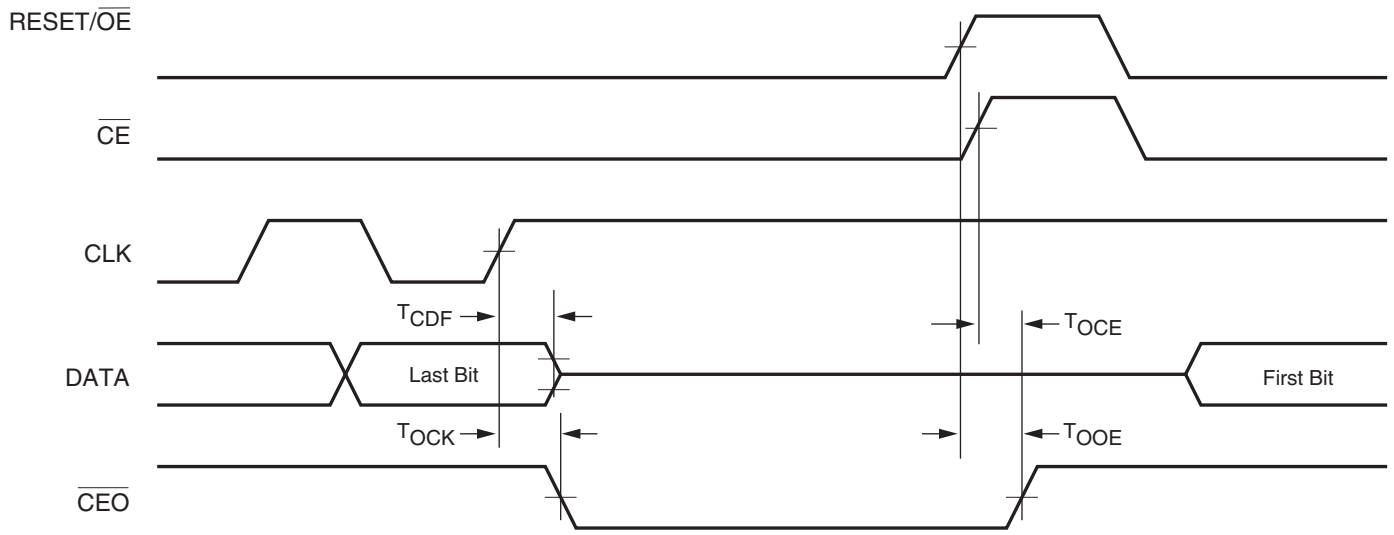
DS073_05_031606

Symbol	Description	Min	Max	Units
T_{OE}	$\overline{OE}$ to data delay	–	15	ns
T_{CE}	$\overline{CE}$ to data delay	–	20	ns
T_{CAC}	CLK to data delay(2)	–	20	ns
T_{DF}	$\overline{CE}$ or $\overline{OE}$ to data float delay(3,4)	–	35	ns
T_{OH}	Data hold from $\overline{CE}$, $\overline{OE}$, or CLK(4)	0	–	ns
T_{CYC}	Clock periods	50	–	ns
T_{LC}	CLK Low time(4)	25	–	ns
T_{HC}	CLK High time(4)	25	–	ns
T_{SCE}	$\overline{CE}$ setup time to CLK (to guarantee proper counting)	25	–	ns
T_{HCE}	$\overline{CE}$ hold time to CLK (to guarantee proper counting)	0	–	ns
T_{HOE}	$\overline{OE}$ hold time (guarantees counters are reset)	25	–	ns
T_{SBUSY}	BUSY setup time	5	–	ns
T_{HBUSY}	BUSY hold time	5	–	ns
T_{CEH}	$\overline{CE}$ High time (guarantees counters are reset)	20	–	ns

Notes:

1. AC test load = 50 pF.
2. When BUSY = 0.
3. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
4. Guaranteed by design, not tested.
5. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
6. If T_{CEH} High, 2 µs, T_{CE} = 2 µs.
7. If T_{HOE} High, 2 µs, T_{OE} = 2 µs.

AC Characteristics Over Operating Condition When Cascading



Notes:
1 The XC17V00 RESET/OE input polarity is programmable. The RESET/OE input is shown in the timing diagram with active-high RESET polarity. Timing specifications are identical for both polarity settings.
2 The diagram shows timing of the First Bit and Last Bit for one PROM with respect to signals involved in a cascaded situation. The diagram does not show timing of data as one PROM transfers control to the next PROM. The shown timing information must be applied appropriately to each PROM in a cascaded situation to understand the timing of data during the transfer of control from one PROM to the next.

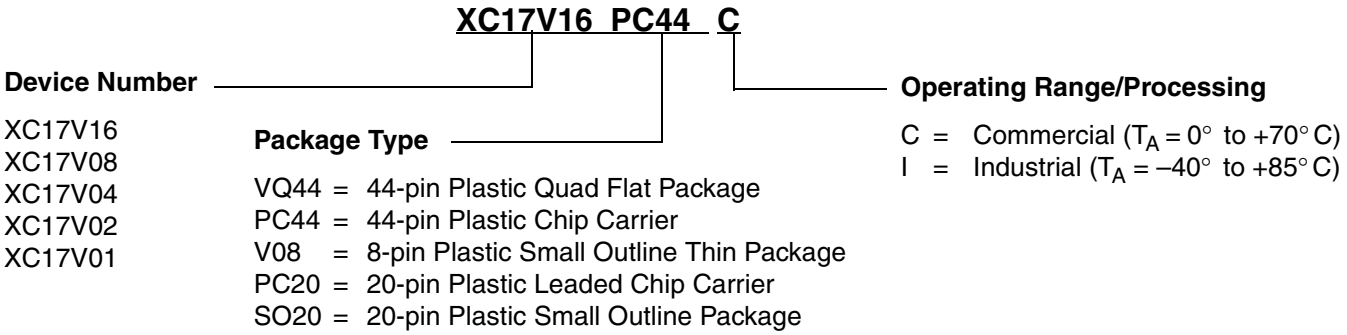
DS026_07_102005

Symbol	Description	Min	Max	Units
T_{CDF}	CLK to data float delay(2,3)	–	50	ns
T_{OCK}	CLK to $\overline{CEO}$ delay(3)	–	30	ns
T_{OCE}	CE to $\overline{CEO}$ delay(3)	–	35	ns
T_{OOE}	RESET/$\overline{OE}$ to $\overline{CEO}$ delay(3)	–	30	ns

Notes:

1. AC test load = 50 pF
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.

Ordering Information

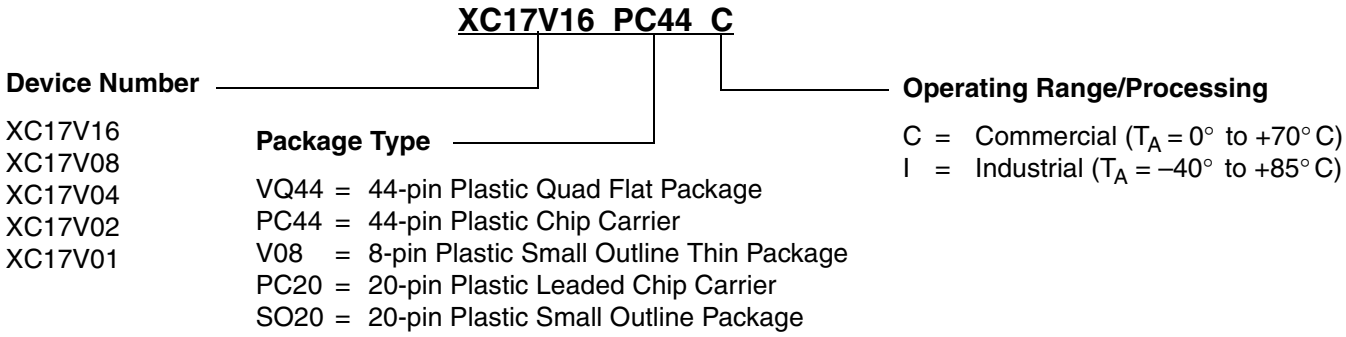


Valid Ordering Combinations

XC17V16VQ44C	XC17V08VQ44C	XC17V04PC20C	XC17V02PC20C	XC17V01PC20C
XC17V16PC44C	XC17V08PC44C	XC17V04PC44C	XC17V02PC44C	XC17V01VO8C
XC17V16VQ44I	XC17V08VQ44I	XC17V04VQ44C	XC17V02VQ44C	XC17V01SO20C
XC17V16PC44I	XC17V08PC44I	XC17V04PC20I	XC17V02PC20I	XC17V01PC20I
		XC17V04PC44I	XC17V02PC44I	XC17V01VO8I
		XC17V04VQ44I	XC17V02VQ44I	XC17V01SO20I

Marking Information

Due to the small size of the commercial serial PROM packages, the complete ordering part number cannot be marked on the package. The XC prefix is deleted and the package code is simplified. Device marking is as follows:



Revision History

The following table shows the revision history for this document.

Date	Version	Revision
07/26/00	1.0	Initial Xilinx release.
10/09/00	1.1	Updated 20-pin PLCC Pinouts.
11/16/00	1.2	Updated pinouts for XC17V16 and XC17V08, I_{CCA} DC Characteristic from standby to active mode; C_{IN} and C_{OUT} from 10 pF to 15 pF, added I_{CCS} for XC17V16 and XC17V08 at 500 µA.
02/20/01	1.3	Added note to pinouts for “no connect,” updated Figure 3.
04/04/01	1.4	Added XC2V products to Compatible PROM table, updated Figure 3, updated text for Virtex-II FPGAs.
10/09/01	1.5	Corrected bitstream length for SCV405E, added power-on supply requirements and note for power-on reset, updated configuration bits for Virtex-II devices, removed $\overline{CF}$ from Figure 3, and updated FPGA list.
02/27/02	1.6	Added Virtex-II Pro™ FPGAs to the Xilinx FPGAs and Compatible PROMs, page 6.
06/14/02	1.7	Made additions and changes to Xilinx FPGAs and Compatible PROMs, page 6.
07/29/02	1.8	Added Virtex-II Pro FPGAs to Xilinx FPGAs and Compatible PROMs, page 6.
11/05/02	1.9	Added pinout diagrams, changed Xilinx FPGAs and Compatible PROMs, page 6, and added footnotes to AC Characteristics Over Operating Condition for XC17V04, XC17V02, and XC17V01, page 10 and AC Characteristics Over Operating Condition for XC17V16 and XC17V08, page 11.
04/10/03	1.10	Added Spartan-3 FPGAs to Truth Table for XC17V00 Control Inputs, page 7.
06/07/07	1.11	• Figure 2, page 2 updated to show correct three-state control on output data buses. • Corrected XC3S50 bitstream size in Xilinx FPGAs and Compatible PROMs, page 6. • Added section Selecting Reset Polarity and Configuration Modes, page 7. • Removed maximum soldering temperature (T_{SOL}) from "Absolute Maximum Ratings(1)," page 9. Refer to Xilinx Device Package User Guide for package soldering guidelines. • Added notes to timing diagram under AC Characteristics Over Operating Condition for XC17V04, XC17V02, and XC17V01, page 10 for clarification. • Added notes and updated timing diagram AC Characteristics Over Operating Condition for XC17V16 and XC17V08, page 11 for clarification. • Reversed polarity of RESET/OE signal in timing diagram under , page 12 for consistency and added notes for clarification.