Virtex-5Q FPGA Data Sheet: DC and Switching Characteristics

Virtex-5Q FPGA Electrical Characteristics

Defense-grade Virtex®-5Q FPGAs are available in -2I, -1I, and -1M (only FX70T and FX100T devices in -1M) speed grades, with -2I having the highest performance. Virtex-5Q FPGA DC and AC characteristics are specified for the industrial temperature range. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This Virtex-5Q FPGA data sheet, part of an overall set of documentation on the Virtex-5 family of FPGAs, is available on the Xilinx website:

- DS174, *Virtex-5Q Family Overview*
- UG190, *Virtex-5 FPGA User Guide*
- UG191, *Virtex-5 FPGA Configuration Guide*
- UG192, *Virtex-5 FPGA System Monitor User Guide*
- UG193, *Virtex-5 FPGA XtremeDSP™ Design Considerations User Guide*
- UG194, *Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC User Guide*
- UG195, *Virtex-5 FPGA Packaging and Pinout Specification*
- UG196, *Virtex-5 FPGA RocketIO™ GTP Transceiver User Guide*
- UG197, *Virtex-5 FPGA Integrated Endpoint Block User Guide for PCI Express® Designs*
- UG198, *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*
- UG200, *Embedded Processor Block in Virtex-5 FPGAs Reference Guide*
- UG203, *Virtex-5 FPGA PCB Designer's Guide*

All specifications are subject to change without notice.

Virtex-5Q FPGA DC Characteristics

Table 1: **Absolute Maximum Ratings(1)**

Symbol	Description	Range	Units
V_{CCINT}	Internal supply voltage relative to GND	–0.5 to 1.1	V
V_{CCAUX}	Auxiliary supply voltage relative to GND	–0.5 to 3.0	V
V_{CCO}	Output drivers supply voltage relative to GND	–0.5 to 3.75	V
V_{BATT}	Key memory battery backup supply	–0.5 to 4.05	V
V_{REF}	Input reference voltage	–0.5 to 3.75	V
V_{IN}(3)	3.3V I/O input voltage relative to GND(2) (user and dedicated I/Os)	–0.75 to 4.05	V
	3.3V I/O input voltage relative to GND (restricted to maximum of 100 user I/Os)(4)	–0.85 to 4.3 (Industrial Temperature)	V
	2.5V or below I/O input voltage relative to GND (user and dedicated I/Os)	–0.75 to V_{CCO} + 0.5	V
I_{IN}	Current applied to an I/O pin, powered or unpowered	±100	mA
	Total current applied to all I/O pins, powered or unpowered	±100	mA
V_{TS}	Voltage applied to 3-state 3.3V output(2) (user and dedicated I/Os)	–0.75 to 4.05	V
	Voltage applied to 3-state 2.5V or below output (user and dedicated I/Os)	–0.75 to V_{CCO} + 0.5	V
T_{STG}	Storage temperature (ambient)	–65 to 150	°C

Table 1: **Absolute Maximum Ratings[(1)] *(Cont'd)***

Symbol	Description	Range	Units
T_{SOL}	Maximum soldering temperature[(5)]	+220	°C
T_j	Maximum junction temperature[(5)]	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. For 3.3V I/O operation, refer to *Virtex-5 FPGA User Guide*, Chapter 6, 3.3V I/O Design Guidelines.
3. 3.3V I/O absolute maximum limit applied to DC and AC signals.
4. For more flexibility in specific designs, a maximum of 100 user I/Os can be stressed beyond the normal specification for no more than 20% of a data period.
5. For soldering guidelines, refer to UG112: *Device Package User Guide*. For thermal considerations, refer to UG195: *Virtex-5 FPGA Packaging and Pinout Specification* on the Xilinx website.

Table 2: **Recommended Operating Conditions**

Symbol	Description	Temperature Range	Min	Max	Units
V_{CCINT}	Internal supply voltage relative to GND, T_j = –40°C to +100°C	Industrial	0.95	1.05	V
V_{CCAUX}[(1)]	Auxiliary supply voltage relative to GND, T_j = –40°C to +100°C	Industrial	2.375	2.625	V
V_{CCO}[(2)(3)(4)]	Supply voltage relative to GND, T_j = –40°C to +100°C	Industrial	1.14	3.45	V
V_{IN}	3.3V supply voltage relative to GND, T_j = –40°C to +100°C	Industrial	GND – 0.20	3.45	V
	2.5V and below supply voltage relative to GND, T_j = –40°C to +100°C	Industrial	GND – 0.20	V_{CCO} + 0.2	V
I_{IN}	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	Industrial		10	mA
V_{BATT}[(5)]	Battery voltage relative to GND, T_j = –40°C to +100°C	Industrial	1.0	3.6	V

Notes:

1. Recommended maximum voltage drop for V_{CCAUX} is 10 mV/ms.
2. Configuration data is retained even if V_{CCO} drops to 0V.
3. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
4. The configuration supply voltage V_{CC_CONFIG} is also known as V_{CCO_0}.
5. V_{BATT} is required only when using bitstream encryption. If battery is not used, connect V_{BATT} to either ground or V_{CCAUX}.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75			V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	2.0			V
I_{REF}	V_{REF} leakage current per pin			10	µA
I_L	Input or output leakage current per pin (sample-tested)			10	µA
C_{IN}	Input capacitance (sample-tested)			8	pF
I_{RPU}[(1)]	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V	20		150	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V	10		90	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V	5		45	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V	3		30	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V	2		15	µA
I_{RPD}[(1)]	Pad pull-down (when selected) @ V_{IN} = 2.5V	5		110	µA
I_{BATT}[(2)]	Battery supply current			150	nA
n	Temperature diode ideality factor		1.0002		n
r	Series resistance		5.0		Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Maximum value specified for worst case process at 25°C.

Important Note

Typical values for quiescent supply current are now specified at nominal voltage, 85°C junction temperatures (T_j). Xilinx recommends analyzing static power consumption at T_j = 85°C because the majority of designs operate near the high end of the commercial temperature range. Data sheets for older products (e.g., Virtex-4 devices) still specify typical quiescent supply current at T_j = 25°C. Quiescent supply current is specified by speed grade for Virtex-5Q devices. Use the XPOWER Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to calculate static power consumption for conditions other than those specified in Table 4.

Table 4: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed and Temperature Grade			Units
			-2 (I)	-1 (I)	-1 (M)	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XQ5VLX30T	507	317	N/A	mA
		XQ5VLX85	1072	833	N/A	mA
		XQ5VLX110	1391	1109	N/A	mA
		XQ5VLX110T	1448	1154	N/A	mA
		XQ5VLX155T	2674	2188	N/A	mA
		XQ5VLX220T	2844	2328	N/A	mA
		XQ5VLX330T	N/A	3492	N/A	mA
		XQ5VSX50T	1092	840	N/A	mA
		XQ5VSX95T	1924	1475	N/A	mA
		XQ5VSX240T	N/A	3168	N/A	mA
		XQ5VFX70T	1658	1658	1658	mA
		XQ5VFX100T	2875	2875	2875	mA
		XQ5VFX130T	3041	3041	N/A	mA
		XQ5VFX200T	N/A	3755	N/A	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XQ5VLX30T	1.5	1.5	N/A	mA
		XQ5VLX85	3	3	N/A	mA
		XQ5VLX110	4	4	N/A	mA
		XQ5VLX110T	4	4	N/A	mA
		XQ5VLX155T	8	8	N/A	mA
		XQ5VLX220T	8	8	N/A	mA
		XQ5VLX330T	N/A	12	N/A	mA
		XQ5VSX50T	2	2	N/A	mA
		XQ5VSX95T	4	4	N/A	mA
		XQ5VSX240T	N/A	12	N/A	mA
		XQ5VFX70T	6	6	6	mA
		XQ5VFX100T	7	7	7	mA
		XQ5VFX130T	8	8	N/A	mA
		XQ5VFX200T	N/A	10	N/A	mA

Table 4: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed and Temperature Grade			Units
			-2 (I)	-1 (I)	-1 (M)	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XQ5VLX30T	43	43	N/A	mA
		XQ5VLX85	93	93	N/A	mA
		XQ5VLX110	125	125	N/A	mA
		XQ5VLX110T	130	130	N/A	mA
		XQ5VLX155T	177	177	N/A	mA
		XQ5VLX220T	236	236	N/A	mA
		XQ5VLX330T	N/A	353	N/A	mA
		XQ5VSX50T	74	74	N/A	mA
		XQ5VSX95T	131	131	N/A	mA
		XQ5VSX240T	N/A	300	N/A	mA
		XQ5VFX70T	110	110	110	mA
		XQ5VFX100T	150	150	150	mA
		XQ5VFX130T	180	180	N/A	mA
		XQ5VFX200T	N/A	250	N/A	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j). Industrial (I) and Military (M) grade devices have the same typical values as commercial (C) grade devices at 85°C, but higher values at 100°C (I) and 125°C (M). Use the XPE/XPA power tools to calculate values for conditions other than specified in this data sheet.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. If DCI or differential signaling is used, more accurate quiescent current estimates can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply.

The power supplies can be turned on in any sequence, though the specifications shown in Table 5 are for the recommended power-on sequence of V_{CCINT}, V_{CCAUX}, and V_{CCO}. The I/O will remain 3-stated through power-on if the recommended power-on sequence is followed. Xilinx does not specify the current or I/O behavior for other power-on sequences.

Table 5 shows the minimum current required by Virtex-5Q devices for proper power-on and configuration.

If the current minimums shown in Table 5 are met, the device powers on properly after all three supplies have passed through their power-on reset threshold voltages.

The FPGA must be configured after V_{CCINT} is applied.

Once initialized and configured, use the XPOWER tools to estimate current drain on these supplies.

Table 5: **Power-On Current for Virtex-5Q Devices**

Device	$I_{CCINTMIN}$ Typ(1)	$I_{CCAUXMIN}$ Typ(1)	I_{CCOMIN} Typ(1)	Units
XQ5VLX30T	246	86	50	mA
XQ5VLX85	492	186	100	mA
XQ5VLX110	623	250	100	mA
XQ5VLX110T	651	260	100	mA
XQ5VLX155T	728	368	100	mA
XQ5VLX220T	1056	472	150	mA
XQ5VLX330T	1509	706	150	mA
XQ5VSX50T	472	148	50	mA
XQ5VSX95T	804	262	100	mA
XQ5VSX240T	1632	662	150	mA
XQ5VFX70T	695	232	100	mA
XQ5VFX100T	749	298	100	mA
XQ5VFX130T	1111	392	150	mA
XQ5VFX200T	1222	534	150	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. The maximum startup current can be obtained using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools and adding the quiescent plus dynamic current consumption.

Table 6: **Power Supply Ramp Time**

Symbol	Description	Ramp Time	Units
V_{CCINT}	Internal supply voltage relative to GND	0.20 to 50.0	ms
V_{CCO}	Output drivers supply voltage relative to GND	0.20 to 50.0	ms
V_{CCAUX}	Auxiliary supply voltage relative to GND	0.20 to 50.0	ms

SelectIO™ DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 7: **SelectIO DC Input and Output Levels**

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL	–0.3	0.8	2.0	3.45	0.4	2.4	Note 3	Note 3
LVCMOS33, LVDCI33	–0.3	0.8	2.0	3.45	0.4	V_{CCO} – 0.4	Note 3	Note 3
LVCMOS25, LVDCI25	–0.3	0.7	1.7	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	Note 3	Note 3
LVCMOS18, LVDCI18	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	0.45	V_{CCO} – 0.45	Note 4	Note 4
LVCMOS15, LVDCI15	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note 4	Note 4
LVCMOS12	–0.3	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	Note 6	Note 6
PCI33_3(5)	–0.2	30% V_{CCO}	50% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}	Note 5	Note 5
PCI66_3(5)	–0.2	30% V_{CCO}	50% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}	Note 5	Note 5
PCI-X(5)	–0.2	35% V_{CCO}	50% V_{CCO}	V_{CCO}	10% V_{CCO}	90% V_{CCO}	Note 5	Note 5
GTLP	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	–	0.6	–	36	–
GTL	–0.3	V_{REF} – 0.05	V_{REF} + 0.05	–	0.4	–	32	–
HSTL I_12	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	25% V_{CCO}	75% V_{CCO}	6.3	6.3
HSTL I(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	8	–8
HSTL II(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	16	–16
HSTL III(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	24	–8
HSTL IV(2)	–0.3	V_{REF} – 0.1	V_{REF} + 0.1	V_{CCO} + 0.3	0.4	V_{CCO} – 0.4	48	–8
DIFF HSTL I(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
DIFF HSTL II(2)	–0.3	50% V_{CCO} – 0.1	50% V_{CCO} + 0.1	V_{CCO} + 0.3	–	–	–	–
SSTL2 I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.61	V_{TT} + 0.61	8.1	–8.1
SSTL2 II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCO} + 0.3	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
DIFF SSTL2 I	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL2 II	–0.3	50% V_{CCO} – 0.15	50% V_{CCO} + 0.15	V_{CCO} + 0.3	–	–	–	–
SSTL18 I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.47	V_{TT} + 0.47	6.7	–6.7
SSTL18 II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.3	V_{TT} – 0.60	V_{TT} + 0.60	13.4	–13.4
DIFF SSTL18 I	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–
DIFF SSTL18 II	–0.3	50% V_{CCO} – 0.125	50% V_{CCO} + 0.125	V_{CCO} + 0.3	–	–	–	–

Notes:

1. Tested according to relevant specifications.
2. Applies to both 1.5V and 1.8V HSTL.
3. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
4. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
5. For more information on PCI33_3, PCI66_3, and PCI-X, refer to *Virtex-5 FPGA User Guide, Chapter 6, 3.3V I/O Design Guidelines*.
6. Supported drive strengths of 2, 4, 6, or 8 mA.

HT DC Specifications (HT_25)

Table 8: **HT DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OD}	Differential Output Voltage	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals	495	600	840	mV
ΔV_{OD}	Change in V_{OD} Magnitude		–15		15	mV
V_{OCM}	Output Common Mode Voltage	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals	495	600	715	mV
ΔV_{OCM}	Change in V_{OCM} Magnitude		–15		15	mV
V_{ID}	Input Differential Voltage		200	600	1000	mV
ΔV_{ID}	Change in V_{ID} Magnitude		–15		15	mV
V_{ICM}	Input Common Mode Voltage		440	600	780	mV
ΔV_{ICM}	Change in V_{ICM} Magnitude		–15		15	mV

LVDS DC Specifications (LVDS_25)

Table 9: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals			1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals	0.825			V
V_{ODIFF}	Differential Output Voltage $(Q - \overline{Q})$, Q = High $(\overline{Q} - Q)$, $\overline{Q}$ = High	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals	1.125	1.250	1.375	V
V_{IDIFF}	Differential Input Voltage $(Q - \overline{Q})$, Q = High $(\overline{Q} - Q)$, $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.3	1.2	2.2	V

Extended LVDS DC Specifications (LVDSEXT_25)

Table 10: **Extended LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.38	2.5	2.63	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals		–	1.785	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals	0.715	–	–	V
V_{ODIFF}	Differential Output Voltage $(Q - \overline{Q})$, Q = High $(\overline{Q} - Q)$, $\overline{Q}$ = High	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals	350	–	820	mV
V_{OCM}	Output Common-Mode Voltage	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals	1.025	1.250	1.475	V
V_{IDIFF}	Differential Input Voltage $(Q - \overline{Q})$, Q = High $(\overline{Q} - Q)$, $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	–	1000	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.3	1.2	2.2	V

LVPECL DC Specifications (LVPECL_25)

These values are valid when driving a 100Ω differential load only, i.e., a 100Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. Table 11 summarizes the DC output specifications of LVPECL. For more information on using LVPECL, see *Virtex-5 FPGA User Guide, Chapter 6, SelectIO Resources*.

Table 11: **LVPECL DC Specifications**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{OH}	Output High Voltage	V_{CC} – 1.025	1.545	V_{CC} – 0.88	V
V_{OL}	Output Low Voltage	V_{CC} – 1.81	0.795	V_{CC} – 1.62	V
V_{ICM}	Input Common-Mode Voltage	0.6		2.2	V
V_{IDIFF}	Differential Input Voltage(1)(2)	0.100		1.5	V

Notes:

1. Recommended input maximum voltage not to exceed V_{CCAUX} + 0.2V.
2. Recommended input minimum voltage not to go below –0.5V.

PowerPC 440 Switching Characteristics

Consult the *Embedded Processor Block in Virtex-5 FPGAs Reference Guide* for further information.

Table 12: **Processor Block Switching Characteristics**

Clock Name	Description	Speed Grade			Units
		-2I	-1I	-1M	
CPMC440CLK	CPU clock	475	400	400	MHz
CPMINTERCONNECTCLK	Xbar clock	316.6	266.6	266.6	MHz
CPMPPCS0PLBCLK	Slave 0 PLB clock(1)	158.3	133.3	133.3	MHz
CPMPPCS1PLBCLK	Slave 1 PLB clock(1)	158.3	133.3	133.3	MHz
CPMPPCMPLBCLK	Master PLB clock(1)	158.3	133.3	133.3	MHz
CPMMCCLK	Memory interface clock(1)(2)	316.6	266.6	266.6	MHz
CPMFCMCLK	FCM clock(1)	237.5	200	200	MHz
CPMDCRCLK	FPGA logic DCR clock(1)	158.3	133.3	133.3	MHz
CPMDMA0LLCLK	DMA0 LL clock(1)	250	200	200	MHz
CPMDMA1LLCLK	DMA1 LL clock(1)	250	200	200	MHz
CPMDMA2LLCLK	DMA2 LL clock(1)	250	200	200	MHz
CPMDMA3LLCLK	DMA3 LL clock(1)	250	200	200	MHz
JTGC440TCK	JTAG clock	50	50	50	MHz
CPMC440TIMERCLOCK	Timer clock	237.5	200	200	MHz

Notes:

1. Typical bus frequencies are provided for reference only, actual frequencies are user-design dependent.
2. Refer to DS567, *DDR2 Memory Controller for PowerPC 440 Processors*, for maximum clock speed of designs using the DDR2 Memory Controller for PowerPC® 440 processors.

Table 13: **Processor Block MIB Switching Characteristics**

Clock Name	Reference Clock	Speed Grade			Units
		-2I	-1I	-1M	
Clock-to-out and setup relative to clock					
$T_{CK\_CONTROL}$	CPMMCCLK	1.247	1.463	1.463	ps
$T_{CK\_ADDRESS}$	CPMMCCLK	1.136	1.38	1.38	ps
T_{CK_DATA}	CPMMCCLK	1.172	1.38	1.38	ps
$T_{CONTROL\_CK}$	CPMMCCLK	0.844	0.941	0.941	ps
T_{DATA_CK}	CPMMCCLK	0.95	1.058	1.058	ps

Table 14: **Processor Block PLBM Switching Characteristics**

Clock Name	Reference Clock	Speed Grade			Units
		-2I	-1I	-1M	
Clock-to-out and setup relative to clock					
$T_{CK\_CONTROL}$	CPMPPCMPLBCLK	1.095	1.354	1.354	ps
$T_{CK\_ADDRESS}$	CPMPPCMPLBCLK	1.372	1.673	1.673	ps
T_{CK_DATA}	CPMPPCMPLBCLK	1.257	1.535	1.535	ps
$T_{CONTROL\_CK}$	CPMPPCMPLBCLK	1.79	1.86	1.86	ps
T_{DATA_CK}	CPMPPCMPLBCLK	0.914	1.059	1.059	ps

Table 15: **Processor Block PLBS0 Switching Characteristics**

Clock Name	Reference Clock	Speed Grade			Units
		-2I	-1I	-1M	
Clock-to-out and setup relative to clock					
$T_{CK\_CONTROL}$	CPMPPCS0PLBCLK	1.196	1.462	1.462	ps
T_{CK_DATA}	CPMPPCS0PLBCLK	1.189	1.461	1.461	ps
$T_{CONTROL\_CK}$	CPMPPCS0PLBCLK	1.545	1.836	1.836	ps
$T_{ADDRESS\_CK}$	CPMPPCS0PLBCLK	1.492	1.787	1.787	ps
T_{DATA_CK}	CPMPPCS0PLBCLK	0.971	1.124	1.124	ps

Table 16: **Processor Block PLBS1 Switching Characteristics**

Clock Name	Reference Clock	Speed Grade			Units
		-2I	-1I	-1M	
Clock-to-out and setup relative to clock					
$T_{CK\_CONTROL}$	CPMPPCS1PLBCLK	1.234	1.525	1.525	ps
T_{CK_DATA}	CPMPPCS1PLBCLK	1.298	1.615	1.615	ps
$T_{CONTROL\_CK}$	CPMPPCS1PLBCLK	1.596	1.921	1.921	ps
$T_{ADDRESS\_CK}$	CPMPPCS1PLBCLK	1.568	1.864	1.864	ps
T_{DATA_CK}	CPMPPCS1PLBCLK	0.969	1.127	1.127	ps

Table 17: **Processor Block DMA0 Switching Characteristics**

Clock Name	Reference Clock	Speed Grade			Units
		-2I	-1I	-1M	
Clock-to-out and setup relative to clock					
$T_{CK\_CONTROL}$	CPMDMA0LLCLK	1.42	1.665	1.665	ps
T_{CK_DATA}	CPMDMA0LLCLK	1.472	1.712	1.712	ps
$T_{CONTROL\_CK}$	CPMDMA0LLCLK	0.558	0.716	0.716	ps
T_{DATA_CK}	CPMDMA0LLCLK	–0.105	–0.104	–0.104	ps

Table 18: **Processor Block DMA1 Switching Characteristics**

Clock Name	Reference Clock	Speed Grade			Units
		-2I	-1I	-1M	
Clock-to-out and setup relative to clock					
$T_{CK\_CONTROL}$	CPMDMA1LLCLK	1.266	1.474	1.474	ps
T_{CK_DATA}	CPMDMA1LLCLK	1.418	1.645	1.645	ps
$T_{CONTROL\_CK}$	CPMDMA1LLCLK	0.555	0.717	0.717	ps
T_{DATA_CK}	CPMDMA1LLCLK	0.01	0.046	0.046	ps

Table 19: **Processor Block DMA2 Switching Characteristics**

Clock Name	Reference Clock	Speed Grade			Units
		-2I	-1I	-1M	
Clock-to-out and setup relative to clock					
$T_{CK\_CONTROL}$	CPMDMA2LLCLK	1.235	1.437	1.437	ps
T_{CK_DATA}	CPMDMA2LLCLK	1.262	1.463	1.463	ps
$T_{CONTROL\_CK}$	CPMDMA2LLCLK	0.924	1.155	1.155	ps
T_{DATA_CK}	CPMDMA2LLCLK	0.142	0.168	0.168	ps

Table 20: **Processor Block DMA3 Switching Characteristics**

Clock Name	Reference Clock	Speed Grade			Units
		-2I	-1I	-1M	
Clock-to-out and setup relative to clock					
$T_{CK\_CONTROL}$	CPMDMA3LLCLK	1.242	1.462	1.462	ps
T_{CK_DATA}	CPMDMA3LLCLK	1.184	1.376	1.376	ps
$T_{CONTROL\_CK}$	CPMDMA3LLCLK	0.767	0.965	0.965	ps
T_{DATA_CK}	CPMDMA3LLCLK	0.119	0.116	0.116	ps

Table 21: **Processor Block DCR Switching Characteristics**

Clock Name	Reference Clock	Speed Grade			Units
		-2I	-1I	-1M	
Clock-to-out and setup relative to clock					
$T_{CK\_CONTROL}$	CPMDCRCLK	–	–	–	
$T_{CK\_ADDRESS}$	CPMDCRCLK	–	–	–	
T_{CK_DATA}	CPMDCRCLK	–	–	–	
$T_{CONTROL\_CK}$	CPMDCRCLK	–	–	–	
$T_{ADDRESS\_CK}$	CPMDCRCLK	–	–	–	
T_{DATA_CK}	CPMDCRCLK	–	–	–	

Table 22: **Processor Block FCM Switching Characteristics**

Clock Name	Reference Clock	Speed Grade			Units
		-2I	-1I	-1M	
Clock-to-out and setup relative to clock					
$T_{CK\_CONTROL}$	CPMFCMCLK	1.084	1.324	1.324	ps
T_{CK_DATA}	CPMFCMCLK	1.158	1.4	1.4	ps
$T_{CK\_INSTRUCTION}$	CPMFCMCLK	0.818	1.06	1.06	ps
$T_{CONTROL\_CK}$	CPMFCMCLK	1.218	1.395	1.395	ps
T_{DATA_CK}	CPMFCMCLK	0.698	0.768	0.768	ps
T_{RESULT_CK}	CPMFCMCLK	0.698	0.768	0.768	ps

Table 23: **Processor Block MISC Switching Characteristics**

Clock Name	Reference Clock	Speed Grade			Units
		-2I	-1I	-1M	
Clock-to-out and setup relative to clock					
$T_{CK\_CONTROL}$	CLK1	–	–	–	
$T_{CK\_ADDRESS}$	CLK2	–	–	–	
T_{CK_DATA}	CLK3	–	–	–	
$T_{CONTROL\_CK}$	CLK4	–	–	–	
$T_{ADDRESS\_CK}$	CLK5	–	–	–	
T_{DATA_CK}	CLK6	–	–	–	

GTP_DUAL Tile Specifications

GTP_DUAL Tile DC Characteristics

Table 24: **Absolute Maximum Ratings for GTP_DUAL Tiles**

Symbol	Description		Units
MGTAVCCPLL	Analog supply voltage for the GTP_DUAL shared PLL relative to GND	–0.5 to 1.32	V
MGTAVTTTX	Analog supply voltage for the GTP_DUAL transmitters relative to GND	–0.5 to 1.32	V
MGTAVTTRX	Analog supply voltage for the GTP_DUAL receivers relative to GND	–0.5 to 1.32	V
MGTAVCC	Analog supply voltage for the GTP_DUAL common circuits relative to GND	–0.5 to 1.1	V
MGTAVTTRXC	Analog supply voltage for the resistor calibration circuit of the GTP_DUAL column	–0.5 to 1.32	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 25: **Recommended Operating Conditions for GTP_DUAL Tiles(1)(2)**

Symbol	Description	Min	Max	Units
MGTAVCCPLL(1)	Analog supply voltage for the GTP_DUAL shared PLL relative to GND	1.14	1.26	V
MGTAVTTTX(1)	Analog supply voltage for the GTP_DUAL transmitters relative to GND	1.14	1.26	V
MGTAVTTRX(1)	Analog supply voltage for the GTP_DUAL receivers relative to GND	1.14	1.26	V
MGTAVCC(1)	Analog supply voltage for the GTP_DUAL common circuits relative to GND	0.95	1.05	V
MGTAVTTRXC(1)	Analog supply voltage for the resistor calibration circuit of the GTP_DUAL column	1.14	1.26	V

Notes:

1. Each voltage listed requires the filter circuit described in *Virtex-5 FPGA RocketIO GTP Transceiver User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +100°C.

Table 26: **DC Characteristics Over Recommended Operating Conditions for GTP_DUAL Tiles(1)**

Symbol	Description	Min	Typ	Max	Units
$I_{MGTAVTTTX}$	GTP_DUAL tile transmitter termination supply current(2)		71	90	mA
$I_{MGTAVCCPLL}$	GTP_DUAL tile shared PLL supply current		36	60	mA
$I_{MGTAVTTRXC}$	GTP_DUAL tile resistor termination calibration supply current		0.1	0.5	mA
$I_{MGTAVTTRX}$	GTP_DUAL tile receiver termination supply current(3)		0.1	0.5	mA
$I_{MGTAVCC}$	GTP_DUAL tile internal analog supply current		56	110	mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	49.9 ± 1% tolerance			Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 3.2 Gb/s line rate.
2. I_{CC} numbers are given per GTP_DUAL tile with both GTP transceivers operating with default settings.
3. AC coupled TX/RX link.

Table 27: **GTP_DUAL Tile Quiescent Supply Current**

Symbol	Description	Typ(1)	Max	Units
$I_{AVTTTXQ}$	Quiescent MGTAVTTTX (transmitter termination) supply current	8.5	18	mA
$I_{AVCCPLLQ}$	Quiescent MGTAVCCPLL (PLL) supply current	8	18	mA
$I_{AVTTRXQ}$	Quiescent MGTAVTTRX (receiver termination) supply current. Includes MGTAVTTRXCQ.	0.1	0.8	mA
I_{AVCCQ}	Quiescent MGTAVCC (analog) supply current	2.5	11	mA

Notes:
1. Typical values are specified at nominal voltage, 25°C.
2. Device powered and unconfigured.
3. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
4. GTP_DUAL tile quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTP_DUAL tiles in the target LXT or SXT device.

GTP_DUAL Tile DC Input and Output Levels

Table 28 summarizes the DC output specifications of the GTP_DUAL tiles in Virtex-5Q FPGAs. Figure 1, page 14 shows the single-ended output voltage swing. Figure 2, page 14 shows the peak-to-peak differential output voltage.

Consult *Virtex-5 FPGA RocketIO GTP Transceiver User Guide* for further details.

Table 28: **GTP_DUAL Tile DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled ≤ 3.2 Gb/s	150		2000	mV
		External AC coupled > 3.2 Gb/s	180		2000	mV
V_{IN}	Absolute input voltage	DC coupled	–400		MGTAVTTRX + 400 up to 1320	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTAVTTRX = 1.2V		800		mV
DV_{PPOUT}	Differential peak-to-peak output voltage(1)	TXBUFDIFFCTRL = 000, TX_DIFF_BOOST = ON			1400	mV
V_{SEOUT}	Single-ended output voltage swing(1)	TXBUFDIFFCTRL = 000, TX_DIFF_BOOST = ON			700	mV
V_{CMOUT}	Common mode output voltage	Equation based MGTAVTTTX = 1.2V	1200 – Amplitude/2			mV
R_{IN}	Differential input resistance		90	100	120	Ω
R_{OUT}	Differential output resistance		90	100	120	Ω
T_{OSKEW}	Transmitter output skew				15	ps
C_{EXT}	Recommended external AC coupling capacitor(2)		75	100	200	nF

Notes:
1. The output swing and preemphasis levels are programmable using the attributes discussed in *Virtex-5 FPGA RocketIO GTP Transceiver User Guide* and can result in values lower than reported in this table.
2. Values outside of this range can be used as appropriate to conform to specific protocols and standards.

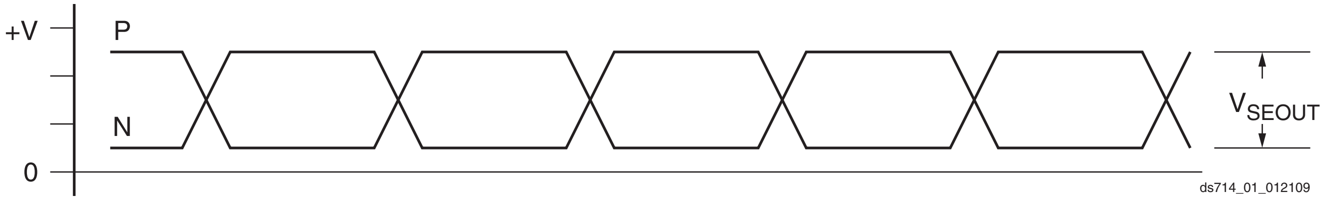

Figure 1: **Single-Ended Output Voltage Swing**

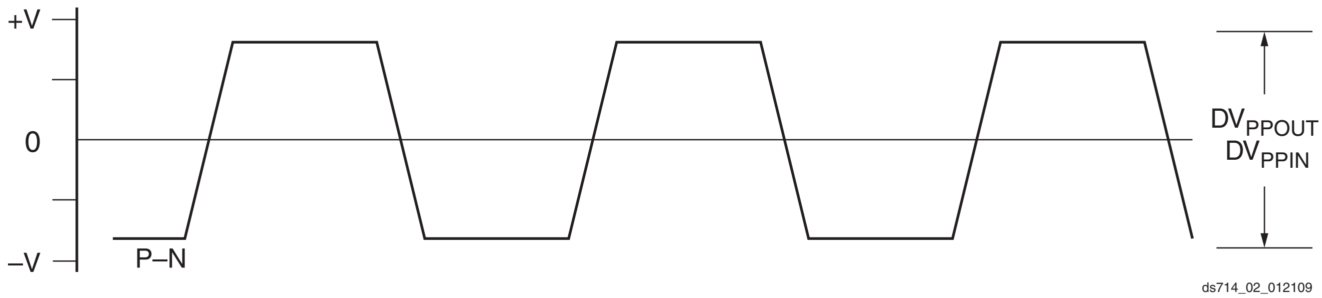

Figure 2: **Peak-to-Peak Differential Output Voltage**

Table 29 summarizes the DC specifications of the clock input of the GTP_DUAL tile. Figure 3 shows the single-ended input voltage swing. Figure 4 shows the peak-to-peak differential clock input voltage swing. Consult *Virtex-5 FPGA RocketIO GTP Transceiver User Guide* for further details.

Table 29: **GTP_DUAL Tile Clock DC Input Specifications(1)**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage		200	800	2000	mV
V_{ISE}	Single-ended input voltage		100	400	1000	mV
R_{IN}	Differential input resistance		80	105	130	Ω
C_{EXT}	Required external AC coupling capacitor		75	100	200	nF

Notes:

1. V_{MIN} = 0V and V_{MAX} = 1200 mV

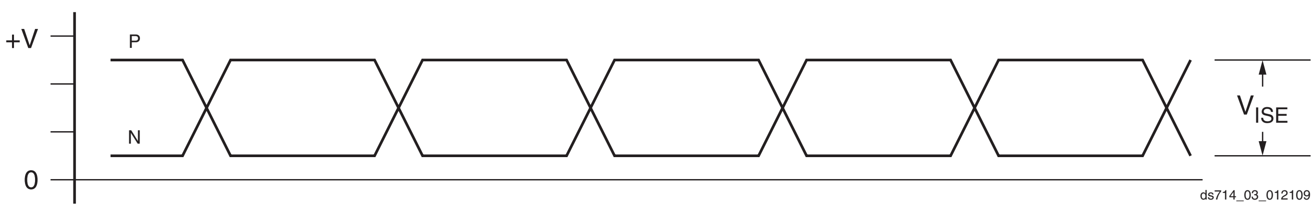

Figure 3: **Single-Ended Clock Input Voltage Swing Peak-to-Peak**

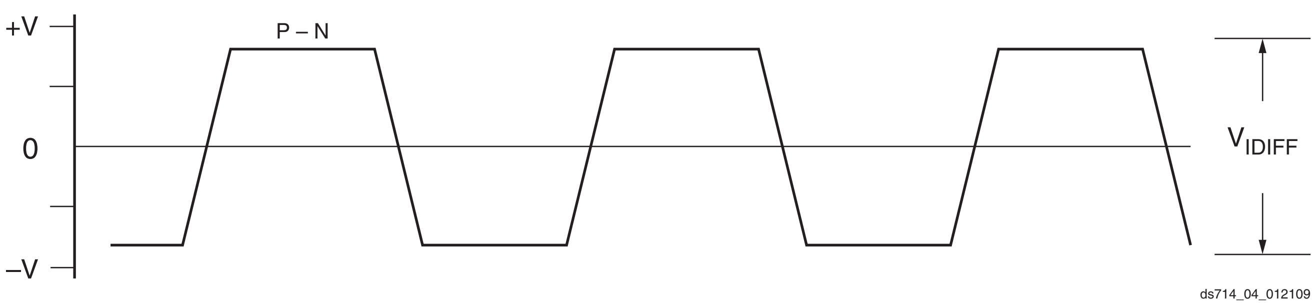

Figure 4: **Differential Clock Input Voltage Swing Peak-to-Peak**

GTP_DUAL Tile Switching Characteristics

Consult *Virtex-5 FPGA RocketIO GTP Transceiver User Guide* for further information.

Table 30: **GTP_DUAL Tile Performance**

Symbol	Description	Speed Grade		Units
		-2I	-1I	
F_{GTPMAX}	Maximum GTP transceiver data rate	3.75	3.2	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	2.0	2.0	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	1.0	1.0	GHz

Table 31: **Dynamic Reconfiguration Port (DRP) in the GTP_DUAL Tile Switching Characteristics**

Symbol	Description	Speed Grade		Units
		-2I	-1I	
$F_{GTPDRPCLK}$	GTPDRPCLK maximum frequency	175	150	MHz

Table 32: **GTP_DUAL Tile Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range(1)	CLK	60		350	MHz
T_{RCLK}	Reference clock rise time	20% – 80%		200	400	ps
T_{FCLK}	Reference clock fall time	80% – 20%		200	400	ps
T_{DCREF}	Reference clock duty cycle(2)	CLK	40	50	60	%
T_{GJTT}	Reference clock total jitter, peak-peak(3)	CLK			40	ps
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock			1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock			200	µs

Notes:

1. The clock from the GTP_DUAL differential clock pin pair can be used for all serial bit rates. GREFCLK can be used for serial bit rates up to 1 Gb/s.
2. For reference clock rates above 325 MHz, a duty cycle of 45% to 55% must be maintained.
3. Measured at the package pin. GTP_DUAL jitter characteristics measured using a clock with specification T_{GJTT}.

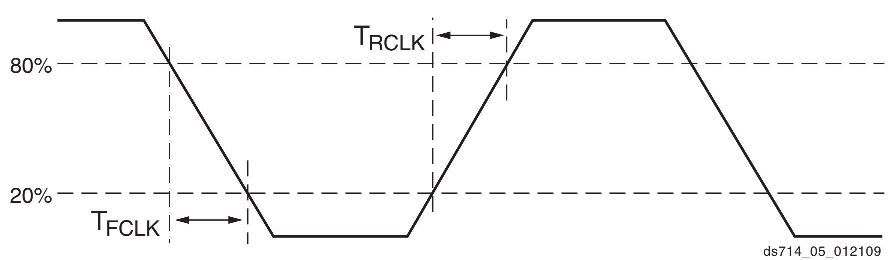

Figure 5: **Reference Clock Timing Parameters**

Table 33: **GTP_DUAL Tile User Clock Switching Characteristics**[(1)]

Symbol	Description	Conditions	Speed Grade		Units
			-2I	-1I	
F_{TXOUT}	TXOUTCLK maximum frequency		375	320	MHz
F_{RXREC}	RXRECCLK maximum frequency		375	320	MHz
T_{RX}	RXUSRCLK maximum frequency		375	320	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	RXDATAWIDTH = 0	350	320	MHz
		RXDATAWIDTH = 1	187.5	160	MHz
T_{TX}	TXUSRCLK maximum frequency		375	320	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	TXDATAWIDTH = 0	350	320	MHz
		TXDATAWIDTH = 1	187.5	160	MHz

Notes:
1. Clocking must be implemented as described in *Virtex-5 FPGA RocketIO GTP Transceiver User Guide.*

Table 34: **GTP_DUAL Tile Transmitter Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTPTX}	Serial data rate range		0.1		F_{GTPMAX}	Gb/s
T_{RTX}	TX Rise time			140		ps
T_{FTX}	TX Fall time			120		ps
T_{LLSKEW}	TX lane-to-lane skew[(1)]				855	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude				20	mV
$T_{TXOOBTRANS}$	Electrical idle transition time				40	ns
$T_{J3.75}$	Total Jitter[(2)]	3.75 Gb/s			0.35	UI
$D_{J3.75}$	Deterministic Jitter[(2)]				0.19	UI
$T_{J3.2}$	Total Jitter[(2)]	3.20 Gb/s			0.35	UI
$D_{J3.2}$	Deterministic Jitter[(2)]				0.19	UI
$T_{J2.5}$	Total Jitter[(2)]	2.50 Gb/s			0.30	UI
$D_{J2.5}$	Deterministic Jitter[(2)]				0.14	UI
$T_{J2.0}$	Total Jitter[(2)]	2.00 Gb/s			0.30	UI
$D_{J2.0}$	Deterministic Jitter[(2)]				0.14	UI
$T_{J1.25}$	Total Jitter[(2)]	1.25 Gb/s			0.20	UI
$D_{J1.25}$	Deterministic Jitter[(2)]				0.10	UI
$T_{J1.00}$	Total Jitter[(2)]	1.00 Gb/s			0.20	UI
$D_{J1.00}$	Deterministic Jitter[(2)]				0.10	UI
T_{J500}	Total Jitter[(2)]	500 Mb/s			0.10	UI
D_{J500}	Deterministic Jitter[(2)]				0.04	UI
T_{J100}	Total Jitter[(2)]	100 Mb/s			0.02	UI
D_{J100}	Deterministic Jitter[(2)]				0.01	UI

Notes:
1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTP_DUAL sites.
2. Using PLL_DIVSEL_FB = 2, INTDATAWIDTH = 1.
3. All jitter values are based on a Bit-Error Ratio of $1e^{-12}$.

Table 35: **GTP_DUAL Tile Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTPRX}	Serial data rate	RX oversampler not enabled	0.5		F_{GTPMAX}	Gb/s
		RX oversampler enabled	0.1		0.5	Gb/s
$R_{XOOBVDPP}$	OOB detect threshold peak-to-peak	OOBDETECT_THRESHOLD = 100	60	105	165	mV
R_{XSST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000		0	ppm
R_{XRL}	Run length (CID)	Internal AC capacitor bypassed			150	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	CDR 2nd-order loop disabled with PLL_RXDIVSEL_OUT = 1(2)	–200		200	ppm
		CDR 2nd-order loop disabled with PLL_RXDIVSEL_OUT = 2(2)	–200		200	ppm
		CDR 2nd-order loop disabled with PLL_RXDIVSEL_OUT = 4(2)	–100		100	ppm
		CDR 2nd-order loop enabled	–1000		1000	ppm
SJ Jitter Tolerance						
$JT\_SJ_{3.75}$	Sinusoidal Jitter(3)	3.75 Gb/s	0.30			UI
$JT\_SJ_{3.2}$	Sinusoidal Jitter(3)	3.20 Gb/s	0.40			UI
$JT\_SJ_{2.50}$	Sinusoidal Jitter(3)	2.50 Gb/s	0.40			UI
$JT\_SJ_{2.00}$	Sinusoidal Jitter(3)	2.00 Gb/s	0.40			UI
$JT\_SJ_{1.00}$	Sinusoidal Jitter(3)	1.00 Gb/s	0.30			UI
JT_SJ_{500}	Sinusoidal Jitter(3)	500 Mb/s	0.30			UI
JT_SJ_{500}	Sinusoidal Jitter(3)	500 Mb/s OS	0.30			UI
JT_SJ_{100}	Sinusoidal Jitter(3)	100 Mb/s OS	0.30			UI
SJ Jitter Tolerance with Stressed Eye						
$JT\_TJSE_{3.2}$	Total Jitter with Stressed Eye(4)	3.20 Gb/s	0.87			UI
$JT\_SJSE_{3.2}$	Sinusoidal Jitter with Stressed Eye(4)	3.20 Gb/s	0.30			UI

Notes:

1. Using PLL_RXDIVSEL_OUT = 1 only.
2. CDR 1st-order step size set to 2.
3. Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
4. Stimulus signal includes 0.4UI of DJ and 0.17UI of RJ. RX equalizer is enabled.
5. All jitter values are based on a Bit Error Ratio of $1e^{-12}$.

GTX_DUAL Tile Specifications

GTX_DUAL Tile DC Characteristics

Table 36: **Absolute Maximum Ratings for GTX_DUAL Tiles**

Symbol	Description		Units
MGTAVCCPLL	Analog supply voltage for the GTX_DUAL shared PLL relative to GND	–0.5 to 1.1	V
MGTAVTTTX	Analog supply voltage for the GTX_DUAL transmitters relative to GND	–0.5 to 1.32	V
MGTAVTTRX	Analog supply voltage for the GTX_DUAL receivers relative to GND	–0.5 to 1.32	V
MGTAVCC	Analog supply voltage for the GTX_DUAL common circuits relative to GND	–0.5 to 1.1	V
MGTAVTTRXC	Analog supply voltage for the resistor calibration circuit of the GTX_DUAL column	–0.5 to 1.32	V

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 37: **Recommended Operating Conditions for GTX_DUAL Tiles(1)(2)**

Symbol	Description	Min	Max	Units
MGTAVCCPLL(1)	Analog supply voltage for the GTX_DUAL shared PLL relative to GND	0.95	1.05	V
MGTAVTTTX(1)	Analog supply voltage for the GTX_DUAL transmitters relative to GND	1.14	1.26	V
MGTAVTTRX(1)	Analog supply voltage for the GTX_DUAL receivers relative to GND	1.14	1.26	V
MGTAVCC(1)	Analog supply voltage for the GTX_DUAL common circuits relative to GND	0.95	1.05	V
MGTAVTTRXC(1)	Analog supply voltage for the resistor calibration circuit of the GTX_DUAL column	1.14	1.26	V

Notes:

1. Each voltage listed requires the filter circuit described in *Virtex-5 FPGA RocketIO GTX Transceiver User Guide*.
2. Voltages are specified for the temperature range of T_j = –40°C to +100°C.

Table 38: **DC Characteristics Over Recommended Operating Conditions for GTX_DUAL Tiles(1)**

Symbol	Description	Min	Typ	Max	Units
$I_{MGTAVTTTX}$	GTX_DUAL tile transmitter termination supply current(2)		43.3	86.3	mA
$I_{MGTAVCCPLL}$	GTX_DUAL tile shared PLL supply current		38.0	99.4	mA
$I_{MGTAVTTRXC}$	GTX_DUAL tile resistor termination calibration supply current		0.1	0.5	mA
$I_{MGTAVTTRX}$	GTX_DUAL tile receiver termination supply current(3)		40.3	56.5	mA
$I_{MGTAVCC}$	GTX_DUAL tile internal analog supply current		80.5	179.5	mA
$MGTR_{REF}$	Precision reference resistor for internal calibration termination	59.0 ± 1% tolerance			Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 3.2 Gb/s line rate.
2. I_{CC} numbers are given per GTX_DUAL tile with both GTX transceivers operating with default settings.
3. AC coupled TX/RX link.
4. Values for currents other than the values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.

Table 39: **GTX_DUAL Tile Quiescent Supply Current**

Symbol	Description	Typ(1)	Max	Units
$I_{AVTTTXQ}$	Quiescent MGTAVTTTX (transmitter termination) supply current	8.2	21.6	mA
$I_{AVCCPLLQ}$	Quiescent MGTAVCCPLL (PLL) supply current	0.8	4.8	mA
$I_{AVTTRXQ}$	Quiescent MGTAVTTRX (receiver termination) supply current. Includes MGTAVTTRXCQ.	1.2	12.0	mA
I_{AVCCQ}	Quiescent MGTAVCC (analog) supply current	9.0	50.4	mA

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. Device powered and unconfigured.
3. Currents for conditions other than values specified in this table can be obtained by using the XPOWER Estimator (XPE) or XPOWER Analyzer (XPA) tools.
4. GTX_DUAL tile quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTX_DUAL tiles in the target FXT device.

GTX_DUAL Tile DC Input and Output Levels

Table 40 summarizes the DC output specifications of the GTX_DUAL tiles in Virtex-5Q FPGAs. Figure 6, page 20 shows the single-ended output voltage swing. Figure 7, page 20 shows the peak-to-peak differential output voltage.

Consult *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* for further details.

Table 40: **GTX_DUAL Tile DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPIN}	Differential peak-to-peak input voltage	External AC coupled ≤ 4.25 Gb/s	200		1800	mV
		External AC coupled > 4.25 Gb/s	125		1800	mV
V_{IN}	Absolute input voltage	DC coupled MGTAVTTRX = 1.2V	–400		MGTAVTTRX +400 up to 1320	mV
V_{CMIN}	Common mode input voltage	DC coupled MGTAVTTRX = 1.2V		800		mV
DV_{PPOUT}	Differential peak-to-peak output voltage(1)	TXBUFDIFFCTRL = `111`			1400	mV
V_{SEOUT}	Single-ended output voltage swing(1)	TXBUFDIFFCTRL = `111`			700	mV
V_{CMOUT}	Common mode output voltage	Equation based MGTAVTTTX = 1.2V	$1200 - DV_{PPOUT}/2$			mV
R_{IN}	Differential input resistance		85	100	120	Ω
R_{OUT}	Differential output resistance		85	100	120	Ω
T_{OSKEW}	Transmitter output skew			2	8	ps
C_{EXT}	Recommended external AC coupling capacitor(2)		75	100	200	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* and can result in values lower than reported in this table.
2. Values outside of this range can be used as appropriate to conform to specific protocols and standards.

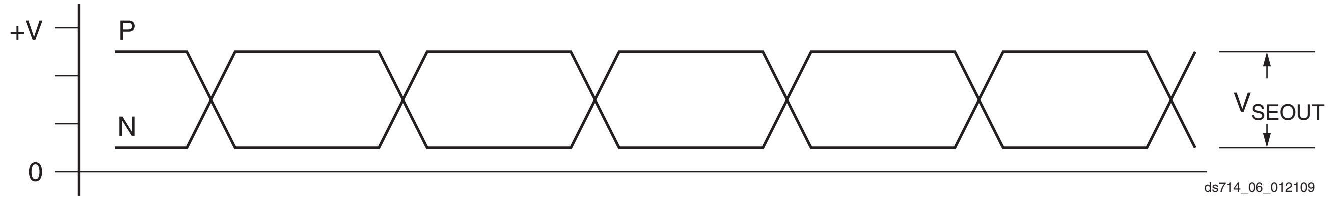

Figure 6: **Single-Ended Output Voltage Swing**

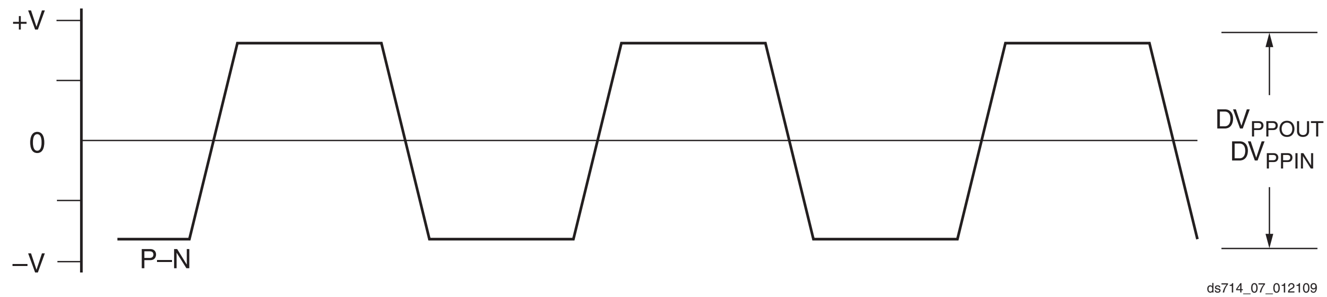

Figure 7: **Peak-to-Peak Differential Output Voltage**

Table 41 summarizes the DC specifications of the clock input of the GTX_DUAL tile. Figure 8 shows the single-ended input voltage swing. Figure 9 shows the peak-to-peak differential clock input voltage swing. Consult *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* for further details.

Table 41: **GTX_DUAL Tile Clock DC Input Level Specification(1)**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage		210	800	2000	mV
V_{ISE}	Single-ended input voltage		105	400	750	mV
R_{IN}	Differential input resistance		90	105	130	Ω
C_{EXT}	Required external AC coupling capacitor			100		nF

Notes:

1. V_{MIN} = 0V and V_{MAX} = 1200 mV

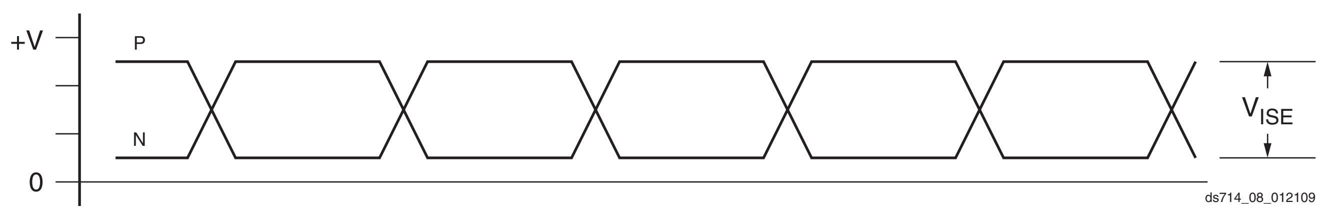

Figure 8: **Single-Ended Clock Input Voltage Swing Peak-to-Peak**

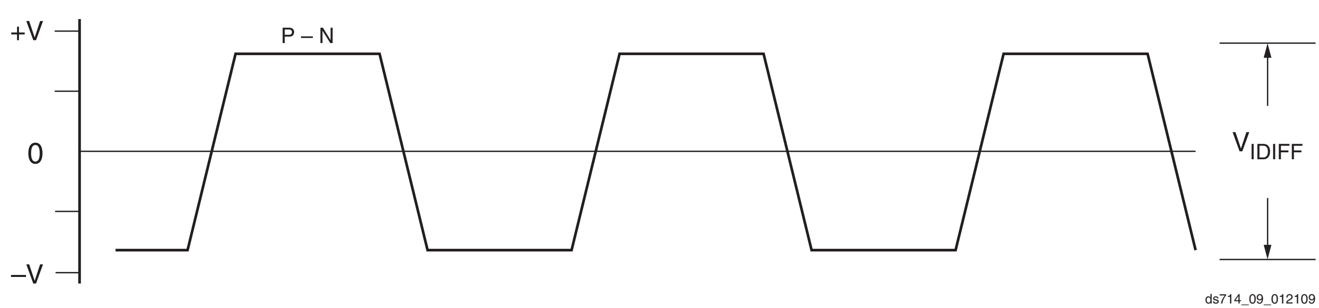

Figure 9: **Differential Clock Input Voltage Swing Peak-to-Peak**

GTX_DUAL Tile Switching Characteristics

Consult *Virtex-5 FPGA RocketIO GTX Transceiver User Guide* for further information.

Table 42: **GTX_DUAL Tile Performance**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
F_{GTXMAX}	Maximum GTX transceiver data rate	6.5	4.25	4.25	Gb/s
$F_{GPLLMAX}$	Maximum PLL frequency	3.25	3.25	3.25	GHz
$F_{GPLLMIN}$	Minimum PLL frequency	1.5	1.5	1.5	GHz

Table 43: **Dynamic Reconfiguration Port (DRP) in the GTX_DUAL Tile Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
$F_{GTXDRPCLK}$	GTXDRPCLK maximum frequency	175	150	150	MHz

Table 44: **GTX_DUAL Tile Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range[(1)]	CLK	60		650	MHz
T_{RCLK}	Reference clock rise time	20% – 80%		200		ps
T_{FCLK}	Reference clock fall time	80% – 20%		200		ps
T_{DCREF}	Reference clock duty cycle	CLK	40	50	60	%
T_{GJTT}	Reference clock total jitter[(2)(3)]	At 100 KHz		–145		dBc/Hz
		At 1 MHz		–150		dBc/Hz
T_{LOCK}	Clock recovery frequency acquisition time	Initial PLL lock		0.25	1	ms
T_{PHASE}	Clock recovery phase acquisition time	Lock to data after PLL has locked to the reference clock			200	µs

Notes:

1. GREFCLK can be used for serial bit rates up to 1 Gb/s; however, Jitter Specifications are not guaranteed when using GREFCLK.
2. GTX_DUAL jitter characteristics measured using a clock with specification T_{GJTT}. A reference clock with higher phase noise can be used with link margin trade off.
3. The selection of the reference clock is application dependent. This parameter describes the quality of the reference clock used during transceiver jitter characterization - see Table 46, page 22 and Table 47, page 23.

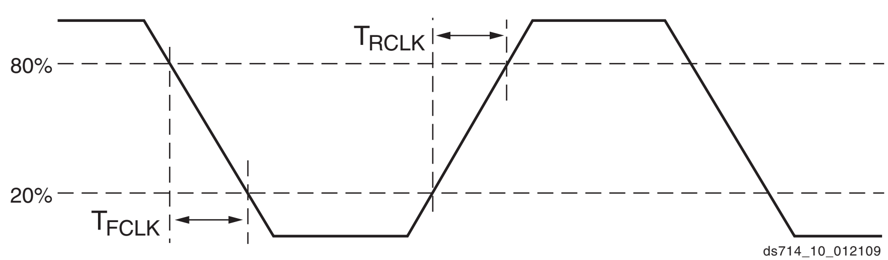

Figure 10: **Reference Clock Timing Parameters**

Table 45: **GTX_DUAL Tile User Clock Switching Characteristics**

Symbol	Description	Conditions	Device	Speed Grade			Units
				-2I	-1I	-1M	
F_{TXOUT}	TXOUTCLK maximum frequency	Internal 20-bit datapath	FXT	325	212.5	212.5	MHz
		Internal 16-bit datapath	FXT	406.25	265.625	265.625	MHz
F_{RXREC}	RXRECCLK maximum frequency		FXT	406.25	265.625	265.625	MHz
T_{RX}	RXUSRCLK maximum frequency	2 byte or 4 byte interface	FXT	406.25	265.625	265.625	MHz
T_{RX2}	RXUSRCLK2 maximum frequency	1 byte interface	FXT	312.5	235.625	235.625	MHz
		2 byte interface		390.625	265.625	265.625	MHz
		4 byte interface		203.125	132.813	132.813	MHz
T_{TX}	TXUSRCLK maximum frequency	2 byte or 4 byte interface	FXT	406.25	265.625	265.625	MHz
T_{TX2}	TXUSRCLK2 maximum frequency	1 byte interface	FXT	312.5	235.625	235.625	MHz
		2 byte interface		390.625	265.625	265.625	MHz
		4 byte interface		203.125	132.813	132.813	MHz

Table 46: **GTX_DUAL Tile Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTXTX}	Serial data rate range		0.15		F_{GTXMAX}	Gb/s
T_{RTX}	TX Rise time	20%–80%		120		ps
T_{FTX}	TX Fall time	80%–20%		120		ps
T_{LLSKEW}	TX lane-to-lane skew(1)				350	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude				15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time				75	ns
$T_{J6.5}$	Total Jitter(2)	6.5 Gb/s			0.33	UI
$D_{J6.5}$	Deterministic Jitter(2)				0.17	UI
$T_{J5.0}$	Total Jitter(2)	5.0 Gb/s			0.33	UI
$D_{J5.0}$	Deterministic Jitter(2)				0.15	UI
$T_{J4.25}$	Total Jitter(2)	4.25 Gb/s			0.35(5)	UI
$D_{J4.25}$	Deterministic Jitter(2)				0.14	UI
$T_{J3.75}$	Total Jitter(2)	3.75 Gb/s			0.34	UI
$D_{J3.75}$	Deterministic Jitter(2)				0.16	UI
$T_{J3.2}$	Total Jitter(2)	3.2 Gb/s			0.20	UI
$D_{J3.2}$	Deterministic Jitter(2)				0.10	UI
$T_{J3.2L}$	Total Jitter(2)	3.2 Gb/s(3)			0.36	UI
$D_{J3.2L}$	Deterministic Jitter(2)				0.16	UI
$T_{J2.5}$	Total Jitter(2)	2.5 Gb/s			0.20	UI
$D_{J2.5}$	Deterministic Jitter(2)				0.08	UI
$T_{J1.25}$	Total Jitter(2)	1.25 Gb/s			0.15	UI
$D_{J1.25}$	Deterministic Jitter(2)				0.06	UI
T_{J750}	Total Jitter(2)(4)	750 Mb/s			0.10	UI
D_{J750}	Deterministic Jitter(2)(4)				0.03	UI
T_{J150}	Total Jitter(2)(4)	150 Mb/s			0.02	UI
D_{J150}	Deterministic Jitter(2)(4)				0.01	UI

Notes:

1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTX_DUAL sites.
2. Using PLL_DIVSEL_FB = 2, INTDATAWIDTH = 1. These values are NOT intended for protocol specific compliance determinations.
3. PLL frequency at 1.6 GHz and OUTDIV = 1.
4. GREFCLK can be used for serial data rates up to 1.0 Gb/s, but performance is not guaranteed.
5. M-temperature only (0.33 UI for I-temperature)

Table 47: **GTX_DUAL Tile Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTXRX}	Serial data rate	RX oversampler not enabled	0.75		F_{GTXMAX}	Gb/s
		RX oversampler enabled	0.15		0.75	Gb/s
$T_{RXELECIDLE}$	TIme for RXELECIDLE to respond to loss or restoration of data	OOBDETECT_THRESHOLD = `110`			75	ns
$R_{XOOBVDPP}$	OOB detect threshold peak-to-peak	OOBDETECT_THRESHOLD = `110`	55		135	mV
R_{XSST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000		0	ppm
R_{XRL}	Run length (CID)	Internal AC capacitor bypassed			512	UI
$R_{XPPMTOL}$	Data/REFCLK PPM offset tolerance	CDR 2nd-order loop disabled	–200		200	ppm
		CDR 2nd-order loop enabled	–2000		2000	ppm
SJ Jitter Tolerance(2)						
$JT\_SJ_{6.5}$	Sinusoidal Jitter(3)	6.5 Gb/s	0.44			UI
$JT\_SJ_{5.0}$	Sinusoidal Jitter(3)	5.0 Gb/s	0.44			UI
$JT\_SJ_{4.25}$	Sinusoidal Jitter(3)	4.25 Gb/s	0.44			UI
$JT\_SJ_{3.75}$	Sinusoidal Jitter(3)	3.75 Gb/s	0.44			UI
$JT\_SJ_{3.2}$	Sinusoidal Jitter(3)	3.2 Gb/s	0.45			UI
$JT\_SJ_{3.2L}$	Sinusoidal Jitter(3)	3.2 Gb/s(4)	0.45			UI
$JT\_SJ_{2.5}$	Sinusoidal Jitter(3)	2.5 Gb/s	0.50			UI
$JT\_SJ_{1.25}$	Sinusoidal Jitter(3)	1.25 Gb/s	0.50			UI
JT_SJ_{750}	Sinusoidal Jitter(3)(5)	750 Mb/s	0.57			UI
JT_SJ_{150}	Sinusoidal Jitter(3)(5)	150 Mb/s	0.57			UI
SJ Jitter Tolerance with Stressed Eye(2)						
$JT\_TJSE_{4.25}$	Total Jitter with Stressed Eye(6)	4.25 Gb/s	0.69			UI
$JT\_SJSE_{4.25}$	Sinusoidal Jitter with Stressed Eye(6)	4.25 Gb/s	0.1			UI

Notes:
1. Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
2. All jitter values are based on a Bit Error Ratio of $1e^{-12}$.
3. Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
4. PLL frequency at 1.6 GHz and OUTDIV = 1.
5. GREFCLK can be used for serial data rates up to 1.0 Gb/s, but performance is not guaranteed.
6. Composite jitter with RX equalizer enabled. DFE disabled.

CRC Block Switching Characteristics

Table 48: **CRC Block Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
F_{CRC}	CRCCLK maximum frequency	325	270	270	MHz

Ethernet MAC Switching Characteristics

Consult *Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC User Guide* for further information.

Table 49: **Maximum Ethernet MAC Performance**

Symbol	Description	Conditions	Speed Grade			Units
			-2I	-1I	-1M	
$F_{TEMACCLIENT}$	Client interface maximum frequency	10 Mb/s – 8-bit width	1.25	1.25	1.25	MHz
		100 Mb/s – 8-bit width	12.5	12.5	12.5	MHz
		1000 Mb/s – 8-bit width	125	125	125	MHz
		2000 Mb/s – 16-bit width	125	125	125	MHz
$F_{TEMACPHY}$	Physical interface maximum frequency	10 Mb/s – 4-bit width	2.5	2.5	2.5	MHz
		100 Mb/s – 4-bit width	25	25	25	MHz
		1000 Mb/s – 8-bit width	125	125	125	MHz
		2000 Mb/s – 8-bit width	250	250	250	MHz

Endpoint Block for PCI Express Designs Switching Characteristics

Consult *Virtex-5 FPGA Integrated Endpoint Block for PCI Express Designs User Guide* for further information.

Table 50: **Maximum Performance for PCI Express Designs**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
$F_{PCIECORE}$	Core clock maximum frequency	250	250	250	MHz
$F_{PCIEUSER}$	User clock maximum frequency	250	250	250	MHz

System Monitor Analog-to-Digital Converter Specification

Table 51: **Analog-to-Digital Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
AV_{DD} = 2.5V ± 2%, V_{REFP} = 2.5V, V_{REFN} = 0V, ADCCLK = 5.2 MHz, T_A = T_{MIN} to T_{MAX}, Typical values at T_A=+25°C						
DC Accuracy: All external input channels such as V_P/V_N and V_{AUXP}[15:0]/V_{AUXN}[15:0], Unipolar Mode, and Common Mode = 0V						
Resolution			10			Bits
Integral Nonlinearity	INL				±2	LSBs
Differential Nonlinearity	DNL	No missing codes (T_{MIN} to T_{MAX}) Guaranteed Monotonic			±0.9	LSBs
Unipolar Offset Error(1)		Uncalibrated		±2	±30	LSBs
Bipolar Offset Error(1)		Uncalibrated measured in bipolar mode		±2	±30	LSBs
Gain Error(1)		Uncalibrated, T_j = –40°C to 100°C		±0.2	±2.0	%
		Uncalibrated, T_j = –55°C to 125°C		±0.2	±2.5	%
Bipolar Gain Error(1)		Uncalibrated measured in bipolar mode, T_j = –40°C to 100°C		±0.2	±2.0	%
		Uncalibrated measured in bipolar mode, T_j = –55°C to 125°C		±0.2	±2.5	%
Total Unadjusted Error (Uncalibrated)	TUE	Deviation from ideal transfer function. V_{REFP} – V_{REFN} = 2.5V		±10		LSBs
Total Unadjusted Error (Calibrated)	TUE	Deviation from ideal transfer function. V_{REFP} – V_{REFN} = 2.5V		±1	±2	LSBs
Calibrated Gain Temperature Coefficient		Variation of FS code with temperature		±0.01		LSB/°C
DC Common-Mode Reject	$CMRR_{DC}$	V_N = V_{CM} = 0.5V ± 0.5V, V_P – V_N = 100mV		70		dB
Conversion Rate(2)						
Conversion Time - Continuous	t_{CONV}	Number of CLK cycles	26		32	
Conversion Time - Event	t_{CONV}	Number of CLK cycles			21	
T/H Acquisition Time	t_{ACQ}	Number of CLK cycles	4			
DRP Clock Frequency	DCLK	DRP clock frequency	8		250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK, T_j = –40°C to 100°C	1		5.2	MHz
		Derived from DCLK, T_j = –55°C to 125°C	2.5		5.2	MHz
CLK Duty cycle			40		60	%
Analog Inputs(3)						
Dedicated Analog Inputs Input Voltage Range V_P - V_N		Unipolar Operation	0		1	V
		Differential Inputs	–0.25		+0.25	
		Unipolar Common Mode Range (FS input)	0		+0.5	
		Differential Common Mode Range (FS input)	+0.3		+0.7	
		Bandwidth		20		MHz
Auxiliary Analog Inputs Input Voltage Range $V_{AUXP[0]}$ /$V_{AUXN[0]}$ to $V_{AUXP[15]}$ /$V_{AUXN[15]}$		Unipolar Operation	0		1	Volts
		Differential Operation	–0.25		+0.25	
		Unipolar Common Mode Range (FS input)	0		+0.5	
		Differential Common Mode Range (FS input)	+0.3		+0.7	
		Bandwidth		10		kHz
Input Leakage Current		A/D not converting, ADCCLK stopped		±1.0		µA
Input Capacitance				10		pF
On-chip Supply Monitor Error		V_{CCINT} and V_{CCAUX} with calibration enabled			±1.0	% Reading

Table 51: **Analog-to-Digital Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
On-chip Temperature Monitor Error		–40°C to +125°C with calibration enabled			±4	°C
External Reference Inputs(4)						
Positive Reference Input Voltage Range	V_{REFP}	Measured Relative to V_{REFN}	2.45	2.5	2.55	Volts
Negative Reference Input Voltage Range	V_{REFN}	Measured Relative to AGND	–50	0	100	mV
Input current	I_{REF}	ADCCLK = 5.2 MHz			100	µA
Power Requirements						
Analog Power Supply	AV_{DD}	Measured Relative to AV_{SS}	2.45	2.5	2.55	V
Analog Supply Current	AI_{DD}	ADCCLK = 5.2 MHz	5		13	mA

Notes:

1. Offset and gain errors are removed by enabling the System Monitor automatic gain calibration feature. See *Virtex-5 FPGA System Monitor User Guide*.
2. See "System Monitor Timing" in *Virtex-5 FPGA System Monitor User Guide*.
3. See "Analog Inputs" in *Virtex-5 FPGA System Monitor User Guide* for a detailed description.
4. Any variation in the reference voltage from the nominal V_{REFP} = 2.5V and V_{REFN} = 0V will result is a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing the supply voltage and reference to vary by ±2% is permitted.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex-5Q devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the Switching Characteristics. Table 52 shows internal (register-to-register) performance.

Table 52: **Register-to-Register Performance**

Description	Register-to-Register (with I/O Delays)			Units
	Speed Grade			
	-2I	-1I	-1M	
Basic Functions				
16:1 Multiplexer	500	450	450	MHz
32:1 Multiplexer	500	450	450	MHz
64:1 Multiplexer	467	407	407	MHz
9 x 9 Logic Multiplier with 4 pipestages	438	428	428	MHz
9 x 9 Logic Multiplier with 5 pipestages	500	428	428	MHz
16-bit Adder	500	450	450	MHz
32-bit Adder	500	447	447	MHz
64-bit Adder	377	323	323	MHz
Register to LUT to Register	500	450	450	MHz
16-bit Counter	500	450	450	MHz
32-bit Counter	500	450	450	MHz
64-bit Counter	381	333	333	MHz
Memory				
Cascaded block RAM (64K)	450	400	400	MHz
Block RAM Pipelined				
Single-Port 512 x 36 bits	500	450	450	MHz
Single-Port 4096 x 4 bits	500	450	450	MHz
Dual-Port A: 4096 x 4 bits and B: 1024 x 18 bits	500	450	450	MHz

Table 52: **Register-to-Register Performance *(Cont'd)***

Description	Register-to-Register (with I/O Delays) Speed Grade			Units
	-2I	-1I	-1M	
Distributed RAM				
Single-Port 16 x 8	500	450	450	MHz
Single-Port 32 x 8	500	450	450	MHz
Single-Port 64 x 8	500	450	450	MHz
Dual-Port 16 x 8				MHz
Shift Register Chain				
16-bit	500	450	450	MHz
32-bit	500	450	450	MHz
64-bit	500	438	438	MHz
Dedicated Arithmetic Logic				
DSP48E Quad 12-bit Adder/Subtracter	500	450	450	MHz
DSP48E Dual 24-bit Adder/Subtracter	500	450	450	MHz
DSP48E 48-bit Adder/Subtracter	500	450	450	MHz
DSP48E 48-bit Counter	500	450	450	MHz
DSP48E 48-bit Comparator	500	450	450	MHz
DSP48E 25 x 18 bit Pipelined Multiplier	500	450	450	MHz
DSP48E Direct 4-tap FIR Filter Pipelined	458	397	397	MHz
DSP48E Systolic n-tap FIR Filter Pipelined	500	450	450	MHz

Notes:

1. Device used is the XQ5VLX50T- FF1136.

Table 53: **Interface Performances**

Description	Speed Grade		
	-2I	-1I	-1M
Networking Applications			
SFI-4.1 (SDR LVDS Interface)(1)	710 MHz	645 MHz	645 MHz
SPI-4.2 (DDR LVDS Interface)(2)	1.25 Gb/s	1.0 Gb/s	1.0 Gb/s
Memory Interfaces			
DDR(3)	200 MHz	200 MHz	200 MHz
DDR2(4)	300 MHz	267 MHz	267 MHz
QDR II SRAM(5)	300 MHz	250 MHz	250 MHz
RLDRAM II(6)	300 MHz	250 MHz	250 MHz

Notes:

1. Performance defined using design implementation described in application note XAPP856, *SFI-4.1 16-Channel SDR Interface with Bus Alignment.*
2. Performance defined using design implementation described in application note XAPP860, *16-Channel, DDR LVDS Interface with Real-time Window Monitoring.*
3. Performance defined using design implementation described in application note XAPP851, *DDR SDRAM Controller.*
4. Performance defined using design implementation described in application note XAPP858, *High-Performance DDR2 SDRAM Interface Data Capture.*
5. Performance defined using design implementation described in application note XAPP853, *QDRII SRAM Interface.*
6. Performance defined using design implementation described in application note XAPP852, *Synthesizable RLDRAM II Controller.*

Switching Characteristics

All values represented in this data sheet are based on speed specification version 1.71. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

Table 54 correlates the current status of each Virtex-5Q device on a per speed grade basis.

Table 54: **Virtex-5Q Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XQ5VLX30T			-2I, -1I
XQ5VLX85			-2I, -1I
XQ5VLX110			-2I, -1I
XQ5VLX110T			-2I, -1I
XQ5VLX155T			-2I, -1I
XQ5VLX220T			-2I, -1I
XQ5VLX330T			-1I
XQ5VSX50T			-2I, -1I
XQ5VSX95T			-2I, -1I
XQ5VSX240T			-1I
XQ5VFX70T			-2I, -1I, -1M
XQ5VFX100T			-2I, -1I, -1M
XQ5VFX130T			-2I, -1I
XQ5VFX200T			-1I

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex-5Q devices.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. Table 55 lists the production released Virtex-5Q family member, speed grade, and the minimum corresponding supported speed specification version and ISE® software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 55: **Virtex-5Q Device Production Software[1] and Speed Specification Release**

Device	Speed Grade Designations		
	-2I	-1I	-1M
XQ5VLX30T	ISE 11.2 v1.65		N/A
XQ5VLX85	ISE 11.2 v1.65		N/A
XQ5VLX110	ISE 11.2 v1.65		N/A
XQ5VLX110T	ISE 11.2 v1.65		N/A
XQ5VLX155T	ISE 11.2 v1.65		N/A
XQ5VLX220T	ISE 12.2 v1.71	ISE 11.2 v1.65	N/A
XQ5VLX330T	N/A	ISE 11.2 v1.65	N/A
XQ5VSX50T	ISE 11.2 v1.65		N/A
XQ5VSX95T	ISE 12.2 v1.71	ISE 11.2 v1.65	N/A
XQ5VSX240T	N/A	ISE 11.2 v1.65	N/A
XQ5VFX70T	ISE 11.2 v1.65		ISE 12.4 v1.71
XQ5VFX100T	ISE 11.2 v1.65		ISE 12.4 v1.71
XQ5VFX130T	ISE 11.2 v1.65		N/A
XQ5VFX200T	N/A	ISE 11.2 v1.65	N/A

Notes:

1. Listed software revisions are those for production-released Virtex-5Q family members.
2. Blank entries indicate a device and/or speed grade in advance or preliminary status.

IOB Pad Input/Output/3-State Switching Characteristics

Table 56 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.

T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.

T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

Table 57, page 34 summarizes the value of T_{IOTPHZ}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).

Table 56: **IOB Switching Characteristics**

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2(I)	-1(I)	-1(M)	-2(I)	-1(I)	-1(M)	-2(I)	-1(I)	-1(M)	
LVDS_25	0.90	1.06	1.11	1.29	1.44	1.79	1.29	1.44	1.79	ns
LVDSEXT_25	1.16	1.30	1.36	1.34	1.49	1.82	1.34	1.49	1.82	ns
HT_25	0.90	1.06	1.11	1.26	1.40	1.79	1.26	1.40	1.79	ns
BLVDS_25	0.90	1.06	1.12	1.38	1.58	1.91	1.38	1.58	1.91	ns
RSDS_25 (point to point)	0.90	1.06	1.11	1.29	1.44	1.79	1.29	1.44	1.79	ns
ULVDS_25	0.90	1.06	1.11	1.27	1.41	1.79	1.27	1.41	1.79	ns
PCI33_3	0.70	0.82	1.05	2.06	2.38	2.41	2.06	2.38	2.41	ns
PCI66_3	0.70	0.82	1.05	2.06	2.38	2.41	2.06	2.38	2.41	ns
PCI-X	0.70	0.82	1.05	1.56	1.80	2.03	1.56	1.80	2.03	ns
GTL	0.85	1.00	1.11	1.63	1.86	2.10	1.63	1.86	2.10	ns
GTLP	0.85	1.00	1.05	1.68	1.93	2.14	1.68	1.93	2.14	ns
HSTL_I	0.85	1.00	1.07	1.57	1.79	1.96	1.57	1.79	1.96	ns
HSTL_II	0.85	1.00	1.05	1.53	1.74	1.84	1.53	1.74	1.84	ns
HSTL_III	0.85	1.00	1.40	1.60	1.85	2.03	1.60	1.85	2.03	ns
HSTL_IV	0.85	1.00	1.40	1.60	1.83	2.07	1.60	1.83	2.07	ns
HSTL_I _18	0.85	1.00	1.26	1.55	1.77	1.91	1.55	1.77	1.91	ns
HSTL_II _18	0.85	1.00	1.13	1.51	1.72	1.79	1.51	1.72	1.79	ns
HSTL_III _18	0.85	1.00	1.45	1.61	1.85	1.98	1.61	1.85	1.98	ns
HSTL_IV_18	0.85	1.00	1.45	1.57	1.81	1.92	1.57	1.81	1.92	ns
SSTL2_I	0.85	1.00	1.11	1.64	1.78	1.94	1.64	1.78	1.94	ns
SSTL2_II	0.85	1.00	1.11	1.55	1.76	1.83	1.55	1.76	1.83	ns
LVTTL, Slow, 2 mA	0.70	0.82	1.02	4.47	5.01	6.05	4.47	5.01	6.05	ns
LVTTL, Slow, 4 mA	0.70	0.82	1.02	3.09	3.41	4.13	3.09	3.41	4.13	ns
LVTTL, Slow, 6 mA	0.70	0.82	1.02	2.91	3.29	3.91	2.91	3.29	3.91	ns
LVTTL, Slow, 8 mA	0.70	0.82	1.02	2.30	2.61	2.91	2.30	2.61	2.91	ns
LVTTL, Slow, 12 mA	0.70	0.82	1.02	2.15	2.46	2.56	2.15	2.46	2.56	ns
LVTTL, Slow, 16 mA	0.70	0.82	1.02	2.04	2.34	2.47	2.04	2.34	2.47	ns
LVTTL, Slow, 24 mA	0.70	0.82	1.02	2.07	2.38	2.48	2.07	2.38	2.48	ns

Table 56: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI} Speed Grade			T_{IOOP} Speed Grade			T_{IOTP} Speed Grade			Units
	-2(I)	-1(I)	-1(M)	-2(I)	-1(I)	-1(M)	-2(I)	-1(I)	-1(M)	
LVTTL, Fast, 2 mA	0.70	0.82	1.02	3.61	4.05	5.58	3.61	4.05	5.58	ns
LVTTL, Fast, 4 mA	0.70	0.82	1.02	2.55	2.90	3.72	2.55	2.90	3.72	ns
LVTTL, Fast, 6 mA	0.70	0.82	1.02	2.31	2.63	3.34	2.31	2.63	3.34	ns
LVTTL, Fast, 8 mA	0.70	0.82	1.02	1.82	2.09	2.39	1.82	2.09	2.39	ns
LVTTL, Fast, 12 mA	0.70	0.82	1.02	1.63	1.89	2.31	1.63	1.89	2.31	ns
LVTTL, Fast, 16 mA	0.70	0.82	1.02	1.57	1.81	2.27	1.57	1.81	2.27	ns
LVTTL, Fast, 24 mA	0.70	0.82	1.02	1.52	1.74	2.27	1.52	1.74	2.27	ns
LVCMOS33, Slow, 2 mA	0.70	0.82	1.02	3.96	4.44	6.05	3.96	4.44	6.05	ns
LVCMOS33, Slow, 4 mA	0.70	0.82	1.02	3.09	3.49	4.13	3.09	3.49	4.13	ns
LVCMOS33, Slow, 6 mA	0.70	0.82	1.02	2.86	3.24	3.89	2.86	3.24	3.89	ns
LVCMOS33, Slow, 8 mA	0.70	0.82	1.02	2.26	2.57	2.91	2.26	2.57	2.91	ns
LVCMOS33, Slow, 12 mA	0.70	0.82	1.02	2.14	2.42	2.56	2.14	2.42	2.56	ns
LVCMOS33, Slow, 16 mA	0.70	0.82	1.02	2.04	2.31	2.44	2.04	2.31	2.44	ns
LVCMOS33, Slow, 24 mA	0.70	0.82	1.02	2.07	2.35	2.48	2.07	2.35	2.48	ns
LVCMOS33, Fast, 2 mA	0.70	0.82	1.02	3.20	3.59	5.56	3.20	3.59	5.56	ns
LVCMOS33, Fast, 4 mA	0.70	0.82	1.02	2.50	2.84	3.70	2.50	2.84	3.70	ns
LVCMOS33, Fast, 6 mA	0.70	0.82	1.02	2.27	2.59	3.32	2.27	2.59	3.32	ns
LVCMOS33, Fast, 8 mA	0.70	0.82	1.02	1.79	2.05	2.35	1.79	2.05	2.35	ns
LVCMOS33, Fast, 12 mA	0.70	0.82	1.02	1.61	1.86	2.31	1.61	1.86	2.31	ns
LVCMOS33, Fast, 16 mA	0.70	0.82	1.02	1.56	1.80	2.28	1.56	1.80	2.28	ns
LVCMOS33, Fast, 24 mA	0.70	0.82	1.02	1.51	1.74	2.26	1.51	1.74	2.26	ns
LVCMOS25, Slow, 2 mA	0.70	0.82	0.82	3.97	4.42	5.06	3.97	4.42	5.06	ns
LVCMOS25, Slow, 4 mA	0.70	0.82	0.82	2.60	2.94	3.71	2.60	2.94	3.71	ns
LVCMOS25, Slow, 6 mA	0.70	0.82	0.82	2.41	2.74	3.42	2.41	2.74	3.42	ns
LVCMOS25, Slow, 8 mA	0.70	0.82	0.82	2.26	2.56	2.93	2.26	2.56	2.93	ns
LVCMOS25, Slow, 12 mA	0.70	0.82	0.82	2.31	2.63	2.73	2.31	2.63	2.73	ns
LVCMOS25, Slow, 16 mA	0.70	0.82	0.82	2.02	2.30	2.31	2.02	2.30	2.31	ns
LVCMOS25, Slow, 24 mA	0.70	0.82	0.82	2.04	2.34	2.37	2.04	2.34	2.37	ns
LVCMOS25, Fast, 2 mA	0.70	0.82	0.82	3.41	3.82	4.48	3.41	3.82	4.48	ns
LVCMOS25, Fast, 4 mA	0.70	0.82	0.82	2.08	2.37	3.23	2.08	2.37	3.23	ns
LVCMOS25, Fast, 6 mA	0.70	0.82	0.82	1.92	2.20	2.89	1.92	2.20	2.89	ns
LVCMOS25, Fast, 8 mA	0.70	0.82	0.82	1.83	2.09	2.38	1.83	2.09	2.38	ns
LVCMOS25, Fast, 12 mA	0.70	0.82	0.82	1.69	1.94	1.94	1.69	1.94	1.94	ns
LVCMOS25, Fast, 16 mA	0.70	0.82	0.82	1.60	1.85	1.99	1.60	1.85	1.99	ns
LVCMOS25, Fast, 24 mA	0.70	0.82	0.82	1.54	1.76	1.98	1.54	1.76	1.98	ns
LVCMOS18, Slow, 2 mA	0.76	0.89	1.14	4.56	5.09	6.81	4.56	5.09	6.81	ns
LVCMOS18, Slow, 4 mA	0.76	0.89	1.14	3.32	3.75	4.30	3.32	3.75	4.30	ns
LVCMOS18, Slow, 6 mA	0.76	0.89	1.14	2.61	2.97	3.76	2.61	2.97	3.76	ns
LVCMOS18, Slow, 8 mA	0.76	0.89	1.14	2.37	2.69	3.32	2.37	2.69	3.32	ns

Table 56: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}			T_{IOOP}			T_{IOTP}			Units
	Speed Grade			Speed Grade			Speed Grade			
	-2(I)	-1(I)	-1(M)	-2(I)	-1(I)	-1(M)	-2(I)	-1(I)	-1(M)	
LVCMOS18, Slow, 12 mA	0.76	0.89	1.14	2.16	2.47	2.59	2.16	2.47	2.59	ns
LVCMOS18, Slow, 16 mA	0.76	0.89	1.14	2.14	2.45	2.53	2.14	2.45	2.53	ns
LVCMOS18, Fast, 2 mA	0.76	0.89	1.14	3.71	4.16	6.23	3.71	4.16	6.23	ns
LVCMOS18, Fast, 4 mA	0.76	0.89	1.14	2.61	2.98	3.80	2.61	2.98	3.80	ns
LVCMOS18, Fast, 6 mA	0.76	0.89	1.14	2.06	2.35	3.30	2.06	2.35	3.30	ns
LVCMOS18, Fast, 8 mA	0.76	0.89	1.14	1.87	2.13	2.66	1.87	2.13	2.66	ns
LVCMOS18, Fast, 12 mA	0.76	0.89	1.14	1.68	1.93	2.07	1.68	1.93	2.07	ns
LVCMOS18, Fast, 16 mA	0.76	0.89	1.14	1.61	1.86	1.97	1.61	1.86	1.97	ns
LVCMOS15, Slow, 2 mA	0.83	0.98	1.23	3.84	4.34	5.08	3.84	4.34	5.08	ns
LVCMOS15, Slow, 4 mA	0.83	0.98	1.23	2.40	2.74	3.48	2.40	2.74	3.48	ns
LVCMOS15, Slow, 6 mA	0.83	0.98	1.23	2.20	2.52	2.55	2.20	2.52	2.55	ns
LVCMOS15, Slow, 8 mA	0.83	0.98	1.23	2.12	2.43	2.46	2.12	2.43	2.46	ns
LVCMOS15, Slow, 12 mA	0.83	0.98	1.23	1.95	2.25	2.28	1.95	2.25	2.28	ns
LVCMOS15, Slow, 16 mA	0.83	0.98	1.23	1.91	2.20	2.23	1.91	2.20	2.23	ns
LVCMOS15, Fast, 2 mA	0.83	0.98	1.23	3.07	3.48	4.99	3.07	3.48	4.99	ns
LVCMOS15, Fast, 4 mA	0.83	0.98	1.23	1.95	2.23	3.39	1.95	2.23	3.39	ns
LVCMOS15, Fast, 6 mA	0.83	0.98	1.23	1.80	2.06	2.41	1.80	2.06	2.41	ns
LVCMOS15, Fast, 8 mA	0.83	0.98	1.23	1.74	2.00	2.26	1.74	2.00	2.26	ns
LVCMOS15, Fast, 12 mA	0.83	0.98	1.23	1.60	1.86	1.99	1.60	1.86	1.99	ns
LVCMOS15, Fast, 16 mA	0.83	0.98	1.23	1.53	1.77	1.92	1.53	1.77	1.92	ns
LVCMOS12, Slow, 2 mA	0.96	1.14	1.61	3.98	4.58	5.58	3.98	4.58	5.58	ns
LVCMOS12, Slow, 4 mA	0.96	1.14	1.61	2.33	2.66	3.13	2.33	2.66	3.13	ns
LVCMOS12, Slow, 6 mA	0.96	1.14	1.61	2.18	2.45	2.54	2.18	2.45	2.54	ns
LVCMOS12, Slow, 8 mA	0.96	1.14	1.61	2.14	2.48	2.51	2.14	2.48	2.51	ns
LVCMOS12, Fast, 2 mA	0.96	1.14	1.61	3.38	3.87	5.54	3.38	3.87	5.54	ns
LVCMOS12, Fast, 4 mA	0.96	1.14	1.61	1.91	2.20	3.01	1.91	2.20	3.01	ns
LVCMOS12, Fast, 6 mA	0.96	1.14	1.61	1.78	2.08	2.44	1.78	2.08	2.44	ns
LVCMOS12, Fast, 8 mA	0.96	1.14	1.61	1.70	1.97	2.28	1.70	1.97	2.28	ns
LVDCI_33	0.70	0.82	1.02	1.66	1.90	2.66	1.66	1.90	2.66	ns
LVDCI_25	0.70	0.82	0.82	1.71	1.93	2.65	1.71	1.93	2.65	ns
LVDCI_18	0.76	0.89	1.14	1.78	1.99	2.85	1.78	1.99	2.85	ns
LVDCI_15	0.83	0.98	1.23	1.75	2.02	2.74	1.75	2.02	2.74	ns
LVDCI_DV2_25	0.70	0.82	0.82	1.51	1.74	2.12	1.51	1.74	2.12	ns
LVDCI_DV2_18	0.76	0.89	1.14	1.60	1.85	2.16	1.60	1.85	2.16	ns
LVDCI_DV2_15	0.83	0.98	1.23	1.65	1.91	2.33	1.65	1.91	2.33	ns
GTL_DCI	0.85	1.00	1.11	1.47	1.65	1.79	1.47	1.65	1.79	ns
GTLP_DCI	0.85	1.00	1.05	1.52	1.76	1.94	1.52	1.76	1.94	ns
LVPECL_25	0.90	1.06	1.12	1.42	1.62	1.91	1.42	1.62	1.91	ns

Table 56: **IOB Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI} Speed Grade -2(I)	-1(I)	-1(M)	T_{IOOP} Speed Grade -2(I)	-1(I)	-1(M)	T_{IOTP} Speed Grade -2(I)	-1(I)	-1(M)	Units
HSTL_I_12	0.85	1.00	1.08	1.61	1.85	1.98	1.61	1.85	1.98	ns
HSTL_I_DCI	0.85	1.00	1.07	1.56	1.77	1.98	1.56	1.77	1.98	ns
HSTL_II_DCI	0.85	1.00	1.05	1.48	1.69	1.86	1.48	1.69	1.86	ns
HSTL_II_T_DCI	0.85	1.00	1.05	1.56	1.77	1.98	1.56	1.77	1.98	ns
HSTL_III_DCI	0.85	1.00	1.40	1.72	1.95	2.27	1.72	1.95	2.27	ns
HSTL_IV_DCI	0.85	1.00	1.40	1.46	1.64	1.84	1.46	1.64	1.84	ns
HSTL_I_DCI_18	0.85	1.00	1.26	1.50	1.70	1.95	1.50	1.70	1.95	ns
HSTL_II_DCI_18	0.85	1.00	1.13	1.43	1.64	1.77	1.43	1.64	1.77	ns
HSTL_II _T_DCI_18	0.85	1.00	1.13	1.50	1.70	1.95	1.50	1.70	1.95	ns
HSTL_III_DCI_18	0.85	1.00	1.45	1.69	1.91	2.16	1.69	1.91	2.16	ns
HSTL_IV_DCI_18	0.85	1.00	1.45	1.44	1.62	1.84	1.44	1.62	1.84	ns
DIFF_HSTL_I_18	0.90	1.06	1.10	1.55	1.77	1.91	1.55	1.77	1.91	ns
DIFF_HSTL_I_DCI_18	0.90	1.06	1.10	1.50	1.70	1.91	1.50	1.70	1.91	ns
DIFF_HSTL_I	0.90	1.06	1.10	1.57	1.79	1.91	1.57	1.79	1.91	ns
DIFF_HSTL_I_DCI	0.90	1.06	1.10	1.56	1.77	1.95	1.56	1.77	1.95	ns
DIFF_HSTL_II_18	0.90	1.06	1.10	1.51	1.72	1.91	1.51	1.72	1.91	ns
DIFF_HSTL_II_DCI_18	0.90	1.06	1.10	1.43	1.64	1.91	1.43	1.64	1.91	ns
DIFF_HSTL_II	0.90	1.06	1.10	1.53	1.74	1.91	1.53	1.74	1.91	ns
DIFF_HSTL_II_DCI	0.90	1.06	1.10	1.48	1.69	1.91	1.48	1.69	1.91	ns
SSTL2_I_DCI	0.85	1.00	1.11	1.56	1.78	3.30	1.56	1.78	3.30	ns
SSTL2_II_DCI	0.85	1.00	1.11	1.48	1.70	1.97	1.48	1.70	1.97	ns
SSTL2_II_T_DCI	0.85	1.00	1.11	1.56	1.78	3.30	1.56	1.78	3.30	ns
SSTL18_I	0.85	1.00	1.08	1.61	1.84	1.94	1.61	1.84	1.94	ns
SSTL18_II	0.85	1.00	1.08	1.53	1.75	1.81	1.53	1.75	1.81	ns
SSTL18_I_DCI	0.85	1.00	1.08	1.53	1.74	1.97	1.53	1.74	1.97	ns
SSTL18_II_DCI	0.85	1.00	1.08	1.44	1.64	1.86	1.44	1.64	1.86	ns
SSTL18_II_T_DCI	0.85	1.00	1.08	1.53	1.74	1.97	1.53	1.74	1.97	ns
DIFF_SSTL2_I	0.90	1.06	1.11	1.64	1.87	1.97	1.64	1.87	1.97	ns
DIFF_SSTL2_I_DCI	0.90	1.06	1.11	1.56	1.78	1.94	1.56	1.78	1.94	ns
DIFF_SSTL18_I	0.90	1.06	1.10	1.61	1.84	1.94	1.61	1.84	1.94	ns
DIFF_SSTL18_I_DCI	0.90	1.06	1.10	1.53	1.74	1.94	1.53	1.74	1.94	ns
DIFF_SSTL2_II	0.90	1.06	1.11	1.55	1.76	1.91	1.55	1.76	1.91	ns
DIFF_SSTL2_II_DCI	0.90	1.06	1.11	1.48	1.70	1.90	1.48	1.70	1.90	ns
DIFF_SSTL18_II	0.90	1.06	1.10	1.53	1.75	1.91	1.53	1.75	1.91	ns
DIFF_SSTL18_II_DCI	0.90	1.06	1.10	1.44	1.64	1.91	1.44	1.64	1.91	ns

Notes:

1. M-temperature IOB delays are slightly larger than timing analyzer/speeds specification values. Correct values are listed in this table. It is necessary to allow for this difference in the design.

Table 57: **IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
T_{IOTPHZ}	T input to Pad high-impedance	1.01	1.12	1.12	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 58 shows the test setup parameters used for measuring input delay.

Table 58: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(5)	V_{REF} (1)(3)(5)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL	0	3.0	1.4	–
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	0	3.3	1.65	–
LVCMOS, 2.5V	LVCMOS25	0	2.5	1.25	–
LVCMOS, 1.8V	LVCMOS18	0	1.8	0.9	–
LVCMOS, 1.5V	LVCMOS15	0	1.5	0.75	–
LVCMOS, 1.2V	LVCMOS12	0	1.2	0.6	–
PCI (Peripheral Component Interconnect), 33 MHz, 3.3V	PCI33_3	Per PCI™ Specification			–
PCI, 66 MHz, 3.3V	PCI66_3	Per PCI Specification			–
PCI-X, 133 MHz, 3.3V	PCIX	Per PCI-X™ Specification			–
GTL (Gunning Transceiver Logic)	GTL	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.80
GTL Plus	GTLP	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.0
HSTL (High-Speed Transceiver Logic), Class I & II	HSTL_I, HSTL_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL, Class III & IV	HSTL_III, HSTL_IV	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL, Class III & IV, 1.8V	HSTL_III_18, HSTL_IV_18	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	1.08
SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V	SSTL3_I, SSTL3_II	V_{REF} – 1.00	V_{REF} + 1.00	V_{REF}	1.5
SSTL, Class I & II, 2.5V	SSTL2_I, SSTL2_II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
AGP-2X/AGP (Accelerated Graphics Port)	AGP	V_{REF} – $(0.2 \times V_{CCO})$	V_{REF} + $(0.2 \times V_{CCO})$	V_{REF}	AGP Spec
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	0(6)	
LVDSEXT (LVDS Extended Mode), 2.5V	LVDSEXT_25	1.2 – 0.125	1.2 + 0.125	0(6)	
LDT (HyperTransport), 2.5V	LDT_25	0.6 – 0.125	0.6 + 0.125	0(6)	
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	1.15 – 0.3	1.15 – 0.3	0(6)	

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVCMOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between V_L and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 11, page 35.
6. The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 11 and Figure 12.

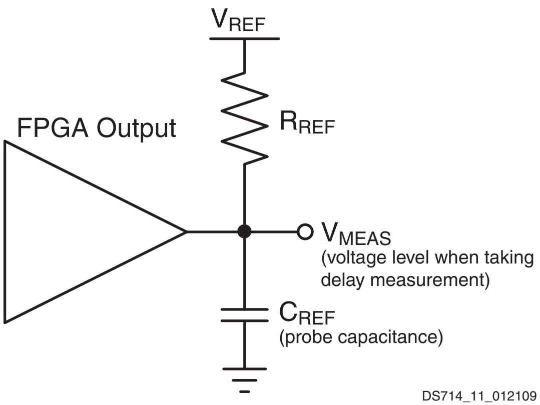

Figure 11: **Single Ended Test Setup**

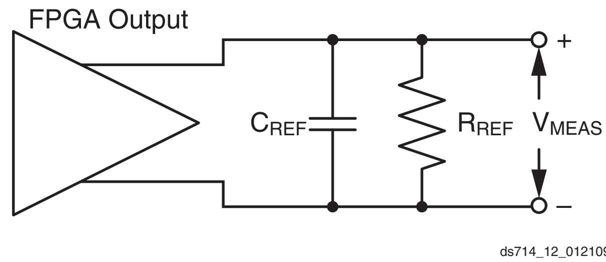

Figure 12: **Differential Test Setup**

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 59.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 59: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[(1)] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVTTL (Low-Voltage Transistor-Transistor Logic)	LVTTL (all)	1M	0	1.4	0
LVCMOS (Low-Voltage CMOS), 3.3V	LVCMOS33	1M	0	1.65	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 1.8V	LVCMOS18	1M	0	0.9	0
LVCMOS, 1.5V	LVCMOS15	1M	0	0.75	0
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
PCI (Peripheral Component Interface), 33 MHz, 3.3V	PCI33_3 (rising edge)	25	10[(2)]	0.94	0
	PCI33_3 (falling edge)	25	10[(2)]	2.03	3.3
PCI, 66 MHz, 3.3V	PCI66_3 (rising edge)	25	10[(2)]	0.94	0
	PCI66_3 (falling edge)	25	10[(2)]	2.03	3.3
PCI-X, 133 MHz, 3.3V	PCIX (rising edge)	25	10[(3)]	0.94	
	PCIX (falling edge	25	10[(3)]	2.03	3.3
GTL (Gunning Transceiver Logic)	GTL	25	0	0.8	1.2
GTL Plus	GTLP	25	0	1.0	1.5
HSTL (High-Speed Transceiver Logic), Class I	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class III	HSTL_III	50	0	0.9	1.5

Table 59: **Output Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[(1)] (pF)	V_{MEAS} (V)	V_{REF} (V)
HSTL, Class IV	HSTL_IV	25	0	0.9	1.5
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSTL, Class III, 1.8V	HSTL_III_18	50	0	1.1	1.8
HSTL, Class IV, 1.8V	HSTL_IV_18	25	0	1.1	1.8
SSTL (Stub Series Terminated Logic), Class I, 1.8V	SSTL18_I	50	0	V_{REF}	0.9
SSTL, Class II, 1.8V	SSTL18_II	25	0	V_{REF}	0.9
SSTL, Class I, 2.5V	SSTL2_I	50	0	V_{REF}	1.25
SSTL, Class II, 2.5V	SSTL2_II	25	0	V_{REF}	1.25
LVDS (Low-Voltage Differential Signaling), 2.5V	LVDS_25	100	0	0[(4)]	1.2
LVDSEXT (LVDS Extended Mode), 2.5V	LVDS_25	100	0	0[(4)]	1.2
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[(4)]	0
LDT (HyperTransport), 2.5V	LDT_25	100	0	0[(4)]	0.6
LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V	LVPECL_25	100	0	0[(4)]	0
LVDCI/HSLVDCI (Low-Voltage Digitally Controlled Impedance), 3.3V	LVDCI_33, HSLVDCI_33	1M	0	1.65	0
LVDCI/HSLVDCI, 2.5V	LVDCI_25, HSLVDCI_25	1M	0	1.25	0
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	1M	0	0.9	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	1M	0	0.75	0
HSTL (High-Speed Transceiver Logic), Class I & II, with DCI	HSTL_I_DCI, HSTL_II_DCI	50	0	V_{REF}	0.75
HSTL, Class III & IV, with DCI	HSTL_III_DCI, HSTL_IV_DCI	50	0	0.9	1.5
HSTL, Class I & II, 1.8V, with DCI	HSTL_I_DCI_18, HSTL_II_DCI_18	50	0	V_{REF}	0.9
HSTL, Class III & IV, 1.8V, with DCI	HSTL_III_DCI_18, HSTL_IV_DCI_18	50	0	1.1	1.8
SSTL (Stub Series Termi.Logic), Class I & II, 1.8V, with DCI	SSTL18_I_DCI, SSTL18_II_DCI	50	0	V_{REF}	0.9
SSTL, Class I & II, 2.5V, with DCI	SSTL2_I_DCI, SSTL2_II_DCI	50	0	V_{REF}	1.25
GTL (Gunning Transceiver Logic) with DCI	GTL_DCI	50	0	0.8	1.2
GTL Plus with DCI	GTLP_DCI	50	0	1.0	1.5

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. Per PCI-X specifications.
4. The value given is the differential input voltage.

Input/Output Logic Switching Characteristics

Table 60: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
Setup/Hold					
T_{ICE1CK}/T_{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.49 –0.24	0.59 –0.24	0.59 –0.17	ns
T_{ISRCK}/T_{ICKSR}	SR/REV pin Setup/Hold with respect to CLK	1.00 –0.20	1.22 –0.20	1.22 –0.22	ns
T_{IDOCK}/T_{IOCKD}	D pin Setup/Hold with respect to CLK without Delay	0.37 –0.12	0.39 –0.12	0.39 –0.12	ns
T_{IDOCKD}/T_{IOCKDD}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.33 –0.09	0.36 –0.08	0.36 –0.08	ns
Combinatorial					
T_{IDI}	D pin to O pin propagation delay, no Delay	0.26	0.30	0.30	ns
T_{IDID}	DDLY pin to O pin propagation delay (using IODELAY)	0.22	0.26	0.26	ns
Sequential Delays					
T_{IDLO}	D pin to Q1 pin using flip-flop as a latch without Delay	0.50	0.58	0.58	ns
T_{IDLOD}	DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY)	0.46	0.55	0.55	ns
T_{ICKQ}	CLK to Q outputs	0.52	0.60	0.60	ns
T_{RQ}	SR/REV pin to OQ/TQ out	1.28	1.53	1.53	ns
T_{GSRQ}	Global Set/Reset to Q outputs	7.30	10.10	10.10	ns
Set/Reset					
T_{RPW}	Minimum Pulse Width, SR/REV inputs	0.95	1.20	1.20	ns, Min

Table 61: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
Setup/Hold					
T_{ODCK}/T_{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.36 –0.21	0.44 –0.21	0.44 –0.14	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.19 –0.07	0.23 –0.07	0.23 –0.04	ns
T_{OSRCK}/T_{OCKSR}	SR/REV pin Setup/Hold with respect to CLK	1.02 –0.20	1.16 –0.20	1.16 –0.20	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.34 –0.18	0.41 –0.18	0.41 –0.12	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.23 –0.06	0.29 –0.06	0.29 –0.01	ns
Combinatorial					
T_{DOQ}	D1 to OQ out or T1 to TQ out	0.70	0.83	0.83	ns
Sequential Delays					
T_{OCKQ}	CLK to OQ/TQ out	0.62	0.62	0.62	ns
T_{RQ}	SR/REV pin to OQ/TQ out	1.89	2.27	2.27	ns
T_{GSRQ}	Global Set/Reset to Q outputs	7.30	10.10	10.10	ns
Set/Reset					
T_{RPW}	Minimum Pulse Width, SR/REV inputs	0.98	1.25	1.25	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 62: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
Setup/Hold for Control Lines					
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.11 0.00	0.12 0.00	0.12 0.00	ns
T_{ISCCK_CE} / T_{ISCKC_CE}(2)	CE pin Setup/Hold with respect to CLK (for CE1)	0.49 –0.24	0.59 –0.24	0.59 –0.17	ns
T_{ISCCK_CE2} / T_{ISCKC_CE2}(2)	CE pin Setup/Hold with respect to CLKDIV (for CE2)	0.04 0.13	0.06 0.15	0.06 0.15	ns
Setup/Hold for Data Lines					
T_{ISDCK_D} /T_{ISCKD_D}	D pin Setup/Hold with respect to CLK	0.37 –0.12	0.39 –0.12	0.39 –0.12	ns
T_{ISDCK_DDLY} /T_{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IODELAY)	0.33 –0.09	0.36 –0.08	0.36 –0.08	ns
T_{ISDCK_DDR} /T_{ISCKD_DDR}	D pin Setup/Hold with respect to CLK at DDR mode	0.37 –0.12	0.39 –0.12	0.39 –0.12	ns
$T_{ISDCK\_DDLY\_DDR}$ $T_{ISCKD\_DDLY\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY)	0.33 –0.09	0.36 –0.08	0.36 –0.08	ns
Sequential Delays					
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.51	0.60	0.60	ns
Propagation Delays					
T_{ISDO_DO}	D input to DO output pin	0.22	0.26	0.26	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as T_{ISCCK_CE}/T_{ISCKC_CE} in TRACE report.

Output Serializer/Deserializer Switching Characteristics

Table 63: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
Setup/Hold					
T_{OSDCK_D}/T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.24 –0.02	0.30 –0.02	0.30 –0.02	ns
T_{OSDCK_T}/T_{OSCKD_T}[(1)]	T input Setup/Hold with respect to CLK	0.34 –0.18	0.41 –0.18	0.41 –0.12	ns
$T_{OSDCK\_T2}/T_{OSCKD\_T2}$[(1)]	T input Setup/Hold with respect to CLKDIV	0.24 –0.03	0.28 –0.03	0.28 –0.03	ns
$T_{OSCCK\_OCE}/T_{OSCKC\_OCE}$	OCE input Setup/Hold with respect to CLK	0.19 –0.07	0.23 –0.07	0.23 –0.04	ns
T_{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.58	0.70	0.70	ns
$T_{OSCCK\_TCE}/T_{OSCKC\_TCE}$	TCE input Setup/Hold with respect to CLK	0.23 –0.06	0.29 –0.06	0.29 –0.01	ns
Sequential Delays					
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.60	0.61	0.61	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.62	0.62	0.62	ns
Combinatorial					
T_{OSDO_TTQ}	T input to TQ Out	0.70	0.83	0.83	ns
T_{OSCO_OQ}	Asynchronous Reset to OQ	1.82	2.19	2.19	ns
T_{OSCO_TQ}	Asynchronous Reset to TQ	1.89	2.27	2.27	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in TRACE report.

Input/Output Delay Switching Characteristics

Table 64: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
IDELAYCTRL					
$T_{IDELAYCTRLCO\_RDY}$	Reset to Ready for IDELAYCTRL	3.00	3.00	3.00	µs
$F_{IDELAYCTRL\_REF}$	REFCLK frequency	200.00	200.00	200.00	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum Reset pulse width	50.00	50.00	50.00	ns
IODELAY					
$T_{IDELAYRESOLUTION}$	IODELAY Chain Delay Resolution	$1/(64 \times F_{REF} \times 1e^{6})$(1)			ps
$T_{IDELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern	0	0	0	Note 2
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)	±5	±5	±5	Note 2
$T_{IODELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IODELAY	250	250	250	MHz
T_{IODCCK_CE} / T_{IODCKC_CE}	CE pin Setup/Hold with respect to CK	0.34 –0.06	0.42 –0.06	0.42 –0.06	ns
T_{IODCK_INC}/ T_{IODCKC_INC}	INC pin Setup/Hold with respect to CK	0.20 0.04	0.24 0.06	0.24 0.06	ns
T_{IODCK_RST}/ T_{IODCKC_RST}	RST pin Setup/Hold with respect to CK	0.28 –0.12	0.33 –0.12	0.33 –0.12	ns
T_{IODDO_T}	TSCONTROL delay to MUXE/MUXF switching and through IODELAY	Note 3	Note 3	Note 3	
$T_{IODDO\_IDATAIN}$	Propagation delay through IODELAY	Note 3	Note 3	Note 3	
$T_{IODDO\_ODATAIN}$	Propagation delay through IODELAY	Note 3	Note 3	Note 3	

Notes:

1. Average Tap Delay at 200 MHz = 78 ps.
2. Units in ps, peak-to-peak per tap, in High Performance mode.
3. Delay depends on IODELAY tap setting. See TRACE report for actual values.

CLB Switching Characteristics

Table 65: **CLB Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
Combinatorial Delays					
T_{ILO}	An – Dn LUT address to A	0.09	0.10	0.10	ns, Max
	An – Dn LUT address to AMUX/CMUX	0.22	0.25	0.25	ns, Max
	An – Dn LUT address to BMUX_A	0.35	0.40	0.40	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs	0.77	0.90	0.90	ns, Max
T_{AXA}	AX inputs to AMUX output	0.44	0.53	0.53	ns, Max
T_{AXB}	AX inputs to BMUX output	0.52	0.61	0.61	ns, Max
T_{AXC}	AX inputs to CMUX output	0.36	0.42	0.42	ns, Max
T_{AXD}	AX inputs to DMUX output	0.62	0.73	0.73	ns, Max
T_{BXB}	BX inputs to BMUX output	0.41	0.48	0.48	ns, Max

Table 65: **CLB Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
T_{BXD}	BX inputs to DMUX output	0.51	0.59	0.59	ns, Max
T_{CXB}	CX inputs to CMUX output	0.36	0.42	0.42	ns, Max
T_{CXD}	CX inputs to DMUX output	0.42	0.49	0.49	ns, Max
T_{DXD}	DX inputs to DMUX output	0.42	0.49	0.49	ns, Max
T_{OPCYA}	An input to COUT output	0.50	0.59	0.59	ns, Max
T_{OPCYB}	Bn input to COUT output	0.44	0.51	0.51	ns, Max
T_{OPCYC}	Cn input to COUT output	0.37	0.43	0.43	ns, Max
T_{OPCYD}	Dn input to COUT output	0.34	0.40	0.40	ns, Max
T_{AXCY}	AX input to COUT output	0.42	0.50	0.50	ns, Max
T_{BXCY}	BX input to COUT output	0.30	0.37	0.37	ns, Max
T_{CXCY}	CX input to COUT output	0.22	0.26	0.26	ns, Max
T_{DXCY}	DX input to COUT output	0.22	0.26	0.26	ns, Max
T_{BYP}	CIN input to COUT output	0.10	0.11	0.11	ns, Max
T_{CINA}	CIN input to AMUX output	0.27	0.31	0.31	ns, Max
T_{CINB}	CIN input to BMUX output	0.30	0.35	0.35	ns, Max
T_{CINC}	CIN input to CMUX output	0.32	0.36	0.36	ns, Max
T_{CIND}	CIN input to DMUX output	0.35	0.41	0.41	ns, Max
Sequential Delays					
T_{CKO}	Clock to AQ – DQ outputs	0.40	0.47	0.47	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK					
T_{DICK}/T_{CKDI}	AX – DX input to CLK on A – D Flip Flops	0.41 0.21	0.49 0.24	0.49 0.31	ns, Min
T_{RCK}	DX input to CLK when used as REV	0.42	0.51	0.51	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK on A – D Flip Flops	0.20 –0.04	0.23 –0.04	0.23 –0.03	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D Flip Flops	0.49 –0.19	0.59 –0.19	0.59 –0.19	ns, Min
T_{CINCK}/T_{CKCIN}	CIN input to CLK on A – D Flip Flops	0.16 0.16	0.18 0.19	0.18 0.26	ns, Min
Set/Reset					
T_{SRMIN}	SR input minimum pulse width	0.90	0.90	0.90	ns, Min
T_{RQ}	Delay from SR or REV input to AQ – DQ flip-flops	0.86	1.03	1.03	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.52	0.63	0.63	ns, Max
F_{TOG}	Toggle frequency (for export control)	1265	1098	1098	MHz

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. These items are of interest for Carry Chain applications.

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 66: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
Sequential Delays					
T_{SHCKO}	Clock to A – B outputs	1.26	1.54	1.54	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	1.38	1.68	1.68	ns, Max
Setup and Hold Times Before/After Clock CLK					
T_{DS}/T_{DH}	A – D inputs to CLK	0.84 0.22	1.03 0.26	1.03 0.26	ns, Min
T_{AS}/T_{AH}	Address An inputs to clock	0.46 0.22	0.54 0.27	0.54 0.27	ns, Min
T_{WS}/T_{WH}	WE input to clock	0.39 –0.04	0.46 –0.02	0.46 –0.02	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.42 –0.07	0.51 –0.06	0.51 –0.06	ns, Min
Clock CLK					
T_{MPW}	Minimum pulse width	0.82	1.00	1.00	ns, Min
T_{MCP}	Minimum clock period	1.64	2.00	2.00	ns, Min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. T_{SHCKO} also represents the CLK to XMUX output. Refer to TRACE report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 67: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
Sequential Delays					
T_{REG}	Clock to A – D outputs	1.43	1.73	1.73	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.55	1.87	1.87	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	1.15	1.38	1.38	ns, Max
Setup and Hold Times Before/After Clock CLK					
T_{WS}/T_{WH}	WE input	0.24 –0.04	0.29 –0.02	0.29 –0.02	ns, Min
T_{CECK}/T_{CKCE}	CE input to CLK	0.27 –0.07	0.33 –0.06	0.33 –0.06	ns, Min
T_{DS}/T_{DH}	A – D inputs to CLK	0.66 0.09	0.78 0.11	0.78 0.11	ns, Min
Clock CLK					
T_{MPW}	Minimum pulse width	0.70	0.85	0.85	ns, Min

Notes:

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values cannot be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Block RAM and FIFO Switching Characteristics

Table 68: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
Block RAM and FIFO Clock to Out Delays					
T_{RCKO_DO} and T_{RCKO_DOR}[1]	Clock CLK to DOUT output (without output register)[2][3]	1.92	2.19	2.19	ns, Max
	Clock CLK to DOUT output (with output register)[4][5]	0.69	0.82	0.82	ns, Max
	Clock CLK to DOUT output with ECC (without output register)[2][3]	3.03	3.61	3.61	ns, Max
	Clock CLK to DOUT output with ECC (with output register)[4][5]	0.77	0.93	0.93	ns, Max
	Clock CLK to DOUT output with Cascade (without output register)[2]	2.44	2.94	2.94	ns, Max
	Clock CLK to DOUT output with Cascade (with output register)[4]	1.07	1.30	1.30	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs[6]	0.87	1.02	1.02	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointer outputs[7]	1.26	1.48	1.48	ns, Max
T_{RCKO_ECCR}	Clock CLK to BITERR (with output register)	0.77	0.93	0.93	ns, Max
T_{RCKO_ECC}	Clock CLK to BITERR (without output register)	2.85	3.41	3.41	ns, Max
	Clock CLK to ECCPARITY in standard ECC mode	1.47	1.74	1.74	ns, Max
	Clock CLK to ECCPARITY in ECC encode only mode	0.89	1.05	1.05	ns, Max
Setup and Hold Times Before/After Clock CLK					
$T_{RCCK\_ADDR}/T_{RCKC\_ADDR}$	ADDR inputs[8]	0.40 0.32	0.48 0.36	0.48 0.36	ns, Min
T_{RDCK_DI}/T_{RCKD_DI}	DIN inputs[9]	0.30 0.28	0.35 0.29	0.35 0.29	ns, Min
$T_{RDCK\_DI\_ECC}/T_{RCKD\_DI\_ECC}$	DIN inputs with ECC in standard mode[9]	0.37 0.33	0.42 0.36	0.42 0.47	ns, Min
	DIN inputs with ECC encode only[9]	0.72 0.33	0.77 0.36	0.77 0.47	ns, Min
T_{RCCK_EN}/T_{RCKC_EN}	Block RAM Enable (EN) input	0.36 0.15	0.42 0.15	0.42 0.15	ns, Min
$T_{RCCK\_REGCE}/T_{RCKC\_REGCE}$	CE input of output register	0.16 0.24	0.18 0.27	0.18 0.27	ns, Min
$T_{RCCK\_SSR}/T_{RCKC\_SSR}$	Synchronous Set/ Reset (SSR) input	0.21 0.25	0.26 0.28	0.26 0.28	ns, Min
T_{RCCK_WE}/T_{RCKC_WE}	Write Enable (WE) input	0.51 0.17	0.63 0.18	0.63 0.18	ns, Min
$T_{RCCK\_WREN}/T_{RCKC\_WREN}$	WREN/RDEN FIFO inputs[10]	0.41 0.34	0.48 0.40	0.48 0.40	ns, Min
Reset Delays					
T_{RCO_FLAGS}	Reset RST to FIFO Flags/Pointers[11]	1.26	1.48	1.48	ns, Max

Table 68: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
Maximum Frequency					
F_{MAX}	Block RAM in all modes	500	450	450	MHz
$F_{MAX\_CASCADE}$	Block RAM in cascade configuration	450	400	400	MHz
F_{MAX_FIFO}	FIFO in all modes	500	450	450	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	375	325	325	MHz

Notes:

1. TRACE will report all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted even though WE is deasserted. Otherwise, block RAM data corruption is possible.
9. T_{RCKO_DI} includes both A and B inputs as well as the parity inputs of A and B.
10. These parameters also apply to RDEN.
11. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.

DSP48E Switching Characteristics

Table 69: **DSP48E Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
Setup and Hold Times of Data/Control Pins to the Input Register Clock					
TDSPDCK_{AA, BB, ACINA, BCINB}/ TDSPCKD_{AA, BB, ACINA, BCINB}	{A, B, ACIN, BCIN} input to {A, B} register CLK	0.21 0.23	0.26 0.30	0.26 0.30	ns
TDSPDCK_CC/TDSPCKD_CC	C input to C register CLK	0.16 0.31	0.20 0.37	0.20 0.50	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock					
TDSPDCK_{AM, BM, ACINM, BCINM}/ TDSPCKD_{AM, BM, ACINM, BCINM}	{A, B, ACIN, BCIN} input to M register CLK	1.44 0.19	1.71 0.19	1.71 0.19	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock					
TDSPDCK_{AP, BP, ACINP, BCINP}_M/ TDSPCKD_{AP, BP, ACINP, BCINP}_M	{A, B, ACIN, BCIN} input to P register CLK using multiplier	2.74 –0.30	3.25 –0.30	3.25 –0.30	ns
TDSPDCK_{AP, BP, ACINP, BCINP}_NM/ TDSPCKD_{AP, BP, ACINP, BCINP}_NM	{A, B, ACIN, BCIN} input to P register CLK not using multiplier	1.54 –0.10	1.83 –0.10	1.83 –0.10	ns
TDSPDCK_CP/TDSPCKD_CP	C input to P register CLK	1.42 –0.13	1.70 –0.13	1.70 –0.13	ns
TDSPDCK_{PCINP, CRYCINP, MULTSIGNINP}/ TDSPCKD_{PCINP, CRYCINP, MULTSIGNINP}	{PCIN, CARRYCASCIN, MULTSIGNIN} input to P register CLK	1.17 0.11	1.31 0.11	1.31 0.11	ns
Setup and Hold Times of the CE Pins					
TDSPCCK_{CEA1A, CEA2A, CEB1B, CEB2B}/ TDSPCKC_{CEA1A, CEA2A, CEB1A, CEB2B}	{CEA1, CEA2A, CEB1B, CEB2B} input to {A, B} register CLK	0.28 0.25	0.33 0.31	0.33 0.31	ns
TDSPCCK_CECC/TDSPCKC_CECC	CEC input to C register CLK	0.21 0.21	0.26 0.28	0.26 0.28	ns
TDSPCCK_CEMM/TDSPCKC_CEMM	CEM input to M register CLK	0.29 0.21	0.36 0.26	0.36 0.26	ns

Table 69: **DSP48E Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
TDSPCCK_CEPP/TDSPCKC_CEPP	CEP input to P register CLK	0.63 0.01	0.73 0.01	0.73 0.01	ns
Setup and Hold Times of the RST Pins					
TDSPCCK_{RSTAA, RSTBB}/ TDSPCKC_{RSTAA, RSTBB}	{RSTA, RSTB} input to {A, B} register CLK	0.28 0.26	0.33 0.31	0.33 0.31	ns
TDSPCCK_RSTCC/ TDSPCKC_RSTCC	RSTC input to C register CLK	0.21 0.21	0.26 0.28	0.26 0.28	ns
TDSPCCK_RSTMM/ TDSPCKC_RSTMM	RSTM input to M register CLK	0.29 0.21	0.36 0.26	0.36 0.26	ns
TDSPCCK_RSTPP/TDSPCKC_RSTPP	RSTP input to P register CLK	0.63 0.01	0.73 0.01	0.73 0.01	ns
Combinatorial Delays from Input Pins to Output Pins					
TDSPDO_{AP, ACRYOUT, BP, BCRYOUT}_M	{A, B} input to {P, CARRYOUT} output using multiplier	3.22	3.84	3.84	ns
TDSPDO_{AP, ACRYOUT, BP, BCRYOUT}_NM	{A, B} input to {P, CARRYOUT} output not using multiplier	1.77	2.22	2.22	ns
TDSPDO_{CP, CCRYOUT, CRYINP, CRYINCRYOUT}	{C, CARRYIN} input to {P, CARRYOUT} output	1.67	2.08	2.08	ns
Combinatorial Delays from Input Pins to Cascading Output Pins					
TDSPDO_{AACOUT, BBCOUT}	{A, B} input to {ACOUT, BCOUT} output	1.12	1.31	1.31	ns
TDSPDO_{APCOUT, ACRYCOUT, AMULTSIGNOUT, BPCOUT, BCRYCOUT, BMULTSIGNOUT}_M	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.22	3.84	3.84	ns
TDSPDO_{APCOUT, ACRYCOUT, AMULTSIGNOUT, BPCOUT, BCRYCOUT, BMULTSIGNOUT}_NM	{A, B} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	1.92	2.42	2.42	ns
TDSPDO_{CPCOUT, CCRYCOUT, CMULTSIGNOUT, CRYINPCOUT, CRYINCRYCOUT, CRYINMULTSIGNOUT}	{C, CARRYIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.82	2.28	2.28	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins					
TDSPDO_{ACINP, ACINCRYOUT, BCINP, BCINCRYOUT}_M	{ACIN, BCIN} input to {P, CARRYOUT} output using multiplier	3.22	3.84	3.84	ns
TDSPDO_{ACINP, ACINCRYOUT, BCINP, BCINCRYOUT}_NM	{ACIN, BCIN} input to {P, CARRYOUT} output not using multiplier	1.77	2.22	2.22	ns
TDSPDO_{ACINACOUT, BCINBCOUT}	{ACIN, BCIN} input to {ACOUT, BCOUT} output	1.12	1.31	1.31	ns
TDSPDO_{ACINPCOUT, ACINCRYCOUT, ACINMULTSIGNOUT, BCINPCOUT, BCINCRYCOUT, BCINMULTSIGNOUT}_M	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.22	3.84	3.84	ns
TDSPDO_{ACINPCOUT, ACINCRYCOUT, ACINMULTSIGNOUT, BCINPCOUT, BCINCRYCOUT, BCINMULTSIGNOUT}_NM	{ACIN, BCIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	1.92	2.42	2.42	ns
TDSPDO_{PCINP, CRYCINP, MULTSIGNINP, PCINCRYOUT, CRYCINCRYOUT, MULTSIGNINCRYOUT}	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {P, CARRYOUT} output	1.45	1.82	1.82	ns

Table 69: **DSP48E Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
TDSPDO_{PCINPCOUT, CRYCINPCOUT, MULTSIGNINPCOUT, PCINCRYCOUT, CRYCINCRYCOUT, MULTSIGNINCRYCOUT, PCINMULTSIGNOUT, CRYCINMULTSIGNOUT, MULTSIGNINMULTSIGNOUT}	{PCIN, CARRYCASCIN, MULTSIGNIN} input to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	1.60	2.02	2.02	ns
Clock to Outs from Output Register Clock to Output Pins					
TDSPCKO_{PP, CRYOUTP}	CLK (PREG) to {P, CARRYOUT} output	0.48	0.56	0.56	ns
TDSPCKO_{CRYCOUTP, PCOUTP, MULTSIGNOUTP}	CLK (PREG) to {CARRYCASCOUT, PCOUT, MULTSIGNOUT} output	0.53	0.62	0.62	ns
Clock to Outs from Pipeline Register Clock to Output Pins					
TDSPCKO_{PM, CRYOUTM}	CLK (MREG) to {P, CARRYOUT} output	2.10	2.47	2.47	ns
TDSPCKO_{PCOUTM, CRYCOUTM, MULTSIGNOUTM}	CLK (MREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.13	2.66	2.66	ns
Clock to Outs from Input Register Clock to Output Pins					
TDSPCKO_{PA, CRYOUTA, PB, CRYOUTB}_M	CLK (AREG, BREG) to {P, CARRYOUT} output using multiplier	3.57	4.23	4.23	ns
TDSPCKO_{PA, CRYOUTA, PB, CRYOUTB}_NM	CLK (AREG, BREG) to {P, CARRYOUT} output not using multiplier	2.11	2.63	2.63	ns
TDSPCKO_{PC, CRYOUTC}	CLK (CREG) to {P, CARRYOUT} output	2.11	2.62	2.62	ns
Clock to Outs from Input Register Clock to Cascading Output Pins					
TDSPCKO_{ACOUTA, BCOUTB}	CLK (AREG, BREG) to {ACOUT, BCOUT}	0.68	0.79	0.79	ns
TDSPCKO_{PCOUTA, CRYCOUTA, MULTSIGNOUTA, PCOUTB, CRYCOUTB, MULTSIGNOUTB}_M	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output using multiplier	3.57	4.23	4.23	ns
TDSPCKO_{PCOUTA, CRYCOUTA, MULTSIGNOUTA, PCOUTB, CRYCOUTB, MULTSIGNOUTB}_NM	CLK (AREG, BREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output not using multiplier	2.27	2.82	2.82	ns
TDSPCKO_{PCOUTC, CRYCOUTC, MULTSIGNOUTC}	CLK (CREG) to {PCOUT, CARRYCASCOUT, MULTSIGNOUT} output	2.26	2.82	2.82	ns
Maximum Frequency					
F_{MAX}	With all registers used	500	450	450	MHz
F_{MAX_PATDET}	With pattern detector	465	410	410	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	324	275	275	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	300	254	254	MHz

Configuration Switching Characteristics

Table 70: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
Power-up Timing Characteristics					
T_{PL}	Program Latency	3	3	3	ms, Max
T_{POR}	Power-on-Reset	10 50	10 50	10 50	ms, Min/Max
T_{ICCK}	CCLK (output) delay	400	400	400	ns, Min
$T_{PROGRAM}$	Program Pulse Width	250	250	250	ns, Min
Master/Slave Serial Mode Programming Switching[(1)]					
T_{DCCK}/T_{CCKD}	DIN Setup/Hold, slave mode	4.0 0.0	4.0 0.0	5.0 0.0	ns, Min
T_{DSCCK}/T_{SCCKD}	DIN Setup/Hold, master mode	4.0 0.0	4.0 0.0	5.0 0.0	ns, Min
T_{CCO}	DOUT	7.5	7.5	7.5	ns, Max
F_{MCCK}	Maximum Frequency, master mode with respect to nominal CCLK.	100	100	100	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance, master mode with respect to nominal CCLK.	±50	±50	±50	%
F_{MSCCK}	Slave mode external CCLK	100	100	100	MHz
SelectMAP Mode Programming Switching[(1)]					
T_{SMDCCK}/T_{SMCCKD}	SelectMAP Data Setup/Hold	3.0 0.5	3.0 0.5	3.0 0.5	ns, Min
$T_{SMCSCCK}/T_{SMCCKCS}$	CS_B Setup/Hold	3.0 0.5	3.0 0.5	3.0 0.5	ns, Min
T_{SMCCKW}/T_{SMWCCK}	RDWR_B Setup/Hold	8.0 0.5	8.0 0.5	8.0 0.5	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330Ω pull-up resistor required)	10	10	10	ns, Min
T_{SMCO}	CCLK to DATA out in readback	9.0	9.0	9.0	ns, Max
T_{SMCKBY}	CCLK to BUSY out in readback	7.5	7.5	7.5	ns, Max
F_{SMCCK}	Maximum Frequency with respect to nominal CCLK	100	100	100	MHz, Max
F_{RBCCK}	Maximum Readback Frequency with respect to nominal CCLK	60	60	60	MHz, Max
$F_{MCCKTOL}$	Frequency Tolerance with respect to nominal CCLK	±50	±50	±50	%
Boundary-Scan Port Timing Specifications					
T_{TAPTCK}	TMS and TDI Setup time before TCK	1.0	1.0	1.0	ns, Min
T_{TCKTAP}	TMS and TDI Hold time after TCK	2.0	2.0	2.0	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output valid	6	6	6	ns, Max
F_{TCK}	Maximum configuration TCK clock frequency	66	66	66	MHz, Max
F_{TCKB}	Maximum boundary-scan TCK clock frequency	66	66	66	MHz, Max

Table 70: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
BPI Master Flash Mode Programming Switching					
T_{BPICCO}[(4)]	ADDR[25:0], RS[1:0], FCS_B, FOE_B, FWE_B outputs valid after CCLK rising edge	10	10	10	ns
T_{BPIDCC}/T_{BPICCD}	Setup/Hold on D[15:0] data input pins	3.0 0.5	3.0 0.5	3.0 0.5	ns
$T_{INITADDR}$	Minimum period of initial ADDR[25:0] address cycles	3.0	3.0	3.0	CCLK cycles
SPI Master Flash Mode Programming Switching					
$T_{SPIDCC}/T_{SPIDCCD}$	DIN Setup/Hold before/after the rising CCLK edge	4.0 0.0	4.0 0.0	5.0 0.0	ns
T_{SPICCM}	MOSI clock to out	10	10	10	ns
$T_{SPICCFC}$	FCS_B clock to out	10	10	10	ns
$T_{FSINIT}/T_{FSINITH}$	FS[2:0] to INIT_B rising edge Setup and Hold	2	2	2	μs
CCLK Output (Master Modes)					
T_{MCCKL}	Master CCLK clock minimum Low time	3.0	3.0	3.0	ns, Min
T_{MCCKH}	Master CCLK clock minimum High time	3.0	3.0	3.0	ns, Min
CCLK Input (Slave Modes)					
T_{SCCKL}	Slave CCLK clock minimum Low time	2.0	2.0	2.0	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time	2.0	2.0	2.0	ns, Min
Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK					
F_{DCK}	Maximum frequency for DCLK	450	400	400	MHz
$T_{DMCCK\_DADDR}/T_{DMCKC\_DADDR}$	DADDR Setup/Hold	1.35 0.0	1.56 0.0	1.56 0.0	ns
$T_{DMCCK\_DI}/T_{DMCKC\_DI}$	DI Setup/Hold	1.35 0.0	1.56 0.0	1.56 0.0	ns
$T_{DMCCK\_DEN}/T_{DMCKC\_DEN}$	DEN Setup/Hold time	1.35 0.0	1.56 0.0	1.56 0.0	ns
$T_{DMCCK\_DWE}/T_{DMCKC\_DWE}$	DWE Setup/Hold time	1.35 0.0	1.56 0.0	1.56 0.0	ns
T_{DMCKO_DO}	CLK to out of DO[(3)]	1.12	1.30	1.30	ns
T_{DMCKO_DRDY}	CLK to out of DRDY	1.12	1.30	1.30	ns

Notes:

1. Maximum frequency and setup/hold timing parameters are for 3.3V and 2.5V configuration voltages.
2. To support longer delays in configuration, use the design solutions described in the *Virtex-5 FPGA User Guide*.
3. DO will hold until next DRP operation.
4. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

Clock Buffers and Networks

Table 71: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Devices	Speed Grade			Units
			-2I	-1I	-1M	
$T_{BCCCK\_CE}/T_{BCCKC\_CE}$ [1]	CE pins Setup/Hold	All	0.27 0.00	0.31 0.00	0.31 0.00	ns
T_{BCCCK_S}/T_{BCCKC_S} [1]	S pins Setup/Hold	All	0.27 0.00	0.31 0.00	0.31 0.00	ns
T_{BCCKO_O} [2]	BUFGCTRL delay from I0/I1 to O	LX30T, LX85, LX110, LX110T, SX50T, FX70T, FX100T, and FX130T	0.22	0.25	0.25	ns
		LX155T	0.14	0.30	N/A	ns
		LX220T, LX330T, SX95T, SX240T, and FX200T	0.22	0.25	N/A	ns
Maximum Frequency						
F_{MAX}	Global clock tree (BUFG)	LX30T, LX85, LX110, LX110T, SX50T, and FX70T(I)	667	600	N/A	MHz
		LX155T, FX70T(M), and FX100T	600	550	550	MHz
		FX130T	500	450	N/A	MHz
		LX220T, LX330T, SX95T, SX240T, and FX200T	500	450	N/A	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX_VIRTEX4 primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 72: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
$T_{BUFIOCKO\_O}$	Clock to out delay from I to O	1.16	1.29	1.29	ns
Maximum Frequency					
F_{MAX}	I/O clock tree (BUFIO)	710	644	644	MHz

Table 73: **Regional Clock Switching Characteristics (BUFR)**

Symbol	Description	Devices	Speed Grade			Units
			-2I	-1I	-1M	
T_{BRCKO_O}	Clock to out delay from I to O	LX30T, LX85, LX110, LX110T, SX50T, FX100T, and FX130T	0.59	0.67	0.67	ns
		FX70T	0.74	0.83	0.83	ns
		LX155T	0.80	0.90	N/A	ns
		LX220T, LX330T, SX95T, SX240T, and FX200T	0.59	0.67	N/A	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	LX30T, LX85, LX110, LX110T, SX50T, FX70T, FX100T, and FX130T	0.24	0.26	0.26	ns
		LX155T	0.26	0.30	N/A	ns
		LX220T, LX330T, SX95T, SX240T, and FX200T	0.24	0.26	N/A	ns
T_{BRDO_CLRO}	Propagation delay from CLR to O	All	0.70	0.82	0.82	ns
Maximum Frequency						
F_{MAX}	Regional clock tree (BUFR)	All	250	250	250	MHz

PLL Switching Characteristics

Table 74: **PLL Specification**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
F_{INMAX}	Maximum Input Clock Frequency	710	645	645	MHz
F_{INMIN}	Minimum Input Clock Frequency	19	19	19	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter	<20% of clock input period or 1 ns Max			
F_{INDUTY}	Allowable Input Duty Cycle: 19—49 MHz	25/75			%
	Allowable Input Duty Cycle: 50—199 MHz	30/70			%
	Allowable Input Duty Cycle: 200—399 MHz	35/65			%
	Allowable Input Duty Cycle: 400—499 MHz	40/60			%
	Allowable Input Duty Cycle: >500 MHz	45/55			%
F_{VCOMIN}	Minimum PLL VCO Frequency	400	400	400	MHz
F_{VCOMAX}	Maximum PLL VCO Frequency	1200	1000	1000	MHz
$F_{BANDWIDTH}$	Low PLL Bandwidth at Typical(1)	1	1	1	MHz
	High PLL Bandwidth at Typical(1)	4	4	4	MHz
$T_{STAPHAOFFSET}$	Static Phase Offset of the PLL Outputs	120	120	120	ps
$T_{OUTJITTER}$	PLL Output Jitter(2)	Note 1			
$T_{OUTDUTY}$	PLL Output Clock Duty Cycle Precision(3)	±200	±200	±200	ps
$T_{LOCKMAX}$	PLL Maximum Lock Time(4)	100	100	100	µs
F_{OUTMAX}	PLL Maximum Output Frequency for LX30T, LX85, LX110, LX110T, SX50T, and FX70T(I) devices	667	600	N/A	MHz
	PLL Maximum Output Frequency for LX155T, FX70T(M), and FX100T devices	600	550	550	MHz
	PLL Maximum Output Frequency for FX130T devices	500	450	N/A	MHz
	PLL Maximum Output Frequency for LX220T, LX330T, SX95T, SX240T, and FX200T devices	500	450	N/A	MHz
F_{OUTMIN}	PLL Minimum Output Frequency(5)	3.125	3.125	3.125	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max			
$RST_{MINPULSE}$	Minimum Reset Pulse Width	5	5	5	ns
F_{PFDMAX}	Maximum Frequency at the Phase Frequency Detector	500	450	450	MHz
F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	19	19	19	MHz
$T_{FBDELAY}$	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle			

Notes:

1. The PLL does not filter typical spread spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. Values for this parameter are available in the Architecture Wizard.
3. Includes global clock buffer.
4. The LOCK signal must be sampled after $T_{LOCKMAX}$. The LOCK signal is invalid after configuration or reset until the $T_{LOCKMAX}$ time has expired.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Table 75: **PLL in PMCD Mode Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
$T_{PLLCCK\_REL}/T_{PLLCKC\_REL}$	REL Setup and Hold for all Outputs	0.00 0.60	0.00 0.60	0.00 0.60	ns
$T_{PLLCCKO}$	Maximum Clock Propagation Delay	4.6	5.2	5.2	ns
CLKIN_FREQ_MAX	Maximum Input Frequency	710	645	645	MHz
CLKIN_FREQ_MIN	Minimum Input Frequency	1	1	1	MHz
CLKIN_DUTY_CYCLE	Allowable Input Duty Cycle: 1—49 MHz	25/75			%
	Allowable Input Duty Cycle: 50—199 MHz	30/70			%
	Allowable Input Duty Cycle: 200—399 MHz	35/65			%
	Allowable Input Duty Cycle: 400—499 MHz	40/60			%
	Allowable Input Duty Cycle: >500 MHz	45/55			%
RES_REL_PULSE_MIN	Minimum Pulse Width for RST and REL	5	5	5	ns

DCM Switching Characteristics

Table 76: **Operating Frequency Ranges for DCM in Maximum Speed (MS) Mode**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
Outputs Clocks (Low Frequency Mode)					
$F_{1XLFMSMIN}$	CLK0, CLK90, CLK180, CLK270	32.00	32.00	32.00	MHz
$F_{1XLFMSMAX}$		135.00	120.00	120.00	MHz
$F_{2XLFMSMIN}$	CLK2X, CLK2X180	64.00	64.00	64.00	MHz
$F_{2XLFMSMAX}$		270.00	240.00	240.00	MHz
$F_{DVLFMSMIN}$	CLKDV(5)	2.0	2.0	2.0	MHz
$F_{DVLFMSMAX}$		90.00	80.00	80.00	MHz
$F_{FXLFMSMIN}$	CLKFX, CLKFX180	32.00	32.00	32.00	MHz
$F_{FXLFMSMAX}$		160.00	140.00	140.00	MHz
Input Clocks (Low Frequency Mode)					
$F_{DLLLFMSMIN}$	CLKIN (using DLL outputs)(1)(3)(4)	32.00	32.00	32.00	MHz
$F_{DLLLFMSMAX}$		135.00	120.00	120.00	MHz
$F_{CLKINLFFXMSMIN}$	CLKIN (using DFS outputs only)(2)(3)(4)	1.00	1.00	1.00	MHz
$F_{CLKINLFFXMSMAX}$		160.00	140.00	140.00	MHz
$F_{PSCLKLFMSMIN}$	PSCLK	1.00	1.00	1.00	KHz
$F_{PSCLKLFMSMAX}$		500.00	450.00	450.00	MHz
Outputs Clocks (High Frequency Mode)					
$F_{1XHFMSMIN}$	CLK0, CLK90, CLK180, CLK270	120.00	120.00	120.00	MHz
$F_{1XHFMSMAX}$		500.00	450.00	450.00	MHz
$F_{2XHFMSMIN}$	CLK2X, CLK2X180	240.00	240.00	240.00	MHz
$F_{2XHFMSMAX}$		500.00	450.00	450.00	MHz
$F_{DVHFMSMIN}$	CLKDV(5)	7.5	7.5	7.5	MHz
$F_{DVHFMSMAX}$		333.34	300.00	300.00	MHz
$F_{FXHFMSMIN}$	CLKFX, CLKFX180(5)	140.00	140.00	140.00	MHz
$F_{FXHFMSMAX}$		375.00	350.00	350.00	MHz
Input Clocks (High Frequency Mode)					
$F_{DLLHFMSMIN}$	CLKIN (using DLL outputs)(1)(3)(4)	120.00	120.00	120.00	MHz
$F_{DLLHFMSMAX}$		500.00	450.00	450.00	MHz
$F_{CLKINHFFXMSMIN}$	CLKIN (using DFS outputs only)(2)(3)(4)(5)	25.00	25.00	25.00	MHz
$F_{CLKINHFFXMSMAX}$		375.00	350.00	350.00	MHz
$F_{PSCLKHFMSMIN}$	PSCLK	1.00	1.00	1.00	KHz
$F_{PSCLKHFMSMAX}$		500.00	450.00	450.00	MHz

Notes:

1. DLL outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. When using the DCMs CLKIN_DIVIDE_BY_2 attribute these values should be doubled. Other resources can limit the maximum input frequency.
4. When using a CLKIN frequency > 400 MHz and the DCMs CLKIN_DIVIDE_BY_2 attribute, the CLKIN duty cycle must be within ±5% (45/55 to 55/45).
5. Only available for I-temperature conditions.

Table 77: **Operating Frequency Ranges for DCM in Maximum Range (MR) Mode[5]**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
Outputs Clocks (Low Frequency Mode)					
$F_{1XMRMIN}$	CLK0, CLK90, CLK180, CLK270	19.00	19.00	19.00	MHz
$F_{1XMRMAX}$		32.00	32.00	32.00	MHz
$F_{2XMRMIN}$	CLK2X, CLK2X180	38.00	38.00	38.00	MHz
$F_{2XMRMAX}$		64.00	64.00	64.00	MHz
$F_{DLLMRMIN}$	CLKDV	1.19	1.19	1.19	MHz
$F_{DLLMRMAX}$		21.34	21.34	21.34	MHz
$F_{FXMRMIN}$	CLKFX, CLKFX180	19.00	19.00	19.00	MHz
$F_{FXMRMAX}$		40.00	40.00	40.00	MHz
Input Clocks (Low Frequency Mode)					
$F_{CLKINDLLMRMIN}$	CLKIN (using DLL outputs)[1][3][4]	19.00	19.00	19.00	MHz
$F_{CLKINDLLMRMAX}$		32.00	32.00	32.00	MHz
$F_{CLKINFXMRMIN}$	CLKIN (using DFS outputs only)[2][3][4]	1.00	1.00	1.00	MHz
$F_{CLKINFXMRMAX}$		40.00	40.00	40.00	MHz
$F_{PSCLKMRMIN}$	PSCLK	1.00	1.00	1.00	KHz
$F_{PSCLKMRMAX}$		270.00	240.00	240.00	MHz

Notes:

1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. When using the DCMs CLKIN_DIVIDE_BY_2 attribute these values should be doubled. Other resources can limit the maximum input frequency.
4. When using a CLKIN frequency > 400 MHz and the DCMs CLKIN_DIVIDE_BY_2 attribute, the CLKIN duty cycle must be within ±5% (45/55 to 55/45).
5. Maximum range is not available outside of I-temperature conditions.

Table 78: **Input Clock Tolerances**

Symbol	Description	Frequency Range	Value		Units
Duty Cycle Input Tolerance (in %)					
$T_{DUTYCYCRANGE\_1}$	PSCLK only	< 1 MHz	25 - 75		%
$T_{DUTYCYCRANGE\_1\_50}$	PSCLK and CLKIN	1 - 50 MHz	25 - 75		%
$T_{DUTYCYCRANGE\_50\_100}$		50 - 100 MHz	30 - 70		%
$T_{DUTYCYCRANGE\_100\_200}$		100 - 200 MHz	40 - 60		%
$T_{DUTYCYCRANGE\_200\_400}$		200 - 400 MHz[4]	45 - 55		%
$T_{DUTYCYCRANGE\_400}$		> 400 MHz	45 - 55		%
Input Clock Cycle-Cycle Jitter (Low Frequency Mode)		**Speed Grade**			**Units**
		-2I	**-1I**	**-1M**	
$T_{CYCLFDLL}$	CLKIN (using DLL outputs)[1]	300.00	345.00	345.00	ps
$T_{CYCLFFX}$	CLKIN (using DFS outputs)[2]	300.00	345.00	345.00	ps
Input Clock Cycle-Cycle Jitter (High Frequency Mode)					
$T_{CYCHFDLL}$	CLKIN (using DLL outputs)[1]	150.00	173.00	173.00	ps
$T_{CYCHFFX}$	CLKIN (using DFS outputs)[2]	150.00	173.00	173.00	ps
Input Clock Period Jitter (Low Frequency Mode)					
$T_{PERLFDLL}$	CLKIN (using DLL outputs)[1]	1.00	1.15	1.15	ns
$T_{PERLFFX}$	CLKIN (using DFS outputs)[2]	1.00	1.15	1.15	ns
Input Clock Period Jitter (High Frequency Mode)					
$T_{PERHFDLL}$	CLKIN (using DLL outputs)[1]	1.00	1.15	1.15	ns
$T_{PERHFFX}$	CLKIN (using DFS outputs)[2]	1.00	1.15	1.15	ns
Feedback Clock Path Delay Variation					
$T_{CLKFB\_DELAY\_VAR}$	CLKFB off-chip feedback	1.00	1.15	1.15	ns

Notes:

1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. If both DLL and DFS outputs are used, follow the more restrictive specifications.
4. This duty cycle specification does not apply to the GTP_DUAL to DCM or GTX_DUAL to DCM connection. The GTP transceivers drive the DCMs at the following frequencies: 320 MHz for -1I speed grade devices, or 375 MHz for -2I speed grade devices. The GTX transceivers drive the DCMs at the following frequencies: 450 MHz for -1I speed grade devices or 500 MHz for -2I speed grade devices.

Output Clock Jitter

Table 79: **Output Clock Jitter**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
Clock Synthesis Period Jitter					
$T_{PERJITT\_0}$	CLK0	±120	±120	±120	ps
$T_{PERJITT\_90}$	CLK90	±120	±120	±120	ps
$T_{PERJITT\_180}$	CLK180	±120	±120	±120	ps
$T_{PERJITT\_270}$	CLK270	±120	±120	±120	ps
$T_{PERJITT\_2X}$	CLK2X, CLK2X180	±200	±230	±230	ps
$T_{PERJITT\_DV1}$	CLKDV (integer division)	±150	±180	±180	ps
$T_{PERJITT\_DV2}$	CLKDV (non-integer division)	±300	±345	±345	ps
$T_{PERJITT\_FX}$	CLKFX, CLKFX180	Note 1	Note 1	Note 1	ps

Notes:

1. Values for this parameter are available in the Architecture Wizard.

Output Clock Phase Alignment

Table 80: **Output Clock Phase Alignment**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
Phase Offset Between CLKIN and CLKFB					
$T_{IN\_FB\_OFFSET}$	CLKIN/CLKFB	±50	±60	±60	ps
Phase Offset Between Any DCM Outputs(1)					
$T_{OUT\_OFFSET\_1X}$	CLK0, CLK90, CLK180, CLK270	±140	±160	±160	ps
$T_{OUT\_OFFSET\_2X}$	CLK2X, CLK2X180, CLKDV	±150	±200	±200	ps
$T_{OUT\_OFFSET\_FX}$	CLKFX, CLKFX180	±160	±220	±220	ps
Duty Cycle Precision(2)					
$T_{DUTY\_CYC\_DLL}$	DLL outputs(3)	±150	±180	±180	ps
$T_{DUTY\_CYC\_FX}$	DFS outputs(4)	±150	±180	±180	ps

Notes:

1. All phase offsets are with respect to group CLK1X.
2. CLKOUT_DUTY_CYCLE_DLL applies to the 1X clock outputs (CLK0, CLK90, CLK180, and CLK270) only if DUTY_CYCLE_CORRECTION = TRUE. The duty cycle distortion includes the global clock tree (BUFG).
3. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
4. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.

Table 81: **Miscellaneous Timing Parameters**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
Time Required to Achieve LOCK					
T_{DLL_240}	DLL output – Frequency range > 240 MHz(1)	80.00	80.00	80.00	µs
$T_{DLL\_120\_240}$	DLL output – Frequency range 120 - 240 MHz(1)	250.00	250.00	250.00	µs
$T_{DLL\_60\_120}$	DLL output – Frequency range 60 - 120 MHz(1)	900.00	900.00	900.00	µs
$T_{DLL\_50\_60}$	DLL output – Frequency range 50 - 60 MHz(1)	1300.00	1300.00	1300.00	µs
$T_{DLL\_40\_50}$	DLL output – Frequency range 40 - 50 MHz(1)	2000.00	2000.00	2000.00	µs
$T_{DLL\_30\_40}$	DLL output – Frequency range 30 - 40 MHz(1)	3600.00	3600.00	3600.00	µs
$T_{DLL\_24\_30}$	DLL output – Frequency range 24 - 30 MHz(1)	5000.00	5000.00	5000.00	µs
T_{DLL_30}	DLL output – Frequency range < 30 MHz(1)	5000.00	5000.00	5000.00	µs
T_{FX_MIN}	DFS outputs(2)	10.00	10.00	10.00	ms
T_{FX_MAX}		10.00	10.00	10.00	ms
$T_{DLL\_FINE\_SHIFT}$	Multiplication factor for DLL lock time with Fine Shift	2.00	2.00	2.00	
Fine Phase Shifting					
T_{RANGE_MS}	Absolute shifting range in maximum speed mode	7.00	7.00	7.00	ns
T_{RANGE_MR}(3)	Absolute shifting range in maximum range mode	10.00	10.00	10.00	ns
Delay Lines					
$T_{TAP\_MS\_MIN}$	Tap delay resolution (Min) in maximum speed mode	7.00	7.00	7.00	ps
$T_{TAP\_MS\_MAX}$	Tap delay resolution (Max) in maximum speed mode	30.00	30.00	30.00	ps
$T_{TAP\_MR\_MIN}$(3)	Tap delay resolution (Min) in maximum range mode	10.00	10.00	10.00	ps
$T_{TAP\_MR\_MAX}$(3)	Tap delay resolution (Max) in maximum range mode	40.00	40.00	40.00	ps

Notes:
1. DLL Outputs are used in these instances to describe the outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV.
2. DFS Outputs are used in these instances to describe the outputs: CLKFX and CLKFX180.
3. Maximum range is not available outside of I-temperature conditions.

Table 82: **Frequency Synthesis**

Attribute	Min	Max
CLKFX_MULTIPLY	2	33
CLKFX_DIVIDE	1	32

Table 83: **DCM Switching Characteristics**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
T_{DMCCK_PSEN}/ T_{DMCKC_PSEN}	PSEN Setup/Hold	1.35 0.00	1.56 0.00	1.56 0.00	ns
$T_{DMCCK\_PSINCDEC}$/ $T_{DMCKC\_PSINCDEC}$	PSINCDEC Setup/Hold	1.35 0.00	1.56 0.00	1.56 0.00	ns
T_{DMCKO_PSDONE}	Clock to out of PSDONE	1.12	1.30	1.30	ns

Virtex-5Q Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 84. Values are expressed in nanoseconds unless otherwise noted.

Table 84: **Global Clock Input to Output Delay Without DCM or PLL**

Symbol	Description	Device	Speed Grade			Units
			-2I	-1I	-1M	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *without* DCM or PLL						
T_{ICKOF}	Global Clock and OUTFF *without* DCM or PLL	XQ5VLX30T	6.04	6.73	N/A	ns
		XQ5VLX85	6.28	6.99	N/A	ns
		XQ5VLX110	6.35	7.06	N/A	ns
		XQ5VLX110T	6.35	7.06	N/A	ns
		XQ5VLX155T	6.68	7.52	N/A	ns
		XQ5VLX220T	6.99	7.71	N/A	ns
		XQ5VLX330T	N/A	7.91	N/A	ns
		XQ5VSX50T	6.27	6.97	N/A	ns
		XQ5VSX95T	6.59	7.30	N/A	ns
		XQ5VSX240T	N/A	7.98	N/A	ns
		XQ5VFX70T	6.33	7.04	7.04	ns
		XQ5VFX100T	6.73	7.44	7.44	ns
		XQ5VFX130T	6.80	7.52	N/A	ns
		XQ5VFX200T	N/A	7.91	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 85: **Global Clock Input to Output Delay With DCM in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-2I	-1I	-1M	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM in System-Synchronous Mode						
$T_{ICKOFDCM}$	Global Clock and OUTFF *with* DCM	XQ5VLX30T	2.56	2.93	N/A	ns
		XQ5VLX85	2.63	3.00	N/A	ns
		XQ5VLX110	2.69	3.06	N/A	ns
		XQ5VLX110T	2.69	3.06	N/A	ns
		XQ5VLX155T	2.74	3.10	N/A	ns
		XQ5VLX220T	2.83	3.18	N/A	ns
		XQ5VLX330T	N/A	3.37	N/A	ns
		XQ5VSX50T	2.69	3.05	N/A	ns
		XQ5VSX95T	2.64	3.00	N/A	ns
		XQ5VSX240T	N/A	3.36	N/A	ns
		XQ5VFX70T	2.74	3.12	3.12	ns
		XQ5VFX100T	2.59	3.00	3.00	ns
		XQ5VFX130T	2.67	3.07	N/A	ns
		XQ5VFX200T	N/A	3.27	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 86: **Global Clock Input to Output Delay With DCM in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-2I	-1I	-1M	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM in Source-Synchronous Mode						
$T_{ICKOFDCM\_0}$	Global Clock and OUTFF *with* DCM	XQ5VLX30T	3.71	4.15	N/A	ns
		XQ5VLX85	3.86	4.29	N/A	ns
		XQ5VLX110	3.92	4.36	N/A	ns
		XQ5VLX110T	3.92	4.36	N/A	ns
		XQ5VLX155T	4.18	4.62	N/A	ns
		XQ5VLX220T	4.41	4.85	N/A	ns
		XQ5VLX330T	N/A	5.04	N/A	ns
		XQ5VSX50T	3.91	4.35	N/A	ns
		XQ5VSX95T	4.16	4.59	N/A	ns
		XQ5VSX240T	N/A	5.11	N/A	ns
		XQ5VFX70T	3.96	4.41	4.41	ns
		XQ5VFX100T	4.10	4.53	4.53	ns
		XQ5VFX130T	4.29	4.74	N/A	ns
		XQ5VFX200T	N/A	5.03	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 87: **Global Clock Input to Output Delay With PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-2I	-1I	-1M	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* PLL in System-Synchronous Mode						
$T_{ICKOFPLL}$	Global Clock and OUTFF *with* PLL	XQ5VLX30T	2.30	2.70	N/A	ns
		XQ5VLX85	2.49	2.88	N/A	ns
		XQ5VLX110	2.53	2.92	N/A	ns
		XQ5VLX110T	2.53	2.92	N/A	ns
		XQ5VLX155T	2.60	3.01	N/A	ns
		XQ5VLX220T	2.74	3.12	N/A	ns
		XQ5VLX330T	N/A	3.27	N/A	ns
		XQ5VSX50T	2.36	2.76	N/A	ns
		XQ5VSX95T	2.29	2.69	N/A	ns
		XQ5VSX240T	N/A	3.34	N/A	ns
		XQ5VFX70T	2.71	3.10	3.10	ns
		XQ5VFX100T	2.70	3.10	3.10	ns
		XQ5VFX130T	2.75	3.17	N/A	ns
		XQ5VFX200T	N/A	3.35	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

Table 88: **Global Clock Input to Output Delay With PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-2I	-1I	-1M	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* PLL in Source-Synchronous Mode						
$T_{ICKOFPLL\_0}$	Global Clock and OUTFF *with* PLL	XQ5VLX30T	4.32	4.82	N/A	ns
		XQ5VLX85	4.40	4.88	N/A	ns
		XQ5VLX110	4.44	4.92	N/A	ns
		XQ5VLX110T	4.44	4.92	N/A	ns
		XQ5VLX155T	4.66	5.16	N/A	ns
		XQ5VLX220T	4.85	5.29	N/A	ns
		XQ5VLX330T	N/A	5.44	N/A	ns
		XQ5VSX50T	4.54	5.02	N/A	ns
		XQ5VSX95T	4.68	5.14	N/A	ns
		XQ5VSX240T	N/A	5.51	N/A	ns
		XQ5VFX70T	4.54	5.02	5.02	ns
		XQ5VFX100T	4.70	5.19	5.19	ns
		XQ5VFX130T	4.86	5.40	N/A	ns
		XQ5VFX200T	N/A	5.55	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

Table 89: **Global Clock Input to Output Delay With DCM and PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-2I	-1I	-1M	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM and PLL in System-Synchronous Mode						
$T_{ICKOFDCM\_PLL}$	Global Clock and OUTFF with DCM and PLL	XQ5VLX30T	2.48	2.84	N/A	ns
		XQ5VLX85	2.55	2.91	N/A	ns
		XQ5VLX110	2.61	2.97	N/A	ns
		XQ5VLX110T	2.61	2.97	N/A	ns
		XQ5VLX155T	2.66	3.01	N/A	ns
		XQ5VLX220T	2.75	3.09	N/A	ns
		XQ5VLX330T	N/A	3.28	N/A	ns
		XQ5VSX50T	2.61	2.96	N/A	ns
		XQ5VSX95T	2.56	2.91	N/A	ns
		XQ5VSX240T	N/A	3.27	N/A	ns
		XQ5VFX70T	2.66	3.03	3.03	ns
		XQ5VFX100T	2.51	2.91	2.91	ns
		XQ5VFX130T	2.59	2.98	N/A	ns
		XQ5VFX200T	N/A	3.18	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Table 90: **Global Clock Input to Output Delay With DCM and PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-2I	-1I	-1M	
LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, *with* DCM and PLL in Source-Synchronous Mode						
$T_{ICKOFDCM0\_PLL}$	Global Clock and OUTFF with DCM and PLL	XQ5VLX30T	3.63	4.06	N/A	ns
		XQ5VLX85	3.78	4.20	N/A	ns
		XQ5VLX110	3.84	4.27	N/A	ns
		XQ5VLX110T	3.84	4.27	N/A	ns
		XQ5VLX155T	4.10	4.53	N/A	ns
		XQ5VLX220T	4.33	4.76	N/A	ns
		XQ5VLX330T	N/A	4.95	N/A	ns
		XQ5VSX50T	3.83	4.26	N/A	ns
		XQ5VSX95T	4.08	4.50	N/A	ns
		XQ5VSX240T	N/A	5.02	N/A	ns
		XQ5VFX70T	3.88	4.32	4.32	ns
		XQ5VFX100T	4.02	4.44	4.44	ns
		XQ5VFX130T	4.21	4.65	N/A	ns
		XQ5VFX200T	N/A	4.94	N/A	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Virtex-5Q Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 91. Values are expressed in nanoseconds unless otherwise noted.

Table 91: **Global Clock Setup and Hold without DCM or PLL**

Symbol	Description	Device	Speed Grade			Units
			-2I	-1I	-1M	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard[1]						
T_{PSFD}/ T_{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock and IFF[2] without DCM or PLL	XQ5VLX30T	1.60 –0.35	1.76 –0.35	N/A	ns
		XQ5VLX85	1.89 –0.49	2.09 –0.49	N/A	ns
		XQ5VLX110	1.88 –0.43	2.09 –0.43	N/A	ns
		XQ5VLX110T	1.88 –0.43	2.09 –0.43	N/A	ns
		XQ5VLX155T	2.36 –0.50	2.78 –0.49	N/A	ns
		XQ5VLX220T	2.57 –0.74	2.86 –0.74	N/A	ns
		XQ5VLX330T	N/A	2.86 –0.56	N/A	ns
		XQ5VSX50T	1.74 –0.31	1.93 –0.31	N/A	ns
		XQ5VSX95T	2.10 –0.44	2.32 –0.44	N/A	ns
		XQ5VSX240T	N/A	2.28 0.18	N/A	ns
		XQ5VFX70T	2.06 –0.30	2.35 –0.30	2.35 –0.30	ns
		XQ5VFX100T	2.38 –0.42	2.66 –0.42	2.66 –0.42	ns
		XQ5VFX130T	2.59 –0.54	2.95 –0.54	N/A	ns
		XQ5VFX200T	N/A	2.81 –0.43	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Table 92: **Global Clock Setup and Hold with DCM in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-2I	-1I	-1M	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard[1]						
T_{PSDCM}/ T_{PHDCM}	No Delay Global Clock and IFF[2] with DCM in System-Synchronous Mode	XQ5VLX30T	1.70 –0.50	1.88 –0.50	N/A	ns
		XQ5VLX85	1.76 –0.43	1.95 –0.43	N/A	ns
		XQ5VLX110	1.76 –0.37	1.95 –0.37	N/A	ns
		XQ5VLX110T	1.76 –0.37	1.95 –0.37	N/A	ns
		XQ5VLX155T	2.16 –0.32	2.38 –0.32	N/A	ns
		XQ5VLX220T	2.17 –0.27	2.44 –0.27	N/A	ns
		XQ5VLX330T	N/A	2.44 –0.10	N/A	ns
		XQ5VSX50T	1.76 –0.37	1.95 –0.37	N/A	ns
		XQ5VSX95T	2.34 –0.41	2.35 –0.41	N/A	ns
		XQ5VSX240T	N/A	2.54 –0.10	N/A	ns
		XQ5VFX70T	1.86 –0.36	1.98 –0.36	1.98 –0.36	ns
		XQ5VFX100T	2.35 –0.51	2.49 –0.49	2.49 –0.49	ns
		XQ5VFX130T	2.48 –0.43	2.72 –0.42	N/A	ns
		XQ5VFX200T	N/A	2.43 –0.21	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 93: **Global Clock Setup and Hold with DCM in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-2I	-1I	-1M	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard[1]						
T_{PSDCM0}/ T_{PHDCM0}	No Delay Global Clock and IFF[2] with DCM in Source-Synchronous Mode	XQ5VLX30T	0.27 0.62	0.27 0.66	N/A	ns
		XQ5VLX85	0.24 0.76	0.24 0.80	N/A	ns
		XQ5VLX110	0.24 0.82	0.24 0.87	N/A	ns
		XQ5VLX110T	0.24 0.82	0.24 0.87	N/A	ns
		XQ5VLX155T	0.14 1.08	0.16 1.13	N/A	ns
		XQ5VLX220T	0.21 1.31	0.22 1.36	N/A	ns
		XQ5VLX330T	N/A	0.22 1.55	N/A	ns
		XQ5VSX50T	0.25 0.82	0.25 0.86	N/A	ns
		XQ5VSX95T	0.24 1.06	0.24 1.11	N/A	ns
		XQ5VSX240T	N/A	0.21 1.62	N/A	ns
		XQ5VFX70T	0.14 0.86	0.14 0.92	0.14 0.92	ns
		XQ5VFX100T	0.21 1.00	0.21 1.05	0.21 1.05	ns
		XQ5VFX130T	0.21 1.19	0.24 1.25	N/A	ns
		XQ5VFX200T	N/A	0.16 1.55	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 94: **Global Clock Setup and Hold with PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-2I	-1I	-1M	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard[1]						
T_{PSPLL}/ T_{PHPLL}	No Delay Global Clock and IFF[2] with PLL in System-Synchronous Mode	XQ5VLX30T	1.68 –0.80	1.90 –0.79	N/A	ns
		XQ5VLX85	1.95 –0.62	2.09 –0.61	N/A	ns
		XQ5VLX110	1.96 –0.57	2.10 –0.57	N/A	ns
		XQ5VLX110T	1.96 –0.57	2.10 –0.57	N/A	ns
		XQ5VLX155T	2.09 –0.49	2.37 –0.47	N/A	ns
		XQ5VLX220T	1.93 –0.36	2.09 –0.36	N/A	ns
		XQ5VLX330T	N/A	2.34 –0.21	N/A	ns
		XQ5VSX50T	2.07 –0.72	2.20 –0.72	N/A	ns
		XQ5VSX95T	2.17 –0.80	2.35 –0.79	N/A	ns
		XQ5VSX240T	N/A	2.33 –0.14	N/A	ns
		XQ5VFX70T	1.90 –0.30	2.07 –0.30	2.07 –0.30	ns
		XQ5VFX100T	1.91 –0.40	2.09 –0.38	2.09 –0.38	ns
		XQ5VFX130T	1.95 –0.28	2.14 –0.24	N/A	ns
		XQ5VFX200T	N/A	2.29 –0.14	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 95: **Global Clock Setup and Hold with PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-2I	-1I	-1M	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard[1]						
T_{PSPLL0}/ T_{PHPLL0}	No Delay Global Clock and IFF[2] with PLL in Source-Synchronous Mode	XQ5VLX30T	–0.33 1.22	–0.33 1.34	N/A	ns
		XQ5VLX85	–0.23 1.30	–0.22 1.39	N/A	ns
		XQ5VLX110	–0.24 1.34	–0.23 1.43	N/A	ns
		XQ5VLX110T	–0.25 1.34	–0.23 1.43	N/A	ns
		XQ5VLX155T	–0.12 1.56	–0.10 1.67	N/A	ns
		XQ5VLX220T	–0.34 1.75	–0.30 1.80	N/A	ns
		XQ5VLX330T	N/A	–0.30 1.95	N/A	ns
		XQ5VSX50T	–0.26 1.44	–0.25 1.53	N/A	ns
		XQ5VSX95T	–0.26 1.58	–0.24 1.65	N/A	ns
		XQ5VSX240T	N/A	–0.31 2.02	N/A	ns
		XQ5VFX70T	–0.10 1.44	–0.09 1.53	–0.09 1.53	ns
		XQ5VFX100T	–0.18 1.60	–0.18 1.71	–0.18 1.71	ns
		XQ5VFX130T	–0.11 1.76	–0.09 1.92	N/A	ns
		XQ5VFX200T	N/A	–0.10 2.06	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 96: **Global Clock Setup and Hold with DCM and PLL in System-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-2I	-1I	-1M	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVCMOS25 Standard[1]						
$T_{PSDCMPLL}$/ $T_{PHDCMPLL}$	No Delay Global Clock and IFF[2] with DCM and PLL in System-Synchronous Mode	XQ5VLX30T	1.89 –0.58	2.06 –0.58	N/A	ns
		XQ5VLX85	1.93 –0.51	2.13 –0.51	N/A	ns
		XQ5VLX110	1.93 –0.45	2.13 –0.45	N/A	ns
		XQ5VLX110T	1.93 –0.45	2.13 –0.45	N/A	ns
		XQ5VLX155T	2.31 –0.40	2.55 –0.40	N/A	ns
		XQ5VLX220T	2.32 –0.35	2.61 –0.35	N/A	ns
		XQ5VLX330T	N/A	2.61 –0.18	N/A	ns
		XQ5VSX50T	1.94 –0.45	2.14 –0.45	N/A	ns
		XQ5VSX95T	2.51 –0.49	2.53 –0.49	N/A	ns
		XQ5VSX240T	N/A	2.70 –0.18	N/A	ns
		XQ5VFX70T	2.03 –0.44	2.16 –0.44	2.16 –0.44	ns
		XQ5VFX100T	2.51 –0.59	2.66 –0.58	2.66 –0.58	ns
		XQ5VFX130T	2.64 –0.51	2.89 –0.51	N/A	ns
		XQ5VFX200T	N/A	2.59 –0.30	N/A	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 97: **Global Clock Setup and Hold with DCM and PLL in Source-Synchronous Mode**

Symbol	Description	Device	Speed Grade			Units
			-2I	-1I	-1M	
Example Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin,(1) using DCM, PLL, and Global Clock Buffer. For situations where clock and data inputs conform to different standards, adjust the setup and hold values accordingly using the values shown in IOB Switching Characteristics.						
$T_{PSDCMPLL\_0}$/ $T_{PHDCMPLL\_0}$	No Delay Global Clock and IFF(2) with DCM and PLL in Source-Synchronous Mode	XQ5VLX30T	0.46 0.54	0.46 0.57	N/A	ns
		XQ5VLX85	0.42 0.68	0.42 0.71	N/A	ns
		XQ5VLX110	0.41 0.74	0.41 0.78	N/A	ns
		XQ5VLX110T	0.41 0.74	0.41 0.78	N/A	ns
		XQ5VLX155T	0.29 1.00	0.33 1.04	N/A	ns
		XQ5VLX220T	0.36 1.23	0.38 1.27	N/A	ns
		XQ5VLX330T	N/A	0.38 1.46	N/A	ns
		XQ5VSX50T	0.43 0.74	0.43 0.77	N/A	ns
		XQ5VSX95T	0.41 0.98	0.41 1.02	N/A	ns
		XQ5VSX240T	N/A	0.38 1.53	N/A	ns
		XQ5VFX70T	0.32 0.78	0.32 0.83	0.32 0.83	ns
		XQ5VFX100T	0.35 0.92	0.35 0.96	0.35 0.96	ns
		XQ5VFX130T	0.37 1.11	0.41 1.16	N/A	ns
		XQ5VFX200T	N/A	0.33 1.46	N/A	ns

Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. The timing values were measured using the fine-phase adjustment feature of the DCM. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG. Package skew is not included in these measurements.
2. IFF = Input Flip-Flop

Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Virtex-5Q FPGA source-synchronous transmitter and receiver data-valid windows.

Table 98: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade			Units
			-2I	-1I	-1M	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion[(1)]	All	0.12	0.12	0.12	ns
T_{CKSKEW}	Global Clock Tree Skew[(2)]	XQ5VLX30T	0.22	0.22	N/A	ns
		XQ5VLX85	0.43	0.45	N/A	ns
		XQ5VLX110	0.50	0.51	N/A	ns
		XQ5VLX110T	0.50	0.51	N/A	ns
		XQ5VLX155T	0.85	0.88	N/A	ns
		XQ5VLX220T	1.07	1.10	N/A	ns
		XQ5VLX330T	N/A	1.29	N/A	ns
		XQ5VSX50T	0.44	0.45	N/A	ns
		XQ5VSX95T	0.72	0.74	N/A	ns
		XQ5VSX240T	N/A	1.36	N/A	ns
		XQ5VFX70T	0.42	0.43	0.43	ns
		XQ5VFX100T	0.84	0.86	0.86	ns
		XQ5VFX130T	0.84	0.86	N/A	ns
		XQ5VFX200T	N/A	1.29	N/A	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.10	0.10	0.10	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.07	0.08	0.08	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.25	0.25	0.25	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA_Editor and Timing Analyzer tools to evaluate clock skew specific to your application.

Table 99: **Package Skew[(1)]**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew[(2)]	XQ5VLX30T[(3)]	FF323	127	ps
		XQ5VLX85	EF676	142	ps
		XQ5VLX110	EF676	142	ps
		XQ5VLX110	EF1153	173	ps
		XQ5VLX110T	EF1136	163	ps
		XQ5VLX155T	EF1136	147	ps
		XQ5VLX220T	EF1738	156	ps
		XQ5VLX330T	EF1738	155	ps
		XQ5VSX50T	EF665	103	ps
		XQ5VSX95T	EF1136	176	ps
		XQ5VSX240T[(3)]	FF1738	161	ps
		XQ5VFX70T	EF665	102	ps
		XQ5VFX70T	EF1136	153	ps
		XQ5VFX100T	EF1136	144	ps
		XQ5VFX100T	EF1738	172	ps
		XQ5VFX130T	EF1738	181	ps
		XQ5VFX200T[(3)]	FF1738	164	ps

Notes:

1. Package trace length information is available for these device/package combinations. This information can be used to deskew the package.
2. These values represent the worst-case skew between any two SelectIO resources in the package: shortest flight time to longest flight time from Pad to Ball (7.0 ps per mm).
3. The EF package is not available for these devices.

Table 100: **Sample Window**

Symbol	Description	Device	Speed Grade			Units
			-2I	-1I	-1M	
T_{SAMP}	Sampling Error at Receiver Pins[(1)]	All	500	550	550	ps
T_{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO[(2)]	All	400	450	450	ps

Notes:

1. This parameter indicates the total sampling error of Virtex-5Q FPGA DDR input registers across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 DCM jitter
   - DCM accuracy (phase offset)
   - DCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of Virtex-5Q FPGA DDR input registers across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IODELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 101: **Source-Synchronous Pin-to-Pin Setup/Hold and Clock-to-Out**

Symbol	Description	Speed Grade			Units
		-2I	-1I	-1M	
Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO					
T_{PSCS}/T_{PHCS}	Setup/Hold of I/O clock	–0.54 1.72	–0.54 1.91	–0.54 1.91	ns
Pin-to-Pin Clock-to-Out Using BUFIO					
$T_{ICKOFCS}$	Clock-to-Out of I/O clock	4.82	5.40	5.40	ns

Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
05/05/09	1.0	Initial Xilinx release.
12/17/09	2.0	Changed the document classification from Preliminary Product Specification to Product Specification. Updated XQ5VSX240T, XQ5VFX70T, and XQ5VFX200T to production devices in Table 54 and Table 55. Updated package information for XQ5VFX200T and XQ5VSX240T in Table 99.
07/23/10	2.1	Production release of XQ5VFX70T and XQ5VFX100T in the -1M speed grade. This includes changes to Table 54 and Table 55. Added a -1M column to any table with speed grades. Also updated the -2I speed grade software in Table 55 for the XQ5VLX220T and XQ5VSX95T device. Added -1(M) column to Table 4 including values for XQ5VFX70T and XQ5VFX100T. Revised maximum V_{OD} in Table 8. Updated both minimum and maximum V_{OCM} in Table 10. Updated minimum DV_{PPIN} in Table 40. In Table 46, updated $T_{J4.25}$ and added note 5. In Table 51, added I-grade and M-grade delineation for gain error, bipolar gain error, and ADCCLK revised A_{IDD} maximum specification. Added note 1 to Table 57. In Table 71, added the FX70T (M) specification for the global clock tree (BUFG) F_{MAX}. Added the FX70T (M) specification for the F_{OUTMAX} to Table 74. Added note 5 to Table 76. Added note 5 to Table 77. Added note 3 to Table 81.
01/17/11	2.2	Revised production release of the XQ5VFX70T and XQ5VFX100T in the -1M speed grade to software version ISE 12.4 using the v1.71 speed specification (see Table 55).

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