XC4000XLA/XV Family FPGAs

Note: XC4000XLA devices are improved versions of XC4000XL devices. The XC4000XV devices have the same features as XLA devices, incorporate additional interconnect resources and extend gate capacity to 500,000 system gates. The XC4000XV devices require a separate 2.5V power supply for internal logic but maintain 5V I/O compatibility via a separate 3.3V I/O power supply. A general description of the XC4000XLA/XV device architecture in included in the XC4000E and XC4000X Series (Description only) file, v1.4 (11/97) on the Xilinx WEBLINX at: http://www.xilinx.com.

- System-featured Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - Synchronous write option
    - Dual-port RAM option
  - Flexible function generators and abundant flip-flops
  - Dedicated high-speed carry logic
  - Internal 3-state bus capability
  - 8 global low-skew clock or signal distribution networks
- Flexible array architecture
- Low power segmented routing architecture
- Systems-oriented features
  - IEEE 1149.1-compatible boundary scan
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - Unlimited reprogrammability
- Readback capability
  - Program verification and internal node observability

XC4000XLA/XV Electrical Features

- XLA devices require 3.0 - 3.6 Volts (VCC)
- XV devices require 2.3- 2.7 Volts (VCCINT) and 3.0-3.6V (VCCIO)
- 5.0 V TTL compatible I/O
- 3.3 V LVTTL, LVCMOS compliant I/O
- 5.0 V and 3.0 V PCI compliant I/O
- 12-mA or 24-mA current sink capability
- Safe under all power-up sequences
- XLA devices consume 40% less power than do XL devices
- XV devices consume 65% less power than do XL devices
- Optional input clamping to VCC (XLA) or VCCIO (XV)

Additional XC4000XLA/XV Family Features

- **Footprint Compatible with XC4000XL FPGAs** Lower cost with improved performance and lower power.
- **Advanced Technology** — 5 layer metal, 0.25µ CMOS process (XV) or 0.35µ CMOS process (XLA)
- **Highest Performance** — System performance beyond 100 MHz
- **High Capacity** — Up to 500,000 system gates and 270,000 synchronous SRAM bits
- **Low Power** — 3.3V/2.5V technology plus segmented routing architecture
- **Safe and Easy to Use** — Interfaces to any combination of 3.3 V and 5.0 V TTL compatible devices.

Table 1: XC4000XLA Series Field Programmable Gate Arrays

Device	Logic Cells	Max Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. User I/O	Required Configuration Bits
XC4013XLA	1,368	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	192	393,632
XC4020XLA	1,862	20,000	25,088	13,000 - 40,000	28 x 28	784	2,016	224	521,880
XC4028XLA	2,432	28,000	32,768	18,000 - 50,000	32 x 32	1,024	2,560	256	668,184
XC4036XLA	3,078	36,000	41,472	22,000 - 65,000	36 x 36	1,296	3,168	288	832,528
XC4044XLA	3,800	44,000	51,200	27,000 - 80,000	40 x 40	1,600	3,840	320	1,014,928
XC4052XLA	4,598	52,000	61,952	33,000 - 100,000	44 x 44	1,936	4,576	352	1,215,368
XC4062XLA	5,472	62,000	73,728	40,000 - 130,000	48 x 48	2,304	5,376	384	1,433,864
XC4085XLA	7,448	85,000	100,352	55,000 - 180,000	56 x 56	3,136	7,168	448	1,924,992
XC40110XV	9,728	110,000	131,072	75,000 - 235,000	64 x 64	4,096	9,216	448	2,686,136
XC40150XV	12,312	150,000	165,888	100,000 - 300,000	72 x 72	5,184	11,520	448	3,373,448
XC40200XV	16,758	200,000	225,792	130,000 - 400,000	84 x 84	7,056	15,456	448	4,551,056
XC40250XV	20,102	250,000	270,848	180,000 - 500,000	92 x 92	8,464	18,400	448	5,433,888

* Maximum values of gate range assume 20-30% of CLBs used as RAM

Xilinx SRAM XC4000 Series FPGAs

XC4000 Series high-performance, high-capacity Field Programmable Gate Arrays (FPGAs) provide the benefits of custom CMOS VLSI, while avoiding the initial cost, long development cycle, and inherent risk of a conventional masked gate array.

The result of fifteen years of FPGA design experience and feedback from thousands of customers, these FPGAs combine architectural versatility, increased speed, abundant routing resources, and new, sophisticated software to achieve fully automated implementation of complex, high-density, high-performance designs.

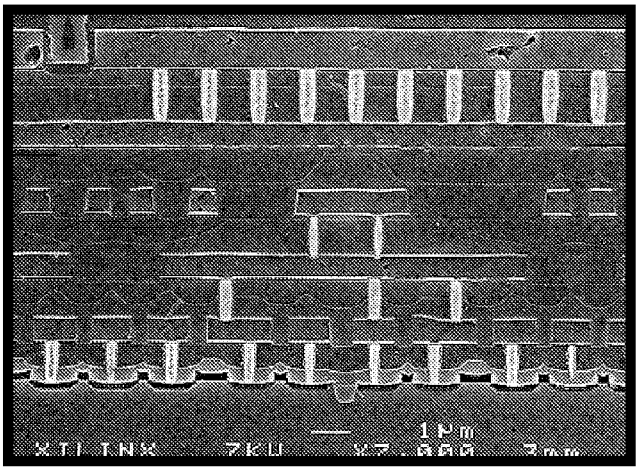


Figure 1: Cross Section of Xilinx 0.25 micron, 5 layer metal XC4000XV FPGA. Visible features are five layers of metallization, tungsten plug vias and trench isolation. The small gaps above the lowest layer are 0.25 micron polysilicon MOSFET gates. The excellent planarity of each metal layer is due to the use of "chemical-mechanical polishing" or CMP. In effect, each layer is ground flat before a new layer is added.

XC4000XLA/XV FPGAs

XC4000XLA/XV FPGAs use 5 layer metal silicon technology to improve performance while reducing device cost and power. In addition, IOB enhancements provide full PCI compliance and the JTAG functionality is expanded.

XC4000XV FPGAs

XC4000XV FPGAs incorporate all the features of the XLA devices but require a separate 2.5V power supply for internal logic. I/O pads are still driven from a 3.3V power supply. The 2.5V logic supply is named VCCINT and the 3.3 V IO supply is named VCCIO.

The XV devices also incorporate additional routing resources in the form of 8 octal-length segmented routing channels vertically and horizontally per row and column.

Differences Between the XC4000XLA/XV and XC4000XL FPGAs

The XC4000XLA/XV families of FPGAs are logically identical to XC4000EX and XC4000XL FPGAs, however I/O, configuration logic, JTAG functionality, and performance have been enhanced. In addition, they deliver:

- **Improved Performance**
  XLA/XV devices benefit from advance processing technology and a reduction in interconnect capacitance which improves performance over XL devices by more than 30%.
- **Lower Power**
  XLA/XV devices have reduced power requirements compared to equivalent XL devices.
- **Shorter routing delays**
  The smaller die of XLA/XV devices directly reduces clock delays and the delay of high-fanout signals. The reduction in clock delay allows improved pin-to-pin I/O specifications.
- **Lower Cost**
  XLA/XV device cost is directly related to the die size and has been reduced significantly from that of equivalent XL devices.
- **Express mode configuration**
  Express mode configuration is available on the XLA and XV devices.

IOB Enhancements

- **12/24 mA Output Drive**
  The XLA/XV family of FPGAs allow individual IOBs to be configured as high drive outputs. Each output can be configured to have 24 mA drive strength as opposed to the standard default strength of 12 mA.
- **VCC Clamping Diode**
  XLA and XV FPGAs have an optional clamping diode connected from each output to VCC (VCCIO for XV). When enabled they clamp ringing transients back to the 3.3V supply rail. This clamping action is required in 3.3V PCI applications. VCC clamping is a global option affecting all I/O pins. If enabled, TTL I/O compatibility is maintained, but full 5.0 Volt I/O tolerance is sacrificed.
- **Enhanced ESD protection**
  An improved ESD structure allows XV devices to safely pass the stringent 5V PCI (4.2.1.3) ringing test. This test applies an 11V pulse to each IOB for 11 ns via a 55 ohm resistor.

- **Full 3.3V and 5.0V PCI compliance**
  The addition of 12/24 mA drive, optional 3.3V clamping and improved ESD provides full compliance with either 3.3V or 5.0V PCI specifications.

Three-State Register

XC4000XLA/XV devices incorporate an optional register controlling the three-state enable in the IOBs.The use of the three-state control register can significantly improve output enable and disable time.

FastCLK Clock Buffers

The XLA/XV devices incorporate FastCLK clock buffers. Two FastCLK buffers are available on each of the right and left edges of the die. Each FastCLK buffer can provide a fast clock signal (typically < 1.5 ns clock delay) to all the IOBs within the IOB octant containing the buffer. The FastCLK buffers can be instantiated by use of the BUFFCLK symbols. (In addition to FastCLK buffers, the Global Early BUFGE clock buffers #1, #2, #5, and #6 can also provide fast clock signals (typically < 1.5 ns clock delay) to IOBs on the top and bottom of the die.

XLA, XV Power Requirements

XC4000XLA devices require 40% less power per CLB than equivalent XL devices. XC4000XV devices require 42% less power per CLB than equivalent XLA devices and 65% less power than XL devices The representative K-Factor for the following families can be found in Table 2. The K-Factor predicts device current for typical user designs and is based on filling the FPGA with active 16-Bit counters and measuring the device current at 1 MHz. This technique is described in XBRF14 "A Simple Method of Estimating Power in XC4000XL/EX/E FPGAs". To predict device power (P) using the K-Factor use the following formula:

P=V*K*N*F; where:

P= Device Power
V= Power supply voltage
K= the Device K-Factor
N = number of active registers
F = Frequency in MHz

Table 2: K-Factor and Relative Power.

FPGA Family	K-Factor	Power Relative To XL	Power Relative To XLA
XC4000XL	28	1.00	1.65
XC4000XLA	17	0.60	1.00
XC4000XV	13	0.35	0.58

XLA, XV Logic Performance

XC4000XLA/XV devices feature 30% faster device speed than XL devices, and consistent performance is achieved across all family members. Table 3 illustrates the performance of the XLA devices. For details regarding the implementation of these benchmarks refer to XBRF15 "Speed Metrics for High Performance FPGAs".

Table 3: XLA/XV Estimated Benchmark Performance

Register - Register Benchmarks	Size	Maximum Frequency
Adder	8-Bit	172 MHz
	16-Bit	144 MHz
	32-Bit	108 MHz
2 Cascaded Adders	16-Bit	94 MHz
4 Cascaded Adders	16-Bit	57 MHz
Cascaded 4LUTs	1 Level	314 MHz
	2 Level	193 MHz
	4 Level	108 MHz
	6 Level	75 MHz
Interconnect (Manhattan Distance)	1 CLBs	325 MHz
	4 CLBs	260 MHz
	16 CLBs	185 MHz
	64 CLBs	108 MHz
	128 CLBs	81 MHz
Dual Port RAM (Pipelined)	8-Bits by 16	172 MHz
	8-Bits by 256	172 MHz

Using Fast I/O CLKS

There are several issues associated with implementing fast I/O clocks by using multiple FastCLK and BUFGE clock buffers for I/O transfers and a BUFGLS clock buffer for internal logic.

Reduced Clock to Out Period - When transferring data from a BUFGLS clocked register to an IOB output register which is clocked with a fast I/O clock, the total amount of time available for the transfer is reduced.

Using Fast Capture Latch in IOB input - It is necessary to transfer data captured with the fast I/O clock edge to a delayed BUFGLS clock without error. The use of the Fast Capture Latch in the IOBs provides this functionality.

Driving multiple clock inputs - Since each FastCLK input can only reach one octant of IOBs it will usually be necessary to drive multiple FastCLK and BUFGE input pads with a copy of the system clock. Xilinx recommends that systems which use multiple FastCLK and BUFGE input buffers use a "Zero Delay" clock buffer such as the Cypress CY2308 to drive up to 8 input pins. These devices contain a Phase locked loop to eliminate clock delay, and specify less than 250ps output jitter.

PCB layout - The recommended layout is to place the PLL underneath the FPGA on the reverse side of the PCB. All 8 clock lines should be of equal length. This arrangement will allow all the clock line to be less than 2 cm in length which will generally eliminate the need for clock termination.

Advancing the FPGAs clock - An additional advantage to using a PLL-equipped clock buffer is that it can advance the FPGA clocks relative to the system clock by incorporating additional board delay in the feedback path. Approximately 6 inches of trace length are necessary to delay the signal by 1 ns.

Advancing the FPGA's clock directly reduces input hold requirements and improves clock to out delay. FPGA clocks should not be advanced more than the guaranteed minimum Output Hold Time (minus any associated clock jitter) or the outputs may change state before the system clock edge. For XLA and XV FPGAs the Output Hold Time is specified as a minimum Clock to Output Delay in the tables on pages 183, 182, 197, and 198. The maximum recommended clock advance equals this value minus any clock jitter.

Instantiating I/O elements- Depending on the design environment, it may be necessary to instantiate the fast I/O elements. They are found in the libraries as:

- **BUFGE (I,O)** - The Global Early Buffer
- **BUFGLS (I,O)**- The Global Low Skew Buffer
- **BUFFCLK (I,O)** - The FastCLK Buffer
- **ILFFX (D, GF, CE, C, Q)** - The Fast Capture Latch Macro

Locating I/O elements - It is necessary to connect these elements to a particular I/O pad in order to select which buffer or fast capture latch will be used.

Restricted Clock Loading - Because the input hold requirement is a function of internal clock delay, it may be necessary to restrict the routing of BUFGE to IOBs along the top and bottom of the die to obtain sub-ns clock delays.

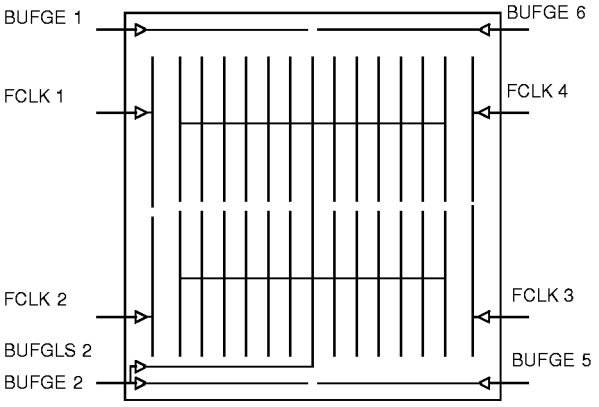


Figure 2: Location of FastCLK, BUFGE and BUFGLS Clock Buffers in XC4000XLA/XV FPGAs

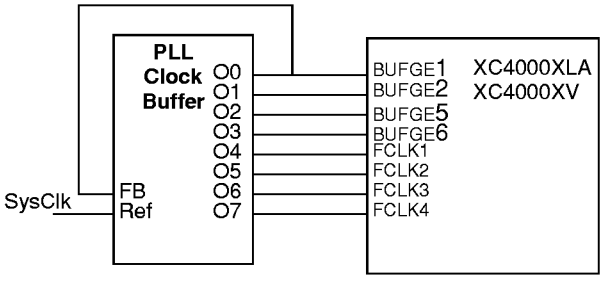


Figure 3: Diagram of XC4000XLA/XV FPGA Connected to PLL Clock Buffer Driving 4 BUFGE and 4 FastCLK Clock Buffers.

JTAG Enhancements

XC4000XLA/XV devices have improved JTAG functionality and performance in the following areas:

- **IDCODE** - The IDCODE register in JTAG is now supported. All future Xilinx FPGAs will support the IDCODE register. By using the IDCODE, the device connected to the JTAG port can be determined. The use of the IDCODE enables selective configuration dependent upon the FPGA found. The IDCODE register has the following binary format:
  `vvvv:ffff:fffa:aaaa:aaaa:cccc:cccc:ccc1`
  Where:
  c = the company code;
  a = the array dimension in CLBs;
  f = the Family code;
  v = the die version number

  Family Codes = 01 for XLA;
  = 02 for SpartanXL;
  = 03 for Virtex;
  = 07 for XV.

  Xilinx company code = 49 (hex)

Table 4: IDCODEs assigned to XC4000XLA/XV FPGAs

FPGA	IDCODE
XC4013XLA	0x00218093
XC4020XLA	0x0021c093
XC4028XLA	0x00220093
XC4036XLA	0x00224093
XC4044XLA	0x00228093
XC4052XLA	0x0022c093
XC4062XLA	0x00230093
XC4085XLA	0x00238093
XC40110XV	0x00e40093
XC40150XV	0x00e48093
XC40200XV	0x00e54093
XC40250XV	0x00e5c093

- **Configuration State** - The configuration state is available to JTAG controllers.
- **Configure Disable** - The JTAG port can be prevented from reconfiguring the FPGA
- **TCK Startup** - TCK can now be used to clock the start-up block in addition to other user clocks.
- **CCLK holdoff** - Changed the requirement for Boundary Scan Configure or EXTEST to be issued prior to the release of INIT pin and CCLK cycling.
- **Reissue configure** - The Boundary Scan Configure can be reissued to recover from an unfinished attempt to configure the device.
- **Bypass FF** - Bypass FF and IOB is modified to provide DRCLOCK only during BYPASS for the bypass flip-flop and during EXTEST or SAMPLE/PRELOAD for the IOB register.

Differences between the XC4000XV and XC4000XLA FPGAs

The high density of the XC4000XV family FPGAs is achieved by using advanced 0.25 micron silicon technology. A 2.5 Volt power supply (VCCINT) is necessary to provide the reduced supply voltage required by 0.25 micron internal logic, however to maintain TTL compatibility a 3.3V power supply (VCCIO) is required by the I/O.

To accommodate the higher gate capacity of XV devices, additional interconnect has been added. These differences are detailed below.

- **VCCINT (2.5 Volt) Power Supply Pins**
  The XV family of FPGAs requires a 2.5V power supply for internal logic, which is named VCCINT. The pins assigned to the VCCINT supply are named in the pinout guide for the XC4000XV FPGAs and in Table 5 on page 166.
- **VCCIO (3.3 Volt) Power Supply Pins**
  Both the XV and XLA FPGAs use a 3.3V power supply to power the I/O pins. The I/O supply is named VCCIO in the XV family.
- **Octal-Length Interconnect Channels**
  The XC40110XV, XC40150XV, XC40200XV, and XC40250XV have enhanced routing. Eight routing channels of octal length have been added to each CLB in both vertical and horizontal dimensions.

XC4000XLA Socket Compatibility with XL FPGAs

The XC4000XLA devices are generally available in the same packages as equivalent XL devices, however the range of packages available for the XC4085XLA has been extended to include smaller packages such as the HQ240.

XC4000XV Socket Compatibility with XL/XLA FPGAs

XC4000XV devices are available in five package options, pin-grid PG599 and ball-grid BG560, BG432, and BG352 and quad-flatpack HQ240. With the exception of the VCCINT power pins, XC4000XV FPGAs are compatible with XL and XLA devices in these packages if the following guidelines are followed:

- Lay out the PCB for the XV pinout.
- When an XL or XLA device is installed disconnect the VCCINT (2.5 V) supply. For the PG599, VCCINT should be connected to 3.3V. For BG560, BG432 and BG352 and HQ240 packages, the VCCINT voltage source should be left unconnected. The unused I/O pins in the

XL/XLA devices connected to VCCINT will be pulled up to 3.3V. Care must be taken to insure that these pins are not driven when the XL/XLA device is operative.

- When an XC4000XV is installed, the VCCINT pins must be connected to a 2.5V power supply.

The differences between the XL and XV packages are detailed below:

PG559 - XLA and XL devices in the PG599 package have 56 VCC pins.The XC4000XV devices allocate 16 of these I/O pins to VCCINT (2.5V).

BG560 - XLA and XL devices in the BG560 package have 448 I/O pins.The XC4000XV devices allocate 16 of these I/O pins to VCCINT (2.5V).

BG432- XLA and XL devices in the BG432 package have 352 I/O pins. The XC4000XV devices allocate 16 of these I/O pins to VCCINT (2.5V).

BG352 - XLA and XL devices in the BG352 package have 289 I/O pins.The XC4000XV devices allocate 15 of these I/O pins to VCCINT (2.5V).

HQ240- XLA and XL devices in the HQ240 package have 193 I/O pins.The XC4000XV devices allocate 15 of these I/O pins to VCCINT (2.5V).

Table 5: VCCINT (2.5 V) Pins in XV Packages

HQ240	BG352	BG432	BG560	PG559
P198	D10	A10	E12	H12
P185	D5	AB2	AD2	H18
P164	K4	AB30	AD32	H26
P154	N3	AG28	AK31	H32
P137	W2	AH15	AM17	M8
P116	AE3	AH5	AK5	M36
P104	AC10	AJ10	AK11	V8
P93	AC13	AK22	AN25	V36
P77	AE19	B23	C24	AF8
P55	AB24	B4	D6	AF36
P43	V24	C16	C17	AM8
P27	N24	E28	E30	AM36
P16	J24	K29	K32	AT12
P4	D24	K3	J1	AT18
P225	A20	R2	T3	AT26
-	-	R29	U32	AT32

XC4000XLA/XV I/O Signalling Standards

XLA and XV devices are compatible with TTL, LVTTL, PCI 3V, PCI 5V and LVCMOS signalling. The various standards are illustrated in Table 6 and the signaling environment is illustrated in Figure 4.

VCC Clamping

XLA/XV devices are fully 5V TTL I/O compatible if VCC clamping is not enabled. The I/O pins can withstand input voltages up to 7V. With VCC clamping enabled, the XLA/XV devices will begin to clamp input voltages to one diode voltage drop above VCC. In both cases negative voltage is clamped to one diode voltage drop below ground.

XLA/XV devices maintain LVTTL I/O compatibility when VCC clamping is enabled, however full 5.0V TTL I/O compatibility is sacrificed.

Overshoot and Undershoot

Ringing wave forms are allowed on XLA/XV inputs as long as undershoot is limited to -2.0V and overshoot is limited to +7.0V and current is limited to 100 mA for less than 10 ns. If VCC clamping is enabled then overshoot will begin to be clamped at VCC/VCCIO plus one diode voltage drop and undershoot will be clamped to ground minus one diode voltage drop. In either case the current must be limited to 100 mA per pin for less than 10 ns.

Table 6: I/O Standards supported by XC4000XLA and XV FPGAs

Signaling Standard	VCC Clamping	Output Drive	V_{IH_MAX}	$V_{IH\ MIN}$	$V_{IL\ MAX}$	$V_{OH\ MIN}$	$V_{OL\ MAX}$
TTL	Not allowed	12/24 mA	5.5	2.0	0.8	2.4	0.4
LVTTL	OK	12/24 mA	3.6	2.0	0.8	2.4	0.4
PCI5V	Not allowed	24 mA	5.5	2.0	0.8	2.4	0.4
PCI3V	Required	12 mA	3.6	50% of VCC/VCCIO	30% of VCC/VCCIO	90% of VCC/VCCIO	10% of VCC/VCCIO
LVCMOS 3V	OK	12/24 mA	3.6	50% of VCC/VCCIO	30% of VCC/VCCIO	90% of VCC/VCCIO	10% of VCC/VCCIO

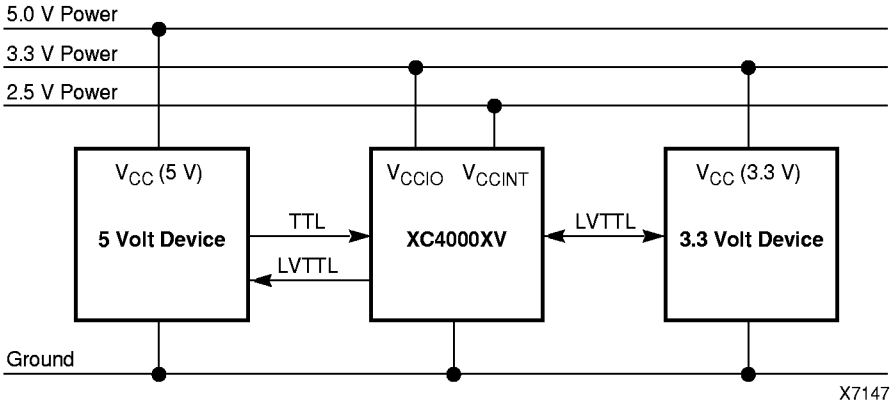


Figure 4: **The Signalling Environment for XLA/XV FPGAS.** For XLA devices the VCCIO and VCCINT supplies are replaced by a single 3.3 Volt VCC supply, however, all indicated I/O signalling is still supported.

Express Configuration Mode

Express configuration mode is similar to Slave Serial configuration mode, except that data is processed one byte per CCLK cycle instead of one bit per CCLK cycle. An external source is used to drive CCLK, while byte-wide data is loaded directly into the configuration data shift registers (Figure 5). A CCLK frequency of 10 MHz is equivalent to a 80 MHz serial rate, because eight bits of configuration data are loaded per CCLK cycle. Express mode does not sup-

port CRC error checking, but does support constant-field error checking. A length count is not used in Express mode.

Express mode must be specified as an option to the BitGen program, which generates the bitstream. The Express mode bitstream is not compatible with the other configuration modes. Express mode is selected by a <010> on the mode pins (M2, M1, M0).

The first byte of parallel configuration data must be available at the D inputs of the FPGA a short setup time before the second rising CCLK edge. Subsequent data bytes are clocked in on each consecutive rising CCLK edge (Figure 6).

Pseudo Daisy Chain

As illustrated in Figures 5 and 6, multiple devices with different configurations can be configured in a pseudo daisy chain provided that all of the devices are in Express mode. A single combined byte-wide data stream is used to configure the chain of Express mode devices. CCLK pins are tied together and D0-D7 pins are tied together as a data buss for all devices along the chain. A status signal is passed from DOUT of each device to the CS1 input of the device which follows it in the chain. Frame data is accepted only when CS1 is High and the device's configuration memory is not already full. The lead device in the chain has its CS1 input tied High (or floating, since there is an internal pullup). The status pin DOUT is initially High for all devices in the chain until the data stream header of seven bytes is loaded. This allows header data to be loaded into all devices in the chain simultaneously. After the header is loaded in all devices, their DOUT pins are pulled Low disabling configuration of all devices in the chain except the first device. As each device in the chain is filled, its DOUT goes High driving High the CS1 input of the next device, thereby enabling configuration of the next device in the pseudo daisy chain.

The requirement that all DONE pins in a daisy chain be wired together applies only to Express mode, and only if all devices in the chain are to become active simultaneously. All 4000XLA/XV devices in Express mode are synchronized to the DONE pin. User I/O for each device becomes active after the DONE pin for that device goes High (The exact timing is determined by BitGen options.)

Since the DONE pin is open-drain and does not drive a High value, tying the DONE pins of all devices together prevents all devices in the chain from going High until the last device in the chain has completed its configuration cycle. If the DONE pin of a device is left unconnected, the device becomes active as soon as that device has been configured.

Table 7: Pin Functions During Configuration (4000XLA/XV Express mode only)

CONFIGURATION MODE <M2:M1:M0>	USER OPERATION
EXPRESS MODE <0:1:0>	**PIN FUNCTION**
M2(LOW) (I)	M2
M1(HIGH) (I)	M1
M0(LOW) (I)	M0
HDC (HIGH)	I/O
$\overline{\text{LDC}}$ (LOW)	I/O
$\overline{\text{INIT}}$	I/O
DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
CCLK (I)	CCLK (I)
DATA 7 (I)	I/O
DATA 6 (I)	I/O
DATA 5 (I)	I/O
DATA 4 (I)	I/O
DATA 3 (I)	I/O
DATA 2 (I)	I/O
DATA 1 (I)	I/O
DATA 0 (I)	I/O
DOUT	SGCK4-I/O
TDI	TDI-I/O
TCK	TCK-I/O
TMS	TMS-I/O
TDO	TDO-(O)
CS1	I/O

Notes
1. A shaded table cell represents the internal pull-up used before and during configuration.
2. (I) represents an input; (O) represents an output.
3. $\overline{\text{INIT}}$ is an open-drain output during configuration.

Because only XC4000XLA/XV, SpartanXL, and XC5200 devices support Express mode, only these devices can be used to form an Express mode pseudo daisy chain.

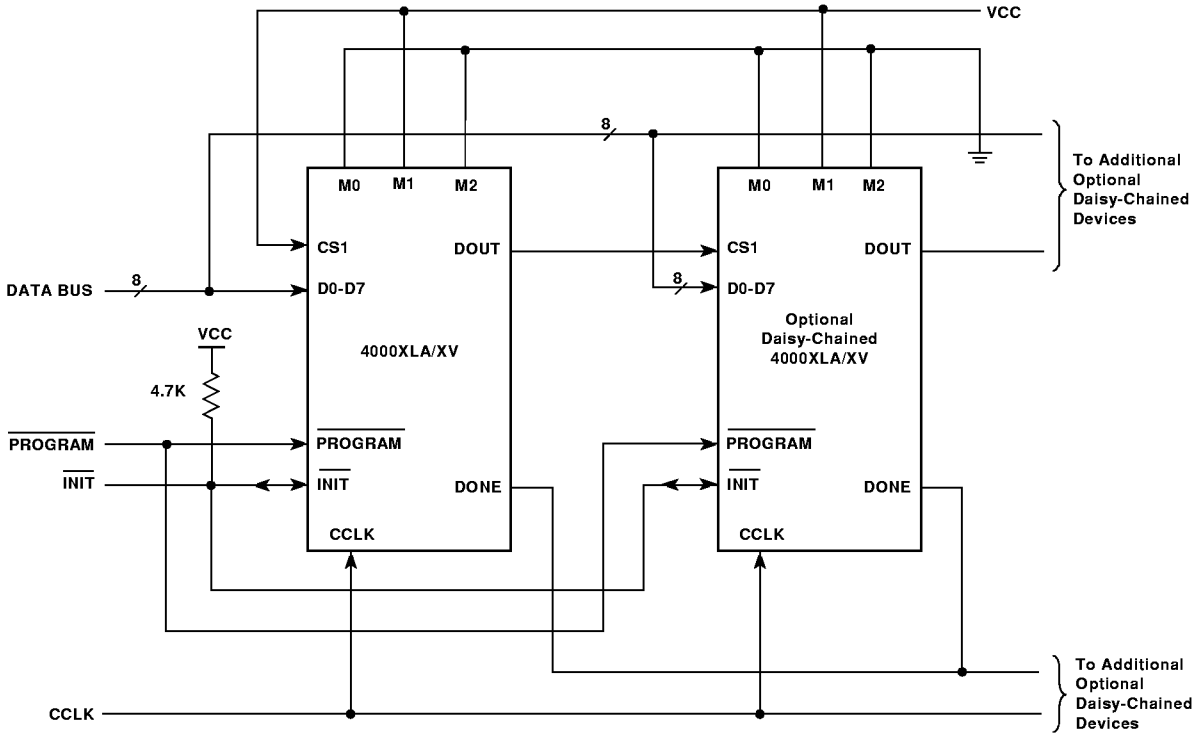
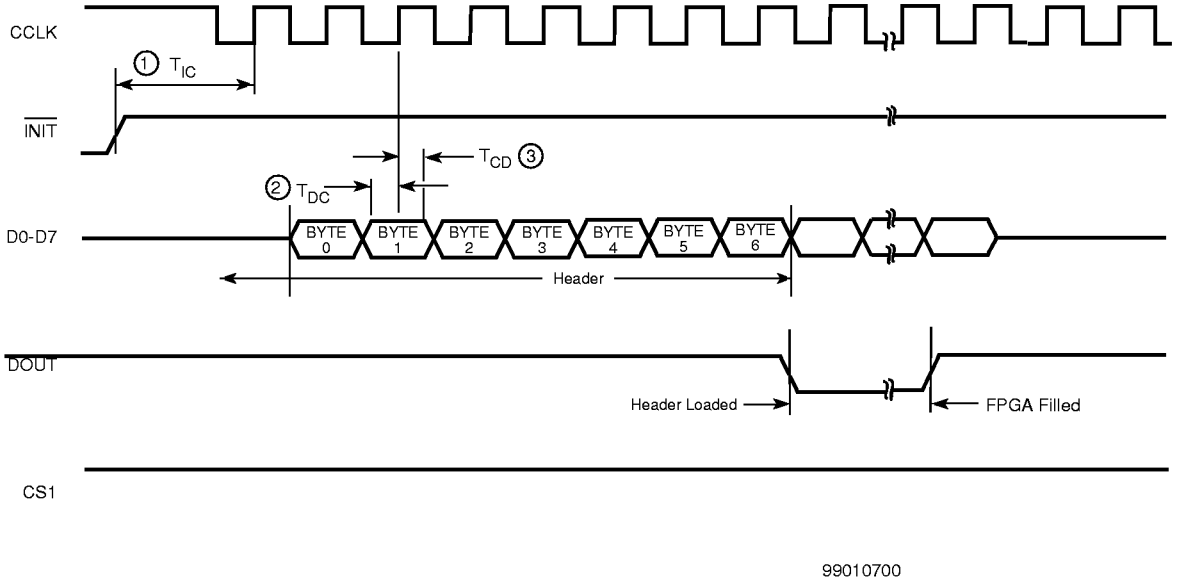


Figure 5: Express Mode Circuit Diagram

Table 8: Express Mode Programming Switching Characteristic

	Description	Symbol	Min	Max	Units
CCLK	$\overline{INIT}$ (High) setup time	T_{IC}	5		µs
	D0 - D7 setup time	T_{DC}	20		ns
	D0 - D7 hold time	T_{CD}	0		ns
	CCLK High time	T_{CCH}	45		ns
	CCLK Low time	T_{CCL}	45		ns
	CCLK Frequency	F_{CC}		10	MHz
			Preliminary		



Note: CS1 *must* remain High throughout loading of the configuration data stream. In the pseudo daisy chain of Figure 5, the 7 byte data stream header is loaded into all devices simultaneously. Each device's data frames are then loaded in turn when its CS1 pin is driven High by the DOUT of the preceding device in the chain.

Figure 6: Express Mode Programming Switching Waveforms

Data Stream Format

The data stream ("bitstream") format is identical for all serial configuration modes, but different for the 4000XLA/XV Express mode. In Express mode, the device becomes active when DONE goes High, therefore no length count is required. Additionally, CRC error checking is not supported in Express mode. The data stream format is shown in Table 9. Express mode data is shown with D0 at the left and D7 at the right.

The configuration data stream begins with two bytes of eight ones each, a preamble code of one byte, followed by three bytes of eight ones each, and finally an end-of-header field check byte. This header of seven bytes is followed by the actual configuration data in frames. The length and number of frames depends on the device type. Each frame begins with a start field and ends with an end-of-frame field check byte. In all cases, additional start-up bytes of data are required to provide six, or more, clocks for the start-up sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All startup bytes are don't-cares; these bytes are not included in bitstreams created by the Xilinx software.

A selection of CRC or non-CRC error checking is allowed by the bitstream generation software. The 4000XLA Express mode only supports non-CRC error checking. The non-CRC error checking tests for a designated end-of-frame field check byte for each frame. non-CRC error checking tests for a designated end-of-frame field check byte for each frame.

Table 9: 4000XLA/XV Express Mode Data Stream Format

Data Type	Express Mode (D0-D7) (4000XLA only)
Fill Byte	FFFFh
Preamble Code	11110010b
Fill Byte	FFFFFFh
End-of-Header Field Check Byte	11010010b
Start Field	11111110b
Data Frame	DATA(n-1:0)
End-of-Frame Field Check Byte	11010010b
Extend Write Cycle	FFD2FFFFFFh
Start-Up Bytes	FFFFFFFFFFFFh

LEGEND:

Unshaded	Once per data stream
Light	Once per data frame

Detection of an error results in the suspension of data loading and the pulling down of the $\overline{INIT}$ pin. The user must detect $\overline{INIT}$ and initialize a new configuration by pulsing the $\overline{PROGRAM}$ pin Low or cycling VCC.

Serial PROM Recommendation

Table 10 shows the physical characteristics of each FPGA family member and the recommended Xilinx Serial PROM recommended for use as configuration storage.

Table 10: Physical Characteristics and Recommended Serial PROM

Device	Max. User I/O	CLB Matrix	Total CLBs	Logic Cells	Number of Flip-Flops	Max. RAM Bits (No Logic)	Required Configur-ation Bits	Serial PROM
XC4013XLA	192	24 x 24	576	1,368	1,536	18,432	393,632	XC17512L
XC4020XLA	224	28 x 28	784	1,862	2,016	25,088	521,880	XC17512L
XC4028XLA	256	32 x 32	1,024	2,432	2,560	32,768	668,184	XC1701L
XC4036XLA	288	36 x 36	1,296	3,078	3,168	41,472	832,528	XC1701L
XC4044XLA	320	40 x 40	1,600	3,800	3,840	51,200	1,014,928	XC1701L
XC4052XLA	352	44 x 44	1,936	4,598	4,576	61,952	1,215,368	XC1702L
XC4062XLA	384	48 x 48	2,304	5,472	5,376	73,728	1,433,864	XC1702L
XC4085XLA	448	56 x 56	3,136	7,448	7,168	100,352	1,924,992	XC1702L
XC40110XV	448	64 x 64	4,096	9,728	9,216	131,072	2,686,136	XC1704L
XC40150XV	448	72 x 72	5,184	12,312	11,520	165,888	3,373,448	XC1704L
XC40200XV	448	84 x 84	7,056	16,758	15,456	225,792	4,551,056	XC1704L+XC17512L
XC40250XV	448	92 x 92	8,464	20,102	18,400	270,848	5,433,888	XC1704L+XC1702L

User I/O Per Package

Table 11 shows the number of user I/Os available in each package for XC4000XLA/XV-Series devices. Call your local sales office for the latest availability information.

Table 11: User I/O Pins Available by Device and Package

		Maximum I/O Acessible per Package											
Device	Max I/O	HQ160	PQ160	HQ208	PQ208	HQ240	PQ240	BG256	HQ304	BG352	BG432	PG559	BG560
XC4013XLA	192		129		160		192	192					
XC4020XLA	224		129		160		193	205					
XC4028XLA	256	129		160		193		205	256	256			
XC4036XLA	288	129		160		193			256	288	288		
XC4044XLA	320	129		160		193			256	289	320		
XC4052XLA	352	129		160		193			256	289	352		352
XC4062XLA	384	129		160		193			256	289	352		384
XC4085XLA	448	129		160		193			256	289	352		448
XC40110XV	448					178				274	336		432
XC40150XV	448					178				274	336	448	432
XC40200XV	448										336		432
XC40250XV	448										336	448	432

Product Availability

XC4000XLA Product Availability

Table 12 shows the planned packages and speed grades for XC4000XLA-Series devices. Call your local sales office for the latest availability information, or see the Xilinx WEBLINX at http://www.xilinx.com for the latest revision of the specifications.

Table 12: Component Availability Chart for XC4000XLA FPGAs

	PINS	84	100	100	144	144	160	160	176	176	208	208	240	240	256	299	304	352	411	432	475	559	560
	TYPE	Plast. PLCC	Plast. PQFP	Plast. VQFP	Plast. TQFP	High-Perf. TQFP	High-Perf. QFP	Plast. PQFP	Plast. TQFP	High-Perf. TQFP	High-Perf. QFP	Plast. PQFP	High-Perf. QFP	Plast. PQFP	Plast. BGA	Ceram. PGA	High-Perf. QFP	Plast. BGA	Ceram. PGA	Plast. BGA	Ceram. PGA	Ceram. PGA	Plast. BGA
	CODE	PC84	PQ100	VQ100	TQ144	HT144	HQ160	PQ160	TQ176	HT176	HQ208	PQ208	HQ240	PQ240	BG256	PG299	HQ304	BG352	PG411	BG432	PG475	PG559	BG560
XC4013XLA	-09							C I				C I		C I	C I								
	-08							C I				C I		C I	C I								
	-07							C				C		C	C								
XC4020XLA	-09							C I				C I		C I	C I								
	-08							C I				C I		C I	C I								
	-07							C				C		C	C								
XC4028XLA	-09						C I				C I		C I		C I			C I					
	-08						C I				C I		C I		C I			C I					
	-07						C				C		C		C			C					
XC4036XLA	-09						C I				C I		C I					C I		C I			
	-08						C I				C I		C I					C I		C I			
	-07						C				C		C					C		C			
XC4044XLA	-09						C I				C I		C I				C I	C I		C I			
	-08						C I				C I		C I				C I	C I		C I			
	-07						C				C		C				C	C		C			
XC4052XLA	-09						C I				C I		C I				C I	C I		C I			C I
	-08						C I				C I		C I				C I	C I		C I			C I
	-07						C				C		C				C	C		C			C
XC4062XLA	-09						C I				C I		C I				C I	C I		C I			C I
	-08						C I				C I		C I				C I	C I		C I			C I
	-07						C				C		C				C	C		C			C
XC4085XLA	-09						C I				C I		C I				C I	C I		C I			C I
	-08						C I				C I		C I				C I	C I		C I			C I
	-07						C				C		C				C	C		C			C

1/25/99

C = Commercial T_J = 0° to +85°C

I= Industrial T_J = -40°C to +100°C

6

XC4000XV Product Availability

Figure 13 shows the planned packages and speed grades for XC4000XV-Series devices. Call your local sales office for the latest availability information, or see the Xilinx WEBLINX at http://www.xilinx.com for the latest revision of the specifications.

Table 13: Component Availability Chart for XC4000XV FPGAs

	PINS	84	100	100	144	144	160	160	176	176	208	208	240	240	256	299	304	352	411	432	475	559	560
	TYPE	Plast. PLCC	Plast. PQFP	Plast. VQFP	Plast. TQFP	High-Perf. TQFP	High-Perf. QFP	Plast. PQFP	Plast. TQFP	High-Perf. TQFP	High-Perf. QFP	Plast. PQFP	High-Perf. QFP	Plast. PQFP	Plast. BGA	Ceram. PGA	High-Perf. QFP	Plast. BGA	Ceram. PGA	Plast. BGA	Ceram. PGA	Ceram. PGA	Plast. BGA
	CODE	PC84	PQ100	VQ100	TQ144	HT144	HQ160	PQ160	TQ176	HT176	HQ208	PQ208	HQ240	PQ240	BG256	PG299	HQ304	BG352	PG411	BG432	PG475	PG559	BG560
XC40110XV	-09												C I					C I		C I			C I
	-08												C I					C I		C I			C I
	-07												C					C		C			C
XC40150XV	-09												C I					C I		C I		C I	C I
	-08												C I					C I		C I		C I	C I
	-07												C					C		C		C	C
XC40200XV	-09																			C I			C I
	-08																			C I			C I
	-07																			C			C
XC40250XV	-09																			C I		C I	C I
	-08																			C I		C I	C I
	-07																			C		C	C

11/2498

C = Commercial T_J = 0° to +85°C

I= Industrial T_J = -40°C to +100°C

XC4000XLA D.C. and Switching Performance Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered final.

Occasionally, values are of mixed classification. These are highlighted in bold face and the tables involved include a note explaining the nature of the bold face entries. All specifications are subject to change without notice.

Additional Specifications

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Absolute Maximum Ratings

Symbol	Description		Values	Units
V_{CC}	Supply voltage relative to GND		-0.5 to 4.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to 5.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to 5.5	V
V_{CCt}	Longest Supply Voltage Rise Time from 1 V to 3V		50	ms
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Notes: 1. Maximum DC overshoot or undershoot above V_{CC} or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to + 7.0 V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	3.0	3.6	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	3.0	3.6	V
V_{IH}	High-level input voltage		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage		0	30% of V_{CC}	V
T_{IN}	Input signal transition time			250	ns

Note: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C. Input and output measurement threshold is ~50% of V_{CC}.

DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0 mA, V_{CC} min (LVTTL)		2.4		V
	High-level output voltage @ I_{OH} = -500 µA, (LVCMOS)		90% V_{CC}		V
V_{OL}	Low-level output voltage @ I_{OL} = 24.0 mA, V_{CC} min (LVTTL) (Note 1)			0.4	V
	Low-level output voltage @ I_{OL} = 1500 µA, (LVCMOS)			10% V_{CC}	V
V_{DR}	Data Retention Supply Voltage (below which configuration data may be lost)		2.5		V
I_{CCO}	Quiescent FPGA supply current (Note 2)			10	mA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, SBGA, PQ, HQ, MQ packages		10	pF
		PGA packages		16	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)		0.02	0.15	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.3	2.0	mA

Notes: 1. With up to 64 pins simultaneously sinking 24 mA
2. With no output current loads, no active input or Longline pull-up resistors, all I/O pins Tri-stated and floating

XC4000XLA Clock Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature. Values apply to all XC4000XLA devices and expressed in nanoseconds unless otherwise noted.

XC4000XLA Global Low Skew Clock Input to Clock K

		Speed Grade	All	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Max**	**Max**	
Delay from pad through Global Low Skew (GLS) clock buffer to any clock input, K.	T_{GLS}	XC4013XLA		2.4	2.1	1.9	ns
		XC4020XLA		2.6	2.3	2.1	ns
		XC4028XLA		2.9	2.6	2.3	ns
		XC4036XLA		3.2	2.8	2.5	ns
		XC4044XLA		3.6	3.1	2.8	ns
		XC4052XLA		3.9	3.4	3.1	ns
		XC4062XLA		4.2	3.7	3.3	ns
		XC4085XLA		5.0	4.4	3.9	ns
			Preliminary				

XC4000XLA FastCLK Input to IOB Clock Input

		Speed Grade	All	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Max**	**Max**	
Delay from pad through FastCLK buffer to any IOB clock input.	T_{FCLK}	XC4013XLA		1.5	1.3	1.1	ns
		XC4020XLA		1.5	1.3	1.2	ns
		XC4028XLA		1.6	1.4	1.3	ns
		XC4036XLA		1.7	1.5	1.4	ns
		XC4044XLA		1.8	1.6	1.4	ns
		XC4052XLA		1.9	1.7	1.5	ns
		XC4062XLA		2.0	1.8	1.6	ns
		XC4085XLA		2.3	2.0	1.8	ns
				Preliminary			

Note: Values in **bold face** are preliminary, all other values are advance.

XC4000XLA Clock Buffer Switching Characteristic Guidelines (Cont)

XC4000XLA Global Early Clock Input to IOB Clock Input; BUFGE #s 1, 2, 5, and 6.

		Speed Grade	All	-09	-08	-07	Units
Description	Symbol	Device	Min	Max	Max	Max	
Delay from pad through Global Early (GE) clock buffer to any IOB clock input for BUFGE #1, 2, 5, and 6.	T_{GE}	XC4013XLA		1.7	1.5	1.3	ns
		XC4020XLA		1.9	1.7	1.5	ns
		XC4028XLA		2.1	1.9	1.7	ns
		XC4036XLA		2.4	2.2	1.9	ns
		XC4044XLA		2.7	2.4	2.2	ns
		XC4052XLA		3.0	2.7	2.4	ns
		XC4062XLA		3.3	3.0	2.7	ns
		XC4085XLA		3.7	3.3	3.0	ns
			Preliminary				

XC4000XLA Global Early Clock Input to IOB Clock Input; BUFGE #s 3, 4, 7, and 8.

		Speed Grade	All	-09	-08	-07	Units
Description	Symbol	Device	Min	Max	Max	Max	
Delay from pad through Global Early (GE) clock buffer to any IOB clock input for BUFGE 3, 4, 7, and 8.	T_{GE}	XC4013XLA		2.4	2.1	1.9	ns
		XC4020XLA		2.6	2.3	2.1	ns
		XC4028XLA		2.9	2.6	2.3	ns
		XC4036XLA		3.2	2.8	2.5	ns
		XC4044XLA		3.6	3.1	2.8	ns
		XC4052XLA		3.9	3.4	3.1	ns
		XC4062XLA		4.2	3.7	3.3	ns
		XC4085XLA		5.0	4.4	3.9	ns
			Preliminary				

XC4000XLA CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XLA devices and expressed in nanoseconds unless otherwise noted.

	Speed Grade	-09		-08		-07		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Combinatorial Delays								
F/G inputs to X/Y outputs	T_{ILO}		1.1		1.0		0.9	ns
F/G inputs via H' to X/Y outputs	T_{IHO}		1.9		1.7		1.5	ns
F/G inputs via transparent latch to Q outputs	T_{ITO}		2.0		1.8		1.6	ns
C inputs via SR/H0 via H to X/Y outputs	T_{HH0O}		1.7		1.6		1.4	ns
C inputs via H1 via H to X/Y outputs	T_{HH1O}		1.6		1.4		1.3	ns
C inputs via DIN/H2 via H to X/Y outputs	T_{HH2O}		1.7		1.6		1.4	ns
C inputs via EC, DIN/H2 to YQ, XQ output (bypass)	T_{CBYP}		1.1		1.0		0.9	ns
CLB Fast Carry Logic								
Operand inputs (F1, F2, G1, G4) to C_{OUT}	T_{OPCY}		1.0		0.9		0.8	ns
Add/Subtract input (F3) to C_{OUT}	T_{ASCY}		1.2		1.1		1.0	ns
Initialization inputs (F1, F3) to C_{OUT}	T_{INCY}		0.8		0.7		0.6	ns
C_{IN} through function generators to X/Y outputs	T_{SUM}		1.7		1.5		1.3	ns
C_{IN} to C_{OUT}, bypass function generators	T_{BYP}		0.1		0.1		0.1	ns
Carry Net Delay, C_{OUT} to C_{IN}	T_{NET}		0.17		0.15		0.13	ns
Sequential Delays								
Clock K to Flip-Flop outputs Q	T_{CKO}		1.5		1.3		1.2	ns
Clock K to Latch outputs Q	T_{CKLO}		1.5		1.3		1.2	ns
Setup Time before Clock K								
F/G inputs	T_{ICK}	0.7		0.7		0.6		ns
F/G inputs via H	T_{IHCK}	1.4		1.3		1.2		ns
C inputs via H0 through H	T_{HH0CK}	1.3		1.2		1.1		ns
C inputs via H1 through H	T_{HH1CK}	1.2		1.1		1.0		ns
C inputs via H2 through H	T_{HH2CK}	1.3		1.2		1.1		ns
C inputs via DIN	T_{DICK}	0.6		0.6		0.5		ns
C inputs via EC	T_{ECCK}	0.7		0.6		0.5		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	0.5		0.4		0.4		ns
CIN input via F/G	T_{CCK}	1.2		1.1		1.0		ns
CIN input via F/G and H	T_{CHCK}	2.0		1.7		1.6		ns
Hold Time after Clock K								
All Hold Times		0.0		0.0		0.0		ns
Clock								
Clock High time	T_{CH}	2.2		1.9		1.7		ns
Clock Low time	T_{CL}	2.2		1.9		1.7		ns
Set/Reset Direct								
Width (High)	T_{RPW}	2.3		2.3		2.3		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		2.5		2.2		2.0	ns
Global Set/Reset								
Minimum GSR Pulse Width	T_{MRW}		12.8		11.4		10.2	ns
Delay from GSR input to any Q	T_{MRQ}	See page 189 for TRRI values per device.						
Toggle Frequency (MHz) (for export control)	F_{TOG}		227		263		294	MHz
		Preliminary						

XC4000XLA RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XLA devices and are expressed in nanoseconds unless otherwise noted.

Single Port RAM	Speed Grade		-09		-08		-07		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	
Write Operation									
Address write cycle time (clock K period)	16x2 32x1	T_{WCS} T_{WCTS}	6.7 6.7		5.9 5.9		5.3 5.3		ns ns
Clock K pulse width (active edge)	16x2 32x1	T_{WPS} T_{WPTS}	3.4 3.4		3.0 3.0		2.7 2.7		ns ns
Address setup time before clock K	16x2 32x1	T_{ASS} T_{ASTS}	1.5 1.5		1.3 1.3		1.2 1.2		ns ns
Address hold time after clock K	16x2 32x1	T_{AHS} T_{AHTS}	0.0 0.0		0.0 0.0		0.0 0.0		ns ns
DIN setup time before clock K	16x2 32x1	T_{DSS} T_{DSTS}	1.5 2.11 .8		1.3 1.6		1.2 1.5		ns ns
DIN hold time after clock K	16x2 32x1	T_{DHS} T_{DHTS}	0.0 0.0		0.0 0.0		0.0 0.0		ns ns
WE setup time before clock K	16x2 32x1	T_{WSS} T_{WSTS}	1.4 1.3		1.3 1.2		1.1 1.1		ns ns
WE hold time after clock K	16x2 32x1	T_{WHS} T_{WHTS}	0.0 0.0		0.0 0.0		0.0 0.0		ns ns
Data valid after clock K	16x2 32x1	T_{WOS} T_{WOTS}		5.0 5.8		4.4 5.2		4.2 4.7	ns ns
Read Operation									
Address read cycle time	16x2 32x1	T_{RC} T_{RCT}	2.6 3.8		2.6 3.8		2.6 3.8		ns ns
Data Valid after address change (no Write Enable)	16x2 32x1	T_{ILO} T_{IHO}		1.1 1.9		1.0 1.7		0.9 1.5	ns ns
Address setup time before clock K	16x2 32x1	T_{ICK} T_{IHCK}	0.7 1.4		0.7 1.3		0.6 1.2		ns ns
			Advance						

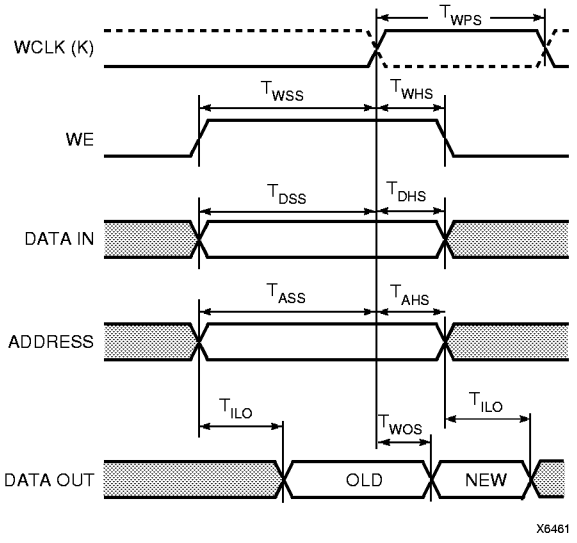
XC4000XLA CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XLA devices and are expressed in nanoseconds unless otherwise noted.

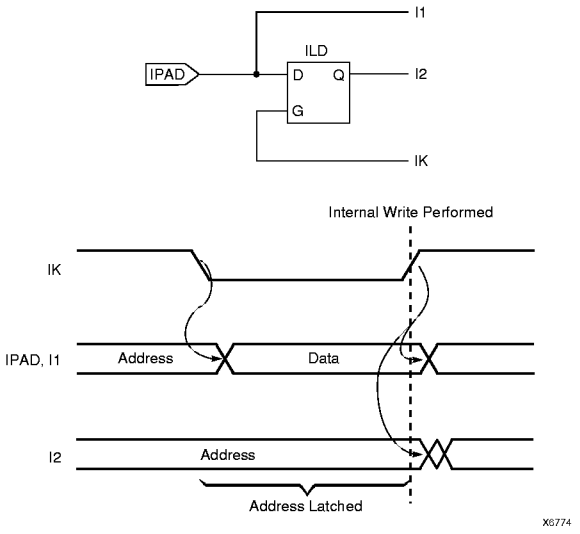
Dual Port RAM	Speed Grade		--09		-08		-07		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	
Address write cycle time (clock K period)	16x1	T_{WCDS}	6.7		5.9		5.3		ns
Clock K pulse width (active edge)	16x1	T_{WPDS}	3.4		3.0		2.7		ns
Address setup time before clock K	16x1	T_{ASDS}	1.5		1.3		1.2		ns
Address hold time after clock K	16x1	T_{AHDS}	0.0		0.0		0.0		ns
DIN setup time before clock K	16x1	T_{DSDS}	1.7		1.6		1.4		ns
DIN hold time after clock K	16x1	T_{DHDS}	0.0		0.0		0.0		ns
WE setup time before clock K	16x1	T_{WSDS}	1.4		1.3		1.1		ns
WE hold time after clock K	16x1	T_{WHDS}	0.0		0.0		0.0		ns
Data valid after clock K	16x1	T_{WODS}		5.7		5.1		4.6	ns
			Preliminary						

6

XC4000XLA CLB RAM Synchronous (Edge-Triggered) Write Timing



Single Port RAM



Dual Port RAM

XC4000XLA Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

XC4000XLA Global Clock Input to Output Delay

		Speed Grade	All	-09	-08	-07	Units
Description	Symbol	Device	Min	Max	Max	Max	
Global Low Skew (GLS) Clock Input to Output Delay using Output Flip-Flop	T_{ICKOF}	XC4013XLA		**5.6**	5.0	4.5	ns
		XC4020XLA		5.8	5.2	4.7	ns
		XC4028XLA		6.1	5.5	4.9	ns
		XC4036XLA		**6.4**	5.7	5.1	ns
		XC4044XLA		6.8	6.0	5.4	ns
		XC4052XLA		**7.1**	6.3	5.7	ns
		XC4062XLA		**7.4**	6.6	5.9	ns
		XC4085XLA		**8.2**	7.3	6.5	ns
For output SLOW option add	T_{SLOW}	All Devices		1.7	1.6	1.4	ns
				Preliminary			

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 7.
Note: Values in **bold face** are preliminary, all other values are advance.

XC4000XLA FastCLK Input to Output Delay for BUFNW, BUFSW, BUFNE, & BUFSE

		Speed Grade	All	-09	-08	-07	Units
Description	Symbol	Device	Min	Max	Max	Max	
FastCLK Input to Output Delay using Output Flip-Flop for FastCLK buffers BUFNW, BUFSW, BUFNE, and BUFSE.	T_{ICKFOF}	XC4013XLA		4.6	4.1	3.7	ns
		XC4020XLA		4.7	4.2	3.7	ns
		XC4028XLA		4.8	4.3	3.8	ns
		XC4036XLA		4.9	4.4	3.9	ns
		XC4044XLA		5.0	4.4	4.0	ns
		XC4052XLA		5.1	4.5	4.1	ns
		XC4062XLA		5.2	4.6	4.1	ns
		XC4085XLA		5.4	4.8	4.3	ns
For output SLOW option add	T_{SLOW}	All Devices		4.6	4.1	3.7	ns
				Preliminary			

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 7.
Note: Values in **bold face** are preliminary, all other values are advance.

XC4000XLA Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

XC4000XLA Global Early Clock Input to Output Delay for BUFGE #s 1, 2, 5, and 6

		Speed Grade	All	-09	-08	-07	Units
Description	Symbol	Device	Min	Max	Max	Max	
Global Clock Signal Input to Output Delay using	T_{ICKEOF}	XC4013XLA		4.9	4.4	3.9	ns
Global Early (GE) clock buffer to clock Output		XC4020XLA		5.1	4.6	4.1	ns
Flip-Flop for BUFGE #s 1, 2, 5, & 6.		XC4028XLA		5.3	4.8	4.3	ns
		XC4036XLA		5.6	5.1	4.5	ns
		XC4044XLA		5.9	5.3	4.8	ns
		XC4052XLA		6.2	5.6	5.0	ns
		XC4062XLA		6.5	5.9	5.3	ns
		XC4085XLA		6.9	6.2	5.6	ns
			Preliminary				

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 7.

XC4000XLA Global Early Clock Input to Output Delay for BUFGE #s 3, 4, 7, and 8

		Speed Grade	All	-09	-08	-07	Units
Description	Symbol	Device	Min	Max	Max	Max	
Global Clock Signal Input to Output Delay using	T_{ICKEOF}	XC4013XLA		5.7	5.1	4.5	ns
Global Early (GE) clock buffer to clock Output		XC4020XLA		5.9	5.3	4.7	ns
Flip-Flop for BUFGE #s 3, 4, 7, & 8.		XC4028XLA		6.1	5.4	4.9	ns
		XC4036XLA		6.3	5.6	5.0	ns
		XC4044XLA		6.5	5.8	5.2	ns
		XC4052XLA		6.8	6.0	5.4	ns
		XC4062XLA		7.0	6.3	5.6	ns
		XC4085XLA		7.5	6.7	6.0	ns
			Preliminary				

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 7.

Capacitive Load Factor

Figure 7 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay.

Figure 7 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

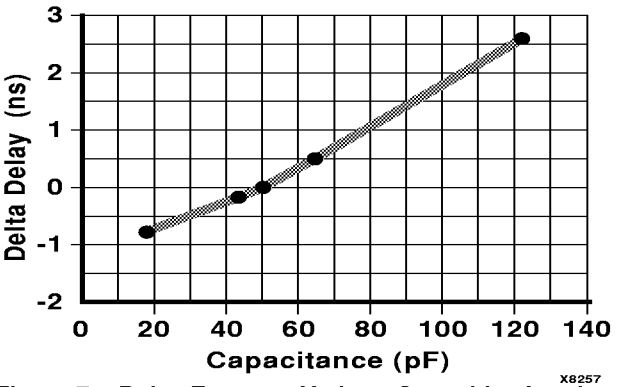


Figure 7: Delay Factor at Various Capacitive Loads

XC4000XLA Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

XC4000XLA Global Low Skew Clock, Set-Up and Hold

		Speed Grade	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Input Setup and Hold Time Relative to Global Clock Input Signal						
No Delay		XC4013XLA	**1.0 / 3.0**	0.8 / 2.6	0.2 / 2.5	ns
Global Low Skew Clock and IFF	T_{PSN}/T_{PHN}	XC4020XLA	0.9 / 3.2	0.7 / 2.9	0.1 / 2.7	ns
		XC4028XLA	0.8 / 3.8	0.6 / 3.3	0.0 / 3.0	ns
		XC4036XLA	**0.6 / 4.0**	0.4 / 3.5	0.0 / 3.3	ns
		XC4044XLA	0.4 / 4.4	0.2 / 3.9	0.0 / 3.6	ns
		XC4052XLA	**0.3 / 4.6**	0.2 / 4.1	0.0 / 3.9	ns
		XC4062XLA	**0.2 / 5.0**	0.1 / 4.5	0.0 / 4.2	ns
		XC4085XLA	**0.0 / 5.4**	0.0 / 4.8	0.0 / 4.5	ns
Partial Delay		XC4013XLA	**4.4 / 0.5**	4.1 / 0.3	3.7/ 0.0	ns
Global Low Skew Clock and IFF	T_{PSP}/T_{PHP}	XC4020XLA	4.5 / 0.6	4.1 / 0.3	3.7 / 0.0	ns
		XC4028XLA	4.6 / 0.7	4.2 / 0.4	3.7/ 0.0	ns
		XC4036XLA	**4.6 / 0.8**	4.2 / 0.4	3.7/ 0.0	ns
		XC4044XLA	4.7 / 0.9	4.3 / 0.5	3.8 / 0.0	ns
		XC4052XLA	**4.8 / 1.0**	4.3 / 0.6	3.8 / 0.2	ns
		XC4062XLA	**5.0 / 1.0**	4.4 / 0.7	3.8 / 0.4	ns
		XC4085XLA	**5.5 / 1.2**	4.7 / 0.9	3.8 / 0.5	ns
Full Delay		XC4013XLA	**4.4 / 0.0**	4.1 / 0.0	3.7 / 0.0	ns
Global Low Skew Clock and IFF	T_{PSD}/T_{PHD}	XC4020XLA	4.6 / 0.0	4.2 / 0.0	3.8 / 0.0	ns
		XC4028XLA	4.8 / 0.0	4.4 / 0.0	3.9 / 0.0	ns
		XC4036XLA	**4.9 / 0.0**	4.5 / 0.0	4.0 / 0.0	ns
		XC4044XLA	5.0 / 0.0	4.6 / 0.0	4.1 / 0.0	ns
		XC4052XLA	**5.2 / 0.0**	4.7 / 0.0	4.2 / 0.0	ns
		XC4062XLA	**5.5 / 0.0**	4.9 / 0.0	4.3 / 0.0	ns
		XC4085XLA	**6.0 / 0.0**	5.2/ 0.0	4.4 / 0.0	ns
				Preliminary		

IFF = Input Flip-Flop or Latch

Notes: Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer (TRCE) to determine the setup and hold times under given design conditions.

XC4000XLA Pin-to-Pin Input Parameter Guidelines (Cont.)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

XC4000XLA FastCLK Input Set-Up and Hold for BUFNW, BUFSW, BUFNE, & BUFSE

		Speed Grade	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Input Setup and Hold Time Relative to FastCLK Input Signal						
No Delay		XC4013XLA	0.0 / 3.2	0.0 / 2.9	0.0 / 2.6	ns
FastCLK and IFF	T_{PSFN}/T_{PHFN}	XC4020XLA	0.0 / 3.3	0.0 / 3.0	0.0 / 2.7	ns
		XC4028XLA	0.0 / 3.4	0.0 / 3.1	0.0 / 2.8	ns
		XC4036XLA	0.0 / 3.5	0.0 / 3.2	0.0 / 2.9	ns
		XC4044XLA	0.0 / 3.6	0.0 / 3.3	0.0 / 3.0	ns
		XC4052XLA	0.0 / 3.7	0.0 / 3.4	0.0 / 3.1	ns
		XC4062XLA	0.0 / 3.8	0.0 / 3.5	0.0 / 3.2	ns
		XC4085XLA	0.0 / 3.9	0.0 / 3.6	0.0 / 3.3	ns
Partial Delay		XC4013XLA	3.5 / 0.6	3.2 / 0.3	2.9 / 0.0	ns
FastCLK and IFF	$T_{PSFP}T_{PHFP}$	XC4020XLA	3.7 / 0.4	3.4 / 0.2	3.1 / 0.0	ns
		XC4028XLA	3.9 / 0.2	3.6 / 0.1	3.3 / 0.0	ns
		XC4036XLA	4.1 / 0.0	3.8 / 0.0	3.5 / 0.0	ns
		XC4044XLA	4.3 / 0.0	4.0 / 0.0	3.7 / 0.0	ns
		XC4052XLA	4.5 / 0.0	4.2 / 0.0	3.9 / 0.0	ns
		XC4062XLA	4.7 / 0.0	4.4 / 0.0	4.1 / 0.0	ns
		XC4085XLA	5.1 / 0.0	4.8 / 0.0	4.5 / 0.0	ns
Full Delay		XC4013XLA	3.5 / 0.6	3.2 / 0.3	2.9 / 0.0	ns
FastCLK and IFF	T_{PSFD}/T_{PHFD}	XC4020XLA	3.8 / 0.4	3.5 / 0.2	3.2 / 0.0	ns
		XC4028XLA	4.0 / 0.2	3.7 / 0.1	3.4 / 0.0	ns
		XC4036XLA	4.3 / 0.0	4.0 / 0.0	3.7 / 0.0	ns
		XC4044XLA	4.6 / 0.0	4.3 / 0.0	4.0 / 0.0	ns
		XC4052XLA	4.9 / 0.0	4.6 / 0.0	4.3 / 0.0	ns
		XC4062XLA	5.3 / 0.0	5.0 / 0.0	4.7 / 0.0	ns
		XC4085XLA	6.1 / 0.0	5.8 / 0.0	5.5 / 0.0	ns
				Preliminary		

IFF = Input Flip-Flop

Notes: Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer(TRCE) to determine the setup and hold times under given design conditions.

XC4000XLA BUFGE #s 1, 2, 5, and 6 Global Early Clock, Set-up and Hold for IFF and FCL

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

		Speed Grade	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Input Setup and Hold Time Relative to Global Clock Input Signal						
No Delay		XC4013XLA	1.0 / 3.2	0.8 / 2.6	0.5 / 1.8	ns
Global Early Clock and IFF	T_{PSEN}/T_{PHEN}	XC4020XLA	1.0 / 3.4	0.8 / 2.8	0.5 / 2.0	ns
Global Early Clock and FCL	T_{PFSEN}/T_{PFHEN}	XC4028XLA	1.0 / 3.5	0.8 / 3.0	0.5 / 2.2	ns
		XC4036XLA	1.0 / 3.6	0.8 / 3.1	0.5 / 2.4	ns
		XC4044XLA	1.0 / 3.8	0.8 / 3.3	0.5 / 2.6	ns
		XC4052XLA	1.0 / 4.0	0.8 / 3.5	0.5 / 2.8	ns
		XC4062XLA	1.0 / 4.2	0.8 / 3.7	0.5 / 3.0	ns
		XC4085XLA	1.0 / 4.6	0.8 / 4.0	0.5 / 3.2	ns
Partial Delay		XC4013XLA	4.6 / 0.0	4.2 / 0.0	3.9 / 0.0	ns
Global Early Clock and IFF	T_{PSEP}/T_{PHEP}	XC4020XLA	4.8 / 0.1	4.4 / 0.1	4.1 / 0.0	ns
Global Early Clock and FCL	T_{PFSEP}/T_{PFHEP}	XC4028XLA	4.9 / 0.1	4.6 / 0.1	4.4 / 0.0	ns
		XC4036XLA	5.0 / 0.2	4.7 / 0.1	4.5 / 0.0	ns
		XC4044XLA	5.5 / 0.3	5.1 / 0.2	4.8 / 0.0	ns
		XC4052XLA	5.8 / 0.3	5.3 / 0.2	5.0 / 0.0	ns
		XC4062XLA	6.2 / 0.4	5.6 / 0.2	5.2 / 0.0	ns
		XC4085XLA	6.5 / 0.5	5.9 / 0.3	5.4 / 0.0	ns
Full Delay		XC4013XLA	4.6 / 0.0	4.2 / 0.0	3.9 / 0.0	ns
Global Early Clock and IFF	T_{PSED}/T_{PHED}	XC4020XLA	4.9 / 0.0	4.5 / 0.0	4.1 / 0.0	ns
		XC4028XLA	5.1 / 0.0	4.7 / 0.0	4.4 / 0.0	ns
		XC4036XLA	5.3 / 0.0	4.9 / 0.0	4.5 / 0.0	ns
		XC4044XLA	5.8 / 0.0	5.3 / 0.0	5.0 / 0.0	ns
		XC4052XLA	6.2 / 0.0	5.7 / 0.0	5.3 / 0.0	ns
		XC4062XLA	6.7 / 0.0	6.1 / 0.0	5.6 / 0.0	ns
		XC4085XLA	7.0 / 0.0	6.4 / 0.0	6.0 / 0.0	ns
				Preliminary		

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Notes: Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer (TRCE) to determine the setup and hold times under given design conditions.

XC4000XLA BUFGE #s 3, 4, 7, and 8 Global Early Clock, Set-up and Hold for IFF and FCL

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

		Speed Grade	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Input Setup and Hold Time Relative to Global Clock Input Signal						
No Delay		XC4013XLA	0.8 / 3.2	0.6 / 2.6	0.4 / 2.0	ns
Global Early Clock and IFF	T_{PSEN}/T_{PHEN}	XC4020XLA	0.8 / 3.4	0.6 / 2.8	0.4 / 2.2	ns
Global Early Clock and FCL	T_{PFSEN}/T_{PFHEN}	XC4028XLA	0.8 / 3.5	0.6 / 3.0	0.4 / 2.4	ns
		XC4036XLA	0.8 / 3.6	0.6 / 3.1	0.4 / 2.6	ns
		XC4044XLA	0.8 / 3.8	0.6 / 3.3	0.4 / 2.8	ns
		XC4052XLA	0.8 / 4.0	0.6 / 3.5	0.4 / 3.0	ns
		XC4062XLA	0.8 / 4.2	0.6 / 3.7	0.4 / 3.2	ns
		XC4085XLA	0.8 / 4.6	0.6 / 4.0	0.4 / 3.4	ns
Partial Delay		XC4013XLA	4.4 / 0.0	4.0 / 0.0	3.6 / 0.0	ns
Global Early Clock and IFF	T_{PSEP}/T_{PHEP}	XC4020XLA	4.6 / 0.1	4.2 / 0.1	3.8 / 0.0	ns
Global Early Clock and FCL	T_{PFSEP}/T_{PFHEP}	XC4028XLA	4.7 / 0.1	4.4 / 0.1	4.1 / 0.0	ns
		XC4036XLA	4.8 / 0.2	4.5 / 0.2	4.2 / 0.0	ns
		XC4044XLA	5.2 / 0.3	4.8 / 0.3	4.4 / 0.0	ns
		XC4052XLA	5.6 / 0.3	5.1 / 0.3	4.6 / 0.0	ns
		XC4062XLA	6.0 / 0.4	5.4 / 0.4	4.8 / 0.0	ns
		XC4085XLA	6.3 / 0.5	5.7 / 0.5	5.0 / 0.0	ns
Full Delay		XC4013XLA	4.4 / 0.0	4.0 / 0.0	3.6 / 0.0	ns
Global Early Clock and IFF	T_{PSED}/T_{PHED}	XC4020XLA	4.7 / 0.0	4.3 / 0.0	3.8 / 0.0	ns
		XC4028XLA	4.9 / 0.0	4.5 / 0.0	4.1 / 0.0	ns
		XC4036XLA	5.1 / 0.0	4.7 / 0.0	4.2 / 0.0	ns
		XC4044XLA	5.6 / 0.0	5.1 / 0.0	4.6 / 0.0	ns
		XC4052XLA	6.0 / 0.0	5.5 / 0.0	4.9 / 0.0	ns
		XC4062XLA	6.5 / 0.0	5.9 / 0.0	5.2 / 0.0	ns
		XC4085XLA	6.8 / 0.0	6.2 / 0.0	5.6 / 0.0	ns
				Preliminary		

, FCL = Fast Capture LatchIFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Notes: Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer (TRCE) to determine the setup and hold times under given design conditions.

XC4000XLA IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

		Speed Grade	-09		-08		-07		Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Clocks									
Clock Enable (EC) to Clock (IK)	T_{ECIK}	All devices	0.0		0.0		0.0		ns
Delay from FCL enable (OK) active edge to IFF clock (IK) active edge	T_{OKIK}	All Devices	1.4		1.3		1.2		ns
Setup Times									
Pad to Clock (IK), no delay	T_{PICK}	All Devices	1.2		1.0		0.9		ns
Pad to Clock (IK), via transparent Fast Capture Latch, no delay	T_{PICKF}	All Devices	1.6		1.4		1.3		ns
Pad to Fast Capture Latch Enable (OK), no delay	T_{POCK}	All Devices	0.8		0.7		0.6		ns
Hold Times									
All Hold Times		All Devices	0.0		0.0		0.0		ns
Global Set/Reset									
Minimum GSR Pulse Width	T_{MRW}	All devices	12.8		11.4		10.2		ns
Global Set/Reset									
Delay from GSR input to any Q	T_{RRI}*	XC4013XLA		11.4		10.2		9.1	ns
		XC4020XLA		13.3		11.9		10.6	ns
		XC4028XLA		14.3		12.8		11.4	ns
		XC4036XLA		16.2		14.5		12.9	ns
		XC4044XLA		18.1		16.2		14.4	ns
		XC4052XLA		19.5		17.4		15.6	ns
		XC4062XLA		20.9		18.7		16.7	ns
		XC4085XLA		24.7		22.1		19.7	ns
Propagation Delays									
Pad to I1, I2	T_{PID}	All devices		1.0		0.9		0.8	ns
Pad to I1, I2 via transparent input latch, no delay	T_{PLI}	All devices		2.1		1.9		1.7	ns
Pad to I1, I2 via transparent FCL and input latch, no delay	T_{PFLI}	All devices		2.5		2.2		2.0	ns
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}	All devices		1.1		1.0		0.9	ns
Clock (IK) to I1, I2 (latch enable, active Low)	T_{IKLI}	All devices		1.2		1.1		1.0	ns
FCL Enable (OK) active edge to I1, I2 (via transparent standard input latch)	T_{OKLI}	All devices		2.4		2.1		1.9	ns
			Preliminary						

Notes: IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch
* Indicates Minimum Amount of Time to Assure Valid Data.

XC4000XLA IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values are expressed in nanoseconds unless otherwise noted.

			-09		-08		-07		Units
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Clocks									
Clock High	T_{CH}		2.2		1.9		1.7		ns
Clock Low	T_{CL}		2.2		1.9		1.7		ns
Propagation Delays									
Clock (OK) to Pad	T_{OKPOF}			3.2		2.9		2.6	ns
Output (O) to Pad	T_{OPF}			2.6		2.4		2.1	ns
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZ}			2.7		2.4		2.2	ns
3-state to Pad active and valid	T_{TSONF}			2.8		2.5		2.3	ns
Output (O) to Pad via Fast Output MUX	T_{OFPF}			3.6		3.2		2.9	ns
Select (OK) to Pad via Fast MUX	T_{OKFPF}			3.3		3.0		2.6	ns
Setup and Hold Times									
Output (O) to clock (OK) setup time	T_{OOK}		0.3		0.3		0.3		ns
Output (O) to clock (OK) hold time	T_{OKO}		0.0		0.0		0.0		ns
Clock Enable (EC) to clock (OK) setup time	T_{ECOK}		0.0		0.0		0.0		ns
Clock Enable (EC) to clock (OK) hold time	T_{OKEC}		0.0		0.0		0.0		ns
Global Set/Reset									
Minimum GSR pulse width	T_{MRW}		12.8		11.4		10.2		ns
Delay from GSR input to any Pad	T_{RPO}*	XC4013XLA		14.4		12.8		11.5	
		XC4020XLA		16.3		14.5		13.0	
		XC4028XLA		17.3		15.4		13.8	
		XC4036XLA		19.1		17.1		15.3	
		XC4044XLA		21.0		18.8		16.8	
		XC4052XLA		22.5		20.1		17.9	
		XC4062XLA		23.9		21.3		19.0	
		XC4085XLA		27.7		24.7		22.1	
Slew Rate Adjustment									
For output SLOW option add	T_{SLOW}		1.7		1.6		1.4		ns
			Preliminary						

* Indicates Minimum Amount of Time to Assure Valid Data

XC4000XV D.C. and Switching Performance Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

All specifications subject to change without notice.

Additional Specifications

Except for pin-to-pin input and output parameters, the a.c. parameter delay specifications included in this document are derived from measuring internal test patterns.All specifications are representative of worst- case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Absolute Maximum Ratings

Symbol	Description		Value	Units
V_{CCINT}	Supply voltage relative to GND		-0.5 to 3.0	V
V_{CCIO}	Supply voltage relative to GND		-0.5 to 4.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to 5.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to 5.5	V
V_{CC}	Longest Supply Voltage Rise Time from 1 V to 3V		50	ms
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Notes: Maximum DC overshoot or undershoot above V_{cc} or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to + 7.0 V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CCINT}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	2.3	2.7	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	2.3	2.7	V
V_{CCIO}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	3.0	3.6	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	3.0	3.6	V
V_{IH}	High-level input voltage		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage		0	30% of V_{CC}	V
T_{IN}	Input signal transition time			250	ns

Notes 1: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
Input and output measurement threshold is ~50% of V_{CC}.

DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0 mA, V_{CC} min (LVTTL)		2.4		V
	High-level output voltage @ I_{OH} = -500 µA, (LVCMOS)		90% V_{CC}		V
V_{OL}	Low-level output voltage @ I_{OL} = 24.0 mA, V_{CC} min (LVTTL) (Note 1)			0.4	V
	Low-level output voltage @ I_{OL} = 1500 µA, (LVCMOS)			10% V_{CC}	V
V_{DRINT}	V_{CCINT} Data Retention Supply Voltage (below which configuration data may be lost)		2.1		V
V_{DRIO}	V_{CCIO} Data Retention Supply Voltage (below which configuration data may be lost)		2.5		V
I_{CCO}	Quiescent FPGA supply current (Note 2)			10	mA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, SBGA, PQ, HQ, & MQ packages		10	pF
		PGA packages		16	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)		0.02	0.15	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.3	2.0	mA

Note 1: With up to 64 pins simultaneously sinking 24 mA.
Note 2: With no output current loads, no active input or Longline pull-up resistors, all I/O pins Tri-stated and floating.

XC4000XV Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

		Speed Grade	All	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Max**	**Max**	
Delay from pad through Global Low Skew (GLS) clock buffer to any clock input, K.	T_{GLS}	XC40110XV		7.7	6.7	5.8	ns
		XC40150XV		7.8	6.8	5.9	ns
		XC40200XV		9.3	8.1	7.0	ns
		XC40250XV		9.4	8.2	7.1	ns
Delay from pad through Global Early (GE) clock buffer to any IOB clock input for BUFGE #s 1, 2, 5, and 6.	T_{GE_1256}	XC40110XV		5.6	4.9	4.2	ns
		XC40150XV		5.7	5.0	4.3	ns
		XC40200XV		6.1	5.3	4.6	ns
		XC40250XV		6.2	5.4	4.7	ns
Delay from pad through Global Early (GE) clock buffer to any IOB clock input for BUFGE #s 3, 4, 7, and 8.	T_{GE_3478}	XC40110XV		5.6	4.9	4.2	ns
		XC40150XV		5.7	5.0	4.3	ns
		XC40200XV		6.1	5.3	4.6	ns
		XC40250XV		6.2	5.4	4.7	ns
Delay from pad through FastCLK buffer to any IOB clock input	T_{FCLK}	XC40110XV		3.0	2.6	2.2	ns
		XC40150XV		3.1	2.7	2.3	ns
		XC40200XV		3.4	3.0	2.6	ns
		XC40250XV		3.5	3.1	2.7	ns
			Advance				

XC4000XV CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values are expressed in nanoseconds unless otherwise noted.

	Speed Grade	-09		-08		-07		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Combinatorial Delays								
F/G inputs to X/Y outputs	T_{ILO}		1.2		1.1		0.9	ns
F/G inputs via H' to X/Y outputs	T_{IHO}		2.3		2.0		1.7	ns
F/G inputs via transparent latch to Q outputs	T_{ITO}		1.9		1.7		1.5	ns
C inputs via SR/H0 via H to X/Y outputs	T_{HH0O}		1.5		1.3		1.1	ns
C inputs via H1 via H to X/Y outputs	T_{HH1O}		1.3		1.1		1.0	ns
C inputs via DIN/H2 via H to X/Y outputs	T_{HH2O}		1.5		1.3		1.1	ns
C inputs via EC, DIN/H2 to YQ, XQ output (bypass0	T_{CBYP}		0.8		0.7		0.6	ns
CLB Fast Carry Logic								
Operand inputs (F1, F2, G1, G4) to C_{OUT}	T_{OPCY}		2.5		2.2		1.9	ns
Add/Subtract input (F3) to C_{OUT}	T_{ASCY}		3.1		2.7		2.4	ns
Initialization inputs (F1, F3) to C_{OUT}	T_{INCY}		1.9		1.6		1.4	ns
C_{IN} through function generators to X/Y outputs	T_{SUM}		2.5		2.2		1.9	ns
C_{IN} to C_{OUT}, bypass function generators	T_{BYP}		0.3		0.3		0.2	ns
Carry Net Delay, C_{OUT} to C_{IN}	T_{NET}		0.4		0.3		0.3	ns
Sequential Delays								
Clock K to Flip-Flop outputs Q	T_{CKO}		1.6		1.4		1.2	ns
Clock K to Latch outputs Q	T_{CKLO}		1.6		1.4		1.2	ns
Setup Time before Clock K								
F/G inputs	T_{ICK}	1.5		1.3		1.2		ns
F/G inputs via H	T_{IHCK}	2.6		2.2		1.9		ns
C inputs via H0 through H	T_{HH0CK}	1.8		1.5		1.3		ns
C inputs via H1 through H	T_{HH1CK}	1.6		1.4		1.2		ns
C inputs via H2 through H	T_{HH2CK}	1.8		1.5		1.3		ns
C inputs via DIN	T_{DICK}	0.7		0.6		0.6		ns
C inputs via EC	T_{ECCK}	0.8		0.7		0.6		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	0.4		0.4		0.3		ns
CIN input via F/G	T_{CCK}	2.8		2.4		2.1		ns
CIN input via F/G and H	T_{CHC}	3.8		3.3		2.9		ns
Hold Time after Clock K								
All Hold Times		0.0		0.0		0.0		ns
Clocks								
Clock High time	T_{CH}	2.7		2.3		2.0		ns
Clock Low time	T_{CL}	2.7		2.3		2.0		ns
Set/Reset Direct								
Width (High)	T_{RPW}	3.0		2.8		2.5		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		2.9		2.5		2.2	ns
Global Set/Reset								
Minimum GSR Pulse Width	T_{MRW}		18.4		16.0		13.9	ns
Delay from GSR input to any Q	T_{MRQ}	See page 201 for TRRI values per device						
Toggle Frequency (MHz) (for export control purposes)	F_{TOG}		188		217		250	MHz
		Advance						

XC4000XV RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XV devices and are expressed in nanoseconds unless otherwise noted.

Single Port RAM	Speed Grade		-09		-08		-07		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	
Write Operation									
Address write cycle time (clock K period)	16x2	T_{WCS}	9.6		8.4		7.3		ns
	32x1	T_{WCTS}	9.6		8.4		7.3		ns
Clock K pulse width (active edge)	16x2	T_{WPS}	4.8		4.2		3.7		ns
	32x1	T_{WPTS}	4.8		4.2		3.7		ns
Address setup time before clock K	16x2	T_{ASS}	2.6		2.3		2.0		ns
	32x1	T_{ASTS}	2.0		1.8		1.5		ns
Address hold time after clock K	16x2	T_{AHS}	0.0		0.0		0.0		ns
	32x1	T_{AHTS}	0.0		0.0		0.0		ns
DIN setup time before clock K	16x2	T_{DSS}	2.0		1.8		1.5		ns
	32x1	T_{DSTS}	2.5		2.2		1.9		ns
DIN hold time after clock K	16x2	T_{DHS}	0.0		0.0		0.0		ns
	32x1	T_{DHTS}	0.0		0.0		0.0		ns
WE setup time before clock K	16x2	T_{WSS}	1.9		1.6		1.4		ns
	32x1	T_{WSTS}	1.8		1.5		1.3		ns
WE hold time after clock K	16x2	T_{WHS}	0.0		0.0		0.0		ns
	32x1	T_{WHTS}	0.0		0.0		0.0		ns
Data valid after clock K	16x2	T_{WOS}		6.2		5.4		4.7	ns
	32x1	T_{WOTS}		7.5		6.5		5.7	ns
Read Operation									
Address read cycle time	16x2	T_{RC}	4.5		3.1		3.1		ns
	32x1	T_{RCT}	6.5		5.5		5.5		ns
Data Valid after address change (no Write Enable)	16x2	T_{ILO}		1.2		1.1		0.9	ns
	32x1	T_{IHO}		2.3		2.0		1.7	ns
Address setup time before clock K	16x2	T_{ICK}	1.5		1.3		1.2		ns
	32x1	T_{IHCK}	2.6		2.2		1.9		ns
			Advance						

6

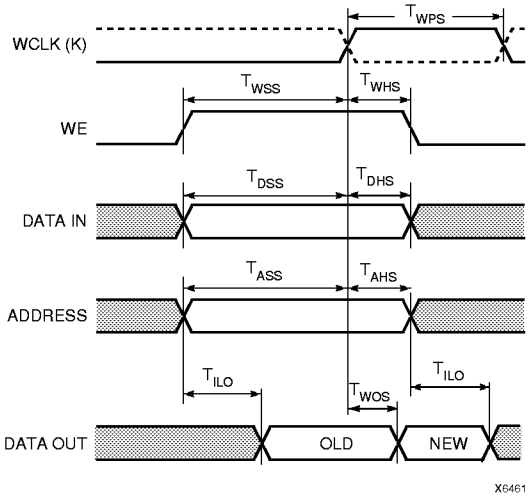
XC4000XV CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

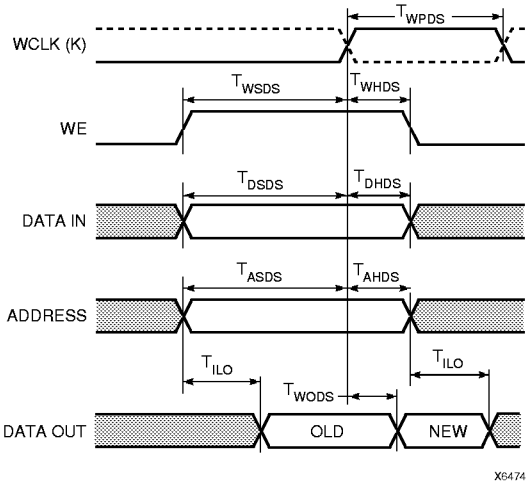
Dual Port RAM	Speed Grade		-09		-08		-07		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	
Address write cycle time (clock K period)	16x1	T_{WCDS}	9.6		8.4		7.3		ns
Clock K pulse width (active edge)	16x1	T_{WPDS}	4.8		4.2		3.7		ns
Address setup time before clock K	16x1	T_{ASDS}	2.6		2.3		2.0		ns
Address hold time after clock K	16x1	T_{AHDS}	0.0		0.0		0.0		ns
DIN setup time before clock K	16x1	T_{DSDS}	2.4		2.1		1.8		ns
DIN hold time after clock K	16x1	T_{DHDS}	0.0		0.0		0.0		ns
WE setup time before clock K	16x1	T_{WSDS}	1.9		1.6		1.4		ns
WE hold time after clock K	16x1	T_{WHDS}	0.0		0.0		0.0		ns
Data valid after clock K	16x1	T_{WODS}		7.3		6.4		5.6	ns
			Advance						

Note: Timing for 16x1 option is identical to 16x2 RAM.

XC4000XV CLB RAM Synchronous (Edge-Triggered) Write Timing



Single Port RAM



Dual Port RAM

XC4000XV Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

XC4000XV Global Clock Input to Output Delay

		Speed Grade	All	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Max**	**Max**	
Global Low Skew (GLS) Clock Input to Output Delay using Output Flip-Flop.	T_{ICKOF}	XC40110XV		10.6	9.2	8.0	ns
		XC40150XV		10.7	9.3	8.1	ns
		XC40200XV		12.2	10.6	9.2	ns
		XC40250XV		12.3	10.7	9.3	ns
For output SLOW option add	T_{SLOW}	All Devices		1.7	1.6	1.4	ns
			Advance				

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with fewer number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs in FAST mode specification.
Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 8.

XC4000XV FastCLK Input to Output Delay for BUFNW, BUFSW, BUFNE, and BUFSE

		Speed Grade	All	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Max**	**Max**	
FastCLK Input to Output Delay using Output Flip-Flop for FastCLK buffers BUFNW, BUFSW, BUFNE, and BUFSE.	T_{ICKFOF}	XC40110XV		5.9	5.1	4.4	ns
		XC40150XV		6.0	5.2	4.5	ns
		XC40200XV		6.3	5.5	4.8	ns
		XC40250XV		6.4	5.6	4.9	ns
			Advance				

OFF = Output Flip Flop
Notes: Listed above are representative values where one FastCLK input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the FastCLK net.
Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with fewer number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs in FAST slew mode specification.
Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 8.

XC4000XV Pin-to-Pin Output Parameter Guidelines

XC4000XV Global Early Clock Input to Output Delay for BUFGE #s 1, 2, 5, and 6

Description	Symbol	Speed Grade / Device	All Min	-09 Max	-08 Max	-07 Max	Units
Global Clock Signal Input to Output Delay using Global Early (GE) clock buffer to clock Output Flip-Flop for BUFGE #s 1, 2, 5, and 6.	T_{ICKEOF_1256}	XC40110XV		8.5	7.4	6.4	ns
		XC40150XV		8.6	7.5	6.5	ns
		XC40200XV		9.0	7.8	6.8	ns
		XC40250XV		9.1	7.9	6.9	ns
			Advance				

OFF = Output Flip Flop

Notes: Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with fewer number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs in FAST mode specification.

Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 8.

XC4000XV Global Early Clock Input to Output Delay for BUFGE #s 3, 4, 7, and 8

Description	Symbol	Speed Grade / Device	All Min	-09 Max	-08 Max	-07 Max	Units
Global Clock Signal Input to Output Delay using Global Early (GE) clock buffer to clock Output Flip-Flop for BUFGE #s 3, 4, 7, and 8.	T_{ICKEOF_3478}	XC40110XV		8.5	7.4	6.4	ns
		XC40150XV		8.6	7.5	6.5	ns
		XC40200XV		9.0	7.8	6.8	ns
		XC40250XV		9.1	7.9	6.9	ns
			Advance				

OFF = Output Flip Flop

Notes: Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with fewer number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs in FAST mode specification.

Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 8.

Capacitive Load Factor

Figure 8 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay.

Figure 8 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

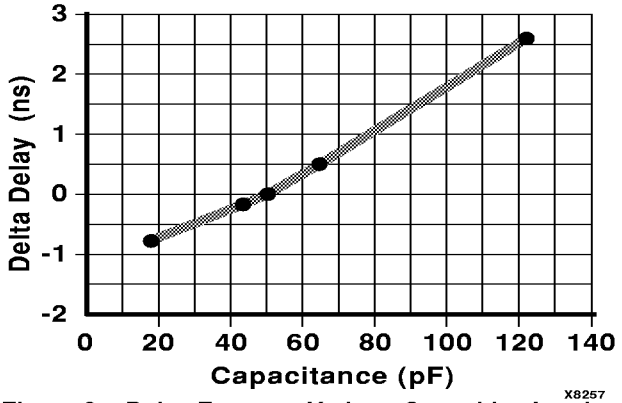


Figure 8: Delay Factor at Various Capacitive Loads

XC4000XV Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

XC4000XV Global Low Skew Clock, Set-Up and Hold

		Speed Grade	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Input Setup and Hold Time Relative to Global Clock Input Signal						
No Delay		XC40110XV	0.0 / 6.8	0.0 / 5.9	0.0 / 5.1	ns
Global Low Skew Clock and IFF	T_{PSN}/T_{PHN}	XC40150XV	0.0 / 6.9	0.0 / 6.0	0.0 / 5.2	ns
Global Low Skew Clock and FCL		XC40200XV	0.0 / 7.9	0.0 / 6.9	0.0 / 6.0	ns
		XC40250XV	0.0 / 8.7	0.0 / 7.6	0.0 / 6.6	ns
Partial Delay		XC40110XV	5.7 / 1.0	5.0 / 0.9	4.3 / 0.8	ns
Global Low Skew Clock and IFF	T_{PSP}/T_{PHP}	XC40150XV	5.8 / 1.0	5.1 / 0.9	4.4 / 0.8	ns
Global Low Skew Clock and FCL		XC40200XV	6.2 / 1.0	5.4 / 0.9	4.7 / 0.8	ns
		XC40250XV	6.6 / 1.0	5.8 / 0.9	5.0 / 0.8	ns
Full Delay		XC40110XV	6.5 / 0.0	5.7 / 0.0	4.9 / 0.0	ns
Global Low Skew Clock and IFF	T_{PSD}/T_{PHD}	XC40150XV	6.6 / 0.0	5.8 / 0.0	5.0 / 0.0	ns
		XC40200XV	7.3 / 0.0	6.3 / 0.0	5.5 / 0.0	ns
		XC40250XV	7.9 / 0.0	6.9 / 0.0	6.0 / 0.0	ns
				Advance		

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Notes: Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer (TRCE) to determine the setup and hold times under given design conditions.

XC4000XV FastCLK Input Set-Up and Hold for BUFNW, BUFSW, BUFNE, & BUFSE

		Speed Grade	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Input Setup and Hold Time Relative to FastCLK Input Signal						
No Delay		XC40110XV	3.3 / 2.6	2.9 / 2.2	2.5 / 1.9	ns
FastCLK and IFF	T_{PSFN}/T_{PHFN}	XC40150XV	3.3 / 2.7	2.9 / 2.3	2.5 / 2.0	ns
		XC40200XV	3.3 / 2.9	2.9 / 2.5	2.5 / 2.2	ns
		XC40250XV	3.3 / 3.2	2.9 / 2.8	2.5 / 2.4	ns
				Advance		

IFF = Input Flip-Flop or Latch

Notes: Setup time is measured relative to the FastCLK input signal with the fastest route and the lightest load. Hold time is measured relative to the FastCLK input signal using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer(TRCE) to determine the setup and hold times under given design conditions.

XC4000XV BUFGE #s 1, 2, 5, & 6 Global Early Clock, Set-Up and Hold for IFF and FCL

		Speed Grade	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Input Setup and Hold Time Relative to Global Clock Input Signal						
No Delay		XC40110XV	0.7 / 5.2	0.6 / 4.5	0.5 / 3.9	ns
Global Early Clock and IFF	T_{PSEN}/T_{PHEN}	XC40150XV	0.7 / 5.3	0.6 / 4.6	0.5 / 4.0	ns
Global Early Clock and FCL	T_{PFSEN}/T_{PFHEN}	XC40200XV	0.7 / 5.6	0.6 / 4.8	0.5 / 4.2	ns
		XC40250XV	0.7 / 5.8	0.6 / 5.1	0.5 / 4.4	ns
Partial Delay		XC40110XV	8.9 / 0.0	7.7 / 0.0	6.7 / 0.0	ns
Global Early Clock andIFF	T_{PSEP}/T_{PHEP}	XC40150XV	9.0 / 0.0	7.8 / 0.0	6.8 / 0.0	ns
Global Early Clock and FCL	T_{PFSEP}/T_{PFHEP}	XC40200XV	9.7 / 0.0	8.4 / 0.0	7.3 / 0.0	ns
		XC40250XV	10.3 / 0.0	9.0 / 0.0	7.8 / 0.0	ns
FullDelay		XC40110XV	9.4 / 0.0	8.2 / 0.0	7.1 / 0.0	ns
Global Early Clock and IFF	T_{PSED}/T_{PHED}	XC40150XV	9.5 / 0.0	8.3 / 0.0	7.2 / 0.0	ns
		XC40200XV	10.7 / 0.0	9.3 / 0.0	8.1 / 0.0	ns
		XC40250XV	11.9 / 0.0	10.4 / 0.0	9.0 / 0.0	ns
				Advance		

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Notes: Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer(TRCE) to determine the setup and hold times under given design conditions.

XC4000XV BUFGE #s 3, 4, 7, & 8 Global Early Clock, Set-Up and Hold for IFF and FCL

		Speed Grade	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Input Setup and Hold Time Relative to Global Clock Input Signal						
No Delay		XC40110XV	0.7 / 5.2	0.6 / 4.5	0.5 / 3.9	ns
Global Early Clock and IFF	T_{PSEN}/T_{PHEN}	XC40150XV	0.7 / 5.3	0.6 / 4.6	0.5 / 4.0	ns
Global Early Clock and FCL	T_{PFSEN}/T_{PFHEN}	XC40200XV	0.7 / 5.6	0.6 / 4.8	0.5 / 4.2	ns
		XC40250XV	0.7 / 5.8	0.6 / 5.1	0.5 / 4.4	ns
Partial Delay		XC40110XV	8.9 / 0.0	7.7 / 0.0	6.7 / 0.0	ns
Global Early Clock and IFF	T_{PSEP}/T_{PHEP}	XC40150XV	9.0 / 0.0	7.8 / 0.0	6.8 / 0.0	ns
Global Early Clock and FCL	T_{PFSEP}/T_{PFHEP}	XC40200XV	9.7 / 0.0	8.4 / 0.0	7.3 / 0.0	ns
		XC40250XV	10.3 / 0.0	9.0 / 0.0	7.8 / 0.0	ns
FullDelay		XC40110XV	9.4 / 0.0	8.2 / 0.0	7.1 / 0.0	ns
Global Early Clock and IFF	T_{PSED}/T_{PHED}	XC40150XV	9.5 / 0.0	8.3 / 0.0	7.2 / 0.0	ns
		XC40200XV	10.7 / 0.0	9.3 / 0.0	8.1 / 0.0	ns
		XC40250XV	11.9 / 0.0	10.4 / 0.0	9.0 / 0.0	ns
				Advance		

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Notes: Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer(TRCE) to determine the setup and hold times under given design conditions.

XC4000XV IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

		Speed Grade	-09		-08		-07		Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Clocks									
Clock Enable (EC) to Clock (IK)	T_{ECIK}	All Devices	0.0		0.0		0.0		ns
Delay from Fast Capture Latch enable (OK) active edge to IFF clock (IK) active edge	T_{OKIK}	All Devices	2.0		1.8		1.5		ns
Setup Times									
Pad to Clock (IK), no delay	T_{PICK}	All Devices	0.7		0.6		0.5		ns
Pad to Clock (IK), via transparent Fast Capture Latch, no delay	T_{PICKF}	Al Devices	1.2		1.1		0.9		ns
Pad to Fast Capture Latch Enable (OK), no delay	T_{POCK}	All Devices	0.2		0.2		0.1		ns
Hold Times									
All Hold Times		All Devices	0.0		0.0		0.0		ns
Global Set/Reset									
Minimum GSR Pulse Width	T_{MRW}	All Devices	18.4		16.0		13.9		ns
Delay from GSR input to any Q	T_{RRI*}	XC40110XV	35.0		30.5		26.5		ns
		XC40150XV	38.5		33.5		29.1		ns
		XC40200XV	42.4		36.9		32.1		ns
		XC40250XV	46.6		40.5		35.3		ns
Propagation Delays									
Pad to I1, I2	T_{PID}	All devices		0.1		0.1		0.1	ns
Pad to I1, I2 via transparent input latch, no delay	T_{PLI}	All devices		1.5		1.3		1.1	ns
Pad to I1, I2 via transparent FCL and input latch, no delay	T_{PFLI}	All Devices		2.0		1.8		1.6	ns
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}	All Devices		1.1		0.9		0.8	ns
Clock (IK) to I1, I2 (latch enable, active Low)	T_{IKLI}	All Devices		1.2		1.1		0.9	ns
FCL Enable (OK) active edge to I1, I2 (via transparent standard input latch)	T_{OKLI}	All Devices		2.8		2.5		2.1	ns
			Advance						

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch.
* Indicates Minimum Amount of Time to Assure Valid Data.

XC4000XV IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

		Speed Grade	-09		-08		-07		Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Clocks									
Clock High	T_{CH}		2.7		2.3		2.0		ns
Clock Low	T_{CL}		2.7		2.3		2.0		ns
Propagation Delays (See Note 1)									
Clock (OK) to Pad	T_{OKPOF}			3.0		2.6		2.3	ns
Output (O) to Pad	T_{OPF}			1.6		1.4		1.2	ns
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZ}			3.7		3.2		2.8	ns
3-state to Pad active and valid	T_{TSONF}			4.1		3.6		3.1	ns
Output (O) to Pad via Fast Output MUX	T_{OFPF}			2.9		2.5		2.2	ns
Select (OK) to Pad via Fast MUX	T_{OKFPF}			2.5		2.2		1.9	ns
Setup and Hold Times									
Output (O) to clock (OK) setup time	T_{OOK}		0.4		0.4		0.3		ns
Output (O) to clock (OK) hold time	T_{OKO}		0.0		0.0		0.0		ns
Clock Enable (EC) to clock (OK) setup time	T_{ECOK}		0.0		0.0		0.0		ns
Clock Enable (EC) to clock (OK) hold time	T_{OKEC}		0.3		0.2		0.1		ns
Global Set/Reset									
Minimum GSR pulse width	T_{MRW}		18.4		16.0		13.9		ns
Delay from GSR input to any Pad	T_{RPO}*	XC40110XV		37.1		32.2		28.0	ns
		XC40150XV		40.5		35.3		30.7	ns
		XC40200XV		44.4		38.6		33.6	ns
		XC40250XV		48.6		42.3		36.8	ns
Slew Rate Adjustment									
For output SLOW option add	T_{SLOW}			1.7		1.6		1.4	ns
			Advance						

Note: Output timing is measured at ~50% V_{CC} threshold, with 50 pF external capacitive loads.
* Indicates Minimum Amount of Time to Assure Valid Data.

XC4013XLA Pinout Table

XC4013XLA Pinout Table

PAD NAME	PQ160	PQ208	PQ240	BG256
VCC	P142	P183	P212	VCC*
I/O (A8)	P143	P184	P213	C10
I/O (A9)	P144	P185	P214	D10
I/O (A19)	P145	P186	P215	A9
I/O (A18)	P146	P187	P216	B9
I/O	–	P188	P217	C9
I/O	–	P189	P218	D9
GND	–	–	P219	GND*
I/O (A10)	P147	P190	P220	A8
I/O (A11)	P148	P191	P221	B8
VCC	–	–	P222	VCC*
I/O	–	–	P223	A6
I/O	–	–	P224	C7
I/O	P149	P192	P225	B6
I/O	P150	P193	P226	A5
GND	P151	P194	P227	GND*
I/O	–	P195	P228	C6
I/O	–	P196	P229	B5
I/O	P152	P197	P230	A4
I/O	P153	P198	P231	C5
I/O (A12)	P154	P199	P232	B4
I/O (A13)	P155	P200	P233	A3
GND	–	–	–	GND*
VCC	–	–	–	VCC*
I/O	–	–	P234	D5
I/O	–	–	P235	C4
I/O	P156	P201	P236	B3
I/O	P157	P202	P237	B2
I/O (A14)	P158	P203	P238	A2
I/O, GCK8 (A15)	P159	P204	P239	C3
VCC	P160	P205	P240	VCC*
GND	P1	P2	P1	GND*
I/O, GCK1 (A16)	P2	P4	P2	B1
I/O (A17)	P3	P5	P3	C2
I/O	P4	P6	P4	D2
I/O	P5	P7	P5	D3
I/O (TDI)	P6	P8	P6	E4
I/O (TCK)	P7	P9	P7	C1
VCC	–	–	–	VCC*
GND	–	–	–	GND*
I/O	P8	P10	P8	D1
I/O	P9	P11	P9	E3
I/O	–	P12	P10	E2
I/O	–	P13	P11	E1
I/O	–	–	P12	F3

XC4013XLA Pinout Table (Continued)

PAD NAME	PQ160	PQ208	PQ240	BG256
I/O	–	–	P13	F2
GND	P10	P14	P14	GND*
I/O, FCLK1	P11	P15	P15	G3
I/O	P12	P16	P16	G2
I/O (TMS)	P13	P17	P17	G1
I/O	P14	P18	P18	H3
VCC	–	–	P19	VCC*
I/O	–	–	P20	H2
I/O	–	–	P21	H1
GND	–	–	P22	GND*
I/O	–	P19	P23	J2
I/O	–	P20	P24	J1
I/O	P15	P21	P25	K2
I/O	P16	P22	P26	K3
I/O	P17	P23	P27	K1
I/O	P18	P24	P28	L1
GND	P19	P25	P29	GND*
VCC	P20	P26	P30	VCC*
I/O	P21	P27	P31	L2
I/O	P22	P28	P32	L3
I/O	P23	P29	P33	L4
I/O	P24	P30	P34	M1
I/O	–	P31	P35	M2
I/O	–	P32	P36	M3
GND	–	–	P37	GND*
I/O	–	–	P38	N1
I/O	–	–	P39	N2
VCC	–	–	P40	VCC*
I/O	P25	P33	P41	P1
I/O	P26	P34	P42	P2
I/O	P27	P35	P43	R1
I/O, FCLK2	P28	P36	P44	P3
GND	P29	P37	P45	GND*
I/O	–	–	P46	T1
I/O	–	–	P47	R3
I/O	–	P38	P48	T2
I/O		P39	P49	U1
I/O	P30	P40	P50	T3
I/O	P31	P41	P51	U2
GND	–	–	–	GND*
VCC	–	–	–	VCC*
I/O	P32	P42	P52	V1
I/O	P33	P43	P53	T4
I/O	P34	P44	P54	U3
I/O	P35	P45	P55	V2
I/O	P36	P46	P56	W1

XC4013XLA Pinout Table (Continued)

PAD NAME	PQ160	PQ208	PQ240	BG256
I/O, GCK2	P37	P47	P57	V3
O (M1)	P38	P48	P58	W2
GND	P39	P49	P59	GND*
I (M0)	P40	P50	P60	Y1
VCC	P41	P55	P61	VCC*
I (M2)	P42	P56	P62	W3
I/O, GCK3	P43	P57	P63	Y2
I/O (HDC)	P44	P58	P64	W4
I/O	P45	P59	P65	V4
I/O	P46	P60	P66	U5
I/O	P47	P61	P67	Y3
I/O (/LDC)	P48	P62	P68	Y4
VCC	–	–	–	VCC*
GND	–	–	–	GND*
I/O	P49	P63	P69	V5
I/O	P50	P64	P70	W5
I/O	–	P65	P71	Y5
I/O	–	P66	P72	V6
I/O	–	–	P73	W6
I/O	–	–	P74	Y6
GND	P51	P67	P75	GND*
I/O	P52	P68	P76	W7
I/O	P53	P69	P77	Y7
I/O	P54	P70	P78	V8
I/O	P55	P71	P79	W8
VCC	–	–	P80	VCC*
I/O	–	P72	P81	Y8
I/O	–	P73	P82	U9
GND	–	–	P83	GND*
I/O	–	–	P84	Y9
I/O	–	–	P85	W10
I/O	P56	P74	P86	V10
I/O	P57	P75	P87	Y10
I/O	P58	P76	P88	Y11
I/O (/INIT)	P59	P77	P89	W11
VCC	P60	P78	P90	VCC*
GND	P61	P79	P91	GND*
I/O	P62	P80	P92	V11
I/O	P63	P81	P93	U11
I/O	P64	P82	P94	Y12
I/O	P65	P83	P95	W12
I/O	–	P84	P96	V12
I/O	–	P85	P97	U12
GND	–	–	P98	GND*
I/O	–	–	P99	V13
I/O	–	–	P100	Y14

XC4013XLA Pinout Table (Continued)

PAD NAME	PQ160	PQ208	PQ240	BG256
VCC	–	–	P101	VCC*
I/O	P66	P86	P102	Y15
I/O	P67	P87	P103	V14
I/O	P68	P88	P104	W15
I/O	P69	P89	P105	Y16
GND	P70	P90	P106	GND*
I/O	–	–	P107	V15
I/O	–	–	P108	W16
I/O	–	P91	P109	Y17
I/O	–	P92	P110	V16
I/O	P71	P93	P111	W17
I/O	P72	P94	P112	Y18
GND	–	–	–	GND*
VCC	–	–	–	VCC*
I/O	P73	P95	P113	U16
I/O	P74	P96	P114	V17
I/O	P75	P97	P115	W18
I/O	P76	P98	P116	Y19
I/O	P77	P99	P117	V18
I/O, GCK4	P78	P100	P118	W19
GND	P79	P101	P119	GND*
DONE	P80	P103	P120	Y20
VCC	P81	P106	P121	VCC*
/PROGRAM	P82	P108	P122	V19
I/O (D7)	P83	P109	P123	U19
I/O, GCK5	P84	P110	P124	U18
I/O	P85	P111	P125	T17
I/O	P86	P112	P126	V20
I/O	–	–	P127	U20
I/O	–	–	P128	T18
VCC	–	–	–	VCC*
GND	–	–	–	GND*
I/O (D6)	P87	P113	P129	T19
I/O	P88	P114	P130	T20
I/O	P89	P115	P131	R18
I/O	P90	P116	P132	R19
I/O	–	P117	P133	R20
I/O	–	P118	P134	P18
GND	P91	P119	P135	GND*
I/O	–	–	P136	P20
I/O	–	–	P137	N18
I/O, FCLK3	P92	P120	P138	N19
I/O	P93	P121	P139	N20
VCC	–	–	P140	VCC*
I/O (D5)	P94	P122	P141	M17
I/O (/CS0)	P95	P123	P142	M18

XC4013XLA Pinout Table (Continued)

PAD NAME	PQ160	PQ208	PQ240	BG256
GND	–	–	P143	GND*
I/O	–	P124	P144	M20
I/O	–	P125	P145	L19
I/O	P96	P126	P146	L18
I/O	P97	P127	P147	L20
I/O (D4)	P98	P128	P148	K20
I/O	P99	P129	P149	K19
VCC	P100	P130	P150	VCC*
GND	P101	P131	P151	GND*
I/O (D3)	P102	P132	P152	K18
I/O (/RS)	P103	P133	P153	K17
I/O	P104	P134	P154	J20
I/O	P105	P135	P155	J19
I/O	–	P136	P156	J18
I/O	–	P137	P157	J17
GND	–	–	P158	GND*
I/O (D2)	P106	P138	P159	H19
I/O	P107	P139	P160	H18
VCC	–	–	P161	VCC*
I/O	P108	P140	P162	G19
I/O, FCLK4	P109	P141	P163	F20
I/O	–	–	P164	G18
I/O	—	–	P165	F19
GND	P110	P142	P166	GND*
I/O	–	–	P167	F18
I/O	–	–	P168	E19
I/O	–	P143	P169	D20
I/O	–	P144	P170	E18
I/O	P111	P145	P171	D19
I/O	P112	P146	P172	C20
GND	–	–	–	GND*
VCC	–	–	–	VCC*
I/O (D1)	P113	P147	P173	E17
I/O (/RCK, RDY_/BUSY)	P114	P148	P174	D18
I/O	P115	P149	P175	C19
I/O	P116	P150	P176	B20
I/O (D0, DIN)	P117	P151	P177	C18
I/O, GCK6 (DOUT)	P118	P152	P178	B19
CCLK	P119	P153	P179	A20
VCC	P120	P154	P180	VCC*
O, TDO	P121	P159	P181	A19
GND	P122	P160	P182	GND*
I/O (A0, /WS)	P123	P161	P183	B18
I/O, GCK7 (A1)	P124	P162	P184	B17
I/O	P125	P163	P185	C17
I/O	P126	P164	P186	D16

XC4013XLA Pinout Table (Continued)

PAD NAME	PQ160	PQ208	PQ240	BG256
I/O, (CS1, A2)	P127	P165	P187	A18
I/O (A3)	P128	P166	P188	A17
VCC	–	–	–	VCC*
GND	–	–	–	GND*
I/O	–	–	P189	C16
I/O	–	–	P190	B16
I/O	P129	P167	P191	A16
I/O	P130	P168	P192	C15
I/O	–	P169	P193	B15
I/O	–	P170	P194	A15
GND	P131	P171	P196	GND*
I/O	P132	P172	P197	B14
I/O	P133	P173	P198	A14
I/O	–	–	P199	C13
I/O	–	–	P200	B13
VCC	–	–	P201	VCC*
I/O (A4)	P134	P174	P202	C12
I/O (A5)	P135	P175	P203	B12
GND	–	–	P204	GND*
I/O	–	P176	P205	A12
I/O	P136	P177	P206	B11
I/O (A21)	P137	P178	P207	C11
I/O (A20)	P138	P179	P208	A11
I/O (A6)	P139	P180	P209	A10
I/O (A7)	P140	P181	P210	B10
GND	P141	P182	P211	GND*
VCC	–	–	–	D6
VCC	–	–	–	D11
VCC	–	–	–	D15
VCC	–	–	–	F4
VCC	–	–	–	F17
VCC	–	–	–	K4
VCC	–	–	–	L17
VCC	–	–	–	R4
VCC	–	–	–	R17
VCC	–	–	–	U6
VCC	–	–	–	U10
VCC	–	–	–	U15
VCC	–	–	–	C14
VCC	–	–	–	F1
VCC	–	–	–	R2
VCC	–	–	–	E20
VCC	–	–	–	P19
VCC	–	–	–	V7
VCC	–	–	–	D7

XC4013XLA Pinout Table (Continued)

PAD NAME	PQ160	PQ208	PQ240	BG256
VCC	–	–	–	D14
VCC	–	–	–	G17
VCC	–	–	–	P17
VCC	–	–	–	W20
VCC	–	–	–	U14
VCC	–	–	–	U7
VCC	–	–	–	P4
VCC	–	–	–	G4
GND	–	–	–	A1
GND	–	–	–	D4
GND	–	–	–	D8
GND	–	–	–	D13
GND	–	–	–	D17
GND	–	–	–	H4
GND	–	–	–	H17
GND	–	–	–	N4
GND	–	–	–	N17
GND	–	–	–	U4
GND	–	–	–	U8
GND	–	–	–	U13
GND	–	–	–	U17
GND	–	–	–	B7
GND	–	–	–	N3

XC4013XLA Pinout Table (Continued)

PAD NAME	PQ160	PQ208	PQ240	BG256
GND	–	–	–	W14
GND	–	–	–	G20
NC	–	P1	P195	A7
NC	–	P3	–	C8
NC	–	P51	–	D12
NC	–	P52	–	A13
NC	–	P53	–	H20
NC	–	P54	–	Y13
NC	–	P102	–	W13
NC	–	P104	–	M19
NC	–	P105	–	W9
NC	–	P107	–	V9
NC	–	P155	–	M4
NC	–	P156	–	J3
NC	–	P157	–	J4
NC	–	P158	–	–
NC	–	P206	–	–
NC	–	P207	–	–
NC	–	P208	–	–

12/18/98

XC4020XLA Pinout Table

XC4020XLA Pinout Table

PAD NAME	PQ160	PQ208	PQ240	BG256
VCC	P142	P183	P212	VCC*
I/O (A8)	P143	P184	P213	C10
I/O (A9)	P144	P185	P214	D10
I/O (A19)	P145	P186	P215	A9
I/O (A18)	P146	P187	P216	B9
I/O	–	P188	P217	C9
I/O	–	P189	P218	D9
GND	–	–	P219	GND*
I/O (A10)	P147	P190	P220	A8
I/O (A11)	P148	P191	P221	B8
I/O	–	–	–	C8
I/O	–	–	–	A7
VCC	–	–	P222	VCC*
I/O	–	–	P223	A6
I/O	–	–	P224	C7
I/O	P149	P192	P225	B6
I/O	P150	P193	P226	A5
GND	P151	P194	P227	GND*
I/O	–	P195	P228	C6
I/O	–	P196	P229	B5
I/O	P152	P197	P230	A4
I/O	P153	P198	P231	C5
I/O (A12)	P154	P199	P232	B4
I/O (A13)	P155	P200	P233	A3
GND	–	–	–	GND*
VCC	–	–	–	VCC*
I/O	–	–	P234	D5
I/O	–	–	P235	C4
I/O	P156	P201	P236	B3
I/O	P157	P202	P237	B2
I/O (A14)	P158	P203	P238	A2
I/O, GCK8 (A15)"	P159	P204	P239	C3
VCC	P160	P205	P240	VCC
GND	P1	P2	P1	GND*
I/O, GCK1 (A16)	P2	P4	P2	B1
I/O (A17)	P3	P5	P3	C2
I/O	P4	P6	P4	D2
I/O	P5	P7	P5	D3
I/O (TDI)	P6	P8	P6	E4
I/O (TCK)	P7	P9	P7	C1
VCC	–	–	–	VCC*
GND	–	–	–	GND*
I/O	P8	P10	P8	D1
I/O	P9	P11	P9	E3
I/O	–	P12	P10	E2
I/O	–	P13	P11	E1
I/O	–	–	P12	F3
I/O	–	–	P13	F2
GND	P10	P14	P14	GND*
I/O, FCLK1	P11	P15	P15	G3
I/O	P12	P16	P16	G2
I/O (TMS)	P13	P17	P17	G1
I/O	P14	P18	P18	H3
VCC	–	–	P19	VCC*
I/O	–	–	P20	H2

XC4020XLA Pinout Table (Continued)

PAD NAME	PQ160	PQ208	PQ240	BG256
I/O	–	–	P21	H1
GND	–	–	P22	GND*
I/O	–	–	–	J4
I/O	–	–	–	J3
I/O	–	P19	P23	J2
I/O	–	P20	P24	J1
I/O	P15	P21	P25	K2
I/O	P16	P22	P26	K3
I/O	P17	P23	P27	K1
I/O	P18	P24	P28	L1
GND	P19	P25	P29	GND*
VCC	P20	P26	P30	VCC*
I/O	P21	P27	P31	L2
I/O	P22	P28	P32	L3
I/O	P23	P29	P33	L4
I/O	P24	P30	P34	M1
I/O	–	P31	P35	M2
I/O	–	P32	P36	M3
I/O	–	–	–	M4
GND	–	–	P37	GND*
I/O	–	–	P38	N1
I/O	–	–	P39	N2
VCC	–	–	P40	VCC*
I/O	P25	P33	P41	P1
I/O	P26	P34	P42	P2
I/O	P27	P35	P43	R1
I/O, FCLK2	P28	P36	P44	P3
GND	P29	P37	P45	GND*
I/O	–	–	P46	T1
I/O	–	–	P47	R3
I/O	–	P38	P48	T2
I/O	–	P39	P49	U1
I/O	P30	P40	P50	T3
I/O	P31	P41	P51	U2
GND	–	–	–	GND*
VCC	–	–	–	VCC*
I/O	P32	P42	P52	V1
I/O	P33	P43	P53	T4
I/O	P34	P44	P54	U3
I/O	P35	P45	P55	V2
I/O	P36	P46	P56	W1
I/O, GCK2	P37	P47	P57	V3
O (M1)	P38	P48	P58	W2
GND	P39	P49	P59	GND*
I (M0)	P40	P50	P60	Y1
VCC	P41	P55	P61	VCC*
I (M2)	P42	P56	P62	W3
I/O, GCK3	P43	P57	P63	Y2
I/O (HDC)	P44	P58	P64	W4
I/O	P45	P59	P65	V4
I/O	P46	P60	P66	U5
I/O	P47	P61	P67	Y3
I/O (/LDC)	P48	P62	P68	Y4
VCC	–	–	–	VCC*
GND	–	–	–	GND*
I/O	P49	P63	P69	V5
I/O	P50	P64	P70	W5

XC4020XLA Pinout Table (Continued)

PAD NAME	PQ160	PQ208	PQ240	BG256
I/O	–	P65	P71	Y5
I/O	–	P66	P72	V6
I/O	–	–	P73	W6
I/O	–	–	P74	Y6
GND	P51	P67	P75	GND*
I/O	P52	P68	P76	W7
I/O	P53	P69	P77	Y7
I/O	P54	P70	P78	V8
I/O	P55	P71	P79	W8
VCC	–		P80	VCC*
I/O	–	P72	P81	Y8
I/O	–	P73	P82	U9
GND	–	–	P83	GND*
I/O	–	–	–	V9
I/O	–	–	–	W9
I/O	–	–	P84	Y9
I/O	–	–	P85	W10
I/O	P56	P74	P86	V10
I/O	P57	P75	P87	Y10
I/O	P58	P76	P88	Y11
I/O (/INIT)	P59	P77	P89	W11
VCC	P60	P78	P90	VCC*
GND	P61	P79	P91	GND*
I/O	P62	P80	P92	V11
I/O	P63	P81	P93	U11
I/O	P64	P82	P94	Y12
I/O	P65	P83	P95	W12
I/O	–	P84	P96	V12
I/O	–	P85	P97	U12
I/O	–	–	–	Y13
I/O	–	–	–	W13
GND	–	–	P98	GND*
I/O	–	–	P99	V13
I/O	–	–	P100	Y14
VCC	–	–	P101	VCC*
I/O	P66	P86	P102	Y15
I/O	P67	P87	P103	V14
I/O	P68	P88	P104	W15
I/O	P69	P89	P105	Y16
GND	P70	P90	P106	GND*
I/O	–	–	P107	V15
I/O	–	–	P108	W16
I/O	–	P91	P109	Y17
I/O	–	P92	P110	V16
I/O	P71	P93	P111	W17
I/O	P72	P94	P112	Y18
GND	–	–	–	GND*
VCC	–	–	–	VCC*
I/O	P73	P95	P113	U16
I/O	P74	P96	P114	V17
I/O	P75	P97	P115	W18
I/O	P76	P98	P116	Y19
I/O	P77	P99	P117	V18
I/O, GCK4	P78	P100	P118	W19
GND	P79	P101	P119	GND*
DONE	P80	P103	P120	Y20
VCC	P81	P106	P121	VCC*

XC4020XLA Pinout Table (Continued)

PAD NAME	PQ160	PQ208	PQ240	BG256
/PROGRAM	P82	P108	P122	V19
I/O (D7)	P83	P109	P123	U19
I/O, GCK5	P84	P110	P124	U18
I/O	P85	P111	P125	T17
I/O	P86	P112	P126	V20
I/O	–	–	P127	U20
I/O	–	–	P128	T18
VCC	–	–	–	VCC*
GND	–	–	–	GND*
I/O (D6)	P87	P113	P129	T19
I/O	P88	P114	P130	T20
I/O	P89	P115	P131	R18
I/O	P90	P116	P132	R19
I/O	–	P117	P133	R20
I/O	–	P118	P134	P18
GND	P91	P119	P135	GND*
I/O	–	–	P136	P20
I/O	–	–	P137	N18
I/O, FCLK3	P92	P120	P138	N19
I/O	P93	P121	P139	N20
VCC	–	–	P140	VCC*
I/O (D5)	P94	P122	P141	M17
I/O (/CS0)	P95	P123	P142	M18
GND	–	–	P143	GND*
I/O	–	–	–	M19
I/O	–	P124	P144	M20
I/O	–	P125	P145	L19
I/O	P96	P126	P146	L18
I/O	P97	P127	P147	L20
I/O (D4)	P98	P128	P148	K20
I/O	P99	P129	P149	K19
VCC	P100	P130	P150	VCC*
GND	P101	P131	P151	GND*
I/O (D3)	P102	P132	P152	K18
I/O (/RS)	P103	P133	P153	K17
I/O	P104	P134	P154	J20
I/O	P105	P135	P155	J19
I/O	–	P136	P156	J18
I/O	–	P137	P157	J17
I/O	–	–	–	H20
GND	–	–	P158	GND*
I/O (D2)	P106	P138	P159	H19
I/O	P107	P139	P160	H18
VCC	–	–	P161	VCC*
I/O	P108	P140	P162	G19
I/O, FCLK4	P109	P141	P163	F20
I/O	–	–	P164	G18
I/O	–	–	P165	F19
GND	P110	P142	P166	GND*
I/O	–	–	P167	F18
I/O	–	–	P168	E19
I/O	–	P143	P169	D20
I/O	–	P144	P170	E18
I/O	P111	P145	P171	D19
I/O	P112	P146	P172	C20
GND	–	–	–	GND*
VCC	–	–	–	VCC*

XC4020XLA Pinout Table (Continued)

PAD NAME	PQ160	PQ208	PQ240	BG256
I/O (D1)	P113	P147	P173	E17
I/O (/RCK, RDY_/BUSY)	P114	P148	P174	D18
I/O	P115	P149	P175	C19
I/O	P116	P150	P176	B20
I/O (D0, DIN)	P117	P151	P177	C18
I/O, GCK6 (DOUT)	P118	P152	P178	B19
CCLK	P119	P153	P179	A20
VCC	P120	P154	P180	VCC*
O, TDO	P121	P159	P181	A19
GND	P122	P160	P182	GND*
I/O (A0, /WS)	P123	P161	P183	B18
I/O, GCK7 (A1)"	P124	P162	P184	B17
I/O	P125	P163	P185	C17
I/O	P126	P164	P186	D16
I/O, (CS1, A2)	P127	P165	P187	A18
I/O (A3)	P128	P166	P188	A17
VCC	–	–	–	VCC*
GND	–	–	–	GND*
I/O	–	–	P189	C16
I/O	–	–	P190	B16
I/O	P129	P167	P191	A16
I/O	P130	P168	P192	C15
I/O	–	P169	P193	B15
I/O	–	P170	P194	A15
GND	P131	P171	P196	GND*
I/O	P132	P172	P197	B14
I/O	P133	P173	P198	A14
I/O	–	–	P199	C13
I/O	–	–	P200	B13
VCC	–	–	P201	VCC*
I/O	–	–	–	A13
I/O	–	–	–	D12
I/O (A4)	P134	P174	P202	C12
I/O (A5)	P135	P175	P203	B12
GND	–	–	P204	GND*
I/O	–	P176	P205	A12
I/O	P136	P177	P206	B11
I/O (A21)	P137	P178	P207	C11
I/O (A20)	P138	P179	P208	A11
I/O (A6)	P139	P180	P209	A10
I/O (A7)	P140	P181	P210	B10
GND	P141	P182	P211	GND*
VCC	–	–	–	D6
VCC	–	–	–	D11
VCC	–	–	–	D15
VCC	–	–	–	F4
VCC	–	–	–	F17
VCC	–	–	–	K4
VCC	–	–	–	L17
VCC	–	–	–	R4
VCC	–	–	–	R17
VCC	–	–	–	U6
VCC	–	–	–	U10
VCC	–	–	–	U15
VCC	–	–	–	C14
VCC	–	–	–	F1

XC4020XLA Pinout Table (Continued)

PAD NAME	PQ160	PQ208	PQ240	BG256
VCC	–	–	–	R2
VCC	–	–	–	E20
VCC	–	–	–	P19
VCC	–	–	–	V7
VCC	–	–	–	D7-CORE
VCC	–	–	–	D14-CORE
VCC	–	–	–	G17
VCC	–	–	–	P17
VCC	–	–	–	W20
VCC	–	–	–	U14-CORE
VCC	–	–	–	U7-CORE
VCC	–	–	–	P4
VCC	–	–	–	G4-CORE
GND	–	–	–	A1
GND	–	–	–	D4
GND	–	–	–	D8
GND	–	–	–	D13
GND	–	–	–	D17
GND	–	–	–	H4
GND	–	–	–	H17
GND	–	–	–	N4
GND	–	–	–	N17
GND	–	–	–	U4
GND	–	–	–	U8
GND	–	–	–	U13
GND	–	–	–	U17
GND	–	–	–	B7
GND	–	–	–	N3
GND	–	–	–	W14
GND	–	–	–	G20
NC	–	P1	P195	–
NC	–	P3	–	–
NC	–	P51	–	–
NC	–	P52	–	–
NC	–	P53	–	–
NC	–	P54	–	–
NC	–	P102	–	–
NC	–	P104	–	–
NC	–	P105	–	–
NC	–	P107	–	–
NC	–	P155	–	–
NC	–	P156	–	–
NC	–	P157	–	–
NC	–	P158	–	–
NC	–	P206	–	–
NC	–	P207	–	–
NC	–	P208	–	–

12/18/98

6

XC4028XLA Pinout Table

XC4028XLA Pinout Table

PAD NAME	HQ160	HQ208	HQ240	BG256	HQ304	BG352
VCC	P142	P183	P212	VCC*	P38	VCC*
I/O (A8)	P143	P184	P213	C10	P37	D14
I/O (A9)	P144	P185	P214	D10	P36	C14
I/O (A19)	P145	P186	P215	A9	P35	A15
I/O (A18)	P146	P187	P216	B9	P34	B15
I/O	–	P188	P217	C9	P33	C15
I/O	–	P189	P218	D9	P32	D15
I/O (A10)	P147	P190	P220	A8	P31	A16
I/O (A11)	P148	P191	P221	B8	P30	B16
GND	–	–	–	GND*	–	GND*
I/O	–	–	–	–	P29	C16
I/O	–	–	–	–	P28	B17
I/O	–	–	–	C8	P27	C17
I/O	–	–	–	A7	P26	B18
VCC	–	–	P222	VCC*	P25	VCC*
I/O	–	–	P223	A6	P23	C18
I/O	–	–	P224	C7	P22	D17
I/O	P149	P192	P225	B6	P21	A20
I/O	P150	P193	P226	A5	P20	B19
GND	P151	P194	P227	GND*	P19	GND*
I/O	–	–	–	–	P18	C19
I/O	–	–	–	–	P17	D18
I/O	–	P195	P228	C6	P16	A21
I/O	–	P196	P229	B5	P15	B20
I/O	P152	P197	P230	A4	P14	C20
I/O	P153	P198	P231	C5	P13	B21
I/O (A12)	P154	P199	P232	B4	P12	B22
I/O (A13)	P155	P200	P233	A3	P10	C21
GND	–	–	–	GND*	–	GND*
VCC	–	–	–	VCC*	–	VCC*
I/O	–	–	–	–	P9	D20
I/O	–	–	–	–	P8	A23
I/O	–	–	P234	D5	P7	D21
I/O	–	–	P235	C4	P6	C22
I/O	P156	P201	P236	B3	P5	B24
I/O	P157	P202	P237	B2	P4	C23
I/O (A14)	P158	P203	P238	A2	P3	D22
I/O, GCK8 (A15)	P159	P204	P239	C3	P2	C24
VCC	P160	P205	P240	VCC*	P1	VCC*
GND	P1	P2	P1	GND*	P304	GND*
I/O, GCK1 (A16)	P2	P4	P2	B1	P303	D23
I/O (A17)	P3	P5	P3	C2	P302	C25
I/O	P4	P6	P4	D2	P301	D24
I/O	P5	P7	P5	D3	P300	E23
I/O (TDI)	P6	P8	P6	E4	P299	C26
I/O (TCK)	P7	P9	P7	C1	P298	E24
I/O	–	–	–	–	P297	F24
I/O	–	–	–	–	P296	E25
VCC	–	–	–	VCC*	–	VCC*
GND	–	–	–	GND*	–	GND*
I/O	P8	P10	P8	D1	P295	D26
I/O	P9	P11	P9	E3	P294	G24
I/O	–	P12	P10	E2	P293	F25
I/O	–	P13	P11	E1	P292	F26
I/O	–	–	P12	F3	P291	H23

XC4028XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	BG256	HQ304	BG352
I/O	–	–	P13	F2	P290	H24
I/O	–	–	–	–	P289	G25
I/O	–	–	–	–	P288	G26
GND	P10	P14	P14	GND*	P287	GND*
I/O, FCLK1	P11	P15	P15	G3	P286	J23
I/O	P12	P16	P16	G2	P285	J24
I/O (TMS)	P13	P17	P17	G1	P284	H25
I/O	P14	P18	P18	H3	P283	K23
VCC	–	–	P19	VCC*	P282	VCC*
I/O	–	–	P20	H2	P280	K24
I/O	–	–	P21	H1	P279	J25
I/O	–	–	–	–	P278	L24
I/O	–	–	–	–	P277	K25
GND	–	–	P22	GND*		GND*
I/O	–	–	–	J4	P276	L25
I/O	–	–	–	J3	P275	L26
I/O	–	P19	P23	J2	P274	M23
I/O	–	P20	P24	J1	P273	M24
I/O	P15	P21	P25	K2	P272	M25
I/O	P16	P22	P26	K3	P271	M26
I/O	P17	P23	P27	K1	P270	N24
I/O	P18	P24	P28	L1	P269	N25
GND	P19	P25	P29	GND*	P268	GND*
VCC	P20	P26	P30	VCC*	P267	VCC*
I/O	P21	P27	P31	L2	P266	N26
I/O	P22	P28	P32	L3	P265	P25
I/O	P23	P29	P33	L4	P264	P23
I/O	P24	P30	P34	M1	P263	P24
I/O	–	P31	P35	M2	P262	R26
I/O	–	P32	P36	M3	P261	R25
I/O	–	–	–	M4	P260	R24
I/O	–	–	–		P259	R23
GND	–	–	P37	GND*	–	GND*
I/O	–	–	–	–	P258	T26
I/O	–	–	–	–	P257	T25
I/O	–	–	P38	N1	P256	T23
I/O	–	–	P39	N2	P255	V26
VCC	–	–	P40	VCC*	P253	VCC*
I/O	P25	P33	P41	P1	P252	U24
I/O	P26	P34	P42	P2	P251	V25
I/O	P27	P35	P43	R1	P250	V24
I/O, FCLK2	P28	P36	P44	P3	P249	U23
GND	P29	P37	P45	GND*	P248	GND*
I/O	–	–	–	–	P247	Y26
I/O	–	–	–	–	P246	W25
I/O	–	–	P46	T1	P245	W24
I/O	–	–	P47	R3	P244	V23
I/O	–	P38	P48	T2	P243	AA26
I/O	–	P39	P49	U1	P242	Y25
I/O	P30	P40	P50	T3	P241	Y24
I/O	P31	P41	P51	U2	P240	AA25
GND	–	–	–	GND*	–	GND*
VCC	–	–	–	VCC*	–	VCC*
I/O	–	–	–	–	P239	AB25
I/O	–	–	–	–	P238	AA24
I/O	P32	P42	P52	V1	P237	Y23
I/O	P33	P43	P53	T4	P236	AC26

XC4028XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	BG256	HQ304	BG352
I/O	P34	P44	P54	U3	P235	AA23
I/O	P35	P45	P55	V2	P234	AB24
I/O	P36	P46	P56	W1	P233	AD25
I/O, GCK2	P37	P47	P57	V3	P232	AC24
O (M1)	P38	P48	P58	W2	P231	AB23
GND	P39	P49	P59	GND*	P230	GND*
I (M0)	P40	P50	P60	Y1	P229	AD24
VCC	P41	P55	P61	VCC*	P228	VCC*
I (M2)	P42	P56	P62	W3	P227	AC23
I/O, GCK3	P43	P57	P63	Y2	P226	AE24
I/O (HDC)	P44	P58	P64	W4	P225	AD23
I/O	P45	P59	P65	V4	P224	AC22
I/O	P46	P60	P66	U5	P223	AF24
I/O	P47	P61	P67	Y3	P222	AD22
I/O (/LDC)	P48	P62	P68	Y4	P221	AE23
I/O	–	–	–	–	P220	AE22
I/O	–	–	–	–	P219	AF23
VCC	–	–	–	VCC*	–	VCC*
GND	–	–	–	GND*	–	GND*
I/O	P49	P63	P69	V5	P218	AD20
I/O	P50	P64	P70	W5	P217	AE21
I/O	–	P65	P71	Y5	P216	AF21
I/O	–	P66	P72	V6	P215	AC19
I/O	–	–	P73	W6	P214	AD19
I/O	–	–	P74	Y6	P213	AE20
I/O	–	–	–	–	P212	AF20
I/O	–	–	–	–	P211	AC18
GND	P51	P67	P75	GND*	P210	GND*
I/O	P52	P68	P76	W7	P209	AD18
I/O	P53	P69	P77	Y7	P208	AE19
I/O	P54	P70	P78	V8	P207	AC17
I/O	P55	P71	P79	W8	P206	AD17
VCC	–	–	P80	VCC*	P204	VCC*
I/O	–	P72	P81	Y8	P203	AE18
I/O	–	P73	P82	U9	P202	AF18
I/O	–	–	–	–	P201	AE17
I/O		–	–	–	P200	AE16
GND	–	–	P83	GND*	–	GND*
I/O	–	–	–	V9	P199	AF16
I/O	–	–	–	W9	P198	AC15
I/O	–	–	P84	Y9	P197	AD15
I/O	–	–	P85	W10	P196	AE15
I/O	P56	P74	P86	V10	P195	AF15
I/O	P57	P75	P87	Y10	P194	AD14
I/O	P58	P76	P88	Y11	P193	AE14
I/O (/INIT)	P59	P77	P89	W11	P192	AF14
VCC	P60	P78	P90	VCC*	P191	VCC*
GND	P61	P79	P91	GND*	P190	GND*
I/O	P62	P80	P92	V11	P189	AE13
I/O	P63	P81	P93	U11	P188	AC13
I/O	P64	P82	P94	Y12	P187	AD13
I/O	P65	P83	P95	W12	P186	AF12
I/O	–	P84	P96	V12	P185	AE12
I/O	–	P85	P97	U12	P184	AD12
I/O	–	–	–	Y13	P183	AC12
I/O	–	–	–	W13	P182	AF11
GND	–	–	P98	GND*	–	GND*

XC4028XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	BG256	HQ304	BG352
I/O	–	–	–	–	P181	AE11
I/O	–	–	–	–	P180	AD11
I/O	–	–	P99	V13	P179	AF9
I/O	–	–	P100	Y14	P178	AD10
VCC	–	–	P101	VCC*	P177	VCC*
I/O	P66	P86	P102	Y15	P175	AE9
I/O	P67	P87	P103	V14	P174	AD9
I/O	P68	P88	P104	W15	P173	AC10
I/O	P69	P89	P105	Y16	P172	AF7
GND	P70	P90	P106	GND*	P171	GND*
I/O	–	–	–	–	P170	AE8
I/O	–	–	–	–	P169	AD8
I/O	–	–	–	V15	P168	AC9
I/O	–	–	–	W16	P167	AF6
I/O	–	–	–	Y17	P166	AE7
I/O	–	P92	P110	V16	P165	AD7
I/O	P71	P93	P111	W17	P164	AE6
I/O	P72	P94	P112	Y18	P163	AE5
GND	–	–	–	GND*	–	GND*
VCC	–	–	–	VCC*	–	VCC*
I/O	–	–	–	–	P162	AD6
I/O	–	–	–	–	P161	AC7
I/O	P73	P95	P113	U16	P160	AF4
I/O	P74	P96	P114	V17	P159	AF3
I/O	P75	P97	P115	W18	P158	AD5
I/O	P76	P98	P116	Y19	P157	AE3
I/O	P77	P99	P117	V18	P156	AD4
I/O, GCK4	P78	P100	P118	W19	P155	AC5
GND	P79	P101	P119	GND*	P154	GND*
DONE	P80	P103	P120	Y20	P153	AD3
VCC	P81	P106	P121	VCC*	P152	VCC*
/PROGRAM	P82	P108	P122	V19	P151	AC4
I/O (D7)	P83	P109	P123	U19	P150	AD2
I/O, GCK5	P84	P110	P124	U18	P149	AC3
I/O	P85	P111	P125	T17	P148	AB4
I/O	P86	P112	P126	V20	P147	AD1
I/O	–	–	P127	U20	P146	AA4
I/O	–	–	P128	T18	P145	AA3
I/O	–	–	–	–	P144	AB2
I/O	–	–	–	–	P143	AC1
VCC	–	–	–	VCC*	–	VCC*
GND	–	–	–	GND*	–	GND*
I/O (D6)	P87	P113	P129	T19	P142	Y3
I/O	P88	P114	P130	T20	P141	AA2
I/O	P89	P115	P131	R18	P140	AA1
I/O	P90	P116	P132	R19	P139	W4
I/O	–	P117	P133	R20	P138	W3
I/O	–	P118	P134	P18	P137	Y2
I/O	–	–	–	–	P136	Y1
I/O	–	–	–	–	P135	V4
GND	P91	P119	P135	GND*	P134	GND*
I/O	–	–	P136	P20	P133	V3
I/O	–	–	P137	N18	P132	W2
I/O, FCLK3	P92	P120	P138	N19	P131	U4
I/O	P93	P121	P139	N20	P130	U3
VCC			P140	VCC*	P129	VCC*
I/O (D5)	P94	P122	P141	M17	P127	V2

XC4028XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	BG256	HQ304	BG352
I/O (/CS0)	P95	P123	P142	M18	P126	V1
I/O	–	–	–	–	P125	U2
I/O	–	–	–	–	P124	T2
GND	–	–	P143*	GND*	–	GND*
I/O	–	–	–	–	P123	T1
I/O	–	–	–	M19	P122	R4
I/O	–	P124	P144	M20	P121	R3
I/O	–	P125	P145	L19	P120	R2
I/O	P96	P126	P146	L18	P119	R1
I/O	P97	P127	P147	L20	P118	P3
I/O (D4)	P98	P128	P148	K20	P117	P2
I/O	P99	P129	P149	K19	P116	P1
VCC	P100	P130	P150	VCC*	P115	VCC*
GND	P101	P131	P151	GND*	P114	GND*
I/O (D3)	P102	P132	P152	K18	P113	N2
I/O (/RS)	P103	P133	P153	K17	P112	N4
I/O	P104	P134	P154	J20	P111	N3
I/O	P105	P135	P155	J19	P110	M1
I/O	–	P136	P156	J18	P109	M2
I/O	–	P137	P157	J17	P108	M3
I/O	–	–	–	H20	P107	M4
I/O	–	–	–		P106	L1
GND	–	–	–	GND*	–	GND*
I/O	–	–	–	–	P105	L2
I/O	–	–	–	–	P104	L3
I/O (D2)	P106	P138	P159	H19	P103	J1
I/O	P107	P139	P160	H18	P102	K3
VCC			P161	VCC*	P101	VCC*
I/O	P108	P140	P162	G19	P99	J2
I/O, FCLK4	P109	P141	P163	F20	P98	J3
I/O	–	–	P164	G18	P97	K4
I/O	–	–	P165	F19	P96	G1
GND	P110	P142	P166	GND*	P95	GND*
I/O	–	–	–	–	P94	H2
I/O	–	–	–	–	P93	H3
I/O	–	–	P167	F18	P92	J4
I/O	–	–	P168	E19	P91	F1
I/O	–	P143	P169	D20	P90	G2
I/O	–	P144	P170	E18	P89	G3
I/O	P111	P145	P171	D19	P88	F2
I/O	P112	P146	P172	C20	P87	E2
GND	–	–	–	GND*	–	GND*
VCC	–	–	–	VCC*	–	VCC*
I/O (D1)	P113	P147	P173	E17	P86	F3
I/O (/RCK, RDY_/BUSY)	P114	P148	P174	D18	P85	G4
I/O	–	–	–	–	P84	D2
I/O	–	–	–	–	P83	F4
I/O	P115	P149	P175	C19	P82	E3
I/O	P116	P150	P176	B20	P81	C2
I/O (D0, DIN)	P117	P151	P177	C18	P80	D3
I/O, GCK6 (DOUT)	P118	P152	P178	B19	P79	E4
CCLK	P119	P153	P179	A20	P78	C3
VCC	P120	P154	P180	VCC*	P77	VCC*
O, TDO	P121	P159	P181	A19	P76	D4
GND	P122	P160	P182	GND*	P75	GND*
I/O (A0, /WS)	P123	P161	P183	B18	P74	B3
I/O, GCK7 (A1)	P124	P162	P184	B17	P73	C4

XC4028XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	BG256	HQ304	BG352
I/O	P125	P163	P185	C17	P72	D5
I/O	P126	P164	P186	D16	P71	A3
I/O, (CS1, A2)	P127	P165	P187	A18	P70	D6
I/O (A3)	P128	P166	P188	A17	P69	C6
I/O	–	–	–	–	P68	B5
I/O	–	–	–	–	P67	A4
VCC	–	–	–	VCC*	–	VCC*
GND	–	–	–	GND*	–	GND*
I/O	–	–	P189	C16	P66	C7
I/O	–	–	P190	B16	P65	B6
I/O	P129	P167	P191	A16	P64	A6
I/O	P130	P168	P192	C15	P63	D8
I/O	–	P169	P193	B15	P62	B7
I/O	–	P170	P194	A15	P61	A7
I/O	–	–	P195	—	P60	D9
I/O	–	–	–	–	P59	C9
GND	P131	P171	P196	GND*	P58	GND*
I/O	P132	P172	P197	B14	P57	B8
I/O	P133	P173	P198	A14	P56	D10
I/O	–	–	P199	C13	P55	C10
I/O	–	–	P200	B13	P54	B9
VCC*	–	–	P201	VCC*	P52	VCC*
I/O	–	–	–	A13	P51	A9
I/O	–	–	–	D12	P50	D11
I/O	–	–	–	–	P49	B11
I/O	–	–	–	–	P48	A11
GND	–	–	–	GND*	–	GND*
I/O (A4)	P134	P174	P202	C12	P47	D12
I/O (A5)	P135	P175	P203	B12	P46	C12
I/O		P176	P205	A12	P45	B12
I/O	P136	P177	P206	B11	P44	A12
I/O (A21)	P137	P178	P207	C11	P43	C13
I/O (A20)	P138	P179	P208	A11	P42	B13
I/O (A6)	P139	P180	P209	A10	P41	A13
I/O (A7)	P140	P181	P210	B10	P40	B14
GND	P141	P182	P211	GND*	P39	GND*
VCC	–	–	–	D6	–	A10
VCC	–	–	–	D11	–	A17
VCC	–	–	–	D15	–	AC14
VCC	–	–	–	F4	–	AC20
VCC	–	–	–	F17	–	AC8
VCC	–	–	–	K4	–	AF10
VCC	–	–	–	L17	–	AF17
VCC	–	–	–	R4	–	D7
VCC	–	–	–	R17	–	D13
VCC	–	–	–	U6	–	D19
VCC	–	–	–	U10	–	G23
VCC	–	–	–	U15	–	H4
VCC	–	–	–	C14	–	K1
VCC	–	–	–	F1	–	K26
VCC	–	–	–	R2	–	N23
VCC	–	–	–	E20	–	P4
VCC	–	–	–	P19	–	U1
VCC	–	–	–	V7	–	U26
VCC	–	–	–	–	–	W23
VCC	–	–	–	–	–	Y4
VCC	–	–	–	D7	–	B2

XC4028XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	BG256	HQ304	BG352
VCC	–	–	–	D14	–	B25
VCC	–	–	–	G17	–	AE2
VCC	–	–	–	P17	–	AE25
VCC	–	–	–	W20	–	–
VCC	–	–	–	U14	–	–
VCC	–	–	–	U7	–	–
VCC	–	–	–	P4	–	–
VCC	–	–	–	G4	–	–
GND	–	–	–	A1	–	A1
GND	–	–	–	D4	–	A14
GND	–	–	–	D8	–	A19
GND	–	–	–	D13	–	A2
GND	–	–	–	D17	–	A22
GND	–	–	–	H4	–	A25
GND	–	–	–	H17	–	A26
GND	–	–	–	N4	–	A5
GND	–	–	–	N17	–	A8
GND	–	–	–	U4	–	AB1
GND	–	–	–	U8	–	AB26
GND	–	–	–	U13	–	AE1
GND	–	–	–	U17	–	AE26
GND	–	–	–	B7	–	AF1
GND	–	–	–	N3	–	AF13
GND	–	–	–	W14	–	AF19
GND	–	–	–	G20	–	AF2
GND	–	–	–	–	–	AF22
GND	–	–	–	–	–	AF25
GND	–	–	–	–	–	AF26
GND	–	–	–	–	–	AF5
GND	–	–	–	–	–	AF8
GND	–	–	–	–	–	B1
GND	–	–	–	–	–	B26
GND	–	–	–	–	–	E1
GND	–	–	–	–	–	E26
GND	–	–	–	–	–	H1
GND	–	–	–	–	–	H26
GND	–	–	–	–	–	N1
GND	–	–	–	–	–	P26
GND	–	–	–	–	–	W1
GND	–	–	–	–	–	W26
GND	–	–	P204	–	–	–
GND	–	–	P219	–	–	–
NC	–	P1	–	–	P11	A18
NC	–	P3	–	–	P24	A24
NC	–	P51	–	–	P53	B4
NC	–	P52	–	–	P100	B10
NC	–	P53	–	–	P128	B23
NC	–	P54	–	–	P176	C1
NC	–	P102	–	–	P205	C5
NC	–	P104	–	–	P254	C11
NC	–	P105	–	–	P281	D1
NC	–	P107	–	–	–	D16
NC	–	P155	–	–	–	D25
NC	–	P156	–	–	–	F23
NC	–	P157	–	–	–	J26

XC4028XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	BG256	HQ304	BG352
NC	–	P158	–	–	–	L23
NC	–	P206	–	–	–	T3
NC	–	P207	–	–	–	T4
NC	–	P208	–	–	–	T24
NC	–	–	–	–	–	U25
NC	–	–	–	–	–	AB3
NC	–	–	–	–	–	AC2
NC	–	–	–	–	–	AC6
NC	–	–	–	–	–	AC11
NC	–	–	–	–	–	AC16
NC	–	–	–	–	–	AC21
NC	–	–	–	–	–	AC25
NC	–	–	–	–	–	AD16
NC	–	–	–	–	–	AD21
NC	–	–	–	–	–	AD26
NC	–	–	–	–	–	AE4
NC	–	–	–	–	–	AE10
NC	–	–	–	–	–	C8
NC	–	–	–	–	–	L4
NC	–	–	–	–	–	K2

12/18/98

XC4036XLA Pinout Table

XC4036XLA Pinout Table

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432
VCC	P142	P183	P212	P38	VCC*	VCC*
I/O (A8)	P143	P184	P213	P37	D14	D17
I/O (A9)	P144	P185	P214	P36	C14	A17
I/O (A19)	P145	P186	P215	P35	A15	C18
I/O (A18)	P146	P187	P216	P34	B15	D18
I/O	–	P188	P217	P33	C15	B18
I/O	–	P189	P218	P32	D15	A19
I/O (A10)	P147	P190	P220	P31	A16	B19
I/O (A11)	P148	P191	P221	P30	B16	C19
VCC	–	–	–	–	VCC*	VCC*
GND	–	–	–	–	GND*	GND*
I/O	–	–	–	P29	C16	D19
I/O	–	–	–	P28	B17	A20
I/O	–	–	–	–	D16	B20
I/O	–	–	–	–	A18	C20
I/O	–	–	–	P27	C17	C21
I/O	–	–	–	P26	B18	A22
VCC	–	–	P222	P25	VCC*	VCC*
I/O	–	–	P223	P23	C18	B22
I/O	–	–	P224	P22	D17	C22
I/O	P149	P192	P225	P21	A20	B23
I/O	P150	P193	P226	P20	B19	A24
GND	P151	P194	P227	P19	GND*	GND*
I/O	–	–	–	P18	C19	D22
I/O	–	–	–	P17	D18	C23
I/O	–	P195	P228	P16	A21	B24
I/O	–	P196	P229	P15	B20	C24
I/O	P152	P197	P230	P14	C20	A26
I/O	P153	P198	P231	P13	B21	C25
I/O (A12)	P154	P199	P232	P12	B22	D24
I/O (A13)	P155	P200	P233	P10	C21	B26
GND	–	–	–	–	GND*	GND*
VCC	–	–	–	–	VCC*	VCC*
I/O	–	–	–	P9	D20	A27
I/O	–	–	–	P8	A23	D25
I/O	–	–	–	–	A24	C26
I/O	–	–	–	–	B23	B27
I/O	–	–	P234	P7	D21	C27
I/O	–	–	P235	P6	C22	B28
I/O	P156	P201	P236	P5	B24	D27
I/O	P157	P202	P237	P4	C23	B29
I/O (A14)	P158	P203	P238	P3	D22	C28
I/O, GCK8 (A15)	P159	P204	P239	P2	C24	D28
VCC	P160	P205	P240	P1	VCC*	VCC*
GND	P1	P2	P1	P304	GND*	GND*
I/O, GCK1 (A16)	P2	P4	P2	P303	D23	D29
I/O (A17)	P3	P5	P3	P302	C25	C30
I/O	P4	P6	P4	P301	D24	E28
I/O	P5	P7	P5	P300	E23	E29
I/O (TDI)	P6	P8	P6	P299	C26	D30
I/O (TCK)	P7	P9	P7	P298	E24	D31
I/O	–	–	–	–	D25	E30
I/O	–	–	–	–	F23	E31
I/O	–	–	–	P297	F24	G28
I/O	–	–	–	P296	E25	G29

XC4036XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432
VCC	–	–	–	–	VCC*	VCC*
GND	–	–	–	–	GND*	GND*
I/O	P8	P10	P8	P295	D26	H28
I/O	P9	P11	P9	P294	G24	H29
I/O	–	P12	P10	P293	F25	G30
I/O	–	P13	P11	P292	F26	H30
I/O	–	–	P12	P291	H23	J28
I/O	–	–	P13	P290	H24	J29
I/O	–	–	–	P289	G25	H31
I/O	–	–	–	P288	G26	J30
GND	P10	P14	P14	P287	GND*	GND*
I/O, FCLK1	P11	P15	P15	P286	J23	K28
I/O	P12	P16	P16	P285	J24	K29
I/O (TMS)	P13	P17	P17	P284	H25	K30
I/O	P14	P18	P18	P283	K23	K31
VCC	–	–	P19	P282	VCC*	VCC*
I/O	–	–	P20	P280	K24	L29
I/O	–		P21	P279	J25	L30
I/O	–	–	–	–	J26	M29
I/O	–	–	–	–	L23	M31
I/O	–	–	–	P278	L24	N31
I/O	–	–	–	P277	K25	N28
GND			P22	–	GND*	GND*
VCC	–	–	–	–	VCC*	VCC*
I/O	–	–	–	P276	L25	P30
I/O	–	–	–	P275	L26	P28
I/O	–	P19	P23	P274	M23	P29
I/O	–	P20	P24	P273	M24	R31
I/O	P15	P21	P25	P272	M25	R30
I/O	P16	P22	P26	P271	M26	R28
I/O	P17	P23	P27	P270	N24	R29
I/O	P18	P24	P28	P269	N25	T31
GND	P19	P25	P29	P268	GND*	GND*
VCC	P20	P26	P30	P267	VCC*	VCC*
I/O	P21	P27	P31	P266	N26	T30
I/O	P22	P28	P32	P265	P25	T29
I/O	P23	P29	P33	P264	P23	U31
I/O	P24	P30	P34	P263	P24	U30
I/O	–	P31	P35	P262	R26	U28
I/O	–	P32	P36	P261	R25	U29
I/O	–	–	–	P260	R24	V30
I/O	–	–	–	P259	R23	V29
VCC	–	–	–	–	VCC*	VCC*
GND	–	–	P37	–	GND*	GND*
I/O	–	–	–	P258	T26	W30
I/O	–	–	–	P257	T25	W29
I/O	–	–	–	–	T24	Y30
I/O	–	–	–	–	U25	Y29
I/O	–	–	P38	P256	T23	Y28
I/O	–	–	P39	P255	V26	AA30
VCC	–	–	P40	P253	VCC*	VCC*
I/O	P25	P33	P41	P252	U24	AA29
I/O	P26	P34	P42	P251	V25	AB31
I/O	P27	P35	P43	P250	V24	AB30
I/O, FCLK2	P28	P36	P44	P249	U23	AB29
GND	P29	P37	P45	P248	GND*	GND*
I/O	–	–	–	P247	Y26	AB28

XC4036XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432
I/O	–	–	–	P246	W25	AC30
I/O	–	–	P46	P245	W24	AC29
I/O	–	–	P47	P244	V23	AC28
I/O	–	P38	P48	P243	AA26	AD29
I/O	–	P39	P49	P242	Y25	AD28
I/O	P30	P40	P50	P241	Y24	AE30
I/O	P31	P41	P51	P240	AA25	AE29
GND	–	–	–	–	GND*	GND*
VCC	–	–	–	–	VCC*	VCC*
I/O	–	–	–	P239	AB25	AF31
I/O	–	–	–	P238	AA24	AE28
I/O	P32	P42	P52	P237	Y23	AG31
I/O	P33	P43	P53	P236	AC26	AF28
I/O	–	–	–	–	AD26	AG30
I/O	–	–	–	–	AC25	AG29
I/O	P34	P44	P54	P235	AA23	AH31
I/O	P35	P45	P55	P234	AB24	AG28
I/O	P36	P46	P56	P233	AD25	AH30
I/O, GCK2	P37	P47	P57	P232	AC24	AJ30
O (M1)	P38	P48	P58	P231	AB23	AH29
GND	P39	P49	P59	P230	GND*	GND*
I (M0)	P40	P50	P60	P229	AD24	AH28
VCC	P41	P55	P61	P228	VCC*	VCC*
I (M2)	P42	P56	P62	P227	AC23	AJ28
I/O, GCK3	P43	P57	P63	P226	AE24	AK29
I/O (HDC)	P44	P58	P64	P225	AD23	AH27
I/O	P45	P59	P65	P224	AC22	AK28
I/O	P46	P60	P66	P223	AF24	AJ27
I/O	P47	P61	P67	P222	AD22	AL28
I/O (/LDC)	P48	P62	P68	P221	AE23	AH26
I/O	–	–	–	–	AC21	AL27
I/O	–	–	–	–	AD21	AH25
I/O	–	–	–	P220	AE22	AK26
I/O	–	–	–	P219	AF23	AL26
VCC	–	–	–	–	VCC*	VCC*
GND	–	–	–	–	GND*	GND*
I/O	P49	P63	P69	P218	AD20	AH24
I/O	P50	P64	P70	P217	AE21	AJ25
I/O	–	P65	P71	P216	AF21	AK25
I/O	–	P66	P72	P215	AC19	AJ24
I/O	–	–	P73	P214	AD19	AL24
I/O	–	–	P74	P213	AE20	AH22
I/O	–	–	–	P212	AF20	AJ23
I/O	–	–	–	P211	AC18	AK23
GND	P51	P67	P75	P210	GND*	GND*
I/O	P52	P68	P76	P209	AD18	AJ22
I/O	P53	P69	P77	P208	AE19	AK22
I/O	P54	P70	P78	P207	AC17	AL22
I/O	P55	P71	P79	P206	AD17	AJ21
VCC	–	–	P80	P204	VCC*	VCC*
I/O	–	P72	P81	P203	AE18	AH20
I/O	–	P73	P82	P202	AF18	AK21
I/O	–	–	–	–	AC16	AK20
I/O	–	–	–	–	AD16	AJ19
I/O	–	–	–	P201	AE17	AL20
I/O	–	–	–	P200	AE16	AH18
GND	–	–	P83	–	GND*	GND*

XC4036XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432
VCC	–	–	–	–	VCC*	VCC*
I/O	–	–	–	P199	AF16	AK19
I/O	–	–	–	P198	AC15	AJ18
I/O	–	–	P84	P197	AD15	AL19
I/O	–	–	P85	P196	AE15	AK18
I/O	P56	P74	P86	P195	AF15	AH17
I/O	P57	P75	P87	P194	AD14	AJ17
I/O	P58	P76	P88	P193	AE14	AJ16
I/O (/INIT)	P59	P77	P89	P192	AF14	AK16
VCC	P60	P78	P90	P191	VCC*	VCC*
GND	P61	P79	P91	P190	GND*	GND*
I/O	P62	P80	P92	P189	AE13	AL16
I/O	P63	P81	P93	P188	AC13	AH15
I/O	P64	P82	P94	P187	AD13	AK15
I/O	P65	P83	P95	P186	AF12	AJ14
I/O	–	P84	P96	P185	AE12	AH14
I/O	–	P85	P97	P184	AD12	AK14
I/O	–	–	–	P183	AC12	AL13
I/O	–	–	–	P182	AF11	AK13
VCC	–	–	–	–	VCC*	VCC*
GND	–	–	P98	–	GND*	GND*
I/O	–	–	–	P181	AE11	AJ13
I/O	–	–	–	P180	AD11	AH13
I/O	–	–	–	–	AE10	AL12
I/O	–	–	–	–	AC11	AK12
I/O	–	–	P99	P179	AF9	AH12
I/O	–	–	P100	P178	AD10	AJ11
VCC	–	–	P101	P177	VCC*	VCC*
I/O	P66	P86	P102	P175	AE9	AL10
I/O	P67	P87	P103	P174	AD9	AK10
I/O	P68	P88	P104	P173	AC10	AJ10
I/O	P69	P89	P105	P172	AF7	AK9
GND	P70	P90	P106	P171	GND*	GND*
I/O	–	–	–	P170	AE8	AL8
I/O	–	–	–	P169	AD8	AH10
I/O	–	–	P107	P168	AC9	AJ9
I/O	–	–	P108	P167	AF6	AK8
I/O	–	P91	P109	P166	AE7	AK7
I/O	–	P92	P110	P165	AD7	AL6
I/O	P71	P93	P111	P164	AE6	AJ7
I/O	P72	P94	P112	P163	AE5	AH8
GND	–	–	–	–	GND*	GND*
VCC	–	–	–	–	VCC*	VCC*
I/O	–	–	–	P162	AD6	AK6
I/O	–	–	–	P161	AC7	AL5
I/O	P73	P95	P113	P160	AF4	AH7
I/O	P74	P96	P114	P159	AF3	AJ6
I/O	–	–	–	–	AE4	AK5
I/O	–	–	–	–	AC6	AL4
I/O	P75	P97	P115	P158	AD5	AK4
I/O	P76	P98	P116	P157	AE3	AH5
I/O	P77	P99	P117	P156	AD4	AK3
I/O, GCK4	P78	P100	P118	P155	AC5	AJ4
GND	P79	P101	P119	P154	GND*	GND*
DONE	P80	P103	P120	P153	AD3	AH4
VCC	P81	P106	P121	P152	VCC*	VCC*
/PROGRAM	P82	P108	P122	P151	AC4	AH3

XC4036XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432
I/O (D7)	P83	P109	P123	P150	AD2	AJ2
I/O, GCK5	P84	P110	P124	P149	AC3	AG4
I/O	P85	P111	P125	P148	AB4	AG3
I/O	P86	P112	P126	P147	AD1	AH2
I/O	–	–	–	–	AB3	AH1
I/O	–	–	–	–	AC2	AF4
I/O	–	–	P127	P146	AA4	AF3
I/O	–	–	P128	P145	AA3	AG2
I/O	–	–	–	P144	AB2	AE3
I/O	–	–	–	P143	AC1	AF2
VCC	–	–	–	–	VCC*	VCC*
GND	–	–	–	–	GND*	GND*
I/O (D6)	P87	P113	P129	P142	Y3	AF1
I/O	P88	P114	P130	P141	AA2	AD4
I/O	P89	P115	P131	P140	AA1	AD3
I/O	P90	P116	P132	P139	W4	AE2
I/O	–	P117	P133	P138	W3	AC3
I/O	–	P118	P134	P137	Y2	AD1
I/O	–	–	–	P136	Y1	AC2
I/O	–	–	–	P135	V4	AB4
GND	P91	P119	P135	P134	GND*	GND*
I/O	–	–	P136	P133	V3	AB3
I/O	–	–	P137	P132	W2	AB2
I/O, FCLK3	P92	P120	P138	P131	U4	AB1
I/O	P93	P121	P139	P130	U3	AA3
VCC	–	–	P140	P129	VCC*	VCC*
I/O (D5)	P94	P122	P141	P127	V2	AA2
I/O (/CS0)	P95	P123	P142	P126	V1	Y2
I/O	–	–	–	–	T4	Y4
I/O	–	–	–	–	T3	Y3
I/O	–	–	–	P125	U2	W4
I/O	–	–	–	P124	T2	W3
GND	–	–	P143*	–	GND*	GND*
VCC	–	–	–	–	VCC*	VCC*
I/O	–	–	–	P123	T1	V4
I/O	–	–	–	P122	R4	V3
I/O	–	P124	P144	P121	R3	U1
I/O	–	P125	P145	P120	R2	U2
I/O	P96	P126	P146	P119	R1	U4
I/O	P97	P127	P147	P118	P3	U3
I/O (D4)	P98	P128	P148	P117	P2	T1
I/O	P99	P129	P149	P116	P1	T2
VCC	P100	P130	P150	P115	VCC*	VCC*
GND	P101	P131	P151	P114	GND*	GND*
I/O (D3)	P102	P132	P152	P113	N2	T3
I/O (/RS)	P103	P133	P153	P112	N4	R1
I/O	P104	P134	P154	P111	N3	R2
I/O	P105	P135	P155	P110	M1	R4
I/O	–	P136	P156	P109	M2	R3
I/O	–	P137	P157	P108	M3	P2
I/O	–	–	–	P107	M4	P3
I/O	–	–	–	P106	L1	P4
VCC	–	–	–	–	VCC*	VCC*
GND	–	–	P158	–	GND*	GND*
I/O	–	–	–	P105	L2	N3
I/O	–	–	–	P104	L3	N4
I/O	–	–	–	–	K2	M1

XC4036XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432
I/O	–	–	–	–	L4	M2
I/O (D2)	P106	P138	P159	P103	J1	L2
I/O	P107	P139	P160	P102	K3	L3
VCC	–	–	P161	P101	VCC*	VCC*
I/O	P108	P140	P162	P99	J2	K1
I/O, FCLK4	P109	P141	P163	P98	J3	K2
I/O	–	–	P164	P97	K4	K3
I/O	–	–	P165	P96	G1	K4
GND	P110	P142	P166	P95	GND*	GND*
I/O	–	–	–	P94	H2	J2
I/O	–	–	–	P93	H3	J3
I/O	–	–	P167	P92	J4	J4
I/O	–	–	P168	P91	F1	H1
I/O	–	P143	P169	P90	G2	H2
I/O	–	P144	P170	P89	G3	H3
I/O	P111	P145	P171	P88	F2	H4
I/O	P112	P146	P172	P87	E2	G2
GND	–	–	–	–	GND*	GND*
VCC	–	–	–	–	VCC*	VCC*
I/O (D1)	P113	P147	P173	P86	F3	G4
I/O (/RCK, RDY_/BUSY)	P114	P148	P174	P85	G4	F2
I/O	–	–	–	–	D1	F3
I/O	–	–	–	–	C1	E1
I/O	–	–	–	P84	D2	E3
I/O	–	–	–	P83	F4	D1
I/O	P115	P149	P175	P82	E3	E4
I/O	P116	P150	P176	P81	C2	D2
I/O (D0, DIN)"	P117	P151	P177	P80	D3	C2
I/O, GCK6 (DOUT)	P118	P152	P178	P79	E4	D3
CCLK	P119	P153	P179	P78	C3	D4
VCC	P120	P154	P180	P77	VCC*	VCC*
O, TDO	P121	P159	P181	P76	D4	C4
GND	P122	P160	P182	P75	GND*	GND*
I/O (A0, /WS)	P123	P161	P183	P74	B3	B3
I/O, GCK7 (A1)	P124	P162	P184	P73	C4	D5
I/O	P125	P163	P185	P72	D5	B4
I/O	P126	P164	P186	P71	A3	C5
I/O	–	–	–	–	C5	B5
I/O	–	–	–	–	B4	C6
I/O, (CS1, A2)	P127	P165	P187	P70	D6	A5
I/O (A3)	P128	P166	P188	P69	C6	D7
I/O	–	–	–	P68	B5	B6
I/O	–	–	–	P67	A4	A6
VCC	–	–	–	–	VCC*	VCC*
GND	–	–	–	–	GND*	GND*
I/O	–	–	P189	P66	C7	D8
I/O	–	–	P190	P65	B6	C7
I/O	P129	P167	P191	P64	A6	B7
I/O	P130	P168	P192	P63	D8	D9
I/O	–	P169	P193	P62	B7	D10
I/O	–	P170	P194	P61	A7	C9
I/O	–	–	P195	P60	D9	B9
I/O	–	–	–	P59	C9	C10
GND	P131	P171	P196	P58	GND*	GND*
I/O	P132	P172	P197	P57	B8	B10
I/O	P133	P173	P198	P56	D10	A10
I/O	–	–	P199	P55	C10	C11

XC4036XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432
I/O	–	–	P200	P54	B9	D12
VCC	–	–	P201	P52	VCC*	VCC*
I/O	–	–	–	P51	A9	B11
I/O	–	–	–	P50	D11	C12
I/O	–	–	–	–	C11	C13
I/O	–	–	–	–	B10	A12
I/O	–	–	–	P49	B11	D14
I/O	–	–	–	P48	A11	B13
GND	–	–	–	–	GND*	GND*
VCC	–	–	–	–	VCC*	VCC*
I/O (A4)	P134	P174	P202	P47	D12	C14
I/O (A5)	P135	P175	P203	P46	C12	A13
I/O	–	P176	P205	P45	B12	B14
I/O	P136	P177	P206	P44	A12	D15
I/O (A21)	P137	P178	P207	P43	C13	C15
I/O (A20)	P138	P179	P208	P42	B13	B15
I/O (A6)	P139	P180	P209	P41	A13	B16
I/O (A7)	P140	P181	P210	P40	B14	A16
GND	P141	P182	P211	P39	GND*	GND*
VCC	–	–	–	–	A10	A1
VCC	–	–	–	–	A17	A11
VCC	–	–	–	–	AC14	A21
VCC	–	–	–	–	AC20	A31
VCC	–	–	–	–	AC8	D11
VCC	–	–	–	–	AF10	D21
VCC	–	–	–	–	AF17	L1
VCC	–	–	–	–	D7	L4
VCC	–	–	–	–	D13	L28
VCC	–	–	–	–	D19	L31
VCC	–	–	–	–	G23	AA1
VCC	–	–	–	–	H4	AA4
VCC	–	–	–	–	K1	AA28
VCC	–	–	–	–	K26	AA31
VCC	–	–	–	–	N23	AH11
VCC	–	–	–	–	P4	AH21
VCC	–	–	–	–	U1	AL1
VCC	–	–	–	–	U26	AL11
VCC	–	–	–	–	W23	AL21
VCC	–	–	–	–	Y4	AL31
VCC	–	–	–	–	B2	C3
VCC	–	–	–	–	B25	C29
VCC	–	–	–	–	AE2	AJ3
VCC	–	–	–	–	AE25	AJ29
GND	–	–	–	–	A1	A2
GND	–	–	–	–	A14	A3
GND	–	–	–	–	A19	A7
GND	–	–	–	–	A2	A9
GND	–	–	–	–	A22	A14
GND	–	–	–	–	A25	A18
GND	–	–	–	–	A26	A23
GND	–	–	–	–	A5	A25
GND	–	–	–	–	A8	A29
GND	–	–	–	–	AB1	A30
GND	–	–	–	–	AB26	B1
GND	–	–	–	–	AE1	B2
GND	–	–	–	–	AE26	B30

XC4036XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432
GND	–	–	–	–	AF1	B31
GND	–	–	–	–	AF13	C1
GND	–	–	–	–	AF19	C31
GND	–	–	–	–	AF2	D16
GND	–	–	–	–	AF22	G1
GND	–	–	–	–	AF25	G31
GND	–	–	–	–	AF26	J1
GND	–	–	–	–	AF5	J31
GND	–	–	–	–	AF8	P1
GND	–	–	–	–	B1	P31
GND	–	–	–	–	B26	T4
GND	–	–	–	–	E1	T28
GND	–	–	–	–	E26	V1
GND	–	–	–	–	H1	V31
GND	–	–	–	–	H26	AC1
GND	–	–	–	–	N1	AC31
GND	–	–	–	–	P26	AE1
GND	–	–	–	–	W1	AE31
GND	–	–	–	–	W26	AH16
GND	–	–	–	–	–	AJ1
GND	–	–	–	–	–	AJ31
GND	–	–	–	–	–	AK1
GND	–	–	–	–	–	AK2
GND	–	–	–	–	–	AK30
GND	–	–	–	–	–	AK31
GND	–	–	–	–	–	AL2
GND	–	–	–	–	–	AL3
GND	–	–	–	–	–	AL7
GND	–	–	–	–	–	AL9
GND	–	–	–	–	–	AL14
GND	–	–	–	–	–	AL18
GND	–	–	–	–	–	AL23
GND	–	–	–	–	–	AL25
GND	–	–	–	–	–	AL29
GND	–	–	–	–	–	AL30
GND	–		P204	–	–	–
GND	–		P219	–	–	–
NC	–	P1	–	P11	C8	D26
NC	–	P3	–	P24	–	A28
NC	–	P51	–	P53	–	B25
NC	–	P52	–	P100	–	D23
NC	–	P53	–	P128	–	D20
NC	–	P54	–	P176	–	B21
NC	–	P102	–	P205	–	B17
NC	–	P104	–	P254	–	C17
NC	–	P105	–	P281	–	C16
NC	–	P107	–	–	–	A15
NC	–	P155	–	–	–	B12
NC	–	P156	–	–	–	D13
NC	–	P157	–	–	–	A8
NC	–	P158	–	–	–	B8
NC	–	P206	–	–	–	D6
NC	–	P207	–	–	–	A4
NC	–	P208	–	–	–	E2
NC	–	–	–	–	–	F4
NC	–	–	–	–	–	F1

XC4036XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432
NC	–	–	–	–	–	G3
NC	–	–	–	–	–	M4
NC	–	–	–	–	–	M3
NC	–	–	–	–	–	N2
NC	–	–	–	–	–	N1
NC	–	–	–	–	–	V2
NC	–	–	–	–	–	W2
NC	–	–	–	–	–	W1
NC	–	–	–	–	–	Y1
NC	–	–	–	–	–	AC4
NC	–	–	–	–	–	AD2
NC	–	–	–	–	–	AE4
NC	–	–	–	–	–	AG1
NC	–	–	–	–	–	AJ5
NC	–	–	–	–	–	AH6
NC	–	–	–	–	–	AH9
NC	–	–	–	–	–	AJ8
NC	–	–	–	–	–	AK11
NC	–	–	–	–	–	AJ12
NC	–	–	–	–	–	AJ15
NC	–	–	–	–	–	AL15
NC	–	–	–	–	–	AL17
NC	–	–	–	–	–	AK17
NC	–	–	–	–	–	AH19
NC	–	–	–	–	–	AJ20
NC	–	–	–	–	–	AK24
NC	–	–	–	–	–	AH23
NC	–	–	–	–	–	AJ26
NC	–	–	–	–	–	AK27
NC	–	–	–	–	–	AF29
NC	–	–	–	–	–	AF30
NC	–	–	–	–	–	AD30
NC	–	–	–	–	–	AD31
NC	–	–	–	–	–	Y31
NC	–	–	–	–	–	W28
NC	–	–	–	–	–	W31
NC	–	–	–	–	–	V28
NC	–	–	–	–	–	N30
NC	–	–	–	–	–	N29
NC	–	–	–	–	–	M28
NC	–	–	–	–	–	M30
NC	–	–	–	–	–	F31
NC	–	–	–	–	–	F30
NC	–	–	–	–	–	F29
NC	–	–	–	–	–	F28
NC	–	–	–	–	–	C8

12/18/98

XC4044XLA Pinout Table

XC4044XLA Pinout Table

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432
VCC	P142	P183	P212	P38	VCC*	VCC*
I/O (A8)	P143	P184	P213	P37	D14	D17
I/O (A9)	P144	P185	P214	P36	C14	A17
I/O	–	–	–	–	–	C17
I/O	–	–	–	–	–	B17
I/O (A19)	P145	P186	P215	P35	A15	C18
I/O (A18)	P146	P187	P216	P34	B15	D18
I/O	–	P188	P217	P33	C15	B18
I/O	–	P189	P218	P32	D15	A19
I/O (A10)	P147	P190	P220	P31	A16	B19
I/O (A11)	P148	P191	P221	P30	B16	C19
VCC	–	–	–	–	VCC*	VCC*
GND	–	–	–	–	GND*	GND*
I/O	–	–	–	P29	C16	D19
I/O	–	–	–	P28	B17	A20
I/O	–	–	–	–	D16	B20
I/O	–	–	–	–	A18	C20
I/O	–	–	–	P27	C17	C21
I/O	–	–	–	P26	B18	A22
VCC	–	–	P222	P25	VCC*	VCC*
I/O	–	–	P223	P23	C18	B22
I/O	–	–	P224	P22	D17	C22
I/O	P149	P192	P225	P21	A20	B23
I/O	P150	P193	P226	P20	B19	A24
GND	P151	P194	P227	P19	GND*	GND*
I/O	–	–	–	P18	C19	D22
I/O	–	–	–	P17	D18	C23
I/O	–	P195	P228	P16	A21	B24
I/O	–	P196	P229	P15	B20	C24
I/O	–	–	–	–	–	D23
I/O	–	–	–	–	–	B25
I/O	P152	P197	P230	P14	C20	A26
I/O	P153	P198	P231	P13	B21	C25
I/O (A12)	P154	P199	P232	P12	B22	D24
I/O (A13)	P155	P200	P233	P10	C21	B26
GND	–	–	–	–	GND*	GND*
VCC	–	–	–	–	VCC*	VCC*
I/O	–	–	–	P9	D20	A27
I/O	–	–	–	P8	A23	D25
I/O	–	–	–	–	A24	C26
I/O	–	–	–	–	B23	B27
I/O	–	–	P234	P7	D21	C27
I/O	–	–	P235	P6	C22	B28
I/O	P156	P201	P236	P5	B24	D27
I/O	P157	P202	P237	P4	C23	B29
I/O (A14)	P158	P203	P238	P3	D22	C28
I/O, GCK8 (A15)	P159	P204	P239	P2	C24	D28
VCC	P160	P205	P240	P1	VCC*	VCC*
GND	P1	P2	P1	P304	GND*	GND*
I/O, GCK1 (A16)	P2	P4	P2	P303	D23	D29
I/O (A17)	P3	P5	P3	P302	C25	C30
I/O	P4	P6	P4	P301	D24	E28
I/O	P5	P7	P5	P300	E23	E29
I/O (TDI)	P6	P8	P6	P299	C26	D30
I/O (TCK)	P7	P9	P7	P298	E24	D31

XC4044XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432
I/O	–	–	–	–	D25	E30
I/O	–	–	–	–	F23	E31
I/O	–	–	–	P297	F24	G28
I/O	–	–	–	P296	E25	G29
VCC	–	–	–	–	VCC*	VCC*
GND	–	–	–	–	GND*	GND*
I/O	–	–	–	–	–	F30
I/O	–	–	–	–	–	F31
I/O	P8	P10	P8	P295	D26	H28
I/O	P9	P11	P9	P294	G24	H29
I/O	–	P12	P10	P293	F25	G30
I/O	–	P13	P11	P292	F26	H30
I/O	–	–	P12	P291	H23	J28
I/O	–	–	P13	P290	H24	J29
I/O	–	–		P289	G25	H31
I/O	–	–		P288	G26	J30
GND	P10	P14	P14	P287	GND*	GND*
I/O, FCLK1	P11	P15	P15	P286	J23	K28
I/O	P12	P16	P16	P285	J24	K29
I/O (TMS)	P13	P17	P17	P284	H25	K30
I/O	P14	P18	P18	P283	K23	K31
VCC	–	–	P19	P282	VCC*	VCC*
I/O	–	–	P20	P280	K24	L29
I/O	–	–	P21	P279	J25	L30
I/O	–	–	–	–	J26	M29
I/O	–	–	–	–	L23	M31
I/O	–	–	–	P278	L24	N31
I/O	–	–	–	P277	K25	N28
GND	–	–	P22	–	GND*	GND*
VCC	–	–	–	–	VCC*	VCC*
I/O	–	–	–	–	–	N29
I/O	–	–	–	–	–	N30
I/O	–	–	–	P276	L25	P30
I/O	–	–	–	P275	L26	P28
I/O	–	P19	P23	P274	M23	P29
I/O	–	P20	P24	P273	M24	R31
I/O	P15	P21	P25	P272	M25	R30
I/O	P16	P22	P26	P271	M26	R28
I/O	P17	P23	P27	P270	N24	R29
I/O	P18	P24	P28	P269	N25	T31
GND	P19	P25	P29	P268	GND*	GND*
VCC	P20	P26	P30	P267	VCC*	VCC*
I/O	P21	P27	P31	P266	N26	T30
I/O	P22	P28	P32	P265	P25	T29
I/O	P23	P29	P33	P264	P23	U31
I/O	P24	P30	P34	P263	P24	U30
I/O	–	P31	P35	P262	R26	U28
I/O	–	P32	P36	P261	R25	U29
I/O	–	–	–	P260	R24	V30
I/O	–	–	–	P259	R23	V29
I/O	–	–	–	–	–	V28
I/O	–	–	–	–	–	W31
VCC	–	–	–	–	VCC*	VCC*
GND	–	–	P37	–	GND*	GND*
I/O	–	–	–	P258	T26	W30
I/O	–	–	–	P257	T25	W29
I/O	–	–	–	–	T24	Y30

XC4044XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432
I/O	–	–	–	–	U25	Y29
I/O	–	–	P38	P256	T23	Y28
I/O	–	–	P39	P255	V26	AA30
VCC	–	–	P40	P253	VCC*	VCC*
I/O	P25	P33	P41	P252	U24	AA29
I/O	P26	P34	P42	P251	V25	AB31
I/O	P27	P35	P43	P250	V24	AB30
I/O, FCLK2	P28	P36	P44	P249	U23	AB29
GND	P29	P37	P45	P248	GND*	GND*
I/O	–	–	–	P247	Y26	AB28
I/O	–	–	–	P246	W25	AC30
I/O	–	–	P46	P245	W24	AC29
I/O	–	–	P47	P244	V23	AC28
I/O	–	–	–	–	–	AD31
I/O	–	–	–	–	–	AD30
I/O	–	P38	P48	P243	AA26	AD29
I/O	–	P39	P49	P242	Y25	AD28
I/O	P30	P40	P50	P241	Y24	AE30
I/O	P31	P41	P51	P240	AA25	AE29
GND	–	–	–	–	GND*	GND*
VCC	–	–	–	–	VCC*	VCC*
I/O	–	–	–	P239	AB25	AF31
I/O	–	–	–	P238	AA24	AE28
I/O	P32	P42	P52	P237	Y23	AG31
I/O	P33	P43	P53	P236	AC26	AF28
I/O	–	–	–	–	AD26	AG30
I/O	–	–	–	–	AC25	AG29
I/O	P34	P44	P54	P235	AA23	AH31
I/O	P35	P45	P55	P234	AB24	AG28
I/O	P36	P46	P56	P233	AD25	AH30
I/O, GCK2	P37	P47	P57	P232	AC24	AJ30
O (M1)	P38	P48	P58	P231	AB23	AH29
GND	P39	P49	P59	P230	GND*	GND*
I (M0)	P40	P50	P60	P229	AD24	AH28
VCC	P41	P55	P61	P228	VCC*	VCC*
I (M2)	P42	P56	P62	P227	AC23	AJ28
I/O, GCK3	P43	P57	P63	P226	AE24	AK29
I/O (HDC)	P44	P58	P64	P225	AD23	AH27
I/O	P45	P59	P65	P224	AC22	AK28
I/O	P46	P60	P66	P223	AF24	AJ27
I/O	P47	P61	P67	P222	AD22	AL28
I/O (/LDC)	P48	P62	P68	P221	AE23	AH26
I/O	–	–	–	–	AC21	AL27
I/O	–	–	–	–	AD21	AH25
I/O		–	–	P220	AE22	AK26
I/O	–	–	–	P219	AF23	AL26
VCC	–	–	–	–	VCC*	VCC*
GND	–	–	–	–	GND*	GND*
I/O	P49	P63	P69	P218	AD20	AH24
I/O	P50	P64	P70	P217	AE21	AJ25
I/O	–	P65	P71	P216	AF21	AK25
I/O	–	P66	P72	P215	AC19	AJ24
I/O	–	–	–	–	–	AH23
I/O	–	–	–	–	–	AK24
I/O	–	–	P73	P214	AD19	AL24
I/O	–	–	P74	P213	AE20	AH22
I/O	–	–	–	P212	AF20	AJ23

XC4044XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432
I/O	–	–	–	P211	AC18	AK23
GND	P51	P67	P75	P210	GND*	GND*
I/O	P52	P68	P76	P209	AD18	AJ22
I/O	P53	P69	P77	P208	AE19	AK22
I/O	P54	P70	P78	P207	AC17	AL22
I/O	P55	P71	P79	P206	AD17	AJ21
VCC	–	–	P80	P204	VCC*	VCC*
I/O	–	P72	P81	P203	AE18	AH20
I/O	–	P73	P82	P202	AF18	AK21
I/O	–	–	–	–	AC16	AK20
I/O	–	–	–	–	AD16	AJ19
I/O	–	–	–	P201	AE17	AL20
I/O	–	–	–	P200	AE16	AH18
GND	–	–	P83	–	GND*	GND*
VCC	–	–	–	–	VCC*	VCC*
I/O	–	–	–	P199	AF16	AK19
I/O	–	–	–	P198	AC15	AJ18
I/O	–	–	P84	P197	AD15	AL19
I/O	–	–	P85	P196	AE15	AK18
I/O	P56	P74	P86	P195	AF15	AH17
I/O	P57	P75	P87	P194	AD14	AJ17
I/O	–	–	–	–	–	AK17
I/O	–	–	–	–	–	AL17
I/O	P58	P76	P88	P193	AE14	AJ16
I/O (/INIT)	P59	P77	P89	P192	AF14	AK16
VCC	P60	P78	P90	P191	VCC*	VCC*
GND	P61	P79	P91	P190	GND*	GND*
I/O	P62	P80	P92	P189	AE13	AL16
I/O	P63	P81	P93	P188	AC13	AH15
I/O	–	–	–	–	–	AL15
I/O	–	–	–	–	–	AJ15
I/O	P64	P82	P94	P187	AD13	AK15
I/O	P65	P83	P95	P186	AF12	AJ14
I/O	–	P84	P96	P185	AE12	AH14
I/O	–	P85	P97	P184	AD12	AK14
I/O	–	–	–	P183	AC12	AL13
I/O	–	–	–	P182	AF11	AK13
VCC	–	–	–	–	VCC*	VCC*
GND	–	–	P98	–	GND*	GND*
I/O	–		–	P181	AE11	AJ13
I/O	–	–	–	P180	AD11	AH13
I/O	–	–	–	–	AE10	AL12
I/O	–	–	–	–	AC11	AK12
I/O	–	–	P99	P179	AF9	AH12
I/O	–	–	P100	P178	AD10	AJ11
VCC	–	–	P101	P177	VCC*	VCC*
I/O	P66	P86	P102	P175	AE9	AL10
I/O	P67	P87	P103	P174	AD9	AK10
I/O	P68	P88	P104	P173	AC10	AJ10
I/O	P69	P89	P105	P172	AF7	AK9
GND	P70	P90	P106	P171	GND*	GND*
I/O	–	–	–	P170	AE8	AL8
I/O	–	–	–	P169	AD8	AH10
I/O	–	–	P107	P168	AC9	AJ9
I/O	–	–	P108	P167	AF6	AK8
I/O	–	–	–	–	–	AJ8
I/O	–	–	–	–	–	AH9

XC4044XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432
I/O	–	P91	P109	P166	AE7	AK7
I/O	–	P92	P110	P165	AD7	AL6
I/O	P71	P93	P111	P164	AE6	AJ7
I/O	P72	P94	P112	P163	AE5	AH8
GND	–	–	–	–	GND*	GND*
VCC	–	–	–	–	VCC*	VCC*
I/O	–	–	–	P162	AD6	AK6
I/O	–	–	–	P161	AC7	AL5
I/O	P73	P95	P113	P160	AF4	AH7
I/O	P74	P96	P114	P159	AF3	AJ6
I/O	–	–	–	–	AE4	AK5
I/O	–	–	–	–	AC6	AL4
I/O	P75	P97	P115	P158	AD5	AK4
I/O	P76	P98	P116	P157	AE3	AH5
I/O	P77	P99	P117	P156	AD4	AK3
I/O, GCK4	P78	P100	P118	P155	AC5	AJ4
GND	P79	P101	P119	P154	GND*	GND*
DONE	P80	P103	P120	P153	AD3	AH4
VCC	P81	P106	P121	P152	VCC*	VCC*
/PROGRAM	P82	P108	P122	P151	AC4	AH3
I/O (D7)	P83	P109	P123	P150	AD2	AJ2
I/O, GCK5	P84	P110	P124	P149	AC3	AG4
I/O	P85	P111	P125	P148	AB4	AG3
I/O	P86	P112	P126	P147	AD1	AH2
I/O	–	–	–	–	AB3	AH1
I/O	–	–	–	–	AC2	AF4
I/O	–	–	P127	P146	AA4	AF3
I/O	–	–	P128	P145	AA3	AG2
I/O	–	–	–	P144	AB2	AE3
I/O	–	–	–	P143	AC1	AF2
VCC	–	–	–	–	VCC*	VCC*
GND	–	–	–	–	GND*	GND*
I/O (D6)	P87	P113	P129	P142	Y3	AF1
I/O	P88	P114	P130	P141	AA2	AD4
I/O	P89	P115	P131	P140	AA1	AD3
I/O	P90	P116	P132	P139	W4	AE2
I/O	–	–	–	–	–	AD2
I/O	–	–	–	–	–	AC4
I/O	–	P117	P133	P138	W3	AC3
I/O	–	P118	P134	P137	Y2	AD1
I/O	–	–	–	P136	Y1	AC2
I/O	–	–	–	P135	V4	AB4
GND	P91	P119	P135	P134	GND*	GND*
I/O	–	–	P136	P133	V3	AB3
I/O	–	–	P137	P132	W2	AB2
I/O, FCLK3	P92	P120	P138	P131	U4	AB1
I/O	P93	P121	P139	P130	U3	AA3
VCC	–	–	P140	P129	VCC*	VCC*
I/O (D5)	P94	P122	P141	P127	V2	AA2
I/O (/CS0)	P95	P123	P142	P126	V1	Y2
I/O	–	–	–	–	T4	Y4
I/O	–	–	–	–	T3	Y3
I/O	–	–	–	P125	U2	W4
I/O	–	–	–	P124	T2	W3
GND	–	–	P143*	–	GND*	GND*
VCC	–	–	–	–	VCC*	VCC*
I/O	–	–	–	–	–	W2

XC4044XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432
I/O	–	–	–	–	–	V2
I/O	–	–	–	P123	T1	V4
I/O	–	–	–	P122	R4	V3
I/O	–	P124	P144	P121	R3	U1
I/O	–	P125	P145	P120	R2	U2
I/O	P96	P126	P146	P119	R1	U4
I/O	P97	P127	P147	P118	P3	U3
I/O (D4)	P98	P128	P148	P117	P2	T1
I/O	P99	P129	P149	P116	P1	T2
VCC	P100	P130	P150	P115	VCC*	VCC*
GND	P101	P131	P151	P114	GND*	GND*
I/O (D3)	P102	P132	P152	P113	N2	T3
I/O (/RS)	P103	P133	P153	P112	N4	R1
I/O	P104	P134	P154	P111	N3	R2
I/O	P105	P135	P155	P110	M1	R4
I/O	–	P136	P156	P109	M2	R3
I/O	–	P137	P157	P108	M3	P2
I/O	–	–	–	P107	M4	P3
I/O	–	–	–	P106	L1	P4
I/O	–	–	–	–	–	N1
I/O	–	–	–	–	–	N2
VCC	–	–	–	–	VCC*	VCC*
GND	–	–	P158	–	GND*	GND*
I/O	–	–	–	P105	L2	N3
I/O	–	–	–	P104	L3	N4
I/O	–	–	–	–	K2	M1
I/O	–	–	–	–	L4	M2
I/O (D2)	P106	P138	P159	P103	J1	L2
I/O	P107	P139	P160	P102	K3	L3
VCC			P161	P101	VCC*	VCC*
I/O	P108	P140	P162	P99	J2	K1
I/O, FCLK4	P109	P141	P163	P98	J3	K2
I/O	–	–	P164	P97	K4	K3
I/O	–	–	P165	P96	G1	K4
GND	P110	P142	P166	P95	GND*	GND*
I/O	–	–	–	P94	H2	J2
I/O	–	–	–	P93	H3	J3
I/O	–	–	P167	P92	J4	J4
I/O	–	–	P168	P91	F1	H1
I/O	–	P143	P169	P90	G2	H2
I/O	–	P144	P170	P89	G3	H3
I/O	P111	P145	P171	P88	F2	H4
I/O	P112	P146	P172	P87	E2	G2
I/O	–	–	–	–	–	G3
I/O	–	–	–	–	–	F1
GND	–	–	–	–	GND*	GND*
VCC	–	–	–	–	VCC*	VCC*
I/O (D1)	P113	P147	P173	P86	F3	G4
I/O (/RCK, RDY_/BUSY)	P114	P148	P174	P85	G4	F2
I/O	–	–	–	–	D1	F3
I/O	–	–	–	–	C1	E1
I/O	–	–	–	P84	D2	E3
I/O	–	–	–	P83	F4	D1
I/O	P115	P149	P175	P82	E3	E4
I/O	P116	P150	P176	P81	C2	D2
I/O (D0, DIN)	P117	P151	P177	P80	D3	C2

XC4044XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432
I/O, GCK6 (DOUT)	P118	P152	P178	P79	E4	D3
CCLK	P119	P153	P179	P78	C3	D4
VCC	P120	P154	P180	P77	VCC*	VCC*
O, TDO	P121	P159	P181	P76	D4	C4
GND	P122	P160	P182	P75	GND*	GND*
I/O (A0, /WS)	P123	P161	P183	P74	B3	B3
I/O, GCK7 (A1)	P124	P162	P184	P73	C4	D5
I/O	P125	P163	P185	P72	D5	B4
I/O	P126	P164	P186	P71	A3	C5
I/O	–	–	–	–	C5	B5
I/O	–	–	–	–	B4	C6
I/O, (CS1, A2)	P127	P165	P187	P70	D6	A5
I/O (A3)	P128	P166	P188	P69	C6	D7
I/O	–	–	–	P68	B5	B6
I/O	–	–	–	P67	A4	A6
VCC	–	–	–	–	VCC*	VCC*
GND	–	–	–	–	GND*	GND*
I/O	–	–	P189	P66	C7	D8
I/O	–	–	P190	P65	B6	C7
I/O	P129	P167	P191	P64	A6	B7
I/O	P130	P168	P192	P63	D8	D9
I/O	–	–	–	–	C8	B8
I/O	–	–	–	–	–	A8
I/O	–	P169	P193	P62	B7	D10
I/O	–	P170	P194	P61	A7	C9
I/O	–	–	P195	P60	D9	B9
I/O	–	–	–	P59	C9	C10
GND	P131	P171	P196	P58	GND*	GND*
I/O	P132	P172	P197	P57	B8	B10
I/O	P133	P173	P198	P56	D10	A10
I/O	–	–	P199	P55	C10	C11
I/O	–	–	P200	P54	B9	D12
VCC	–	–	P201	P52	VCC*	VCC*
I/O	–	–	–	P51	A9	B11
I/O	–	–	–	P50	D11	C12
I/O	–	–	–	–	C11	C13
I/O	–	–	–	–	B10	A12
I/O	–	–	–	P49	B11	D14
I/O	–	–	–	P48	A11	B13
GND	–	–	–	–	GND*	GND*
VCC	–	–	–	–	VCC*	VCC*
I/O (A4)	P134	P174	P202	P47	D12	C14
I/O (A5)	P135	P175	P203	P46	C12	A13
I/O		P176	P205	P45	B12	B14
I/O	P136	P177	P206	P44	A12	D15
I/O (A21)	P137	P178	P207	P43	C13	C15
I/O (A20)	P138	P179	P208	P42	B13	B15
I/O	–	–	–	–	–	A15
I/O	–	–	–	–	–	C16
I/O (A6)	P139	P180	P209	P41	A13	B16
I/O (A7)	P140	P181	P210	P40	B14	A16
GND	P141	P182	P211	P39	GND*	GND*
VCC	–	–	–	–	A10	A1
VCC	–	–	–	–	A17	A11
VCC	–	–	–	–	AC14	A21
VCC	–	–	–	–	AC20	A31
VCC	–	–	–	–	AC8	D11

XC4044XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432
VCC	–	–	–	–	AF10	D21
VCC	–	–	–	–	AF17	L1
VCC	–	–	–	–	D7	L4
VCC	–	–	–	–	D13	L28
VCC	–	–	–	–	D19	L31
VCC	–	–	–	–	G23	AA1
VCC	–	–	–	–	H4	AA4
VCC	–	–	–	–	K1	AA28
VCC	–	–	–	–	K26	AA31
VCC	–	–	–	–	N23	AH11
VCC	–	–	–	–	P4	AH21
VCC	–	–	–	–	U1	AL1
VCC	–	–	–	–	U26	AL11
VCC	–	–	–	–	W23	AL21
VCC	–	–	–	–	Y4	AL31
VCC	–	–	–	–	B2	C3
VCC	–	–	–	–	B25	C29
VCC	–	–	–	–	AE2	AJ3
VCC	–	–	–	–	AE25	AJ29
GND	–	–	–	–	A1	A2
GND	–	–	–	–	A14	A3
GND	–	–	–	–	A19	A7
GND	–	–	–	–	A2	A9
GND	–	–	–	–	A22	A14
GND	–	–	–	–	A25	A18
GND	–	–	–	–	A26	A23
GND	–	–	–	–	A5	A25
GND	–	–	–	–	A8	A29
GND	–	–	–	–	AB1	A30
GND	–	–	–	–	AB26	B1
GND	–	–	–	–	AE1	B2
GND	–	–	–	–	AE26	B30
GND	–	–	–	–	AF1	B31
GND	–	–	–	–	AF13	C1
GND	–	–	–	–	AF19	C31
GND	–	–	–	–	AF2	D16
GND	–	–	–	–	AF22	G1
GND	–	–	–	–	AF25	G31
GND	–	–	–	–	AF26	J1
GND	–	–	–	–	AF5	J31
GND	–	–	–	–	AF8	P1
GND	–	–	–	–	B1	P31
GND	–	–	–	–	B26	T4
GND	–	–	–	–	E1	T28
GND	–	–	–	–	E26	V1
GND	–	–	–	–	H1	V31
GND	–	–	–	–	H26	AC1
GND	–	–	–	–	N1	AC31
GND	–	–	–	–	P26	AE1
GND	–	–	–	–	W1	AE31
GND	–	–	–	–	W26	AH16
GND	–	–	–	–	–	AJ1
GND	–	–	–	–	–	AJ31
GND	–	–	–	–	–	AK1
GND	–	–	–	–	–	AK2
GND	–	–	–	–	–	AK30

XC4044XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432
GND	–	–	–	–	–	AK31
GND	–	–	–	–	–	AL2
GND	–	–	–	–	–	AL3
GND	–	–	–	–	–	AL7
GND	–	–	–	–	–	AL9
GND	–	–	–	–	–	AL14
GND	–	–	–	–	–	AL18
GND	–	–	–	–	–	AL23
GND	–	–	–	–	–	AL25
GND	–	–	–	–	–	AL29
GND	–	–	–	–	–	AL30
GND	–	–	P219	–	–	–
GND	–	–	P204	–	–	–
NC	–	P1	–	P11	–	D26
NC	–	P3	–	P24	–	A28
NC	–	P51	–	P53	–	D20
NC	–	P52	–	P100	–	B21
NC	–	P53	–	P128	–	B12
NC	–	P54	–	P176	–	D13
NC	–	P102	–	P205	–	D6
NC	–	P104	–	P254	–	A4
NC	–	P105	–	P281	–	E2
NC	–	P107	–	–	–	F4
NC	–	P155	–	–	–	M4
NC	–	P156	–	–	–	M3
NC	–	P157	–	–	–	W1
NC	–	P158	–	–	–	Y1
NC	–	P206	–	–	–	AE4
NC	–	P207	–	–	–	AG1
NC	–	P208	–	–	–	AJ5
NC	–		–	–	–	AH6
NC	–	–	–	–	–	AK11
NC	–	–	–	–	–	AJ12
NC	–	–	–	–	–	AH19
NC	–	–	–	–	–	AJ20
NC	–	–	–	–	–	AJ26
NC	–	–	–	–	–	AK27
NC	–	–	–	–	–	AF29
NC	–	–	–	–	–	AF30
NC	–	–	–	–	–	W28
NC	–	–	–	–	–	Y31
NC	–	–	–	–	–	M28
NC	–	–	–	–	–	M30
NC	–	–	–	–	–	F29
NC	–	–	–	–	–	F28
NC	–	–	–	–	–	C8

12/18/98

XC4052XLA Pinout Table

XC4052XLA Pinout Table

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
VCC	P142	P183	P212	P38	VCC*	VCC*	VCC*
I/O (A8)	P143	P184	P213	P37	D14	D17	A17
I/O (A9)	P144	P185	P214	P36	C14	A17	B18
I/O	-	-	-	-	-	C17	C18
I/O	-	-	-	-	-	B17	E18
GND	-	-	-	-	-	GND*	GND*
I/O (A19)	P145	P186	P215	P35	A15	C18	C19
I/O (A18)	P146	P187	P216	P34	B15	D18	D19
I/O	-	P188	P217	P33	C15	B18	E19
I/O	-	P189	P218	P32	D15	A19	B20
I/O (A10)	P147	P190	P220	P31	A16	B19	C20
I/O (A11)	P148	P191	P221	P30	B16	C19	D20
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	P29	C16	D19	A21
I/O	-	-	-	P28	B17	A20	E20
I/O	-	-	-	-	D16	B20	B21
I/O	-	-	-	-	A18	C20	C21
I/O	-	-	-	-	-	B21	D21
I/O	-	-	-	-	-	D20	B22
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	P27	C17	C21	C23
I/O	-	-	-	P26	B18	A22	E22
VCC	-	-	P222	P25	VCC*	VCC*	VCC*
I/O	-	-	P223	P23	C18	B22	B24
I/O	-	-	P224	P22	D17	C22	D23
I/O	P149	P192	P225	P21	A20	B23	C24
I/O	P150	P193	P226	P20	B19	A24	A25
GND	P151	P194	P227	P19	GND*	GND*	GND*
I/O	-	-	-	P18	C19	D22	E23
I/O	-	-	-	P17	D18	C23	B25
I/O	-	P195	P228	P16	A21	B24	D24
I/O	-	P196	P229	P15	B20	C24	C25
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	D23	E25
I/O	-	-	-	-	-	B25	C27
I/O	P152	P197	P230	P14	C20	A26	D26
I/O	P153	P198	P231	P13	B21	C25	B28
I/O (A12)	P154	P199	P232	P12	B22	D24	B29
I/O (A13)	P155	P200	P233	P10	C21	B26	E26
GND	-	-	-	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	P9	D20	A27	C28
I/O	-	-	-	P8	A23	D25	D27
I/O	-	-	-	-	A24	C26	B30
I/O	-	-	-	-	B23	B27	C29
I/O	-	-	-	-	-	A28	E27
I/O	-	-	-	-	-	D26	A31
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	P234	P7	D21	C27	D28
I/O	-	-	P235	P6	C22	B28	C30
I/O	P156	P201	P236	P5	B24	D27	D29
I/O	P157	P202	P237	P4	C23	B29	E28
I/O (A14)	P158	P203	P238	P3	D22	C28	D30
I/O, GCK8 (A15)	P159	P204	P239	P2	C24	D28	E29

XC4052XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
VCC	P160	P205	P240	P1	VCC*	VCC*	VCC*
GND	P1	P2	P1	P304	GND*	GND*	GND*
I/O, GCK1 (A16)	P2	P4	P2	P303	D23	D29	B33
I/O (A17)	P3	P5	P3	P302	C25	C30	F29
I/O	P4	P6	P4	P301	D24	E28	E30
I/O	P5	P7	P5	P300	E23	E29	D31
I/O (TDI)	P6	P8	P6	P299	C26	D30	F30
I/O (TCK)	P7	P9	P7	P298	E24	D31	C33
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	F28	G29
I/O	-	-	-	-	-	F29	E31
I/O	-	-	-	-	D25	E30	D32
I/O	-	-	-	-	F23	E31	G30
I/O	-	-	-	P297	F24	G28	F31
I/O	-	-	-	P296	E25	G29	H29
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	-	-	F30	H30
I/O	-	-	-	-	-	F31	G31
I/O	P8	P10	P8	P295	D26	H28	J29
I/O	P9	P11	P9	P294	G24	H29	F33
I/O	-	P12	P10	P293	F25	G30	G32
I/O	-	P13	P11	P292	F26	H30	J30
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	P12	P291	H23	J28	K30
I/O	-	-	P13	P290	H24	J29	H33
I/O	-	-	-	P289	G25	H31	L29
I/O	-	-	-	P288	G26	J30	K31
GND	P10	P14	P14	P287	GND*	GND*	GND*
I/O, FCLK1	P11	P15	P15	P286	J23	K28	L30
I/O	P12	P16	P16	P285	J24	K29	K32
I/O (TMS)	P13	P17	P17	P284	H25	K30	J33
I/O	P14	P18	P18	P283	K23	K31	M29
VCC	-	-	P19	P282	VCC*	VCC*	VCC*
I/O	-	-	P20	P280	K24	L29	L32
I/O	-	-	P21	P279	J25	L30	M31
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	M30	N29
I/O	-	-	-	-	-	M28	L33
I/O	-	-	-	-	J26	M29	M32
I/O	-	-	-	-	L23	M31	P29
I/O	-	-	-	P278	L24	N31	P30
I/O	-	-	-	P277	K25	N28	N33
GND	-	-	P22	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	-	-	N29	P31
I/O	-	-	-	-	-	N30	P32
I/O	-	-	-	P276	L25	P30	R29
I/O	-	-	-	P275	L26	P28	R30
I/O	-	P19	P23	P274	M23	P29	R31
I/O	-	P20	P24	P273	M24	R31	R33
GND	-	-	-	-	-	GND*	GND*
I/O	P15	P21	P25	P272	M25	R30	T31
I/O	P16	P22	P26	P271	M26	R28	T29
I/O	P17	P23	P27	P270	N24	R29	U32
I/O	P18	P24	P28	P269	N25	T31	U31
GND	P19	P25	P29	P268	GND*	GND*	GND*

XC4052XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
VCC	P20	P26	P30	P267	VCC*	VCC*	VCC*
I/O	P21	P27	P31	P266	N26	T30	U29
I/O	P22	P28	P32	P265	P25	T29	U30
I/O	P23	P29	P33	P264	P23	U31	V31
I/O	P24	P30	P34	P263	P24	U30	V29
GND	-	-	-	-	-	GND*	GND*
I/O	-	P31	P35	P262	R26	U28	V30
I/O	-	P32	P36	P261	R25	U29	W33
I/O	-	-	-	P260	R24	V30	W31
I/O	-	-	-	P259	R23	V29	W30
I/O	-	-	-	-	-	V28	W29
I/O	-	-	-	-	-	W31	Y32
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	P37	-	GND*	GND*	GND*
I/O	-	-	-	P258	T26	W30	Y31
I/O	-	-	-	P257	T25	W29	Y30
I/O	-	-	-	-	-	W28	AA32
I/O	-	-	-	-	-	Y31	AA31
I/O	-	-	-	-	T24	Y30	AA30
I/O	-	-	-	-	U25	Y29	AB32
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	P38	P256	T23	Y28	AA29
I/O	-	-	P39	P255	V26	AA30	AB31
VCC	-	-	P40	P253	VCC*	VCC*	VCC*
I/O	P25	P33	P41	P252	U24	AA29	AC31
I/O	P26	P34	P42	P251	V25	AB31	AB29
I/O	P27	P35	P43	P250	V24	AB30	AD32
I/O, FCLK2	P28	P36	P44	P249	U23	AB29	AC30
GND	P29	P37	P45	P248	GND*	GND*	GND*
I/O	-	-	-	P247	Y26	AB28	AD31
I/O	-	-	-	P246	W25	AC30	AE33
I/O	-	-	P46	P245	W24	AC29	AC29
I/O	-	-	P47	P244	V23	AC28	AE32
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	AD31	AG33
I/O	-	-	-	-	-	AD30	AH33
I/O	-	P38	P48	P243	AA26	AD29	AE29
I/O	-	P39	P49	P242	Y25	AD28	AG31
I/O	P30	P40	P50	P241	Y24	AE30	AF30
I/O	P31	P41	P51	P240	AA25	AE29	AH32
GND	-	-	-	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	P239	AB25	AF31	AJ32
I/O	-	-	-	P238	AA24	AE28	AF29
I/O	-	-	-	-	-	AF30	AH31
I/O	-	-	-	-	-	AF29	AG30
I/O	P32	P42	P52	P237	Y23	AG31	AK32
I/O	P33	P43	P53	P236	AC26	AF28	AJ31
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	AD26	AG30	AG29
I/O	-	-	-	-	AC25	AG29	AL33
I/O	P34	P44	P54	P235	AA23	AH31	AH30
I/O	P35	P45	P55	P234	AB24	AG28	AK31
I/O	P36	P46	P56	P233	AD25	AH30	AJ30
I/O, GCK2	P37	P47	P57	P232	AC24	AJ30	AH29
O (M1)	P38	P48	P58	P231	AB23	AH29	AK30
GND	P39	P49	P59	P230	GND*	GND*	GND*

XC4052XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
I (M0)	P40	P50	P60	P229	AD24	AH28	AJ29
VCC	P41	P55	P61	P228	VCC*	VCC*	VCC*
I (M2)	P42	P56	P62	P227	AC23	AJ28	AN32
I/O, GCK3	P43	P57	P63	P226	AE24	AK29	AJ28
I/O (HDC)	P44	P58	P64	P225	AD23	AH27	AK29
I/O	P45	P59	P65	P224	AC22	AK28	AL30
I/O	P46	P60	P66	P223	AF24	AJ27	AK28
I/O	P47	P61	P67	P222	AD22	AL28	AM31
I/O (/LDC)	P48	P62	P68	P221	AE23	AH26	AJ27
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	AK27	AN31
I/O	-	-	-	-	-	AJ26	AL29
I/O	-	-	-	-	AC21	AL27	AK27
I/O	-	-	-	-	AD21	AH25	AL28
I/O	-	-	-	P220	AE22	AK26	AJ26
I/O	-	-	-	P219	AF23	AL26	AM30
VCC	-	-	-	-	VCC*	VCC*	VCC
GND	-	-	-	-	GND*	GND*	GND*
I/O	P49	P63	P69	P218	AD20	AH24	AM29
I/O	P50	P64	P70	P217	AE21	AJ25	AK26
I/O	-	P65	P71	P216	AF21	AK25	AL27
I/O	-	P66	P72	P215	AC19	AJ24	AJ25
I/O	-	-	-	-	-	AH23	AN29
I/O	-	-	-	-	-	AK24	AN28
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	P73	P214	AD19	AL24	AL25
I/O	-	-	P74	P213	AE20	AH22	AJ23
I/O	-	-	-	P212	AF20	AJ23	AN26
I/O	-	-	-	P211	AC18	AK23	AL24
GND	P51	P67	P75	P210	GND*	GND*	GND*
I/O	P52	P68	P76	P209	AD18	AJ22	AK23
I/O	P53	P69	P77	P208	AE19	AK22	AN25
I/O	P54	P70	P78	P207	AC17	AL22	AJ22
I/O	P55	P71	P79	P206	AD17	AJ21	AL23
VCC	-	-	P80	P204	VCC*	VCC*	VCC*
I/O	-	P72	P81	P203	AE18	AH20	AM24
I/O	-	P73	P82	P202	AF18	AK21	AK22
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	AJ20	AK21
I/O	-	-	-	-	-	AH19	AM22
I/O	-	-	-	-	AC16	AK20	AJ20
I/O	-	-	-	-	AD16	AJ19	AL21
I/O	-	-	-	P201	AE17	AL20	AN21
I/O	-	-	-	P200	AE16	AH18	AK20
GND	-	-	P83	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	P199	AF16	AK19	AL20
I/O	-	-	-	P198	AC15	AJ18	AJ19
I/O	-	-	P84	P197	AD15	AL19	AM20
I/O	-	-	P85	P196	AE15	AK18	AK19
I/O	P56	P74	P86	P195	AF15	AH17	AL19
I/O	P57	P75	P87	P194	AD14	AJ17	AN19
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	AK17	AL18
I/O	-	-	-	-	-	AL17	AM18
I/O	P58	P76	P88	P193	AE14	AJ16	AK17
I/O (/INIT)	P59	P77	P89	P192	AF14	AK16	AJ17

XC4052XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
VCC	P60	P78	P90	P191	VCC*	VCC*	VCC*
GND	P61	P79	P91	P190	GND*	GND*	GND*
I/O	P62	P80	P92	P189	AE13	AL16	AL17
I/O	P63	P81	P93	P188	AC13	AH15	AM17
I/O	-	-	-	-	-	AL15	AN17
I/O	-	-	-	-	-	AJ15	AK16
GND	-	-	-	-	-	GND*	GND*
I/O	P64	P82	P94	P187	AD13	AK15	AM16
I/O	P65	P83	P95	P186	AF12	AJ14	AL15
I/O	-	P84	P96	P185	AE12	AH14	AK15
I/O	-	P85	P97	P184	AD12	AK14	AJ15
I/O	-	-	-	P183	AC12	AL13	AN15
I/O	-	-	-	P182	AF11	AK13	AM14
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	P98	-	GND*	GND*	GND*
I/O	-	-	-	P181	AE11	AJ13	AL14
I/O	-	-	-	P180	AD11	AH13	AK14
I/O	-	-	-	-	AE10	AL12	AJ14
I/O	-	-	-	-	AC11	AK12	AN13
I/O	-	-	-	-	-	AJ12	AM13
I/O	-	-	-	-	-	AK11	AL13
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	P99	P179	AF9	AH12	AK12
I/O	-	-	P100	P178	AD10	AJ11	AN11
VCC	-	-	P101	P177	VCC*	VCC*	VCC*
I/O	P66	P86	P102	P175	AE9	AL10	AJ12
I/O	P67	P87	P103	P174	AD9	AK10	AL11
I/O	P68	P88	P104	P173	AC10	AJ10	AK11
I/O	P69	P89	P105	P172	AF7	AK9	AM10
GND	P70	P90	P106	P171	GND*	GND*	GND*
I/O	-	-	-	P170	AE8	AL8	AL10
I/O	-	-	-	P169	AD8	AH10	AJ11
I/O	-	-	P107	P168	AC9	AJ9	AN9
I/O	-	-	P108	P167	AF6	AK8	AK10
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	AJ8	AN7
I/O	-	-	-	-	-	AH9	AJ9
I/O	-	P91	P109	P166	AE7	AK7	AL7
I/O	-	P92	P110	P165	AD7	AL6	AK8
I/O	P71	P93	P111	P164	AE6	AJ7	AN6
I/O	P72	P94	P112	P163	AE5	AH8	AM6
GND	-	-	-	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	P162	AD6	AK6	AJ8
I/O	-	-	-	P161	AC7	AL5	AL6
I/O	P73	P95	P113	P160	AF4	AH7	AK7
I/O	P74	P96	P114	P159	AF3	AJ6	AM5
I/O	-	-	-	-	AE4	AK5	AM4
I/O	-	-	-	-	AC6	AL4	AJ7
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	AH6	AL5
I/O	-	-	-	-	-	AJ5	AK6
I/O	P75	P97	P115	P158	AD5	AK4	AN3
I/O	P76	P98	P116	P157	AE3	AH5	AK5
I/O	P77	P99	P117	P156	AD4	AK3	AJ6
I/O, GCK4	P78	P100	P118	P155	AC5	AJ4	AL4
GND	P79	P101	P119	P154	GND*	GND*	GND*

XC4052XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
DONE	P80	P103	P120	P153	AD3	AH4	AJ5
VCC	P81	P106	P121	P152	VCC*	VCC*	VCC*
/PROGRAM	P82	P108	P122	P151	AC4	AH3	AM1
I/O (D7)	P83	P109	P123	P150	AD2	AJ2	AH5
I/O, GCK5	P84	P110	P124	P149	AC3	AG4	AJ4
I/O	P85	P111	P125	P148	AB4	AG3	AK3
I/O	P86	P112	P126	P147	AD1	AH2	AH4
I/O	-	-	-	-	AB3	AH1	AL1
I/O	-	-	-	-	AC2	AF4	AG5
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	P127	P146	AA4	AF3	AJ3
I/O	-	-	P128	P145	AA3	AG2	AK2
I/O	-	-	-	-	-	AG1	AG4
I/O	-	-	-	-	-	AE4	AH3
I/O	-	-	-	P144	AB2	AE3	AF5
I/O	-	-	-	P143	AC1	AF2	AJ2
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	-	GND*	GND*	GND*
I/O (D6)	P87	P113	P129	P142	Y3	AF1	AJ1
I/O	P88	P114	P130	P141	AA2	AD4	AF4
I/O	P89	P115	P131	P140	AA1	AD3	AG3
I/O	P90	P116	P132	P139	W4	AE2	AE5
I/O	-	-	-	-	-	AD2	AH1
I/O	-	-	-	-	-	AC4	AF3
GND	-	-	-	-	-	GND*	GND*
I/O	-	P117	P133	P138	W3	AC3	AE3
I/O	-	P118	P134	P137	Y2	AD1	AC5
I/O	-	-	-	P136	Y1	AC2	AE1
I/O	-	-	-	P135	V4	AB4	AD3
GND	P91	P119	P135	P134	GND*	GND*	GND*
I/O	-	-	P136	P133	V3	AB3	AC4
I/O	-	-	P137	P132	W2	AB2	AD2
I/O, FCLK3	P92	P120	P138	P131	U4	AB1	AB5
I/O	P93	P121	P139	P130	U3	AA3	AC3
VCC	-	-	P140	P129	VCC*	VCC*	VCC*
I/O (D5)	P94	P122	P141	P127	V2	AA2	AA5
I/O (/CS0)	P95	P123	P142	P126	V1	Y2	AB3
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	T4	Y4	AB2
I/O	-	-	-	-	T3	Y3	AA4
I/O	-	-	-	-	-	Y1	AA3
I/O	-	-	-	-	-	W1	Y5
I/O	-	-	-	P125	U2	W4	Y3
I/O	-	-	-	P124	T2	W3	Y2
GND	-	-	P143*	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	-	-	W2	W5
I/O	-	-	-	-	-	V2	W4
I/O	-	-	-	P123	T1	V4	W3
I/O	-	-	-	P122	R4	V3	W1
I/O	-	P124	P144	P121	R3	U1	V3
I/O	-	P125	P145	P120	R2	U2	V5
GND	-	-	-	-	-	GND*	GND*
I/O	P96	P126	P146	P119	R1	U4	V4
I/O	P97	P127	P147	P118	P3	U3	V2
I/O (D4)	P98	P128	P148	P117	P2	T1	U5
I/O	P99	P129	P149	P116	P1	T2	U4

XC4052XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
VCC	P100	P130	P150	P115	VCC*	VCC*	VCC*
GND	P101	P131	P151	P114	GND*	GND*	GND*
I/O (D3)	P102	P132	P152	P113	N2	T3	U3
I/O (/RS)	P103	P133	P153	P112	N4	R1	T2
I/O	P104	P134	P154	P111	N3	R2	T4
I/O	P105	P135	P155	P110	M1	R4	R1
GND	-	-	-	-	-	GND*	GND*
I/O	-	P136	P156	P109	M2	R3	R3
I/O	-	P137	P157	P108	M3	P2	R4
I/O	-	-	-	P107	M4	P3	R5
I/O	-	-	-	P106	L1	P4	P2
I/O	-	-	-	-	-	N1	P3
I/O	-	-	-	-	-	N2	P4
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	P158	-	GND*	GND*	GND*
I/O	-	-	-	P105	L2	N3	N1
I/O	-	-	-	P104	L3	N4	P5
I/O	-	-	-	-	K2	M1	N2
I/O	-	-	-	-	L4	M2	N3
I/O	-	-	-	-	-	M3	N5
I/O	-	-	-	-	-	M4	M3
GND	-	-	-	-	-	GND*	GND*
I/O (D2)	P106	P138	P159	P103	J1	L2	M4
I/O	P107	P139	P160	P102	K3	L3	L1
VCC	-	-	P161	P101	VCC*	VCC*	VCC*
I/O	P108	P140	P162	P99	J2	K1	K2
I/O, FCLK4	P109	P141	P163	P98	J3	K2	L4
I/O	-	-	P164	P97	K4	K3	J1
I/O	-	-	P165	P96	G1	K4	K3
GND	P110	P142	P166	P95	GND*	GND*	GND*
I/O	-	-	-	P94	H2	J2	L5
I/O	-	-	-	P93	H3	J3	J2
I/O	-	-	P167	P92	J4	J4	K4
I/O	-	-	P168	P91	F1	H1	J3
GND	-	-	-	-	-	GND*	GND*
I/O	-	P143	P169	P90	G2	H2	G1
I/O	-	P144	P170	P89	G3	H3	F1
I/O	P111	P145	P171	P88	F2	H4	J5
I/O	P112	P146	P172	P87	E2	G2	G3
I/O	-	-	-	-	-	G3	H4
I/O	-	-	-	-	-	F1	F2
GND	-	-	-	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O (D1)	P113	P147	P173	P86	F3	G4	F3
I/O (/RCK, RDY_/BUSY)	P114	P148	P174	P85	G4	F2	G4
I/O	-	-	-	-	D1	F3	D2
I/O	-	-	-	-	C1	E1	E3
I/O	-	-	-	-	-	F4	G5
I/O	-	-	-	-	-	E2	C1
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	P84	D2	E3	F4
I/O	-	-	-	P83	F4	D1	D3
I/O	P115	P149	P175	P82	E3	E4	B3
I/O	P116	P150	P176	P81	C2	D2	F5
I/O (D0, DIN)	P117	P151	P177	P80	D3	C2	E4

XC4052XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
I/O, GCK6 (DOUT)	P118	P152	P178	P79	E4	D3	D4
CCLK	P119	P153	P179	P78	C3	D4	C4
VCC	P120	P154	P180	P77	VCC*	VCC*	VCC*
O, TDO	P121	P159	P181	P76	D4	C4	E6
GND	P122	P160	P182	P75	GND*	GND*	GND*
I/O (A0, /WS)	P123	P161	P183	P74	B3	B3	D5
I/O, GCK7 (A1)	P124	P162	P184	P73	C4	D5	A2
I/O	P125	P163	P185	P72	D5	B4	D6
I/O	P126	P164	P186	P71	A3	C5	A3
I/O	-	-	-	-	-	A4	E7
I/O	-	-	-	-	-	D6	C5
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	C5	B5	B4
I/O	-	-	-	-	B4	C6	D7
I/O, (CS1, A2)	P127	P165	P187	P70	D6	A5	C6
I/O (A3)	P128	P166	P188	P69	C6	D7	E8
I/O	-	-	-	P68	B5	B6	B5
I/O	-	-	-	P67	A4	A6	A5
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	P189	P66	C7	D8	D8
I/O	-	-	P190	P65	B6	C7	C7
I/O	P129	P167	P191	P64	A6	B7	E9
I/O	P130	P168	P192	P63	D8	D9	A6
I/O	-	-	-	-	C8	B8	B7
I/O	-	-	-	-	-	A8	D9
GND	-	-	-	-	-	GND*	GND*
I/O	-	P169	P193	P62	B7	D10	E11
I/O	-	P170	P194	P61	A7	C9	A9
I/O	-	-	P195	P60	D9	B9	C10
I/O	-	-	-	P59	C9	C10	D11
GND	P131	P171	P196	P58	GND*	GND*	GND*
I/O	P132	P172	P197	P57	B8	B10	B10
I/O	P133	P173	P198	P56	D10	A10	E12
I/O	-	-	P199	P55	C10	C11	C11
I/O	-	-	P200	P54	B9	D12	B11
VCC	-	-	P201	P52	VCC*	VCC*	VCC*
I/O	-	-	-	P51	A9	B11	D12
I/O	-	-	-	P50	D11	C12	A11
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	D13	C13
I/O	-	-	-	-	-	B12	E14
I/O	-	-	-	-	C11	C13	A13
I/O	-	-	-	-	B10	A12	D14
I/O	-	-	-	P49	B11	D14	C14
I/O	-	-	-	P48	A11	B13	B14
GND	-	-	-	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O (A4)	P134	P174	P202	P47	D12	C14	E15
I/O (A5)	P135	P175	P203	P46	C12	A13	D15
I/O	-	P176	P205	P45	B12	B14	C15
I/O	P136	P177	P206	P44	A12	D15	A15
I/O (A21)	P137	P178	P207	P43	C13	C15	C16
I/O (A20)	P138	P179	P208	P42	B13	B15	E16
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	A15	B17

XC4052XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
I/O	-	-	-	-	-	C16	C17
I/O (A6)	P139	P180	P209	P41	A13	B16	E17
I/O (A7)	P140	P181	P210	P40	B14	A16	D17
GND	P141	P182	P211	P39	GND*	GND*	GND*
VCC	-	-	-	-	A10	A1	A4
VCC	-	-	-	-	A17	A11	A10
VCC	-	-	-	-	AC14	A21	A16
VCC	-	-	-	-	AC20	A31	A22
VCC	-	-	-	-	AC8	D11	A26
VCC	-	-	-	-	AF10	D21	A30
VCC	-	-	-	-	AF17	L1	B2
VCC	-	-	-	-	D7	L4	B13
VCC	-	-	-	-	D13	L28	B19
VCC	-	-	-	-	D19	L31	B32
VCC	-	-	-	-	G23	AA1	C3
VCC	-	-	-	-	H4	AA4	C32
VCC	-	-	-	-	K1	AA28	D1
VCC	-	-	-	-	K26	AA31	D33
VCC	-	-	-	-	N23	AH11	H1
VCC	-	-	-	-	P4	AH21	K33
VCC	-	-	-	-	U1	AL1	M1
VCC	-	-	-	-	U26	AL11	N32
VCC	-	-	-	-	W23	AL21	R2
VCC	-	-	-	-	Y4	AL31	T33
VCC	-	-	-	-	B2	-	V1
VCC	-	-	-	-	B25	-	W32
VCC	-	-	-	-	AE2	-	AA2
VCC	-	-	-	-	AE25	-	AB33
VCC	-	-	-	-	-	-	AD1
VCC	-	-	-	-	-	-	AF33
VCC	-	-	-	-	-	-	AK1
VCC	-	-	-	-	-	-	AK33
VCC	-	-	-	-	-	-	AL2
VCC	-	-	-	-	-	-	AL3
VCC	-	-	-	-	-	-	AM2
VCC	-	-	-	-	-	-	AM15
VCC	-	-	-	-	-	-	AM21
VCC	-	-	-	-	-	-	AM32
VCC	-	-	-	-	-	-	AN4
VCC	-	-	-	-	-	-	AN8
VCC	-	-	-	-	-	-	AN12
VCC	-	-	-	-	-	-	AN18
VCC	-	-	-	-	-	-	AN24
VCC	-	-	-	-	-	-	AN30
VCC	-	-	-	-	-	C3	AL31
VCC	-	-	-	-	-	C29	E5
VCC	-	-	-	-	-	AJ3	C31
VCC	-	-	-	-	-	AJ29	AK4
GND	-	-	-	-	A1	A2	A7
GND	-	-	-	-	A14	A3	A12
GND	-	-	-	-	A19	A7	A14
GND	-	-	-	-	A2	A9	A18
GND	-	-	-	-	A22	A14	A20
GND	-	-	-	-	A25	A18	A24
GND	-	-	-	-	A26	A23	A29
GND	-	-	-	-	A5	A25	A32

XC4052XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
GND	-	-	-	-	A8	A29	B1
GND	-	-	-	-	AB1	A30	B6
GND	-	-	-	-	AB26	B1	B9
GND	-	-	-	-	AE1	B2	B15
GND	-	-	-	-	AE26	B30	B23
GND	-	-	-	-	AF1	B31	B27
GND	-	-	-	-	AF13	C1	B31
GND	-	-	-	-	AF19	C31	C2
GND	-	-	-	-	AF2	D16	E1
GND	-	-	-	-	AF22	G1	F32
GND	-	-	-	-	AF25	G31	G2
GND	-	-	-	-	AF26	J1	G33
GND	-	-	-	-	AF5	J31	J32
GND	-	-	-	-	AF8	P1	K1
GND	-	-	-	-	B1	P31	L2
GND	-	-	-	-	B26	T4	M33
GND	-	-	-	-	E1	T28	P1
GND	-	-	-	-	E26	V1	P33
GND	-	-	-	-	H1	V31	R32
GND	-	-	-	-	H26	AC1	T1
GND	-	-	-	-	N1	AC31	V33
GND	-	-	-	-	P26	AE1	W2
GND	-	-	-	-	W1	AE31	Y1
GND	-	-	-	-	W26	AH16	Y33
GND	-	-	-	-	-	AJ1	AB1
GND	-	-	-	-	-	AJ31	AC32
GND	-	-	-	-	-	AK1	AD33
GND	-	-	-	-	-	AK2	AE2
GND	-	-	-	-	-	AK30	AG1
GND	-	-	-	-	-	AK31	AG32
GND	-	-	-	-	-	AL2	AH2
GND	-	-	-	-	-	AL3	AJ33
GND	-	-	-	-	-	AL7	AL32
GND	-	-	-	-	-	AL9	AM3
GND	-	-	-	-	-	AL14	AM11
GND	-	-	-	-	-	AL18	AM19
GND	-	-	-	-	-	AL23	AM25
GND	-	-	-	-	-	AL25	AM28
GND	-	-	-	-	-	AL29	AM33
GND	-	-	-	-	-	AL30	AM7
GND	-	-	-	-	-	-	AN2
GND	-	-	-	-	-	-	AN5
GND	-	-	-	-	-	-	AN10
GND	-	-	-	-	-	-	AN14
GND	-	-	-	-	-	-	AN16
GND	-	-	-	-	-	-	AN20
GND	-	-	-	-	-	-	AN22
GND	-	-	-	-	-	-	AN27
GND	-	-	P219	-	-	-	-
GND	-	-	P204	-	-	-	-
NC	-	P1	-	P11	-	C8	A28
NC	-	P3	-	P24	-	-	A27
NC	-	P51	-	P53	-	-	D25
NC	-	P52	-	P100	-	-	C26
NC	-	P53	-	P128	-	-	A23
NC	-	P54	-	P176	-	-	D22

XC4052XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
NC	-	P102	-	P205	-	-	C22
NC	-	P104	-	P254	-	-	E21
NC	-	P105	-	P281	-	-	D13
NC	-	P107	-	-	-	-	B12
NC	-	P155	-	-	-	-	C12
NC	-	P156	-	-	-	-	E13
NC	-	P157	-	-	-	-	A8
NC	-	P158	-	-	-	-	B8
NC	-	P206		-	-	-	E10
NC	-	P207	-	-	-	-	C8
NC	-	P208	-	-	-	-	H5
NC	-	-	-	-	-	-	E2
NC	-	-	-	-	-	-	J4
NC	-	-	-	-	-	-	H3
NC	-	-	-	-	-	-	M5
NC	-	-	-	-	-	-	L3
NC	-	-	-	-	-	-	M2
NC	-	-	-	-	-	-	N4
NC	-	-	-	-	-	-	Y4
NC	-	-	-	-	-	-	AA1
NC	-	-	-	-	-	-	AC1
NC	-	-	-	-	-	-	AB4
NC	-	-	-	-	-	-	AF2
NC	-	-	-	-	-	-	AD5
NC	-	-	-	-	-	-	AG2
NC	-	-	-	-	-	-	AE4
NC	-	-	-	-	-	-	AL8
NC	-	-	-	-	-	-	AK9
NC	-	-	-	-	-	-	AM8
NC	-	-	-	-	-	-	AJ10
NC	-	-	-	-	-	-	AL12
NC	-	-	-	-	-	-	AM12
NC	-	-	-	-	-	-	AJ13
NC	-	-	-	-	-	-	AK13
NC	-	-	-	-	-	-	AN23
NC	-	-	-	-	-	-	AL22
NC	-	-	-	-	-	-	AJ21
NC	-	-	-	-	-	-	AM23
NC	-	-	-	-	-	-	AM27
NC	-	-	-	-	-	-	AJ24
NC	-	-	-	-	-	-	AL26
NC	-	-	-	-	-	-	AK25
NC	-	-	-	-	-	-	AE30
NC	-	-	-	-	-	-	AF31
NC	-	-	-	-	-	-	AD29
NC	-	-	-	-	-	-	AF32
NC	-	-	-	-	-	-	AC33
NC	-	-	-	-	-	-	AB30
NC	-	-	-	-	-	-	Y29
NC	-	-	-	-	-	-	AA33
NC	-	-	-	-	-	-	N31
NC	-	-	-	-	-	-	N30
NC	-	-	-	-	-	-	M30
NC	-	-	-	-	-	-	L31
NC	-	-	-	-	-	-	K29
NC	-	-	-	-	-	-	H31
NC	-	-	-	-	-	-	E33

XC4052XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
NC	-	-	-	-	-	-	E32
NC	-	-	-	-	-	-	AC2
NC	-	-	-	-	-	-	A1
NC	-	-	-	-	-	-	A33
NC	-	-	-	-	-	-	AN1
NC	-	-	-	-	-	-	AN33
NC	-	-	-	-	-	-	A19
NC	-	-	-	-	-	-	D18
NC	-	-	-	-	-	-	E24
NC	-	-	-	-	-	-	B26
NC	-	-	-	-	-	-	K5
NC	-	-	-	-	-	-	H2
NC	-	-	-	-	-	-	B16
NC	-	-	-	-	-	-	D16
NC	-	-	-	-	-	-	T5
NC	-	-	-	-	-	-	T3
NC	-	-	-	-	-	-	U1
NC	-	-	-	-	-	-	U2
NC	-	-	-	-	-	-	AD4
NC	-	-	-	-	-	-	AF1
NC	-	-	-	-	-	-	AL9
NC	-	-	-	-	-	-	AM9
NC	-	-	-	-	-	-	AL16
NC	-	-	-	-	-	-	AJ16
NC	-	-	-	-	-	-	AK18
NC	-	-	-	-	-	-	AJ18
NC	-	-	-	-	-	-	AK24
NC	-	-	-	-	-	-	AM26
NC	-	-	-	-	-	-	AE31
NC	-	-	-	-	-	-	AD30
NC	-	-	-	-	-	-	V32
NC	-	-	-	-	-	-	U33
NC	-	-	-	-	-	-	T32
NC	-	-	-	-	-	-	T30
NC	-	-	-	-	-	-	J31
NC	-	-	-	-	-	-	H32
NC	-	-	-	-	-	-	C9
NC	-	-	-	-	-	-	D10

12/18/98

XC4062XLA Pinout Table

XC4062XLA Pinout Table

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
VCC	P142	P183	P212	P38	VCC*	VCC*	VCC*
I/O (A8)	P143	P184	P213	P37	D14	D17	A17
I/O (A9)	P144	P185	P214	P36	C14	A17	B18
I/O	-	-	-	-	-	C17	C18
I/O	-	-	-	-	-	B17	E18
I/O	-	-	-	-	-	-	D18
I/O	-	-	-	-	-	-	A19
GND	-	-	-	-	-	GND*	GND*
I/O (A19)	P145	P186	P215	P35	A15	C18	C19
I/O (A18)	P146	P187	P216	P34	B15	D18	D19
I/O	-	P188	P217	P33	C15	B18	E19
I/O	-	P189	P218	P32	D15	A19	B20
I/O (A10)	P147	P190	P220	P31	A16	B19	C20
I/O (A11)	P148	P191	P221	P30	B16	C19	D20
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	P29	C16	D19	A21
I/O	-	-	-	P28	B17	A20	E20
I/O	-	-	-	-	D16	B20	B21
I/O	-	-	-	-	A18	C20	C21
I/O	-	-	-	-	-	B21	D21
I/O	-	-	-	-	-	D20	B22
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	P27	C17	C21	C23
I/O	-	-	-	P26	B18	A22	E22
VCC	-	-	P222	P25	VCC*	VCC*	VCC*
I/O	-	-	P223	P23	C18	B22	B24
I/O	-	-	P224	P22	D17	C22	D23
I/O	P149	P192	P225	P21	A20	B23	C24
I/O	P150	P193	P226	P20	B19	A24	A25
GND	P151	P194	P227	P19	GND*	GND*	GND*
I/O	-	-	-	P18	C19	D22	E23
I/O	-	-	-	P17	D18	C23	B25
I/O	-	P195	P228	P16	A21	B24	D24
I/O	-	P196	P229	P15	B20	C24	C25
I/O	-	-	-	-	-	-	B26
I/O	-	-	-	-	-	-	E24
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	D23	E25
I/O	-	-	-	-	-	B25	C27
I/O	P152	P197	P230	P14	C20	A26	D26
I/O	P153	P198	P231	P13	B21	C25	B28
I/O (A12)	P154	P199	P232	P12	B22	D24	B29
I/O (A13)	P155	P200	P233	P10	C21	B26	E26
GND	-	-	-	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	P9	D20	A27	C28
I/O	-	-	-	P8	A23	D25	D27
I/O	-	-	-	-	A24	C26	B30
I/O	-	-	-	-	B23	B27	C29
I/O	-	-	-	-	-	A28	E27
I/O	-	-	-	-	-	D26	A31
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	P234	P7	D21	C27	D28
I/O	-	-	P235	P6	C22	B28	C30

XC4062XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
I/O	P156	P201	P236	P5	B24	D27	D29
I/O	P157	P202	P237	P4	C23	B29	E28
I/O (A14)	P158	P203	P238	P3	D22	C28	D30
I/O, GCK8 (A15)	P159	P204	P239	P2	C24	D28	E29
VCC	P160	P205	P240	P1	VCC*	VCC*	VCC*
GND	P1	P2	P1	P304	GND*	GND*	GND*
I/O, GCK1 (A16)	P2	P4	P2	P303	D23	D29	B33
I/O (A17)	P3	P5	P3	P302	C25	C30	F29
I/O	P4	P6	P4	P301	D24	E28	E30
I/O	P5	P7	P5	P300	E23	E29	D31
I/O (TDI)	P6	P8	P6	P299	C26	D30	F30
I/O (TCK)	P7	P9	P7	P298	E24	D31	C33
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	F28	G29
I/O	-	-	-	-	-	F29	E31
I/O	-	-	-	-	D25	E30	D32
I/O	-	-	-	-	F23	E31	G30
I/O	-	-	-	P297	F24	G28	F31
I/O	-	-	-	P296	E25	G29	H29
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	-	-	F30	H30
I/O	-	-	-	-	-	F31	G31
I/O	P8	P10	P8	P295	D26	H28	J29
I/O	P9	P11	P9	P294	G24	H29	F33
I/O	-	P12	P10	P293	F25	G30	G32
I/O	-	P13	P11	P292	F26	H30	J30
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	-	H32
I/O	-	-	-	-	-	-	J31
I/O	-	-	P12	P291	H23	J28	K30
I/O	-	-	P13	P290	H24	J29	H33
I/O	-	-	-	P289	G25	H31	L29
I/O	-	-	-	P288	G26	J30	K31
GND	P10	P14	P14	P287	GND*	GND*	GND*
I/O, FCLK1	P11	P15	P15	P286	J23	K28	L30
I/O	P12	P16	P16	P285	J24	K29	K32
I/O (TMS)	P13	P17	P17	P284	H25	K30	J33
I/O	P14	P18	P18	P283	K23	K31	M29
VCC	-	-	P19	P282	VCC*	VCC*	VCC*
I/O	-	-	P20	P280	K24	L29	L32
I/O	-	-	P21	P279	J25	L30	M31
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	M30	N29
I/O	-	-	-	-	-	M28	L33
I/O	-	-	-	-	J26	M29	M32
I/O	-	-	-	-	L23	M31	P29
I/O	-	-	-	P278	L24	N31	P30
I/O	-	-	-	P277	K25	N28	N33
GND	-	-	P22	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	-	-	N29	P31
I/O	-	-	-	-	-	N30	P32
I/O	-	-	-	P276	L25	P30	R29
I/O	-	-	-	P275	L26	P28	R30
I/O	-	P19	P23	P274	M23	P29	R31
I/O	-	P20	P24	P273	M24	R31	R33

XC4062XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
GND	-	-	-	-	-	GND*	GND*
I/O	P15	P21	P25	P272	M25	R30	T31
I/O	P16	P22	P26	P271	M26	R28	T29
I/O	-	-	-	-	-	-	T30
I/O	-	-	-	-	-	-	T32
I/O	P17	P23	P27	P270	N24	R29	U32
I/O	P18	P24	P28	P269	N25	T31	U31
GND	P19	P25	P29	P268	GND*	GND*	GND*
VCC	P20	P26	P30	P267	VCC*	VCC*	VCC*
I/O	P21	P27	P31	P266	N26	T30	U29
I/O	P22	P28	P32	P265	P25	T29	U30
I/O	-	-	-	-	-	-	U33
I/O	-	-	-	-	-	-	V32
I/O	P23	P29	P33	P264	P23	U31	V31
I/O	P24	P30	P34	P263	P24	U30	V29
GND	-	-	-	-	-	GND*	GND*
I/O	-	P31	P35	P262	R26	U28	V30
I/O	-	P32	P36	P261	R25	U29	W33
I/O	-	-	-	P260	R24	V30	W31
I/O	-	-	-	P259	R23	V29	W30
I/O	-	-	-	-	-	V28	W29
I/O	-	-	-	-	-	W31	Y32
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	P37	-	GND*	GND*	GND*
I/O	-	-	-	P258	T26	W30	Y31
I/O	-	-	-	P257	T25	W29	Y30
I/O	-	-	-	-	-	W28	AA32
I/O	-	-	-	-	-	Y31	AA31
I/O	-	-	-	-	T24	Y30	AA30
I/O	-	-	-	-	U25	Y29	AB32
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	P38	P256	T23	Y28	AA29
I/O	-	-	P39	P255	V26	AA30	AB31
VCC	-	-	P40	P253	VCC*	VCC*	VCC*
I/O	P25	P33	P41	P252	U24	AA29	AC31
I/O	P26	P34	P42	P251	V25	AB31	AB29
I/O	P27	P35	P43	P250	V24	AB30	AD32
I/O, FCLK2	P28	P36	P44	P249	U23	AB29	AC30
GND	P29	P37	P45	P248	GND*	GND*	GND*
I/O	-	-	-	P247	Y26	AB28	AD31
I/O	-	-	-	P246	W25	AC30	AE33
I/O	-	-	P46	P245	W24	AC29	AC29
I/O	-	-	P47	P244	V23	AC28	AE32
I/O	-	-	-	-	-	-	AD30
I/O	-	-	-	-	-	-	AE31
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	AD31	AG33
I/O	-	-	-	-	-	AD30	AH33
I/O	-	P38	P48	P243	AA26	AD29	AE29
I/O	-	P39	P49	P242	Y25	AD28	AG31
I/O	P30	P40	P50	P241	Y24	AE30	AF30
I/O	P31	P41	P51	P240	AA25	AE29	AH32
GND	-	-	-	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	P239	AB25	AF31	AJ32
I/O	-	-	-	P238	AA24	AE28	AF29
I/O	-	-	-	-	-	AF30	AH31

XC4062XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
I/O	-	-	-	-	-	AF29	AG30
I/O	P32	P42	P52	P237	Y23	AG31	AK32
I/O	P33	P43	P53	P236	AC26	AF28	AJ31
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	AD26	AG30	AG29
I/O	-	-	-	-	AC25	AG29	AL33
I/O	P34	P44	P54	P235	AA23	AH31	AH30
I/O	P35	P45	P55	P234	AB24	AG28	AK31
I/O	P36	P46	P56	P233	AD25	AH30	AJ30
I/O, GCK2	P37	P47	P57	P232	AC24	AJ30	AH29
O (M1)	P38	P48	P58	P231	AB23	AH29	AK30
GND	P39	P49	P59	P230	GND*	GND*	GND*
I (M0)	P40	P50	P60	P229	AD24	AH28	AJ29
VCC	P41	P55	P61	P228	VCC*	VCC*	VCC*
I (M2)	P42	P56	P62	P227	AC23	AJ28	AN32
I/O, GCK3	P43	P57	P63	P226	AE24	AK29	AJ28
I/O (HDC)	P44	P58	P64	P225	AD23	AH27	AK29
I/O	P45	P59	P65	P224	AC22	AK28	AL30
I/O	P46	P60	P66	P223	AF24	AJ27	AK28
I/O	P47	P61	P67	P222	AD22	AL28	AM31
I/O (/LDC)	P48	P62	P68	P221	AE23	AH26	AJ27
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	AK27	AN31
I/O	-	-	-	-	-	AJ26	AL29
I/O	-	-	-	-	AC21	AL27	AK27
I/O	-	-	-	-	AD21	AH25	AL28
I/O	-	-	-	P220	AE22	AK26	AJ26
I/O	-	-	-	P219	AF23	AL26	AM30
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	-	GND*	GND*	GND*
I/O	P49	P63	P69	P218	AD20	AH24	AM29
I/O	P50	P64	P70	P217	AE21	AJ25	AK26
I/O	-	P65	P71	P216	AF21	AK25	AL27
I/O	-	P66	P72	P215	AC19	AJ24	AJ25
I/O	-	-	-	-	-	AH23	AN29
I/O	-	-	-	-	-	AK24	AN28
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	-	AM26
I/O	-	-	-	-	-	-	AK24
I/O	-	-	P73	P214	AD19	AL24	AL25
I/O	-	-	P74	P213	AE20	AH22	AJ23
I/O	-	-	-	P212	AF20	AJ23	AN26
I/O	-	-	-	P211	AC18	AK23	AL24
GND	P51	P67	P75	P210	GND*	GND*	GND*
I/O	P52	P68	P76	P209	AD18	AJ22	AK23
I/O	P53	P69	P77	P208	AE19	AK22	AN25
I/O	P54	P70	P78	P207	AC17	AL22	AJ22
I/O	P55	P71	P79	P206	AD17	AJ21	AL23
VCC	-	-	P80	P204	VCC*	VCC*	VCC*
I/O	-	P72	P81	P203	AE18	AH20	AM24
I/O	-	P73	P82	P202	AF18	AK21	AK22
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	AJ20	AK21
I/O	-	-	-	-	-	AH19	AM22
I/O	-	-	-	-	AC16	AK20	AJ20
I/O	-	-	-	-	AD16	AJ19	AL21
I/O	-	-	-	P201	AE17	AL20	AN21

XC4062XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
I/O	-	-	-	P200	AE16	AH18	AK20
GND	-	-	P83	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	P199	AF16	AK19	AL20
I/O	-	-	-	P198	AC15	AJ18	AJ19
I/O	-	-	P84	P197	AD15	AL19	AM20
I/O	-	-	P85	P196	AE15	AK18	AK19
I/O	P56	P74	P86	P195	AF15	AH17	AL19
I/O	P57	P75	P87	P194	AD14	AJ17	AN19
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	-	AJ18
I/O	-	-	-	-	-	-	AK18
I/O	-	-	-	-	-	AK17	AL18
I/O	-	-	-	-	-	AL17	AM18
I/O	P58	P76	P88	P193	AE14	AJ16	AK17
I/O (/INIT)	P59	P77	P89	P192	AF14	AK16	AJ17
VCC	P60	P78	P90	P191	VCC*	VCC*	VCC*
GND	P61	P79	P91	P190	GND*	GND*	GND*
I/O	P62	P80	P92	P189	AE13	AL16	AL17
I/O	P63	P81	P93	P188	AC13	AH15	AM17
I/O	-	-	-	-	-	AL15	AN17
I/O	-	-	-	-	-	AJ15	AK16
I/O	-	-	-	-	-	-	AJ16
I/O	-	-	-	-	-	-	AL16
GND	-	-	-	-	-	GND*	GND*
I/O	P64	P82	P94	P187	AD13	AK15	AM16
I/O	P65	P83	P95	P186	AF12	AJ14	AL15
I/O	-	P84	P96	P185	AE12	AH14	AK15
I/O	-	P85	P97	P184	AD12	AK14	AJ15
I/O	-	-	-	P183	AC12	AL13	AN15
I/O	-	-	-	P182	AF11	AK13	AM14
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	P98	-	GND*	GND*	GND*
I/O	-	-	-	P181	AE11	AJ13	AL14
I/O	-	-	-	P180	AD11	AH13	AK14
I/O	-	-	-	-	AE10	AL12	AJ14
I/O	-	-	-	-	AC11	AK12	AN13
I/O	-	-	-	-	-	AJ12	AM13
I/O	-	-	-	-	-	AK11	AL13
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	P99	P179	AF9	AH12	AK12
I/O	-	-	P100	P178	AD10	AJ11	AN11
VCC	-	-	P101	P177	VCC*	VCC*	VCC*
I/O	P66	P86	P102	P175	AE9	AL10	AJ12
I/O	P67	P87	P103	P174	AD9	AK10	AL11
I/O	P68	P88	P104	P173	AC10	AJ10	AK11
I/O	P69	P89	P105	P172	AF7	AK9	AM10
GND	P70	P90	P106	P171	GND*	GND*	GND*
I/O	-	-	-	P170	AE8	AL8	AL10
I/O	-	-	-	P169	AD8	AH10	AJ11
I/O	-	-	P107	P168	AC9	AJ9	AN9
I/O	-	-	P108	P167	AF6	AK8	AK10
I/O	-	-	-	-	-	-	AM9
I/O	-	-	-	-	-	-	AL9
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	AJ8	AN7
I/O	-	-	-	-	-	AH9	AJ9

XC4062XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
I/O	-	P91	P109	P166	AE7	AK7	AL7
I/O	-	P92	P110	P165	AD7	AL6	AK8
I/O	P71	P93	P111	P164	AE6	AJ7	AN6
I/O	P72	P94	P112	P163	AE5	AH8	AM6
GND	-	-	-	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	P162	AD6	AK6	AJ8
I/O	-	-	-	P161	AC7	AL5	AL6
I/O	P73	P95	P113	P160	AF4	AH7	AK7
I/O	P74	P96	P114	P159	AF3	AJ6	AM5
I/O	-	-	-	-	AE4	AK5	AM4
I/O	-	-	-	-	AC6	AL4	AJ7
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	AH6	AL5
I/O	-	-	-	-	-	AJ5	AK6
I/O	P75	P97	P115	P158	AD5	AK4	AN3
I/O	P76	P98	P116	P157	AE3	AH5	AK5
I/O	P77	P99	P117	P156	AD4	AK3	AJ6
I/O, GCK4	P78	P100	P118	P155	AC5	AJ4	AL4
GND	P79	P101	P119	P154	GND*	GND*	GND*
DONE	P80	P103	P120	P153	AD3	AH4	AJ5
VCC	P81	P106	P121	P152	VCC*	VCC*	VCC*
/PROGRAM	P82	P108	P122	P151	AC4	AH3	AM1
I/O (D7)	P83	P109	P123	P150	AD2	AJ2	AH5
I/O, GCK5	P84	P110	P124	P149	AC3	AG4	AJ4
I/O	P85	P111	P125	P148	AB4	AG3	AK3
I/O	P86	P112	P126	P147	AD1	AH2	AH4
I/O	-	-	-	-	AB3	AH1	AL1
I/O	-	-	-	-	AC2	AF4	AG5
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	P127	P146	AA4	AF3	AJ3
I/O	-	-	P128	P145	AA3	AG2	AK2
I/O	-	-	-	-	-	AG1	AG4
I/O	-	-	-	-	-	AE4	AH3
I/O	-	-	-	P144	AB2	AE3	AF5
I/O	-	-	-	P143	AC1	AF2	AJ2
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	-	GND*	GND*	GND*
I/O (D6)	P87	P113	P129	P142	Y3	AF1	AJ1
I/O	P88	P114	P130	P141	AA2	AD4	AF4
I/O	P89	P115	P131	P140	AA1	AD3	AG3
I/O	P90	P116	P132	P139	W4	AE2	AE5
I/O	-	-	-	-	-	AD2	AH1
I/O	-	-	-	-	-	AC4	AF3
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	-	AF1
I/O	-	-	-	-	-	-	AD4
I/O	-	P117	P133	P138	W3	AC3	AE3
I/O	-	P118	P134	P137	Y2	AD1	AC5
I/O	-	-	-	P136	Y1	AC2	AE1
I/O	-	-	-	P135	V4	AB4	AD3
GND	P91	P119	P135	P134	GND*	GND*	GND*
I/O	-	-	P136	P133	V3	AB3	AC4
I/O	-	-	P137	P132	W2	AB2	AD2
I/O, FCLK3	P92	P120	P138	P131	U4	AB1	AB5
I/O	P93	P121	P139	P130	U3	AA3	AC3
VCC	-	-	P140	P129	VCC*	VCC*	VCC*

XC4062XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
I/O (D5)	P94	P122	P141	P127	V2	AA2	AA5
I/O (/CS0)	P95	P123	P142	P126	V1	Y2	AB3
GND	-	-	P143*	-	-	GND*	GND*
I/O	-	-	-	-	T4	Y4	AB2
I/O	-	-	-	-	T3	Y3	AA4
I/O	-	-	-	-	-	Y1	AA3
I/O	-	-	-	-	-	W1	Y5
I/O	-	-	-	P125	U2	W4	Y3
I/O	-	-	-	P124	T2	W3	Y2
GND	-	-	-	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	-	-	W2	W5
I/O	-	-	-	-	-	V2	W4
I/O	-	-	-	P123	T1	V4	W3
I/O	-	-	-	P122	R4	V3	W1
I/O	-	P124	P144	P121	R3	U1	V3
I/O	-	P125	P145	P120	R2	U2	V5
GND	-	-	-	-	-	GND*	GND*
I/O	P96	P126	P146	P119	R1	U4	V4
I/O	P97	P127	P147	P118	P3	U3	V2
I/O	-	-	-	-	-	-	U2
I/O	-	-	-	-	-	-	U1
I/O (D4)	P98	P128	P148	P117	P2	T1	U5
I/O	P99	P129	P149	P116	P1	T2	U4
VCC	P100	P130	P150	P115	VCC*	VCC*	VCC*
GND	P101	P131	P151	P114	GND*	GND*	GND*
I/O (D3)	P102	P132	P152	P113	N2	T3	U3
I/O (/RS)	P103	P133	P153	P112	N4	R1	T2
I/O	-	-	-	-	-	-	T3
I/O	-	-	-	-	-	-	T5
I/O	P104	P134	P154	P111	N3	R2	T4
I/O	P105	P135	P155	P110	M1	R4	R1
GND	-	-	-	-	-	GND*	GND*
I/O	-	P136	P156	P109	M2	R3	R3
I/O	-	P137	P157	P108	M3	P2	R4
I/O	-	-	-	P107	M4	P3	R5
I/O	-	-	-	P106	L1	P4	P2
I/O	-	-	-	-	-	N1	P3
I/O	-	-	-	-	-	N2	P4
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	P158	-	GND*	GND*	GND*
I/O	-	-	-	P105	L2	N3	N1
I/O	-	-	-	P104	L3	N4	P5
I/O	-	-	-	-	K2	M1	N2
I/O	-	-	-	-	L4	M2	N3
I/O	-	-	-	-	-	M3	N5
I/O	-	-	-	-	-	M4	M3
GND	-	-	-	-	-	GND*	GND*
I/O (D2)	P106	P138	P159	P103	J1	L2	M4
I/O	P107	P139	P160	P102	K3	L3	L1
VCC	-	-	P161	P101	VCC*	VCC*	VCC*
I/O	P108	P140	P162	P99	J2	K1	K2
I/O, FCLK4	P109	P141	P163	P98	J3	K2	L4
I/O	-	-	P164	P97	K4	K3	J1
I/O	-	-	P165	P96	G1	K4	K3
GND	P110	P142	P166	P95	GND*	GND*	GND*
I/O	-	-	-	P94	H2	J2	L5

XC4062XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
I/O	-	-	-	P93	H3	J3	J2
I/O	-	-	P167	P92	J4	J4	K4
I/O	-	-	P168	P91	F1	H1	J3
I/O	-	-	-	-	-	-	H2
I/O	-	-	-	-	-	-	K5
GND	-	-	-	-	-	GND*	GND*
I/O	-	P143	P169	P90	G2	H2	G1
I/O	-	P144	P170	P89	G3	H3	F1
I/O	P111	P145	P171	P88	F2	H4	J5
I/O	P112	P146	P172	P87	E2	G2	G3
I/O	-	-	-	-	-	G3	H4
I/O	-	-	-	-	-	F1	F2
GND	-	-	-	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O (D1)	P113	P147	P173	P86	F3	G4	F3
I/O (/RCK, RDY_/BUSY)	P114	P148	P174	P85	G4	F2	G4
I/O	-	-	-	-	D1	F3	D2
I/O	-	-	-	-	C1	E1	E3
I/O	-	-	-	-	-	F4	G5
I/O	-	-	-	-	-	E2	C1
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	P84	D2	E3	F4
I/O	-	-	-	P83	F4	D1	D3
I/O	P115	P149	P175	P82	E3	E4	B3
I/O	P116	P150	P176	P81	C2	D2	F5
I/O (D0, DIN)	P117	P151	P177	P80	D3	C2	E4
I/O, GCK6 (DOUT)	P118	P152	P178	P79	E4	D3	D4
CCLK	P119	P153	P179	P78	C3	D4	C4
VCC	P120	P154	P180	P77	VCC*	VCC*	VCC*
O, TDO	P121	P159	P181	P76	D4	C4	E6
GND	P122	P160	P182	P75	GND*	GND*	GND*
I/O (A0, /WS)	P123	P161	P183	P74	B3	B3	D5
I/O, GCK7 (A1)	P124	P162	P184	P73	C4	D5	A2
I/O	P125	P163	P185	P72	D5	B4	D6
I/O	P126	P164	P186	P71	A3	C5	A3
I/O	-	-	-	-	-	A4	E7
I/O	-	-	-	-	-	D6	C5
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	C5	B5	B4
I/O	-	-	-	-	B4	C6	D7
I/O, (CS1, A2)	P127	P165	P187	P70	D6	A5	C6
I/O (A3)	P128	P166	P188	P69	C6	D7	E8
I/O	-	-	-	P68	B5	B6	B5
I/O	-	-	-	P67	A4	A6	A5
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	P189	P66	C7	D8	D8
I/O	-	-	P190	P65	B6	C7	C7
I/O	P129	P167	P191	P64	A6	B7	E9
I/O	P130	P168	P192	P63	D8	D9	A6
I/O	-	-	-	-	C8	B8	B7
I/O	-	-	-	-	-	A8	D9
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	-	D10
I/O	-	-	-	-	-	-	C9

XC4062XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
I/O	-	P169	P193	P62	B7	D10	E11
I/O	-	P170	P194	P61	A7	C9	A9
I/O	-	-	P195	P60	D9	B9	C10
I/O	-	-	-	P59	C9	C10	D11
GND	P131	P171	P196	P58	GND*	GND*	GND*
I/O	P132	P172	P197	P57	B8	B10	B10
I/O	P133	P173	P198	P56	D10	A10	E12
I/O	-	-	P199	P55	C10	C11	C11
I/O	-	-	P200	P54	B9	D12	B11
VCC	-	-	P201	P52	VCC*	VCC*	VCC*
I/O	-	-	-	P51	A9	B11	D12
I/O	-	-	-	P50	D11	C12	A11
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	D13	C13
I/O	-	-	-	-	-	B12	E14
I/O	-	-	-	-	C11	C13	A13
I/O	-	-	-	-	B10	A12	D14
I/O	-	-	-	P49	B11	D14	C14
I/O	-	-	-	P48	A11	B13	B14
GND	-	-	-	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O (A4)	P134	P174	P202	P47	D12	C14	E15
I/O (A5)	P135	P175	P203	P46	C12	A13	D15
I/O	-	P176	P205	P45	B12	B14	C15
I/O	P136	P177	P206	P44	A12	D15	A15
I/O (A21)	P137	P178	P207	P43	C13	C15	C16
I/O (A20)	P138	P179	P208	P42	B13	B15	E16
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	-	D16
I/O	-	-	-	-	-	-	B16
I/O	-	-	-	-	-	A15	B17
I/O	-	-	-	-	-	C16	C17
I/O (A6)	P139	P180	P209	P41	A13	B16	E17
I/O (A7)	P140	P181	P210	P40	B14	A16	D17
GND	P141	P182	P211	P39	GND*	GND*	GND*
VCC	-	-	-	-	A10	A1	A4
VCC	-	-	-	-	A17	A11	A10
VCC	-	-	-	-	AC14	A21	A16
VCC	-	-	-	-	AC20	A31	A22
VCC	-	-	-	-	AC8	D11	A26
VCC	-	-	-	-	AF10	D21	A30
VCC	-	-	-	-	AF17	L1	B2
VCC	-	-	-	-	D7	L4	B13
VCC	-	-	-	-	D13	L28	B19
VCC	-	-	-	-	D19	L31	B32
VCC	-	-	-	-	G23	AA1	C3
VCC	-	-	-	-	H4	AA4	C32
VCC	-	-	-	-	K1	AA28	D1
VCC	-	-	-	-	K26	AA31	D33
VCC	-	-	-	-	N23	AH11	H1
VCC	-	-	-	-	P4	AH21	K33
VCC	-	-	-	-	U1	AL1	M1
VCC	-	-	-	-	U26	AL11	N32
VCC	-	-	-	-	W23	AL21	R2
VCC	-	-	-	-	Y4	AL31	T33
VCC	-	-	-	-	B2	-	V1
VCC	-	-	-	-	B25	-	W32

XC4062XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
VCC	-	-	-	-	AE2	-	AA2
VCC	-	-	-	-	AE25	-	AB33
VCC	-	-	-	-	-	-	AD1
VCC	-	-	-	-	-	-	AF33
VCC	-	-	-	-	-	-	AK1
VCC	-	-	-	-	-	-	AK33
VCC	-	-	-	-	-	-	AL2
VCC	-	-	-	-	-	-	AL3
VCC	-	-	-	-	-	-	AM2
VCC	-	-	-	-	-	-	AM15
VCC	-	-	-	-	-	-	AM21
VCC	-	-	-	-	-	-	AM32
VCC	-	-	-	-	-	-	AN4
VCC	-	-	-	-	-	-	AN8
VCC	-	-	-	-	-	-	AN12
VCC	-	-	-	-	-	-	AN18
VCC	-	-	-	-	-	-	AN24
VCC	-	-	-	-	-	-	AN30
VCC	-	-	-	-	-	C3	AL31
VCC	-	-	-	-	-	C29	E5
VCC	-	-	-	-	-	AJ3	C31
VCC	-	-	-	-	-	AJ29	AK4
GND	-	-	-	-	A1	A2	A7
GND	-	-	-	-	A14	A3	A12
GND	-	-	-	-	A19	A7	A14
GND	-	-	-	-	A2	A9	A18
GND	-	-	-	-	A22	A14	A20
GND	-	-	-	-	A25	A18	A24
GND	-	-	-	-	A26	A23	A29
GND	-	-	-	-	A5	A25	A32
GND	-	-	-	-	A8	A29	B1
GND	-	-	-	-	AB1	A30	B6
GND	-	-	-	-	AB26	B1	B9
GND	-	-	-	-	AE1	B2	B15
GND	-	-	-	-	AE26	B30	B23
GND	-	-	-	-	AF1	B31	B27
GND	-	-	-	-	AF13	C1	B31
GND	-	-	-	-	AF19	C31	C2
GND	-	-	-	-	AF2	D16	E1
GND	-	-	-	-	AF22	G1	F32
GND	-	-	-	-	AF25	G31	G2
GND	-	-	-	-	AF26	J1	G33
GND	-	-	-	-	AF5	J31	J32
GND	-	-	-	-	AF8	P1	K1
GND	-	-	-	-	B1	P31	L2
GND	-	-	-	-	B26	T4	M33
GND	-	-	-	-	E1	T28	P1
GND	-	-	-	-	E26	V1	P33
GND	-	-	-	-	H1	V31	R32
GND	-	-	-	-	H26	AC1	T1
GND	-	-	-	-	N1	AC31	V33
GND	-	-	-	-	P26	AE1	W2
GND	-	-	-	-	W1	AE31	Y1
GND	-	-	-	-	W26	AH16	Y33
GND	-	-	-	-	-	AJ1	AB1
GND	-	-	-	-	-	AJ31	AC32

XC4062XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
GND	-	-	-	-	-	AK1	AD33
GND	-	-	-	-	-	AK2	AE2
GND	-	-	-	-	-	AK30	AG1
GND	-	-	-	-	-	AK31	AG32
GND	-	-	-	-	-	AL2	AH2
GND	-	-	-	-	-	AL3	AJ33
GND	-	-	-	-	-	AL7	AL32
GND	-	-	-	-	-	AL9	AM3
GND	-	-	-	-	-	AL14	AM11
GND	-	-	-	-	-	AL18	AM19
GND	-	-	-	-	-	AL23	AM25
GND	-	-	-	-	-	AL25	AM28
GND	-	-	-	-	-	AL29	AM33
GND	-	-	-	-	-	AL30	AM7
GND	-	-	-	-	-	-	AN2
GND	-	-	-	-	-	-	AN5
GND	-	-	-	-	-	-	AN10
GND	-	-	-	-	-	-	AN14
GND	-	-	-	-	-	-	AN16
GND	-	-	-	-	-	-	AN20
GND	-	-	-	-	-	-	AN22
GND	-	-	-	-	-	-	AN27
GND	-	-	P204	-	-	-	-
GND	-	-	P219	-	-	-	-
NC	-	P1	-	P11	-	C8	A28
NC	-	P3	-	P24	-	-	A27
NC	-	P51		P53	-	-	D25
NC	-	P52	-	P100	-	-	C26
NC	-	P53	-	P128	-	-	A23
NC	-	P54	-	P176	-	-	D22
NC	-	P102	-	P205	-	-	C22
NC	-	P104	-	P254	-	-	E21
NC	-	P105	-	P281	-	-	D13
NC	-	P107	-	-	-	-	B12
NC	-	P155	-	-	-	-	C12
NC	-	P156	-	-	-	-	E13
NC	-	P157	-	-	-	-	A8
NC	-	P158	-	-	-	-	B8
NC	-	P206	-	-	-	-	E10
NC	-	P207	-	-	-	-	C8
NC	-	P208	-	-	-	-	H5
NC	-	-	-	-	-	-	E2
NC	-	-	-	-	-	-	J4
NC	-	-	-	-	-	-	H3
NC	-	-	-	-	-	-	M5
NC	-	-	-	-	-	-	L3
NC	-	-	-	-	-	-	M2
NC	-	-	-	-	-	-	N4
NC	-	-	-	-	-	-	Y4
NC	-	-	-	-	-	-	AA1
NC	-	-	-	-	-	-	AC1
NC	-	-	-	-	-	-	AB4
NC	-	-	-	-	-	-	AF2
NC	-	-	-	-	-	-	AD5
NC	-	-	-	-	-	-	AG2
NC	-	-	-	-	-	-	AE4

XC4062XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
NC	-	-	-	-	-	-	AL8
NC	-	-	-	-	-	-	AK9
NC	-	-	-	-	-	-	AM8
NC	-	-	-	-	-	-	AJ10
NC	-	-	-	-	-	-	AL12
NC	-	-	-	-	-	-	AM12
NC	-	-	-	-	-	-	AJ13
NC	-	-	-	-	-	-	AK13
NC	-	-	-	-	-	-	AN23
NC	-	-	-	-	-	-	AL22
NC	-	-	-	-	-	-	AJ21
NC	-	-	-	-	-	-	AM23
NC	-	-	-	-	-	-	AM27
NC	-	-	-	-	-	-	AJ24
NC	-	-	-	-	-	-	AL26
NC	-	-	-	-	-	-	AK25
NC	-	-	-	-	-	-	AE30
NC	-	-	-	-	-	-	AF31
NC	-	-	-	-	-	-	AD29
NC	-	-	-	-	-	-	AF32
NC	-	-	-	-	-	-	AC33
NC	-	-	-	-	-	-	AB30
NC	-	-	-	-	-	-	Y29
NC	-	-	-	-	-	-	AA33
NC	-	-	-	-	-	-	N31
NC	-	-	-	-	-	-	N30
NC	-	-	-	-	-	-	M30
NC	-	-	-	-	-	-	L31
NC	-	-	-	-	-	-	K29
NC	-	-	-	-	-	-	H31
NC	-	-	-	-	-	-	E33
NC	-	-	-	-	-	-	E32
NC	-	-	-	-	-	-	A1
NC	-	-	-	-	-	-	A33
NC	-	-	-	-	-	-	AN1
NC	-	-	-	-	-	-	AN33
NC	-	-	-	-	-	-	AC2

12/18/98

XC4085XLA Pinout Table

XC4085XLA Pinout Table

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
VCC	P142	P183	P212	P38	VCC*	VCC*	VCC*
I/O (A8)	P143	P184	P213	P37	D14	D17	A17
I/O (A9)	P144	P185	P214	P36	C14	A17	B18
I/O	-	-	-	-	-	C17	C18
I/O	-	-	-	-	-	B17	E18
I/O	-	-	-	-	-	-	D18
I/O	-	-	-	-	-	-	A19
GND	-	-	-	-	GND*	GND*	GND*
I/O (A19)	P145	P186	P215	P35	A15	C18	C19
I/O (A18)	P146	P187	P216	P34	B15	D18	D19
I/O	-	P188	P217	P33	C15	B18	E19
I/O	-	P189	P218	P32	D15	A19	B20
I/O (A10)	P147	P190	P220	P31	A16	B19	C20
I/O (A11)	P148	P191	P221	P30	B16	C19	D20
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	P29	C16	D19	A21
I/O	-	-	-	P28	B17	A20	E20
I/O	-	-	-	-	D16	B20	B21
I/O	-	-	-	-	A18	C20	C21
I/O	-	-	-	-	-	B21	D21
I/O	-	-	-	-	-	D20	B22
I/O	-	-	-	-	-	-	E21
I/O	-	-	-	-	-	-	C22
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	-	-	-	D22
I/O	-	-	-	-	-	-	A23
I/O	-	-	-	P27	C17	C21	C23
I/O	-	-	-	P26	B18	A22	E22
VCC	-	-	P222	P25	VCC*	VCC*	VCC*
I/O	-	-	P223	P23	C18	B22	B24
I/O	-	-	P224	P22	D17	C22	D23
I/O	P149	P192	P225	P21	A20	B23	C24
I/O	P150	P193	P226	P20	B19	A24	A25
GND	P151	P194	P227	P19	GND*	GND*	GND*
I/O	-	-	-	P18	C19	D22	E23
I/O	-	-	-	P17	D18	C23	B25
I/O	-	P195	P228	P16	A21	B24	D24
I/O	-	P196	P229	P15	B20	C24	C25
I/O	-	-	-	-	-	-	B26
I/O	-	-	-	-	-	-	E24
I/O	-	-	-	-	-	-	C26
I/O	-	-	-	-	-	-	D25
GND	-	-	-	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	-	-	-	A27
I/O	-	-	-	-	-	-	A28
I/O	-	-	-	-	-	D23	E25
I/O	-	-	-	-	-	B25	C27
I/O	P152	P197	P230	P14	C20	A26	D26
I/O	P153	P198	P231	P13	B21	C25	B28
I/O (A12)	P154	P199	P232	P12	B22	D24	B29
I/O (A13)	P155	P200	P233	P10	C21	B26	E26
GND	-	-	-	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*

XC4085XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
I/O	-	-	-	P9	D20	A27	C28
I/O	-	-	-	P8	A23	D25	D27
I/O	-	-	-	-	A24	C26	B30
I/O	-	-	-	-	B23	B27	C29
I/O	-	-	-	-	-	A28	E27
I/O	-	-	-	-	-	D26	A31
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	P234	P7	D21	C27	D28
I/O	-	-	P235	P6	C22	B28	C30
I/O	P156	P201	P236	P5	B24	D27	D29
I/O	P157	P202	P237	P4	C23	B29	E28
I/O (A14)	P158	P203	P238	P3	D22	C28	D30
I/O, GCK8 (A15)	P159	P204	P239	P2	C24	D28	E29
VCC	P160	P205	P240	P1	VCC*	VCC*	VCC*
GND	P1	P2	P1	P304	GND*	GND*	GND*
I/O, GCK1 (A16)	P2	P4	P2	P303	D23	D29	B33
I/O (A17)	P3	P5	P3	P302	C25	C30	F29
I/O	P4	P6	P4	P301	D24	E28	E30
I/O	P5	P7	P5	P300	E23	E29	D31
I/O (TDI)	P6	P8	P6	P299	C26	D30	F30
I/O (TCK)	P7	P9	P7	P298	E24	D31	C33
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	-	-	F28	G29
I/O	-	-	-	-	-	F29	E31
I/O	-	-	-	-	D25	E30	D32
I/O	-	-	-	-	F23	E31	G30
I/O	-	-	-	P297	F24	G28	F31
I/O	-	-	-	P296	E25	G29	H29
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	-	-	-	E32
I/O	-	-	-	-	-	-	E33
I/O	-	-	-	-	-	F30	H30
I/O	-	-	-	-	-	F31	G31
I/O	P8	P10	P8	P295	D26	H28	J29
I/O	P9	P11	P9	P294	G24	H29	F33
I/O	-	P12	P10	P293	F25	G30	G32
I/O	-	P13	P11	P292	F26	H30	J30
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	-	-	-	H31
I/O	-	-	-	-	-	-	K29
I/O	-	-	-	-	-	-	H32
I/O	-	-	-	-	-	-	J31
I/O	-	-	P12	P291	H23	J28	K30
I/O	-	-	P13	P290	H24	J29	H33
I/O	-	-	-	P289	G25	H31	L29
I/O	-	-	-	P288	G26	J30	K31
GND	P10	P14	P14	P287	GND*	GND*	GND*
I/O, FCLK1	P11	P15	P15	P286	J23	K28	L30
I/O	P12	P16	P16	P285	J24	K29	K32
I/O (TMS)	P13	P17	P17	P284	H25	K30	J33
I/O	P14	P18	P18	P283	K23	K31	M29
VCC	-	-	P19	P282	VCC*	VCC*	VCC*
I/O	-	-	-	-	-	-	L31
I/O	-	-	-	-	-	-	M30
I/O	-	-	P20	P280	K24	L29	L32

XC4085XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
I/O	-	-	P21	P279	J25	L30	M31
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	-	-	M30	N29
I/O	-	-	-	-	-	M28	L33
I/O	-	-	-	-	-	-	N30
I/O	-	-	-	-	-	-	N31
I/O	-	-	-	-	J26	M29	M32
I/O	-	-	-	-	L23	M31	P29
I/O	-	-	-	P278	L24	N31	P30
I/O	-	-	-	P277	K25	N28	N33
GND	-	-	P22	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	-	-	N29	P31
I/O	-	-	-	-	-	N30	P32
I/O	-	-	-	P276	L25	P30	R29
I/O	-	-	-	P275	L26	P28	R30
I/O	-	P19	P23	P274	M23	P29	R31
I/O	-	P20	P24	P273	M24	R31	R33
GND	-	-	-	-	GND*	GND*	GND*
I/O	P15	P21	P25	P272	M25	R30	T31
I/O	P16	P22	P26	P271	M26	R28	T29
I/O	-	-	-	-	-	-	T30
I/O	-	-	-	-	-	-	T32
I/O	P17	P23	P27	P270	N24	R29	U32
I/O	P18	P24	P28	P269	N25	T31	U31
GND	P19	P25	P29	P268	GND*	GND*	GND*
VCC	P20	P26	P30	P267	VCC*	VCC*	VCC*
I/O	P21	P27	P31	P266	N26	T30	U29
I/O	P22	P28	P32	P265	P25	T29	U30
I/O	-	-	-	-	-	-	U33
I/O	-	-	-	-	-	-	V32
I/O	P23	P29	P33	P264	P23	U31	V31
I/O	P24	P30	P34	P263	P24	U30	V29
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	P31	P35	P262	R26	U28	V30
I/O	-	P32	P36	P261	R25	U29	W33
I/O	-	-	-	P260	R24	V30	W31
I/O	-	-	-	P259	R23	V29	W30
I/O	-	-	-	-	-	V28	W29
I/O	-	-	-	-	-	W31	Y32
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	P37	-	GND*	GND*	GND*
I/O	-	-	-	P258	T26	W30	Y31
I/O	-	-	-	P257	T25	W29	Y30
I/O	-	-	-	-	-	-	AA33
I/O	-	-	-	-	-	-	Y29
I/O	-	-	-	-	-	W28	AA32
I/O	-	-	-	-	-	Y31	AA31
I/O	-	-	-	-	T24	Y30	AA30
I/O	-	-	-	-	U25	Y29	AB32
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	P38	P256	T23	Y28	AA29
I/O	-	-	P39	P255	V26	AA30	AB31
I/O	-	-	-	-	-	-	AB30
I/O	-	-	-	-	-	-	AC33
VCC	-	-	P40	P253	VCC*	VCC*	VCC*
I/O	P25	P33	P41	P252	U24	AA29	AC31

XC4085XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
I/O	P26	P34	P42	P251	V25	AB31	AB29
I/O	P27	P35	P43	P250	V24	AB30	AD32
I/O, FCLK2	P28	P36	P44	P249	U23	AB29	AC30
GND	P29	P37	P45	P248	GND*	GND*	GND*
I/O	-	-	-	P247	Y26	AB28	AD31
I/O	-	-	-	P246	W25	AC30	AE33
I/O	-	-	P46	P245	W24	AC29	AC29
I/O	-	-	P47	P244	V23	AC28	AE32
I/O	-	-	-	-	-	-	AD30
I/O	-	-	-	-	-	-	AE31
I/O	-	-	-	-	-	-	AF32
I/O	-	-	-	-	-	-	AD29
GND	-	-	-	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	-	-	-	AF31
I/O	-	-	-	-	-	-	AE30
I/O	-	-	-	-	-	AD31	AG33
I/O	-	-	-	-	-	AD30	AH33
I/O	-	P38	P48	P243	AA26	AD29	AE29
I/O	-	P39	P49	P242	Y25	AD28	AG31
I/O	P30	P40	P50	P241	Y24	AE30	AF30
I/O	P31	P41	P51	P240	AA25	AE29	AH32
GND	-	-	-	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	P239	AB25	AF31	AJ32
I/O	-	-	-	P238	AA24	AE28	AF29
I/O	-	-	-	-	-	AF30	AH31
I/O	-	-	-	-	-	AF29	AG30
I/O	P32	P42	P52	P237	Y23	AG31	AK32
I/O	P33	P43	P53	P236	AC26	AF28	AJ31
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	-	AD26	AG30	AG29
I/O	-	-	-	-	AC25	AG29	AL33
I/O	P34	P44	P54	P235	AA23	AH31	AH30
I/O	P35	P45	P55	P234	AB24	AG28	AK31
I/O	P36	P46	P56	P233	AD25	AH30	AJ30
I/O, GCK2	P37	P47	P57	P232	AC24	AJ30	AH29
O (M1)	P38	P48	P58	P231	AB23	AH29	AK30
GND	P39	P49	P59	P230	GND*	GND*	GND*
I (M0)	P40	P50	P60	P229	AD24	AH28	AJ29
VCC	P41	P55	P61	P228	VCC*	VCC*	VCC*
I (M2)	P42	P56	P62	P227	AC23	AJ28	AN32
I/O, GCK3	P43	P57	P63	P226	AE24	AK29	AJ28
I/O (HDC)	P44	P58	P64	P225	AD23	AH27	AK29
I/O	P45	P59	P65	P224	AC22	AK28	AL30
I/O	P46	P60	P66	P223	AF24	AJ27	AK28
I/O	P47	P61	P67	P222	AD22	AL28	AM31
I/O (/LDC)	P48	P62	P68	P221	AE23	AH26	AJ27
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	-	-	AK27	AN31
I/O	-	-	-	-	-	AJ26	AL29
I/O	-	-	-	-	AC21	AL27	AK27
I/O	-	-	-	-	AD21	AH25	AL28
I/O	-	-	-	P220	AE22	AK26	AJ26
I/O	-	-	-	P219	AF23	AL26	AM30
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	-	GND*	GND*	GND*

XC4085XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
I/O	P49	P63	P69	P218	AD20	AH24	AM29
I/O	P50	P64	P70	P217	AE21	AJ25	AK26
I/O	-	P65	P71	P216	AF21	AK25	AL27
I/O	-	P66	P72	P215	AC19	AJ24	AJ25
I/O	-	-	-	-	-	AH23	AN29
I/O	-	-	-	-	-	AK24	AN28
I/O	-	-	-	-	-	-	AK25
I/O	-	-	-	-	-	-	AL26
VCC	-	-	-		VCC*	VCC*	VCC*
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	-	-	-	AJ24
I/O	-	-	-	-	-	-	AM27
I/O	-	-	-	-	-	-	AM26
I/O	-	-	-	-	-	-	AK24
I/O	-	-	P73	P214	AD19	AL24	AL25
I/O	-	-	P74	P213	AE20	AH22	AJ23
I/O	-	-	-	P212	AF20	AJ23	AN26
I/O	-	-	-	P211	AC18	AK23	AL24
GND	P51	P67	P75	P210	GND*	GND*	GND*
I/O	P52	P68	P76	P209	AD18	AJ22	AK23
I/O	P53	P69	P77	P208	AE19	AK22	AN25
I/O	P54	P70	P78	P207	AC17	AL22	AJ22
I/O	P55	P71	P79	P206	AD17	AJ21	AL23
VCC	-	-	P80	P204	VCC*	VCC*	VCC*
I/O	-	P72	P81	P203	AE18	AH20	AM24
I/O	-	P73	P82	P202	AF18	AK21	AK22
I/O	-	-	-	-	-	-	AM23
I/O	-	-	-	-	-	-	AJ21
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	-	-	-	AL22
I/O	-	-	-	-	-	-	AN23
I/O	-	-	-	-	-	AJ20	AK21
I/O	-	-	-	-	-	AH19	AM22
I/O	-	-	-	-	AC16	AK20	AJ20
I/O	-	-	-	-	AD16	AJ19	AL21
I/O	-	-	-	P201	AE17	AL20	AN21
I/O	-	-	-	P200	AE16	AH18	AK20
GND	-	-	P83	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	P199	AF16	AK19	AL20
I/O	-	-	-	P198	AC15	AJ18	AJ19
I/O	-	-	P84	P197	AD15	AL19	AM20
I/O	-	-	P85	P196	AE15	AK18	AK19
I/O	P56	P74	P86	P195	AF15	AH17	AL19
I/O	P57	P75	P87	P194	AD14	AJ17	AN19
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	-	-	-	AJ18
I/O	-	-	-	-	-	-	AK18
I/O	-	-	-	-	-	AK17	AL18
I/O	-	-	-	-	-	AL17	AM18
I/O	P58	P76	P88	P193	AE14	AJ16	AK17
I/O (/INIT)	P59	P77	P89	P192	AF14	AK16	AJ17
VCC	P60	P78	P90	P191	VCC*	VCC*	VCC*
GND	P61	P79	P91	P190	GND*	GND*	GND*
I/O	P62	P80	P92	P189	AE13	AL16	AL17
I/O	P63	P81	P93	P188	AC13	AH15	AM17
I/O	-	-	-	-	-	AL15	AN17

XC4085XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
I/O	-	-	-	-	-	AJ15	AK16
I/O	-	-	-	-	-	-	AJ16
I/O	-	-	-	-	-	-	AL16
GND	-	-	-	-	GND*	GND*	GND*
I/O	P64	P82	P94	P187	AD13	AK15	AM16
I/O	P65	P83	P95	P186	AF12	AJ14	AL15
I/O	-	P84	P96	P185	AE12	AH14	AK15
I/O	-	P85	P97	P184	AD12	AK14	AJ15
I/O	-	-	-	P183	AC12	AL13	AN15
I/O	-	-	-	P182	AF11	AK13	AM14
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	P98	-	GND*	GND*	GND*
I/O	-	-	-	P181	AE11	AJ13	AL14
I/O	-	-	-	P180	AD11	AH13	AK14
I/O	-	-	-	-	AE10	AL12	AJ14
I/O	-	-	-	-	AC11	AK12	AN13
I/O	-	-	-	-	-	AJ12	AM13
I/O	-	-	-	-	-	AK11	AL13
I/O	-	-	-	-	-	-	AK13
I/O	-	-	-	-	-	-	AJ13
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	-	-	-	AM12
I/O	-	-	-	-	-	-	AL12
I/O	-	-	P99	P179	AF9	AH12	AK12
I/O	-	-	P100	P178	AD10	AJ11	AN11
VCC	-	-	P101	P177	VCC*	VCC*	VCC*
I/O	P66	P86	P102	P175	AE9	AL10	AJ12
I/O	P67	P87	P103	P174	AD9	AK10	AL11
I/O	P68	P88	P104	P173	AC10	AJ10	AK11
I/O	P69	P89	P105	P172	AF7	AK9	AM10
GND	P70	P90	P106	P171	GND*	GND*	GND*
I/O	-	-	-	P170	AE8	AL8	AL10
I/O	-	-	-	P169	AD8	AH10	AJ11
I/O	-	-	P107	P168	AC9	AJ9	AN9
I/O	-	-	P108	P167	AF6	AK8	AK10
I/O	-	-	-	-	-	-	AM9
I/O	-	-	-	-	-	-	AL9
I/O	-	-	-	-	-	-	AJ10
I/O	-	-	-	-	-	-	AM8
GND	-	-	-	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	-	-	-	AK9
I/O	-	-	-	-	-	-	AL8
I/O	-	-	-	-	-	AJ8	AN7
I/O	-	-	-	-	-	AH9	AJ9
I/O	-	P91	P109	P166	AE7	AK7	AL7
I/O	-	P92	P110	P165	AD7	AL6	AK8
I/O	P71	P93	P111	P164	AE6	AJ7	AN6
I/O	P72	P94	P112	P163	AE5	AH8	AM6
GND	-	-	-	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	P162	AD6	AK6	AJ8
I/O	-	-	-	P161	AC7	AL5	AL6
I/O	P73	P95	P113	P160	AF4	AH7	AK7
I/O	P74	P96	P114	P159	AF3	AJ6	AM5
I/O	-	-	-	-	AE4	AK5	AM4
I/O	-	-	-	-	AC6	AL4	AJ7

XC4085XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	-	-	AH6	AL5
I/O	-	-	-	-	-	AJ5	AK6
I/O	P75	P97	P115	P158	AD5	AK4	AN3
I/O	P76	P98	P116	P157	AE3	AH5	AK5
I/O	P77	P99	P117	P156	AD4	AK3	AJ6
I/O, GCK4	P78	P100	P118	P155	AC5	AJ4	AL4
GND	P79	P101	P119	P154	GND*	GND*	GND*
DONE	P80	P103	P120	P153	AD3	AH4	AJ5
VCC	P81	P106	P121	P152	VCC*	VCC*	VCC*
/PROGRAM	P82	P108	P122	P151	AC4	AH3	AM1
I/O (D7)	P83	P109	P123	P150	AD2	AJ2	AH5
I/O, GCK5	P84	P110	P124	P149	AC3	AG4	AJ4
I/O	P85	P111	P125	P148	AB4	AG3	AK3
I/O	P86	P112	P126	P147	AD1	AH2	AH4
I/O	-	-	-	-	AB3	AH1	AL1
I/O	-	-	-	-	AC2	AF4	AG5
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	P127	P146	AA4	AF3	AJ3
I/O	-	-	P128	P145	AA3	AG2	AK2
I/O	-	-	-	-	-	AG1	AG4
I/O	-	-	-	-	-	AE4	AH3
I/O	-	-	-	P144	AB2	AE3	AF5
I/O	-	-	-	P143	AC1	AF2	AJ2
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	-	GND*	GND*	GND*
I/O (D6)	P87	P113	P129	P142	Y3	AF1	AJ1
I/O	P88	P114	P130	P141	AA2	AD4	AF4
I/O	P89	P115	P131	P140	AA1	AD3	AG3
I/O	P90	P116	P132	P139	W4	AE2	AE5
I/O	-	-	-	-	-	AD2	AH1
I/O	-	-	-	-	-	AC4	AF3
I/O	-	-	-	-	-	-	AE4
I/O	-	-	-	-	-	-	AG2
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	-	-	-	AD5
I/O	-	-	-	-	-	-	AF2
I/O	-	-	-	-	-	-	AF1
I/O	-	-	-	-	-	-	AD4
I/O	-	P117	P133	P138	W3	AC3	AE3
I/O	-	P118	P134	P137	Y2	AD1	AC5
I/O	-	-	-	P136	Y1	AC2	AE1
I/O	-	-	-	P135	V4	AB4	AD3
GND	P91	P119	P135	P134	GND*	GND*	GND*
I/O	-	-	P136	P133	V3	AB3	AC4
I/O	-	-	P137	P132	W2	AB2	AD2
I/O, FCLK3	P92	P120	P138	P131	U4	AB1	AB5
I/O	P93	P121	P139	P130	U3	AA3	AC3
VCC	-	-	P140	P129	VCC*	VCC*	VCC*
I/O	-	-	-	-	-	-	AB4
I/O	-	-	-	-	-	-	AC1
I/O (D5)	P94	P122	P141	P127	V2	AA2	AA5
I/O (/CS0)	P95	P123	P142	P126	V1	Y2	AB3
GND	-	-	P143	-	GND*	GND*	GND*
I/O	-	-	-	-	T4	Y4	AB2
I/O	-	-	-	-	T3	Y3	AA4

XC4085XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
I/O	-	-	-	-	-	Y1	AA3
I/O	-	-	-	-	-	W1	Y5
I/O	-	-	-	-	-	-	AA1
I/O	-	-	-	-	-	-	Y4
I/O	-	-	-	P125	U2	W4	Y3
I/O	-	-	-	P124	T2	W3	Y2
GND	-	-	-	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O	-	-	-	-	-	W2	W5
I/O	-	-	-	-	-	V2	W4
I/O	-	-	-	P123	T1	V4	W3
I/O	-	-	-	P122	R4	V3	W1
I/O	-	P124	P144	P121	R3	U1	V3
I/O	-	P125	P145	P120	R2	U2	V5
GND	-	-	-	-	GND*	GND*	GND*
I/O	P96	P126	P146	P119	R1	U4	V4
I/O	P97	P127	P147	P118	P3	U3	V2
I/O	-	-	-	-	-	-	U2
I/O	-	-	-	-	-	-	U1
I/O (D4)	P98	P128	P148	P117	P2	T1	U5
I/O	P99	P129	P149	P116	P1	T2	U4
VCC	P100	P130	P150	P115	VCC*	VCC*	VCC*
GND	P101	P131	P151	P114	GND*	GND*	GND*
I/O (D3)	P102	P132	P152	P113	N2	T3	U3
I/O (/RS)	P103	P133	P153	P112	N4	R1	T2
I/O	-	-	-	-	-	-	T3
I/O	-	-	-	-	-	-	T5
I/O	P104	P134	P154	P111	N3	R2	T4
I/O	P105	P135	P155	P110	M1	R4	R1
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	P136	P156	P109	M2	R3	R3
I/O	-	P137	P157	P108	M3	P2	R4
I/O	-	-	-	P107	M4	P3	R5
I/O	-	-	-	P106	L1	P4	P2
I/O	-	-	-	-	-	N1	P3
I/O	-	-	-	-	-	N2	P4
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	P158	-	GND*	GND*	GND*
I/O	-	-	-	P105	L2	N3	N1
I/O	-	-	-	P104	L3	N4	P5
I/O	-	-	-	-	K2	M1	N2
I/O	-	-	-	-	L4	M2	N3
I/O	-	-	-	-	-	-	N4
I/O	-	-	-	-	-	-	M2
I/O	-	-	-	-	-	M3	N5
I/O	-	-	-	-	-	M4	M3
GND	-	-	-	-	GND*	GND*	GND*
I/O (D2)	P106	P138	P159	P103	J1	L2	M4
I/O	P107	P139	P160	P102	K3	L3	L1
I/O	-	-	-	-	-	-	L3
I/O	-	-	-	-	-	-	M5
VCC	-	-	P161	P101	VCC*	VCC*	VCC*
I/O	P108	P140	P162	P99	J2	K1	K2
I/O, FCLK4	P109	P141	P163	P98	J3	K2	L4
I/O	-	-	P164	P97	K4	K3	J1
I/O	-	-	P165	P96	G1	K4	K3
GND	P110	P142	P166	P95	GND*	GND*	GND*

XC4085XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
I/O	-	-	-	P94	H2	J2	L5
I/O	-	-	-	P93	H3	J3	J2
I/O	-	-	P167	P92	J4	J4	K4
I/O	-	-	P168	P91	F1	H1	J3
I/O	-	-	-	-	-	-	H2
I/O	-	-	-	-	-	-	K5
I/O	-	-	-	-	-	-	H3
I/O	-	-	-	-	-	-	J4
GND	-	-	-	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O	-	P143	P169	P90	G2	H2	G1
I/O	-	P144	P170	P89	G3	H3	F1
I/O	P111	P145	P171	P88	F2	H4	J5
I/O	P112	P146	P172	P87	E2	G2	G3
I/O	-	-	-	-	-	G3	H4
I/O	-	-	-	-	-	F1	F2
I/O	-	-	-	-	-	-	E2
I/O	-	-	-	-	-	-	H5
GND	-	-	-	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O (D1)	P113	P147	P173	P86	F3	G4	F3
I/O (/RCK, RDY_/BUSY)	P114	P148	P174	P85	G4	F2	G4
I/O	-	-	-	-	D1	F3	D2
I/O	-	-	-	-	C1	E1	E3
I/O	-	-	-	-	-	F4	G5
I/O	-	-	-	-	-	E2	C1
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	P84	D2	E3	F4
I/O	-	-	-	P83	F4	D1	D3
I/O	P115	P149	P175	P82	E3	E4	B3
I/O	P116	P150	P176	P81	C2	D2	F5
I/O (D0, DIN)	P117	P151	P177	P80	D3	C2	E4
"I/O, GCK6 (DOUT)"	P118	P152	P178	P79	E4	D3	D4
CCLK	P119	P153	P179	P78	C3	D4	C4
VCC	P120	P154	P180	P77	VCC*	VCC*	VCC*
O, TDO	P121	P159	P181	P76	D4	C4	E6
GND	P122	P160	P182	P75	GND*	GND*	GND*
I/O (A0, /WS)	P123	P161	P183	P74	B3	B3	D5
"I/O, GCK7 (A1)"	P124	P162	P184	P73	C4	D5	A2
I/O	P125	P163	P185	P72	D5	B4	D6
I/O	P126	P164	P186	P71	A3	C5	A3
I/O	-	-	-	-	-	A4	E7
I/O	-	-	-	-	-	D6	C5
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	-	C5	B5	B4
I/O	-	-	-	-	B4	C6	D7
I/O, (CS1, A2)	P127	P165	P187	P70	D6	A5	C6
I/O (A3)	P128	P166	P188	P69	C6	D7	E8
I/O	-	-	-	P68	B5	B6	B5
I/O	-	-	-	P67	A4	A6	A5
VCC	-	-	-	-	VCC*	VCC*	VCC*
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	P189	P66	C7	D8	D8
I/O	-	-	P190	P65	B6	C7	C7
I/O	P129	P167	P191	P64	A6	B7	E9

XC4085XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
I/O	P130	P168	P192	P63	D8	D9	A6
I/O	-	-	-	-	C8	B8	B7
I/O	-	-	-	-	-	A8	D9
I/O	-	-	-	-	-	-	C8
I/O	-	-	-	-	-	-	E10
VCC	-	-	-	-	-	VCC*	VCC*
GND	-	-	-	-	-	GND*	GND*
I/O	-	-	-	-	-	-	B8
I/O	-	-	-	-	-	-	A8
I/O	-	-	-	-	-	-	D10
I/O	-	-	-	-	-	-	C9
I/O	-	P169	P193	P62	B7	D10	E11
I/O	-	P170	P194	P61	A7	C9	A9
I/O	-	-	P195	P60	D9	B9	C10
I/O	-	-	-	P59	C9	C10	D11
GND	P131	P171	P196	P58	GND*	GND*	GND*
I/O	P132	P172	P197	P57	B8	B10	B10
I/O	P133	P173	P198	P56	D10	A10	E12
I/O	-	-	P199	P55	C10	C11	C11
I/O	-	-	P200	P54	B9	D12	B11
VCC	-	-	P201	P52	VCC*	VCC*	VCC*
I/O	-	-	-	P51	A9	B11	D12
I/O	-	-	-	P50	D11	C12	A11
I/O	-	-	-	-	-	-	E13
I/O	-	-	-	-	-	-	C12
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	-	-	-	B12
I/O	-	-	-	-	-	-	D13
I/O	-	-	-	-	-	D13	C13
I/O	-	-	-	-	-	B12	E14
I/O	-	-	-	-	C11	C13	A13
I/O	-	-	-	-	B10	A12	D14
I/O	-	-	-	P49	B11	D14	C14
I/O	-	-	-	P48	A11	B13	B14
GND	-	-	-	-	GND*	GND*	GND*
VCC	-	-	-	-	VCC*	VCC*	VCC*
I/O (A4)	P134	P174	P202	P47	D12	C14	E15
I/O (A5)	P135	P175	P203	P46	C12	A13	D15
I/O	-	P176	P205	P45	B12	B14	C15
I/O	P136	P177	P206	P44	A12	D15	A15
I/O (A21)	P137	P178	P207	P43	C13	C15	C16
I/O (A20)	P138	P179	P208	P42	B13	B15	E16
GND	-	-	-	-	GND*	GND*	GND*
I/O	-	-	-	-	-	-	D16
I/O	-	-	-	-	-	-	B16
I/O	-	-	-	-	-	A15	B17
I/O	-	-	-	-	-	C16	C17
I/O (A6)	P139	P180	P209	P41	A13	B16	E17
I/O (A7)	P140	P181	P210	P40	B14	A16	D17
GND	P141	P182	P211	P39	GND*	GND*	GND*
VCC	-	-	-	-	A10	A1	A4
VCC	-	-	-	-	A17	A11	A10
VCC	-	-	-	-	AC14	A21	A16
VCC	-	-	-	-	AC20	A31	A22
VCC	-	-	-	-	AC8	D11	A26
VCC	-	-	-	-	AF10	D21	A30
VCC	-	-	-	-	AF17	L1	B2

XC4085XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
VCC	-	-	-	-	D7	L4	B13
VCC	-	-	-	-	D13	L28	B19
VCC	-	-	-	-	D19	L31	B32
VCC	-	-	-	-	G23	AA1	C3
VCC	-	-	-	-	H4	AA4	C32
VCC	-	-	-	-	K1	AA28	D1
VCC	-	-	-	-	K26	AA31	D33
VCC	-	-	-	-	N23	AH11	H1
VCC	-	-	-	-	P4	AH21	K33
VCC	-	-	-	-	U1	AL1	M1
VCC	-	-	-	-	U26	AL11	N32
VCC	-	-	-	-	W23	AL21	R2
VCC	-	-	-	-	Y4	AL31	T33
VCC	-	-	-	-	B2	-	V1
VCC	-	-	-	-	B25	-	W32
VCC	-	-	-	-	AE2	-	AA2
VCC	-	-	-	-	AE25	-	AB33
VCC	-	-	-	-	-	-	AD1
VCC	-	-	-	-	-	-	AF33
VCC	-	-	-	-	-	-	AK1
VCC	-	-	-	-	-	-	AK33
VCC	-	-	-	-	-	-	AL2
VCC	-	-	-	-	-	-	AL3
VCC	-	-	-	-	-	-	AM2
VCC	-	-	-	-	-	-	AM15
VCC	-	-	-	-	-	-	AM21
VCC	-	-	-	-	-	-	AM32
VCC	-	-	-	-	-	-	AN4
VCC	-	-	-	-	-	-	AN8
VCC	-	-	-	-	-	-	AN12
VCC	-	-	-	-	-	-	AN18
VCC	-	-	-	-	-	-	AN24
VCC	-	-	-	-	-	-	AN30
VCC	-	-	-	-	-	C3	AL31
VCC	-	-	-	-	-	C29	E5
VCC	-	-	-	-	-	AJ3	C31
VCC	-	-	-	-	-	AJ29	AK4
GND	-	-	-	-	A1	A2	A7
GND	-	-	-	-	A14	A3	A12
GND	-	-	-	-	A19	A7	A14
GND	-	-	-	-	A2	A9	A18
GND	-	-	-	-	A22	A14	A20
GND	-	-	-	-	A25	A18	A24
GND	-	-	-	-	A26	A23	A29
GND	-	-	-	-	A5	A25	A32
GND	-	-	-	-	A8	A29	B1
GND	-	-	-	-	AB1	A30	B6
GND	-	-	-	-	AB26	B1	B9
GND	-	-	-	-	AE1	B2	B15
GND	-	-	-	-	AE26	B30	B23
GND	-	-	-	-	AF1	B31	B27
GND	-	-	-	-	AF13	C1	B31
GND	-	-	-	-	AF19	C31	C2
GND	-	-	-	-	AF2	D16	E1
GND	-	-	-	-	AF22	G1	F32
GND	-	-	-	-	AF25	G31	G2

XC4085XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560
GND	-	-	-	-	AF26	J1	G33
GND	-	-	-	-	AF5	J31	J32
GND	-	-	-	-	AF8	P1	K1
GND	-	-	-	-	B1	P31	L2
GND	-	-	-	-	B26	T4	M33
GND	-	-	-	-	E1	T28	P1
GND	-	-	-	-	E26	V1	P33
GND	-	-	-	-	H1	V31	R32
GND	-	-	-	-	H26	AC1	T1
GND	-	-	-	-	N1	AC31	V33
GND	-	-	-	-	P26	AE1	W2
GND	-	-	-	-	W1	AE31	Y1
GND	-	-	-	-	W26	AH16	Y33
GND	-	-	-	-	-	AJ1	AB1
GND	-	-	-	-	-	AJ31	AC32
GND	-	-	-	-	-	AK1	AD33
GND	-	-	-	-	-	AK2	AE2
GND	-	-	-	-	-	AK30	AG1
GND	-	-	-	-	-	AK31	AG32
GND	-	-	-	-	-	AL2	AH2
GND	-	-	-	-	-	AL3	AJ33
GND	-	-	-	-	-	AL7	AL32
GND	-	-	-	-	-	AL9	AM3
GND	-	-	-	-	-	AL14	AM11
GND	-	-	-	-	-	AL18	AM19
GND	-	-	-	-	-	AL23	AM25
GND	-	-	-	-	-	AL25	AM28
GND	-	-	-	-	-	AL29	AM33
GND	-	-	-	-	-	AL30	AM7
GND	-	-		-	-	-	AN2
GND	-	-	-	-	-	-	AN5
GND	-	-	-	-	-	-	AN10
GND	-	-	-	-	-	-	AN14
GND	-	-	-	-	-	-	AN16
GND	-	-	-	-	-	-	AN20
GND	-	-	-	-	-	-	AN22
GND	-	-	-	-	-	-	AN27
GND	-	-	P204	-	-	-	-
GND	-	-	P219	-	-	-	-
NC	-	P1	-	P11	-	C8	A1
NC	-	P3	-	P24	-	-	A33
NC	-	P51	-	P53	-	-	AN1
NC	-	P52	-	P100	-	-	AN33
NC	-	P53	-	P128	-	-	AC2
NC	-	P54	-	P176	-	-	-
NC	-	P102	-	P205	-	-	-
NC	-	P104	-	P254	-	-	-
NC	-	P105	-	P281	-	-	-
NC	-	P107	-	-	-	-	-
NC	-	P155	-	-	-	-	-
NC	-	P156	-	-	-	-	-
NC	-	P157	-	-	-	-	-
NC	-	P158	-	-	-	-	-
NC	-	P206	-	-	-	-	-
NC	-	P207	-	-	-	-	-
NC	-	P208	-	-	-	-	-

XC4085XLA Pinout Table (Continued)

PAD NAME	HQ160	HQ208	HQ240	HQ304	BG352	BG432	BG560

12/18/98

* Note: Pads labelled GND* or VCC* are internally bonded to Ground or VCC planes within the associated package. They have no direct connection to any specific package pin.

XC40110XV Pinout Table

XC40110XV Pinout Table

PAD NAME	EPIC PAD#	HQ240	BG352	BG432	BG560	PG559
VCCIO	-	P240	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O GCK8 (A15)	1	P239	C24	D28	E29	E3
I/O (A14)	2	P238	D22	C28	D30	F4
I/O	3	P237	C23	B29	E28	J7
I/O	4	P236	B24	D27	D29	D2
I/O	5	P235	C22	B28	C30	K8
I/O	6	P234	D21	C27	D28	H6
I/O	7	-	-	-	-	-
I/O	8	-	-	-	-	-
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	-	-	GND*	GND*	GND*
I/O	9	-	-	-	-	-
I/O	10	-	-	-	-	-
I/O	11	-	-	D26	A31	G5
I/O	12	-	-	A28	E27	F2
I/O	13	-	B23	B27	C29	H4
I/O	14	-	A24	C26	B30	G1
I/O	15	-	A23	D25	D27	J5
I/O	16	-	D20	A27	C28	L7
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	-	GND*	GND*	GND*	GND*
I/O (A13)	17	P233	C21	B26	E26	J3
I/O (A12)	18	P232	B22	D24	B29	K4
I/O	19	P231	B21	C25	B28	H2
I/O	20	P230	C20	A26	D26	L5
I/O	21	-	-	B25	C27	J1
I/O	22	-	-	D23	E25	M6
I/O	23	-	-	-	A28	K2
I/O	24	-	-	-	A27	N7
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	-	-	GND*	GND*	GND*
I/O	25	-	-	-	D25	P8
I/O	26	-	-	-	C26	L3
I/O	27	-	-	-	E24	L1
I/O	28	-	-	-	B26	M4
I/O	29	P229	B20	C24	C25	P2
I/O	30	P228	A21	B24	D24	N5
I/O	31	-	D18	C23	B25	R1
I/O	32	-	C19	D22	E23	N3
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	P227	GND*	GND*	GND*	GND*
I/O	33	P226	B19	A24	A25	R7
I/O	34	-	-	-	-	P4
VCCINT	-	P225	A20	VCCINT*	VCCINT*	VCCINT*
I/O	35	P224	D17	C22	D23	T2
I/O	36	P223	C18	B22	B24	T8
VCCIO	-	P222	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	37	-	B18	A22	E22	R5

XC40110XV Pinout Table (Continued)

PAD NAME	EPIC PAD#	HQ240	BG352	BG432	BG560	PG559
I/O	38	-	C17	C21	C23	R3
I/O	39	-	-	-	A23	U1
I/O	40	-	-	-	D22	T4
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	41	-	-	-	C22	U5
I/O	42	-	-	-	E21	V2
I/O	43	-	-	D20	B22	U7
I/O	44	-	-	B21	D21	U3
I/O	45	-	A18	C20	C21	Y2
I/O	46	-	D16	B20	B21	V4
I/O	47	-	B17	A20	E20	V6
I/O	48	-	C16	D19	A21	W5
GND	-	-	GND*	GND*	GND*	GND*
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O (A11)	49	P221	B16	C19	D20	W7
I/O (A10)	50	P220	A16	B19	C20	Y4
I/O	51	P218	D15	A19	B20	AA1
I/O	52	P217	C15	B18	E19	Y6
I/O (A18)	53	P216	B15	D18	D19	AB2
I/O (A19)	54	P215	A15	C18	C19	Y8
I/O	55	-	-	-	-	-
I/O	56	-	-	-	-	-
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	57	-	-	-	-	-
I/O	58	-	-	-	-	-
I/O	59	-	-	-	A19	AA3
I/O	60	-	-	-	D18	AA5
I/O	61	-	-	B17	E18	AC1
I/O	62	-	-	C17	C18	AA7
I/O (A9)	63	P214	C14	A17	B18	AB4
I/O (A8)	64	P213	D14	D17	A17	AB6
VCCIO	-	P212	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	P211	GND*	GND*	GND*	GND*
I/O (A7)	65	P210	B14	A16	D17	AC3
I/O (A6)	66	P209	A13	B16	E17	AC5
VCCINT	-	-	-	VCCINT*	VCCINT*	VCCINT*
I/O	67	-	-	-	-	AD2
I/O	68	-	-	A15	B17	AC7
I/O	69	-	-	-	B16	AF2
I/O	70	-	-	-	D16	AD4
I/O	71	-	-	-	-	-
I/O	72	-	-	-	-	-
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	-	-	GND*	GND*	GND*
I/O	73	-	-	-	-	-
I/O	74	-	-	-	-	-
I/O (A20)	75	P208	B13	B15	E16	AD6
I/O (A21)	76	P207	C13	C15	C16	AE5

XC40110XV Pinout Table (Continued)

PAD NAME	EPIC PAD#	HQ240	BG352	BG432	BG560	PG559
I/O	77	P206	A12	D15	A15	AF4
I/O	78	P205	B12	B14	C15	AG1
I/O (A5)	79	P203	C12	A13	D15	AD8
I/O (A4)	80	P202	D12	C14	E15	AG3
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	-	GND*	GND*	GND*	GND*
I/O	81	-	A11	B13	B14	AH4
I/O	82	-	B11	D14	C14	AE7
I/O	83	-	B10	A12	D14	AH2
I/O	84	-	C11	C13	A13	AF6
I/O	85	-	-	B12	E14	AJ1
I/O	86	-	-	D13	C13	AG5
I/O	87	-	-	-	D13	AJ3
I/O	88	-	-	-	B12	AK4
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	-	-	GND*	GND*	GND*
I/O	89	-	-	-	C12	AG7
I/O	90	-	-	-	E13	AK2
I/O	91	-	D11	C12	A11	AJ5
I/O	92	-	A9	B11	D12	AL3
VCCIO	-	P201	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	93	P200	B9	D12	B11	AM4
I/O	94	P199	C10	C11	C11	AN1
VCCINT	-	P198	D10	VCCINT*	VCCINT*	VCCINT*
I/O	95	-	-	-	-	AL5
I/O	96	P197	B8	B10	B10	AH8
GND	-	P196	GND*	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	97	-	C9	C10	D11	AJ7
I/O	98	P195	D9	B9	C10	AP2
I/O	99	P194	A7	C9	A9	AN3
I/O	100	P193	B7	D10	E11	AP4
I/O	101	-	-	-	C9	AR1
I/O	102	-	-	-	D10	AN5
I/O	103	-	-	-	A8	AM6
I/O	104	-	-	-	B8	AK8
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	105	-	-	-	E10	AL7
I/O	106	-	-	-	C8	AT2
I/O	107	-	-	A8	D9	AR3
I/O	108	-	-	B8	B7	AU1
I/O	109	P192	D8	D9	A6	AT4
I/O	110	P191	A6	B7	E9	AV2
I/O	111	P190	B6	C7	C7	AR5
I/O	112	P189	C7	D8	D8	AN7
GND	-	-	GND*	GND*	GND*	GND*
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	113	-	A4	A6	A5	AW3
I/O	114	-	B5	B6	B5	AV4

XC40110XV Pinout Table (Continued)

PAD NAME	EPIC PAD#	HQ240	BG352	BG432	BG560	PG559
I/O (A3)	115	P188	C6	D7	E8	BA1
I/O, (CS1,A2)	116	P187	D6	A5	C6	AU5
I/O	117	-	B4	C6	D7	AY2
I/O	118	-	C5	B5	B4	AT6
I/O	119	-	-	-	-	-
I/O	120	-	-	-	-	-
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	121	-	-	-	-	-
I/O	122	-	-	-	-	-
I/O	123	-	-	D6	C5	AP8
I/O	124	-	-	A4	E7	AR7
I/O	125	-	-	C5	A3	AY4
I/O	126	P186	A3	-	-	BB2
VCCINT	-	P185	D5	VCCINT*	VCCINT*	VCCINT*
I/O GCK7 (A1)	127	P184	C4	D5	A2	AV6
I/O (A0, /WS)	128	P183	B3	B3	D5	AT8
GND	-	P182	GND*	GND*	GND*	GND*
O, TDO	-	P181	D4	C4	E6	BA3
VCCIO	-	P180	-	VCCIO*	VCCIO*	VCCIO*
CCLK	-	P179	C3	D4	C4	BA5
I/O GCK6 (DOUT)	129	P178	E4	D3	D4	BB4
I/O (D0, DIN)	130	P177	D3	C2	E4	AY6
I/O	131	P176	C2	D2	F5	BC3
I/O	132	P175	E3	E4	B3	AW7
I/O	133	-	F4	D1	D3	BB6
I/O	134	-	D2	E3	F4	AU9
I/O	135	-	-	-	-	-
I/O	136	-	-	-	-	-
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	-	-	GND*	GND*	GND*
I/O	137	-	-	-	-	-
I/O	138	-	-	-	-	-
I/O	139	-	-	E2	C1	AT10
I/O	140	-	-	F4	G5	AV8
I/O	141	-	C1	E1	E3	AY8
I/O	142	-	D1	F3	D2	BC7
I/O (/RCK, RDY_/ BUSY	143	P174	G4	F2	G4	AW9
I/O (D1)	144	P173	F3	G4	F3	BA9
VCCIO	-	-	-	VCCIO*	VCCIO*	VCCIO*
GND	-	-	-	GND*	GND*	GND*
I/O	145	-	-	-	H5	AU11
I/O	146	-	-	-	E2	AY10
I/O	147	-	-	F1	F2	BB8
I/O	148	-	-	G3	H4	AW11

XC40110XV Pinout Table (Continued)

PAD NAME	EPIC PAD#	HQ240	BG352	BG432	BG560	PG559
I/O	149	-	-	G2	G3	BC9
I/O	150	-	-	H4	J5	AV12
GND	-	-	-	-	-	-
I/O	151	P172	E2	H3	F1	AU13
I/O	152	P171	F2	H2	G1	AT14
VCCIO	-	-	-	VCCIO*	VCCIO*	VCCIO*
GND	-	-	-	GND*	GND*	GND*
I/O	153	-	-	-	J4	BA11
I/O	154	-	-	-	H3	AY12
I/O	155	P170	G3	-	K5	BB10
I/O	156	P169	G2	-	H2	AW13
I/O	157	P168	F1	H1	J3	BC11
I/O	158	P167	J4	J4	K4	AU15
I/O	159	-	H3	J3	J2	BB14
I/O	160	-	H2	J2	L5	AT16
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	P166	GND*	GND*	GND*	GND*
I/O	161	P165	G1	K4	K3	BA13
I/O	162	-	-	-	-	AY14
VCCINT	-	P164	K4	VCCINT*	VCCINT*	VCCINT*
I/O, FCLK4	163	P163	J3	K2	L4	BC15
I/O	164	P162	J2	K1	K2	AW15
VCCIO	-	P161	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	165	-	-	-	M5	BA15
I/O	166	-	-	-	L3	AU17
I/O	167	P160	K3	L3	L1	BB16
I/O (D2)	168	P159	J1	L2	M4	AY16
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	169	-	-	M4	M3	AW17
I/O	170	-	-	M3	N5	AV18
I/O	171	-	-	-	M2	BA17
I/O	172	-	-	-	N4	BC17
I/O	173	-	L4	M2	N3	AU19
I/O	174	-	K2	M1	N2	BB18
I/O	175	-	L3	N4	P5	AY18
I/O	176	-	L2	N3	N1	AW19
GND	-	P158	GND*	GND*	GND*	GND*
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	177	-	-	-	-	-
I/O	178	-	-	-	-	-
I/O	179	-	-	N2	P4	AV20
I/O	180	-	-	N1	P3	AT20
I/O	181	-	L1	P4	P2	BB20
I/O	182	-	M4	P3	R5	AY20
I/O	183	P157	M3	P2	R4	BC21
I/O	184	P156	M2	R3	R3	BA21
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-

XC40110XV Pinout Table (Continued)

PAD NAME	EPIC PAD#	HQ240	BG352	BG432	BG560	PG559
I/O	185	P155	M1	R4	R1	AW21
I/O	186	-	-	-	T4	AU21
I/O	187	-	-	-	T5	BB22
I/O	188	-	-	-	-	AY22
I/O	189	-	-	-	-	-
I/O	190	-	-	-	-	-
VCCINT	-	P154	N3	VCCINT*	VCCINT*	VCCINT*
I/O (/RS)	191	P153	N4	R1	T2	AV22
I/O (D3)	192	P152	N2	T3	U3	BA23
GND	-	P151	-	GND*	GND*	GND*
VCCIO	-	P150	-	VCCIO*	VCCIO*	VCCIO*
I/O	193	P149	P1	T2	U4	AW23
I/O (D4)	194	P148	P2	T1	U5	AY24
I/O	195	-	-	-	-	-
I/O	196	-	-	-	-	-
I/O	197	-	-	-	U1	BC23
I/O	198	-	-	-	U2	BA27
I/O	199	P147	P3	U3	V2	AU23
I/O	200	P146	R1	U4	V4	AV24
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	-	-	GND*	GND*	GND*
I/O	201	P145	R2	U2	V5	AY26
I/O	202	P144	R3	U1	V3	BB24
I/O	203	-	R4	V3	W1	AW25
I/O	204	-	T1	V4	W3	BB26
I/O	205	-	-	V2	W4	AT24
I/O	206	-	-	W2	W5	BA29
I/O	207	-	-	-	-	-
I/O	208	-	-	-	-	-
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	P143	GND*	GND*	GND*	GND*
I/O	209	-	T2	W3	Y2	AY28
I/O	210	-	U2	W4	Y3	AU25
I/O	211	-	-	-	Y4	AV26
I/O	212	-	-	-	AA1	BC27
I/O	213	-	-	W1	Y5	AW27
I/O	214	-	-	Y1	AA3	BB28
I/O	215	-	T3	Y3	AA4	BA31
I/O	216	-	T4	Y4	AB2	AY30
VCCIO	-	-	-	VCCIO*	VCCIO*	VCCIO*
GND	-	-	-	GND*	GND*	GND*
I/O (/CS0)	217	P142	V1	Y2	AB3	AW29
I/O (D5)	218	P141	V2	AA2	AA5	BC29
I/O	219	-	-	-	AC1	AU27
I/O	220	-	-	-	AB4	BA33
VCCIO	-	P140	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	221	P139	U3	AA3	AC3	AY32
I/O, FCLK3	222	P138	U4	AB1	AB5	AW31
VCCINT	-	P137	W2	VCCINT*	VCCINT*	VCCINT*

XC40110XV Pinout Table (Continued)

PAD NAME	EPIC PAD#	HQ240	BG352	BG432	BG560	PG559
I/O	223	-	-	-	-	BB30
I/O	224	P136	V3	AB3	AC4	BA35
GND	-	P135	GND*	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	225	-	V4	AB4	AD3	AT28
I/O	226	-	Y1	AC2	AE1	AU29
I/O	227	P134	Y2	AD1	AC5	BC33
I/O	228	P133	W3	AC3	AE3	AY34
I/O	229	-	-	-	AD4	BB34
I/O	230	-	-	-	AF1	AW33
I/O	231	-	-	-	AF2	AU31
I/O	232	-	-	-	AD5	AV32
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	233	-	-	-	AG2	AT30
I/O	234	-	-	-	AE4	AU33
I/O	235	-	-	AC4	AF3	AW35
I/O	236	-	-	AD2	AH1	BC35
I/O	237	P132	W4	AE2	AE5	AY36
I/O	238	P131	AA1	AD3	AG3	BB36
I/O	239	P130	AA2	AD4	AF4	AV36
I/O (D6)	240	P129	Y3	AF1	AJ1	AU35
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	VCCIO*
I/O	241	-	AC1	AF2	AJ2	AT34
I/O	242	-	AB2	AE3	AF5	AW37
I/O	243	-	-	-	-	-
I/O	244	-	-	-	-	-
I/O	245	-	-	AE4	AH3	BC37
I/O	246	-	-	AG1	AG4	AY38
I/O	247	P128	AA3	AG2	AK2	BB38
I/O	248	P127	AA4	AF3	AJ3	BA41
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	249	-	-	-	-	-
I/O	250	-	-	-	-	-
I/O	251	-	AC2	AF4	AG5	AY40
I/O	252	-	AB3	AH1	AL1	BB40
I/O	253	P126	AD1	AH2	AH4	AT36
I/O	254	P125	AB4	AG3	AK3	BA39
I/O, GCK5	255	P124	AC3	AG4	AJ4	AV38
I/O (D7)	256	P123	AD2	AJ2	AH5	BC41
/PROGRAM	-	P122	AC4	AH3	AM1	BB42
VCCIO	-	P121	VCCIO*	VCCIO*	VCCIO*	VCCIO*
DONE	-	P120	AD3	AH4	AJ5	AY42
GND	-	P119	GND*	GND*	GND*	GND*
I/O, GCK4	257	P118	AC5	AJ4	AL4	AW41
I/O	258	P117	AD4	AK3	AJ6	AV40
VCCINT	-	P116	AE3	VCCINT*	VCCINT*	VCCINT*

XC40110XV Pinout Table (Continued)

PAD NAME	EPIC PAD#	HQ240	BG352	BG432	BG560	PG559
I/O	259	-	-	-	-	AV42
I/O	260	P115	AD5	AK4	AN3	AR37
I/O	261	-	-	AJ5	AK6	AP36
I/O	262	-	-	AH6	AL5	AT38
I/O	263	-	-	-	-	-
I/O	264	-	-	-	-	-
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	-	-	GND*	GND*	GND*
I/O	265	-	-	-	-	-
I/O	266	-	-	-	-	-
I/O	267	-	AC6	AL4	AJ7	AU39
I/O	268	-	AE4	AK5	AM4	AU43
I/O	269	P114	AF3	AJ6	AM5	BA43
I/O	270	P113	AF4	AH7	AK7	AT42
I/O	271	-	AC7	AL5	AL6	AR39
I/O	272	-	AD6	AK6	AJ8	AN37
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	-	GND*	GND*	GND*	GND*
I/O	273	P112	AE5	AH8	AM6	AT40
I/O	274	P111	AE6	AJ7	AN6	AP40
I/O	275	P110	AD7	AL6	AK8	AR43
I/O	276	P109	AE7	AK7	AL7	AN39
I/O	277	-	-	AH9	AJ9	AP42
I/O	278	-	-	AJ8	AN7	AM38
I/O	279	-	-	-	AL8	AN43
I/O	280	-	-	-	AK9	AL37
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	-	-	GND*	GND*	GND*
I/O	281	-	-	-	AM8	AK36
I/O	282	-	-	-	AJ10	AR41
I/O	283	-	-	-	AL9	AL41
I/O	284	-	-	-	AM9	AN41
I/O	285	P108	AF6	AK8	AK10	AK42
I/O	286	P107	AC9	AJ9	AN9	AM40
I/O	287	-	AD8	AH10	AJ11	AJ43
I/O	288	-	AE8	AL8	AL10	AJ37
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	P106	GND*	GND*	GND*	GND*
I/O	289	P105	AF7	AK9	AM10	AL39
I/O	290	-	-	-	-	AH36
VCCINT	-	P104	AC10	VCCINT*	VCCINT*	VCCINT*
I/O	291	P103	AD9	AK10	AL11	AH42
I/O	292	P102	AE9	AL10	AJ12	AJ39
VCCIO	-	P101	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	293	P100	AD10	AJ11	AN11	AK40
I/O	294	P99	AF9	AH12	AK12	AG41
I/O	295	-	-	-	AL12	AJ41
I/O	296	-	-	-	AM12	AH40
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-

XC40110XV Pinout Table (Continued)

PAD NAME	EPIC PAD#	HQ240	BG352	BG432	BG560	PG559
I/O	297	-	-	-	AJ13	AG37
I/O	298	-	-	-	AK13	AG43
I/O	299	-	-	AK11	AL13	AG39
I/O	300	-	-	AJ12	AM13	AF38
I/O	301	-	AC11	AK12	AN13	AF42
I/O	302	-	AE10	AL12	AJ14	AD42
I/O	303	-	AD11	AH13	AK14	AF40
I/O	304	-	AE11	AJ13	AL14	AE37
GND	-	P98	GND*	GND*	GND*	GND*
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	305	-	AF11	AK13	AM14	AE39
I/O	306	-	AC12	AL13	AN15	AD40
I/O	307	P97	AD12	AK14	AJ15	AC43
I/O	308	P96	AE12	AH14	AK15	AD38
I/O	309	P95	AF12	AJ14	AL15	AC41
I/O	310	P94	AD13	AK15	AM16	AD36
I/O	311	-	-	-	-	-
I/O	312	-	-	-	-	-
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	313	-	-	-	-	-
I/O	314	-	-	-	-	-
I/O	315	-	-	-	AL16	AC39
I/O	316	-	-	-	AJ16	AC37
I/O	317	-	-	AJ15	AK16	AB40
I/O	318	-	-	AL15	AN17	AB42
VCCINT	-	P93	AC13	VCCINT*	VCCINT*	VCCINT*
I/O	319	-	-	-	-	AB38
I/O	320	P92	AE13	AL16	AL17	AA41
GND	-	P91	GND*	GND*	GND*	GND*
VCCIO	-	P90	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O (/INIT)	321	P89	AF14	AK16	AJ17	AA39
I/O	322	P88	AE14	AJ16	AK17	AA37
I/O	323	-	-	AL17	AM18	Y40
I/O	324	-	-	AK17	AL18	Y38
I/O	325	-	-	-	AK18	AA43
I/O	326	-	-	-	AJ18	W39
I/O	327	-	-	-	-	-
I/O	328	-	-	-	-	-
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	-	-	GND*	GND*	GND*
I/O	329	-	-	-	-	-
I/O	330	-	-	-	-	-
I/O	331	P87	AD14	AJ17	AN19	V40
I/O	332	P86	AF15	AH17	AL19	Y36
I/O	333	P85	AE15	AK18	AK19	U41
I/O	334	P84	AD15	AL19	AM20	Y42
I/O	335	-	AC15	AJ18	AJ19	T40
I/O	336	-	AF16	AK19	AL20	W37
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*

XC40110XV Pinout Table (Continued)

PAD NAME	EPIC PAD#	HQ240	BG352	BG432	BG560	PG559
GND	-	P83	GND*	GND*	GND*	GND*
I/O	337	-	AE16	AH18	AK20	V38
I/O	338	-	AE17	AL20	AN21	U39
I/O	339	-	AD16	AJ19	AL21	V42
I/O	340	-	AC16	AK20	AJ20	R41
I/O	341	-	-	AH19	AM22	U43
I/O	342	-	-	AJ20	AK21	P40
I/O	343	-	-	-	AN23	T42
I/O	344	-	-	-	AL22	U37
VCCIO	-	-	-	VCCIO*	VCCIO*	VCCIO*
GND	-	-	-	GND*	GND*	GND*
I/O	345	-	-	-	AJ21	R39
I/O	346	-	-	-	AM23	N41
I/O	347	P82	AF18	AK21	AK22	R43
I/O	348	P81	AE18	AH20	AM24	M40
VCCIO	-	P80	VCCIO*	VCCIO*	VCCIO*	-
I/O	349	P79	AD17	AJ21	AL23	N39
I/O	350	P78	AC17	AL22	AJ22	T36
VCCINT	-	P77	AE19	VCCINT*	VCCINT*	VCCINT*
I/O	351	-	-	-	-	P42
I/O	352	P76	AD18	AJ22	AK23	R37
GND	-	P75	GND*	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	353	-	AC18	AK23	AL24	L41
I/O	354	-	AF20	AJ23	AN26	L43
I/O	355	P74	AE20	AH22	AJ23	K40
I/O	356	P73	AD19	AL24	AL25	K42
I/O	357	-	-	-	AK24	L39
I/O	358	-	-	-	AM26	J43
I/O	359	-	-	-	AM27	M38
I/O	360	-	-	-	AJ24	P36
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	361	-	-	-	AL26	N37
I/O	362	-	-	-	AK25	H42
I/O	363	-	-	AK24	AN28	J41
I/O	364	-	-	AH23	AN29	G43
I/O	365	P72	AC19	AJ24	AJ25	H40
I/O	366	P71	AF21	AK25	AL27	F42
I/O	367	P70	AE21	AJ25	AK26	J39
I/O	368	P69	AD20	AH24	AM29	L37
GND	-	-	GND*	GND*	GND*	GND*
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	369	-	AF23	AL26	AM30	E41
I/O	370	-	AE22	AK26	AJ26	F40
I/O	371	-	AD21	AH25	AL28	C43
I/O	372	-	AC21	AL27	AK27	G39
I/O	373	-	-	AJ26	AL29	D42
I/O	374	-	-	AK27	AN31	H38
I/O	375	-	-	-	-	-

XC40110XV Pinout Table (Continued)

PAD NAME	EPIC PAD#	HQ240	BG352	BG432	BG560	PG559
I/O	376	-	-	-	-	-
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	377	-	-	-	-	-
I/O	378	-	-	-	-	-
I/O (/LDC)	379	P68	AE23	AH26	AJ27	K36
I/O	380	P67	AD22	AL28	AM31	J37
I/O	381	P66	AF24	AJ27	AK28	B42
I/O	382	P65	AC22	AK28	AL30	D40
I/O (HDC)	383	P64	AD23	AH27	AK29	C41
I/O, GCK3	384	P63	AE24	AK29	AJ28	F38
I (M2)	-	P62	AC23	AJ28	AN32	H36
VCCIO	-	P61	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I (M0)	-	P60	AD24	AH28	AJ29	C39
GND	-	P59	GND*	GND*	GND*	GND*
O (M1)	-	P58	AB23	AH29	AK30	D38
I/O, GCK2	385	P57	AC24	AJ30	AH29	E37
I/O	386	P56	AD25	AH30	AJ30	B40
VCCINT	-	P55	AB24	VCCINT*	VCCINT*	VCCINT*
I/O	387	-	-	-	-	H34
I/O	388	P54	AA23	AH31	AH30	G35
I/O	389	-	AC25	AG29	AL33	F36
I/O	390	-	AD26	AG30	AG29	D36
I/O	391	-	-	-	-	-
I/O	392	-	-	-	-	-
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	-	-	GND*	GND*	GND*
I/O	393	P53	AC26	AF28	AJ31	E35
I/O	394	P52	Y23	AG31	AK32	A41
I/O	395	-	-	AF29	AG30	G33
I/O	396	-	-	AF30	AH31	B38
I/O	397	-	-	-	-	-
I/O	398	-	-	-	-	-
I/O	399	-	AA24	AE28	AF29	D34
I/O	400	-	AB25	AF31	AJ32	E33
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	-	GND*	GND*	GND*	GND*
I/O	401	P51	AA25	AE29	AH32	F32
I/O	402	P50	Y24	AE30	AF30	G31
I/O	403	P49	Y25	AD28	AG31	A37
I/O	404	P48	AA26	AD29	AE29	H30
I/O	405	-	-	AD30	AH33	B36
I/O	406	-	-	AD31	AG33	C33
I/O	407	-	-	-	AE30	C35
I/O	408	-	-	-	AF31	D32
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	-	-	GND*	GND*	GND*
I/O	409	-	-	-	AD29	E31
I/O	410	-	-	-	AF32	G29
I/O	411	-	-	-	AE31	A35

XC40110XV Pinout Table (Continued)

PAD NAME	EPIC PAD#	HQ240	BG352	BG432	BG560	PG559
I/O	412	-	-	-	AD30	H28
I/O	413	P47	V23	AC28	AE32	B34
I/O	414	P46	W24	AC29	AC29	C31
I/O	415	-	W25	AC30	AE33	A33
I/O	416	-	Y26	AB28	AD31	D30
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	P45	GND*	GND*	GND*	GND*
I/O, FCLK2	417	P44	U23	AB29	AC30	E29
I/O	418	-	-	-	-	C29
VCCINT	-	P43	V24	VCCINT*	VCCINT*	VCCINT*
I/O	419	P42	V25	AB31	AB29	B30
I/O	420	P41	U24	AA29	AC31	G27
VCCIO	-	P40	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	421	-	-	-	AC33	D28
I/O	422	-	-	-	AB30	A29
I/O	423	P39	V26	AA30	AB31	E27
I/O	424	P38	T23	Y28	AA29	F26
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	425	-	U25	Y29	AB32	C27
I/O	426	-	T24	Y30	AA30	B28
I/O	427	-	-	Y31	AA31	G25
I/O	428	-	-	W28	AA32	A27
I/O	429	-	-	-	Y29	D26
I/O	430	-	-	-	AA33	B26
I/O	431	-	T25	W29	Y30	E25
I/O	432	-	T26	W30	Y31	F24
GND	-	P37	GND*	GND*	GND*	GND*
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	433	-	-	-	-	-
I/O	434	-	-	-	-	-
I/O	435	-	-	W31	Y32	H24
I/O	436	-	-	V28	W29	B24
I/O	437	-	R23	V29	W30	D24
I/O	438	-	R24	V30	W31	A23
I/O	439	P36	R25	U29	W33	C23
I/O	440	P35	R26	U28	V30	E23
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	441	P34	P24	U30	V29	G23
I/O	442	P33	P23	U31	V31	B22
I/O	443	-	-	-	V32	D22
I/O	444	-	-	-	U33	A21
I/O	445	-	-	-	-	-
I/O	446	-	-	-	-	-
I/O	447	P32	P25	T29	U30	F22
I/O	448	P31	N26	T30	U29	C21
VCCIO	-	P30	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	P29	GND*	GND*	GND*	GND*

XC40110XV Pinout Table (Continued)

PAD NAME	EPIC PAD#	HQ240	BG352	BG432	BG560	PG559
I/O	449	P28	N25	T31	U31	E21
I/O	450	-	-	-	-	D20
VCCINT	-	P27	N24	VCCINT*	VCCINT*	VCCINT*
I/O	451	-	-	-	-	-
I/O	452	-	-	-	-	-
I/O	453	-	-	-	T32	C17
I/O	454	-	-	-	T30	G21
I/O	455	P26	M26	R28	T29	F20
I/O	456	P25	M25	R30	T31	D18
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	-	-	GND*	GND*	GND*
I/O	457	P24	M24	R31	R33	E19
I/O	458	P23	M23	P29	R31	B20
I/O	459	-	L26	P28	R30	H20
I/O	460	-	L25	P30	R29	B18
I/O	461	-	-	N30	P32	C15
I/O	462	-	-	N29	P31	D16
I/O	463	-	-	-	-	-
I/O	464	-	-	-	-	-
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	P22	GND*	GND*	GND*	GND*
I/O	465	-	K25	N28	N33	G19
I/O	466	-	L24	N31	P30	A17
I/O	467	-	L23	M31	P29	F18
I/O	468	-	J26	M29	M32	E17
I/O	469	-	-	-	N31	B16
I/O	470	-	-	-	N30	C13
I/O	471	-	-	M28	L33	A15
I/O	472	-	-	M30	N29	D14
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	-	-	GND*	GND*	GND*
I/O	473	P21	J25	L30	M31	E15
I/O	474	P20	K24	L29	L32	G17
I/O	475	-	-	-	M30	B14
I/O	476	-	-	-	L31	C11
VCCIO	-	P19	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	477	P18	K23	K31	M29	D12
I/O (TMS)	478	P17	H25	K30	J33	A11
VCCINT	-	P16	J24	VCCINT*	VCCINT*	VCCINT*
I/O	479	-	-	-	-	E13
I/O, FCLK1	480	P15	J23	K28	L30	C9
GND	-	P14	GND*	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	481	-	G26	J30	K31	H16
I/O	482	-	G25	H31	L29	B10
I/O	483	P13	H24	J29	H33	G15
I/O	484	P12	H23	J28	K30	A9
I/O	485	-	-	-	J31	D10
I/O	486	-	-	-	H32	B8

XC40110XV Pinout Table (Continued)

PAD NAME	EPIC PAD#	HQ240	BG352	BG432	BG560	PG559
I/O	487	P11	F26	-	K29	E11
I/O	488	P10	F25	-	H31	G13
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	489	P9	G24	H30	J30	F12
I/O	490	P8	D26	G30	G32	H14
I/O	491	-	-	H29	F33	G11
I/O	492	-	-	H28	J29	A7
I/O	493	-	-	F31	G31	E9
I/O	494	-	-	F30	H30	B6
I/O	495	-	-	-	E33	D8
I/O	496	-	-	-	E32	F8
GND	-	-	GND*	GND*	GND*	GND*
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	497	-	E25	G29	H29	G9
I/O	498	-	F24	G28	F31	H10
I/O	499	-	F23	E31	G30	B4
I/O	500	-	D25	E30	D32	E7
I/O	501	-	-	F29	E31	C5
I/O	502	-	-	F28	G29	D6
I/O	503	-	-	-	-	-
I/O	504	-	-	-	-	-
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	505	-	-	-	-	-
I/O	506	-	-	-	-	-
I/O (TCK)	507	P7	E24	D31	C33	D4
I/O (TDI)	508	P6	C26	D30	F30	H8
I/O	509	P5	E23	E29	D31	A3
I/O	510	-	-	-	-	F6
VCCINT	-	P4	D24	VCCINT*	VCCINT*	VCCINT*
I/O (A17)	511	P3	C25	C30	F29	C3
I/O, GCK1 (A16)	512	P2	D23	D29	B33	C1
GND	-	P1	GND*	GND*	GND*	GND*
VCCIO	-	-	A10	A1	A4	A13
VCCIO	-	-	A17	A11	A10	A31
VCCIO	-	-	AC14	A21	A16	A43
VCCIO	-	-	AC20	A31	A22	B2
VCCIO	-	-	AC8	D11	A26	C7
VCCIO	-	-	AF10	D21	A30	C19
VCCIO	-	-	AF17	L1	B2	C25
VCCIO	-	-	D7	L4	B13	C37
VCCIO	-	-	D13	L28	B19	F14
VCCIO	-	-	D19	L31	B32	F30
VCCIO	-	-	G23	AA1	C3	G3
VCCIO	-	-	H4	AA4	C31	G7
VCCIO	-	-	K1	AA28	C32	G37
VCCIO	-	-	K26	AA31	D1	G41
VCCIO	-	-	N23	AH11	D33	N1

XC40110XV Pinout Table (Continued)

PAD NAME	EPIC PAD#	HQ240	BG352	BG432	BG560	PG559
VCCIO	-	-	P4	AH21	E5	N43
VCCIO	-	-	U1	AL1	H1	P6
VCCIO	-	-	U26	AL11	K33	P38
VCCIO	-	-	W23	AL21	M1	W3
VCCIO	-	-	Y4	AL31	N32	W41
VCCIO	-	-	B2	C3	R2	AE3
VCCIO	-	-	B25	C29	T33	AE41
VCCIO	-	-	AE2	AJ3	V1	AK6
VCCIO	-	-	AE25	AJ29	W32	AK38
VCCIO	-	-	-	-	AA2	AL1
VCCIO	-	-	-	-	AB33	AL43
VCCIO	-	-	-	-	AD1	AU3
VCCIO	-	-	-	-	AF33	AU7
VCCIO	-	-	-	-	AK1	AU37
VCCIO	-	-	-	-	AK4	AU41
VCCIO	-	-	-	-	AK33	AV14
VCCIO	-	-	-	-	AL2	AV30
VCCIO	-	-	-	-	AL3	BA7
VCCIO	-	-	-	-	AL31	BA19
VCCIO	-	-	-	-	AM2	BA25
VCCIO	-	-	-	-	AM15	BA37
VCCIO	-	-	-	-	AM21	BC1
VCCIO	-	-	-	-	AM32	BC13
VCCIO	-	-	-	-	AN4	BC31
VCCIO	-	-	-	-	AN8	BC43
VCCIO	-	-	-	-	AN12	-
VCCIO	-	-	-	-	AN18	-
VCCIO	-	-	-	-	AN24	-
VCCIO	-	-	-	-	AN30	-
VCCINT	-	-	-	A10	E12	H12
VCCINT	-	-	-	AB2	AD2	H18
VCCINT	-	-	-	AB30	AD32	H26
VCCINT	-	-	-	AG28	AK31	H32
VCCINT	-	-	-	AH15	AM17	M8
VCCINT	-	-	-	AH5	AK5	M36
VCCINT	-	-	-	AJ10	AK11	V8
VCCINT	-	-	-	AK22	AN25	V36
VCCINT	-	-	-	B23	C24	AF8
VCCINT	-	-	-	B4	D6	AF36
VCCINT	-	-	-	C16	C17	AM8
VCCINT	-	-	-	E28	E30	AM36
VCCINT	-	-	-	K29	K32	AT12
VCCINT	-	-	-	K3	J1	AT18
VCCINT	-	-	-	R2	T3	AT26
VCCINT	-	-	-	R29	U32	AT32
GND	-	-	A1	A2	A7	A5
GND	-	-	A14	A3	A12	A19
GND	-	-	A19	A7	A14	A25

XC40110XV Pinout Table (Continued)

PAD NAME	EPIC PAD#	HQ240	BG352	BG432	BG560	PG559
GND	-	-	A2	A9	A18	A39
GND	-	-	A22	A14	A20	B12
GND	-	-	A25	A18	A24	B32
GND	-	-	A26	A23	A29	E1
GND	-	-	A5	A25	A32	E5
GND	-	-	A8	A29	B1	E39
GND	-	-	AB1	A30	B6	E43
GND	-	-	AB26	B1	B9	F10
GND	-	-	AE1	B2	B15	F16
GND	-	-	AE26	B30	B23	F28
GND	-	-	AF1	B31	B27	F34
GND	-	-	AF13	C1	B31	H22
GND	-	-	AF19	C31	C2	K6
GND	-	-	AF2	D16	E1	K38
GND	-	-	AF22	G1	F32	M2
GND	-	-	AF25	G31	G2	M42
GND	-	-	AF26	J1	G33	T6
GND	-	-	AF5	J31	J32	T38
GND	-	-	AF8	P1	K1	W1
GND	-	-	B1	P31	L2	W43
GND	-	-	B26	T4	M33	AB8
GND	-	-	E1	T28	P1	AB36
GND	-	-	E26	V1	P33	AE1
GND	-	-	H1	V31	R32	AE43
GND	-	-	H26	AC1	T1	AH6
GND	-	-	N1	AC31	V33	AH38
GND	-	-	P26	AE1	W2	AM2
GND	-	-	W1	AE31	Y1	AM42
GND	-	-	W26	AH16	Y33	AP6
GND	-	-	-	AJ1	AB1	AP38
GND	-	-	-	AJ31	AC32	AT22
GND	-	-	-	AK1	AD33	AV10
GND	-	-	-	AK2	AE2	AV16
GND	-	-	-	AK30	AG1	AV28
GND	-	-	-	AK31	AG32	AV34
GND	-	-	-	AL2	AH2	AW1
GND	-	-	-	AL3	AJ33	AW5
GND	-	-	-	AL7	AL32	AW39
GND	-	-	-	AL9	AM3	AW43
GND	-	-	-	AL14	AM11	BB12
GND	-	-	-	AL18	AM19	BB32
GND	-	-	-	AL23	AM25	BC5
GND	-	-	-	AL25	AM28	BC19
GND	-	-	-	AL29	AM33	BC25
GND	-	-	-	AL30	AM7	BC39
GND	-	-	-	-	AN2	-
GND	-	-	-	-	AN5	-
GND	-	-	-	-	AN10	-
GND	-	-	-	-	AN14	-
GND	-	-	-	-	AN16	-

XC40110XV Pinout Table (Continued)

PAD NAME	EPIC PAD#	HQ240	BG352	BG432	BG560	PG559
GND	-	-	-	-	AN20	-
GND	-	-	-	-	AN22	-
GND	-	-	-	-	AN27	-
NC	-	P204	C8	C8	A1	-
NC	-	P219	-	-	A33	-
NC	-	-	-	-	AC2	-
NC	-	-	-	-	AN1	-
NC	-	-	-	-	AN33	-

XC40150XV Pinout Table

PAD NAME	EPIC PAD #	HQ240	BG352	BG432	BG560	PG559
VCCIO	-	P240	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O, GCK8 (A15)	1	P239	C24	D28	E29	E3
I/O (A14)	2	P238	D22	C28	D30	F4
I/O	3	P237	C23	B29	E28	J7
I/O	4	P236	B24	D27	D29	D2
I/O	5	P235	C22	B28	C30	K8
I/O	6	P234	D21	C27	D28	H6
I/O	7	-	-	-	-	-
I/O	8	-	-	-	-	-
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	-	-	GND*	GND*	GND*
I/O	9	-	-	-	-	-
I/O	10	-	-	-	-	-
I/O	11	-	-	-	-	-
I/O	12	-	-	-	-	-
I/O	13	-	-	D26	A31	G5
I/O	14	-	-	A28	E27	F2
I/O	15	-	B23	B27	C29	H4
I/O	16	-	A24	C26	B30	G1
I/O	17	-	A23	D25	D27	J5
I/O	18	-	D20	A27	C28	L7
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	-	GND*	GND*	GND*	GND*
I/O (A13)	19	P233	C21	B26	E26	J3
I/O (A12)	20	P232	B22	D24	B29	K4
I/O	21	P231	B21	C25	B28	H2
I/O	22	P230	C20	A26	D26	L5
I/O	23	-	-	B25	C27	J1
I/O	24	-	-	D23	E25	M6
I/O	25	-	-	-	A28	K2
I/O	26	-	-	-	A27	N7
I/O	27	-	-	-	-	-
I/O	28	-	-	-	-	-
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	-	-	GND*	GND*	GND*
I/O	29	-	-	-	D25	P8
I/O	30	-	-	-	C26	L3
I/O	31	-	-	-	E24	L1
I/O	32	-	-	-	B26	M4
I/O	33	P229	B20	C24	C25	P2
I/O	34	P228	A21	B24	D24	N5
I/O	35	-	D18	C23	B25	R1
I/O	36	-	C19	D22	E23	N3
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	P227	GND*	GND*	GND*	GND*
I/O	37	P226	B19	A24	A25	R7
I/O	38	-	-	-	-	P4
VCCINT	-	P225	A20	VCCINT*	VCCINT*	VCCINT*
I/O	39	P224	D17	C22	D23	T2
I/O	40	P223	C18	B22	B24	T8
VCCIO	-	P222	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	41	-	B18	A22	E22	R5
I/O	42	-	C17	C21	C23	R3
I/O	43	-	-	-	A23	U1

XC40150XV Pinout Table (Continued)

PAD NAME	EPIC PAD #	HQ240	BG352	BG432	BG560	PG559
I/O	44	-	-	-	D22	T4
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	45	-	-	-	-	-
I/O	46	-	-	-	-	-
I/O	47	-	-	-	C22	U5
I/O	48	-	-	-	E21	V2
I/O	49	-	-	D20	B22	U7
I/O	50	-	-	B21	D21	U3
I/O	51	-	A18	C20	C21	Y2
I/O	52	-	D16	B20	B21	V4
I/O	53	-	B17	A20	E20	V6
I/O	54	-	C16	D19	A21	W5
GND	-	-	GND*	GND*	GND*	GND*
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O (A11)	55	P221	B16	C19	D20	W7
I/O (A10)	56	P220	A16	B19	C20	Y4
I/O	57	P218	D15	A19	B20	AA1
I/O	58	P217	C15	B18	E19	Y6
I/O (A18)	59	P216	B15	D18	D19	AB2
I/O (A19)	60	P215	A15	C18	C19	Y8
I/O	61	-	-	-	-	-
I/O	62	-	-	-	-	-
I/O	63	-	-	-	-	-
I/O	64	-	-	-	-	-
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	65	-	-	-	-	-
I/O	66	-	-	-	-	-
I/O	67	-	-	-	A19	AA3
I/O	68	-	-	-	D18	AA5
I/O	69	-	-	B17	E18	AC1
I/O	70	-	-	C17	C18	AA7
I/O (A9)	71	P214	C14	A17	B18	AB4
I/O (A8)	72	P213	D14	D17	A17	AB6
VCCIO	-	P212	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	P211	GND*	GND*	GND*	GND*
I/O (A7)	73	P210	B14	A16	D17	AC3
I/O (A6)	74	P209	A13	B16	E17	AC5
VCCINT	-	-	-	VCCINT*	VCCINT*	VCCINT*
I/O	75	-	-	-	-	AD2
I/O	76	-	-	A15	B17	AC7
I/O	77	-	-	-	B16	AF2
I/O	78	-	-	-	D16	AD4
I/O	79	-	-	-	-	-
I/O	80	-	-	-	-	-
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	-	-	GND*	GND*	GND*
I/O	81	-	-	-	-	-
I/O	82	-	-	-	-	-
I/O	83	-	-	-	-	-
I/O	84	-	-	-	-	-
I/O (A20)	85	P208	B13	B15	E16	AD6
I/O (A21)	86	P207	C13	C15	C16	AE5
I/O	87	P206	A12	D15	A15	AF4
I/O	88	P205	B12	B14	C15	AG1

XC40150XV Pinout Table (Continued)

PAD NAME	EPIC PAD #	HQ240	BG352	BG432	BG560	PG559
I/O (A5)	89	P203	C12	A13	D15	AD8
I/O (A4)	90	P202	D12	C14	E15	AG3
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	-	GND*	GND*	GND*	GND*
I/O	91	-	A11	B13	B14	AH4
I/O	92	-	B11	D14	C14	AE7
I/O	93	-	B10	A12	D14	AH2
I/O	94	-	C11	C13	A13	AF6
I/O	95	-	-	B12	E14	AJ1
I/O	96	-	-	D13	C13	AG5
I/O	97	-	-	-	D13	AJ3
I/O	98	-	-	-	B12	AK4
I/O	99	-	-	-	-	-
I/O	100	-	-	-	-	-
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	-	-	GND*	GND*	GND*
I/O	101	-	-	-	C12	AG7
I/O	102	-	-	-	E13	AK2
I/O	103	0	D11	C12	A11	AJ5
I/O	104	0	A9	B11	D12	AL3
VCCIO	-	P201	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	105	P200	B9	D12	B11	AM4
I/O	106	P199	C10	C11	C11	AN1
VCCINT	-	P198	D10	VCCINT*	VCCINT*	VCCINT*
I/O	107	-	-	-	-	AL5
I/O	108	P197	B8	B10	B10	AH8
GND	-	P196	GND*	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO	VCCIO*	-
I/O	109	-	C9	C10	D11	AJ7
I/O	110	P195	D9	B9	C10	AP2
I/O	111	P194	A7	C9	A9	AN3
I/O	112	P193	B7	D10	E11	AP4
I/O	113	-	-	-	C9	AR1
I/O	114	-	-	-	D10	AN5
I/O	115	-	-	-	A8	AM6
I/O	116	-	-	-	B8	AK8
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	117	-	-	-	-	-
I/O	118	-	-	-	-	-
I/O	119	-	-	-	E10	AL7
I/O	120	-	-	-	C8	AT2
I/O	121	-	-	A8	D9	AR3
I/O	122	-	-	B8	B7	AU1
I/O	123	P192	D8	D9	A6	AT4
I/O	124	P191	A6	B7	E9	AV2
I/O	125	P190	B6	C7	C7	AR5
I/O	126	P189	C7	D8	D8	AN7
GND	-	-	GND*	GND*	GND*	GND*
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	127	-	A4	A6	A5	AW3
I/O	128	-	B5	B6	B5	AV4
I/O (A3)	129	P188	C6	D7	E8	BA1
I/O, (CS1, A2)	130	P187	D6	A5	C6	AU5
I/O	131	-	B4	C6	D7	AY2

XC40150XV Pinout Table (Continued)

PAD NAME	EPIC PAD #	HQ240	BG352	BG432	BG560	PG559
I/O	132	-	C5	B5	B4	AT6
I/O	133	-	-	-	-	-
I/O	134	-	-	-	-	-
I/O	135	-	-	-	-	-
I/O	136	-	-	-	-	-
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	137	-	-	-	-	-
I/O	138	-	-	-	-	-
I/O	139	-	-	D6	C5	AP8
I/O	140	-	-	A4	E7	AR7
I/O	141	-	-	C5	A3	AY4
I/O	142	P186	A3	-	-	BB2
VCCINT	-	P185	D5	VCCINT*	VCCINT*	VCCINT*
I/O, GCK7 (A1)	143	P184	C4	D5	A2	AV6
I/O (A0, /WS)	144	P183	B3	B3	D5	AT8
GND	-	P182	GND*	GND*	GND*	GND*
O, TDO	-	P181	D4	C4	E6	BA3
VCCIO	-	P180	-	VCCIO*	VCCIO*	VCCIO*
CCLK	-	P179	C3	D4	C4	BA5
I/O, GCK6 (DOUT)	145	P178	E4	D3	D4	BB4
I/O (D0, DIN)	146	P177	D3	C2	E4	AY6
I/O	147	P176	C2	D2	F5	BC3
I/O	148	P175	E3	E4	B3	AW7
I/O	149	-	F4	D1	D3	BB6
I/O	150	-	D2	E3	F4	AU9
I/O	151	-	-	-	-	-
I/O	152	-	-	-	-	-
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	-	-	GND*	GND*	GND*
I/O	153	-	-	-	-	-
I/O	154	-	-	-	-	-
I/O	155	-	-	E2	C1	AT10
I/O	156	-	-	F4	G5	AV8
I/O	157	-	C1	E1	E3	AY8
I/O	158	-	D1	F3	D2	BC7
I/O	159	-	-	-	-	-
I/O	160	-	-	-	-	-
I/O (/RCK, RDY_/BUSY)	161	P174	G4	F2	G4	AW9
I/O (D1)	162	P173	F3	G4	F3	BA9
VCCIO	-	-	-	VCCIO*	VCCIO*	VCCIO*
GND	-	-	-	GND*	GND*	GND*
I/O	163	-	-	-	-	-
I/O	164	-	-	-	-	-
I/O	165	-	-	F1	H5	AU11
I/O	166	-	-	G3	E2	AY10
I/O	167	-	-	G2	F2	BB8
I/O	168	-	-	H4	H4	AW11
I/O	169	P172	E2	H3	G3	BC9
I/O	170	P171	F2	H2	J5	AV12
I/O	171	P170	G3	-	F1	AU13
I/O	172	P169	G2	-	G1	AT14
VCCIO	-	-	-	VCCIO*	VCCIO*	VCCIO*
GND	-	-	-	GND*	GND*	GND*

XC40150XV Pinout Table (Continued)

PAD NAME	EPIC PAD #	HQ240	BG352	BG432	BG560	PG559
I/O	173	-	-	-	J4	BA11
I/O	174	-	-	-	H3	AY12
I/O	175	-	-	-	K5	BB10
I/O	176	-	-	-	H2	AW13
I/O	177	P168	F1	H1	J3	BC11
I/O	178	P167	J4	J4	K4	AU15
I/O	179	-	H3	J3	J2	BB14
I/O	180	-	H2	J2	L5	AT16
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	P166	GND*	GND*	GND*	GND*
I/O	181	P165	G1	K4	K3	BA13
I/O	182	-	-	-	-	AY14
VCCINT	-	P164	K4	VCCINT*	VCCINT*	VCCINT*
I/O, FCLK4	183	P163	J3	K2	L4	BC15
I/O	184	P162	J2	K1	K2	AW15
VCCIO	-	P161	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	185	-	-	-	M5	BA15
I/O	186	-	-	-	L3	AU17
I/O	187	P160	K3	L3	L1	BB16
I/O (D2)	188	P159	J1	L2	M4	AY16
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	189	-	-	M4	M3	AW17
I/O	190	-	-	M3	N5	AV18
I/O	191	-	-	-	M2	BA17
I/O	192	-	-	-	N4	BC17
I/O	193	-	-	-	-	-
I/O	194	-	-	-	-	-
I/O	195	-	L4	M2	N3	AU19
I/O	196	-	K2	M1	N2	BB18
I/O	197	-	L3	N4	P5	AY18
I/O	198	-	L2	N3	N1	AW19
GND	-	P158	GND*	GND*	GND*	GND*
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	199	-	-	-	-	-
I/O	200	-	-	-	-	-
I/O	201	-	-	-	-	-
I/O	202	-	-	-	-	-
I/O	203	-	-	N2	P4	AV20
I/O	204	-	-	N1	P3	AT20
I/O	205	-	L1	P4	P2	BB20
I/O	206	-	M4	P3	R5	AY20
I/O	207	P157	M3	P2	R4	BC21
I/O	208	P156	M2	R3	R3	BA21
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	209	P155	M1	R4	R1	AW21
I/O	210	-	-	-	T4	AU21
I/O	211	-	-	-	T5	BB22
I/O	212	-	-	-	-	AY22
I/O	213	-	-	-	-	-
I/O	214	-	-	-	-	-
VCCINT	-	P154	N3	VCCINT*	VCCINT*	VCCINT*
I/O (/RS)	215	P153	N4	R1	T2	AV22
I/O (D3)	216	P152	N2	T3	U3	BA23
GND	-	P151	-	GND*	GND*	GND*

XC40150XV Pinout Table (Continued)

PAD NAME	EPIC PAD #	HQ240	BG352	BG432	BG560	PG559
VCCIO	-	P150	-	VCCIO*	VCCIO*	VCCIO*
I/O	217	P149	P1	T2	U4	AW23
I/O (D4)	218	P148	P2	T1	U5	AY24
I/O	219	-	-	-	-	-
I/O	220	-	-	-	-	-
I/O	221	-	-	-	U1	BC23
I/O	222	-	-	-	U2	BA27
I/O	223	P147	P3	U3	V2	AU23
I/O	224	P146	R1	U4	V4	AV24
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	-	-	GND*	GND*	GND*
I/O	225	P145	R2	U2	V5	AY26
I/O	226	P144	R3	U1	V3	BB24
I/O	227	-	R4	V3	W1	AW25
I/O	228	-	T1	V4	W3	BB26
I/O	229	-	-	V2	W4	AT24
I/O	230	-	-	W2	W5	BA29
I/O	231	-	-	-	-	-
I/O	232	-	-	-	-	-
I/O	233	-	-	-	-	-
I/O	234	-	-	-	-	-
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	P143	GND*	GND*	GND*	GND*
I/O	235	-	T2	W3	Y2	AY28
I/O	236	-	U2	W4	Y3	AU25
I/O	237	-	-	-	Y4	AV26
I/O	238	-	-	-	AA1	BC27
I/O	239	-	-	-	-	-
I/O	240	-	-	-	-	-
I/O	241	-	-	W1	Y5	AW27
I/O	242	-	-	Y1	AA3	BB28
I/O	243	-	T3	Y3	AA4	BA31
I/O	244	-	T4	Y4	AB2	AY30
VCCIO	-	-	-	VCCIO*	VCCIO*	VCCIO*
GND	-	-	-	GND*	GND*	GND*
I/O (/CS0)	245	P142	V1	Y2	AB3	AW29
I/O (D5)	246	P141	V2	AA2	AA5	BC29
I/O	247	-	-	-	AC1	AU27
I/O	248	-	-	-	AB4	BA33
VCCIO	-	P140	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	249	P139	U3	AA3	AC3	AY32
I/O, FCLK3	250	P138	U4	AB1	AB5	AW31
VCCINT	-	P137	W2	VCCINT*	VCCINT*	VCCINT*
I/O	251	-	-	-	-	BB30
I/O	252	P136	V3	AB3	AC4	BA35
GND	-	P135	GND*	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	253	-	V4	AB4	AD3	AT28
I/O	254	-	Y1	AC2	AE1	AU29
I/O	255	P134	Y2	AD1	AC5	BC33
I/O	256	P133	W3	AC3	AE3	AY34
I/O	257	-	-	-	AD4	BB34
I/O	258	-	-	-	AF1	AW33
I/O	259	-	-	-	AF2	AU31
I/O	260	-	-	-	AD5	AV32
GND	-	-	-	GND*	GND*	GND*

XC40150XV Pinout Table (Continued)

PAD NAME	EPIC PAD #	HQ240	BG352	BG432	BG560	PG559
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	261	-	-	-	-	-
I/O	262	-	-	-	-	-
I/O	263	-	-	-	AG2	AT30
I/O	264	-	-	-	AE4	AU33
I/O	265	-	-	AC4	AF3	AW35
I/O	266	-	-	AD2	AH1	BC35
I/O	267	P132	W4	AE2	AE5	AY36
I/O	268	P131	AA1	AD3	AG3	BB36
I/O	269	P130	AA2	AD4	AF4	AV36
I/O (D6)	270	P129	Y3	AF1	AJ1	AU35
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	VCCIO*
I/O	271	-	AC1	AF2	AJ2	AT34
I/O	272	-	AB2	AE3	AF5	AW37
I/O	273	-	-	-	-	-
I/O	274	-	-	-	-	-
I/O	275	-	-	-	-	-
I/O	276	-	-	-	-	-
I/O	277	-	-	AE4	AH3	BC37
I/O	278	-	-	AG1	AG4	AY38
I/O	279	P128	AA3	AG2	AK2	BB38
I/O	280	P127	AA4	AF3	AJ3	BA41
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	281	-	-	-	-	-
I/O	282	-	-	-	-	-
I/O	283	-	AC2	AF4	AG5	AY40
I/O	284	-	AB3	AH1	AL1	BB40
I/O	285	P126	AD1	AH2	AH4	AT36
I/O	286	P125	AB4	AG3	AK3	BA39
I/O, GCK5	287	P124	AC3	AG4	AJ4	AV38
I/O (D7)	288	P123	AD2	AJ2	AH5	BC41
/PROGRAM	-	P122	AC4	AH3	AM1	BB42
VCCIO	-	P121	VCCIO*	VCCIO*	VCCIO*	VCCIO*
DONE	-	P120	AD3	AH4	AJ5	AY42
GND	-	P119	GND*	GND*	GND*	GND*
I/O, GCK4	289	P118	AC5	AJ4	AL4	AW41
I/O	290	P117	AD4	AK3	AJ6	AV40
VCCINT	-	P116	AE3	VCCINT*	VCCINT*	VCCINT*
I/O	291	-	-	-	-	AV42
I/O	292	P115	AD5	AK4	AN3	AR37
I/O	293	-	-	AJ5	AK6	AP36
I/O	294	-	-	AH6	AL5	AT38
I/O	295	-	-	-	-	-
I/O	296	-	-	-	-	-
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	-	-	GND*	GND*	GND*
I/O	297	-	-	-	-	-
I/O	298	-	-	-	-	-
I/O	299	-	-	-	-	-
I/O	300	-	-	-	-	-
I/O	301	-	AC6	AL4	AJ7	AU39
I/O	302	-	AE4	AK5	AM4	AU43
I/O	303	P114	AF3	AJ6	AM5	BA43
I/O	304	P113	AF4	AH7	AK7	AT42

XC40150XV Pinout Table (Continued)

PAD NAME	EPIC PAD #	HQ240	BG352	BG432	BG560	PG559
I/O	305	-	AC7	AL5	AL6	AR39
I/O	306	-	AD6	AK6	AJ8	AN37
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	-	GND*	GND*	GND*	GND*
I/O	307	P112	AE5	AH8	AM6	AT40
I/O	308	P111	AE6	AJ7	AN6	AP40
I/O	309	P110	AD7	AL6	AK8	AR43
I/O	310	P109	AE7	AK7	AL7	AN39
I/O	311	-	-	AH9	AJ9	AP42
I/O	312	-	-	AJ8	AN7	AM38
I/O	313	-	-	-	AL8	AN43
I/O	314	-	-	-	AK9	AL37
I/O	315	-	-	-	-	-
I/O	316	-	-	-	-	-
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	-	-	GND*	GND*	GND*
I/O	317	-	-	-	AM8	AK36
I/O	318	-	-	-	AJ10	AR41
I/O	319	-	-	-	AL9	AL41
I/O	320	-	-	-	AM9	AN41
I/O	321	P108	AF6	AK8	AK10	AK42
I/O	322	P107	AC9	AJ9	AN9	AM40
I/O	323	-	AD8	AH10	AJ11	AJ43
I/O	324	-	AE8	AL8	AL10	AJ37
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	P106	GND*	GND*	GND*	GND*
I/O	325	P105	AF7	AK9	AM10	AL39
I/O	326	-	-	-	-	AH36
VCCINT	-	P104	AC10	VCCINT*	VCCINT*	VCCINT*
I/O	327	P103	AD9	AK10	AL11	AH42
I/O	328	P102	AE9	AL10	AJ12	AJ39
VCCIO	-	P101	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	329	P100	AD10	AJ11	AN11	AK40
I/O	330	P99	AF9	AH12	AK12	AG41
I/O	331	-	-	-	AL12	AJ41
I/O	332	-	-	-	AM12	AH40
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	333	-	-	-	-	-
I/O	334	-	-	-	-	-
I/O	335	-	-	-	AJ13	AG37
I/O	336	-	-	-	AK13	AG43
I/O	337	-	-	AK11	AL13	AG39
I/O	338	-	-	AJ12	AM13	AF38
I/O	339	-	AC11	AK12	AN13	AF42
I/O	340	-	AE10	AL12	AJ14	AD42
I/O	341	-	AD11	AH13	AK14	AF40
I/O	342	-	AE11	AJ13	AL14	AE37
GND	-	P98	GND*	GND*	GND*	GND*
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	343	-	AF11	AK13	AM14	AE39
I/O	344	-	AC12	AL13	AN15	AD40
I/O	345	P97	AD12	AK14	AJ15	AC43
I/O	346	P96	AE12	AH14	AK15	AD38
I/O	347	P95	AF12	AJ14	AL15	AC41
I/O	348	P94	AD13	AK15	AM16	AD36

XC40150XV Pinout Table (Continued)

PAD NAME	EPIC PAD #	HQ240	BG352	BG432	BG560	PG559
I/O	349	-	-	-	-	-
I/O	350	-	-	-	-	-
I/O	351	-	-	-	-	-
I/O	352	-	-	-	-	-
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	353	-	-	-	-	-
I/O	354	-	-	-	-	-
I/O	355	-	-	-	AL16	AC39
I/O	356	-	-	-	AJ16	AC37
I/O	357	-	-	AJ15	AK16	AB40
I/O	358	-	-	AL15	AN17	AB42
VCCINT	-	P93	AC13	VCCINT*	VCCINT*	VCCINT*
I/O	359	-	-	-	-	AB38
I/O	360	P92	AE13	AL16	AL17	AA41
GND	-	P91	GND*	GND*	GND*	GND*
VCCIO	-	P90	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O (/INIT)	361	P89	AF14	AK16	AJ17	AA39
I/O	362	P88	AE14	AJ16	AK17	AA37
I/O	363	-	-	AL17	AM18	Y40
I/O	364	-	-	AK17	AL18	Y38
I/O	365	-	-	-	AK18	AA43
I/O	366	-	-	-	AJ18	W39
I/O	367	-	-	-	-	-
I/O	368	-	-	-	-	-
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	-	-	GND*	GND*	GND*
I/O	369	-	-	-	-	-
I/O	370	-	-	-	-	-
I/O	371	-	-	-	-	-
I/O	372	-	-	-	-	-
I/O	373	P87	AD14	AJ17	AN19	V40
I/O	374	P86	AF15	AH17	AL19	Y36
I/O	375	P85	AE15	AK18	AK19	U41
I/O	376	P84	AD15	AL19	AM20	Y42
I/O	377	-	AC15	AJ18	AJ19	T40
I/O	378	-	AF16	AK19	AL20	W37
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	P83	GND*	GND*	GND*	GND*
I/O	379	-	AE16	AH18	AK20	V38
I/O	380	-	AE17	AL20	AN21	U39
I/O	381	-	AD16	AJ19	AL21	V42
I/O	382	-	AC16	AK20	AJ20	R41
I/O	383	-	-	AH19	AM22	U43
I/O	384	-	-	AJ20	AK21	P40
I/O	385	-	-	-	AN23	T42
I/O	386	-	-	-	AL22	U37
I/O	387	-	-	-	-	-
I/O	388	-	-	-	-	-
VCCIO	-	-	-	VCCIO*	VCCIO*	VCCIO*
GND	-	-	-	GND*	GND*	GND*
I/O	389	-	-	-	AJ21	R39
I/O	390	-	-	-	AM23	N41
I/O	391	P82	AF18	AK21	AK22	R43
I/O	392	P81	AE18	AH20	AM24	M40
VCCIO	-	P80	VCCIO*	VCCIO*	VCCIO*	-

XC40150XV Pinout Table (Continued)

PAD NAME	EPIC PAD #	HQ240	BG352	BG432	BG560	PG559
I/O	393	P79	AD17	AJ21	AL23	N39
I/O	394	P78	AC17	AL22	AJ22	T36
VCCINT	-	P77	AE19	VCCINT*	VCCINT*	VCCINT*
I/O	395	-	-	-	-	P42
I/O	396	P76	AD18	AJ22	AK23	R37
GND	-	P75	GND*	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	397	-	AC18	AK23	AL24	L41
I/O	398	-	AF20	AJ23	AN26	L43
I/O	399	P74	AE20	AH22	AJ23	K40
I/O	400	P73	AD19	AL24	AL25	K42
I/O	401	-	-	-	AK24	L39
I/O	402	-	-	-	AM26	J43
I/O	403	-	-	-	AM27	M38
I/O	404	-	-	-	AJ24	P36
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	405	-	-	-	-	-
I/O	406	-	-	-	-	-
I/O	407	-	-	-	AL26	N37
I/O	408	-	-	-	AK25	H42
I/O	409	-	-	AK24	AN28	J41
I/O	410	-	-	AH23	AN29	G43
I/O	411	P72	AC19	AJ24	AJ25	H40
I/O	412	P71	AF21	AK25	AL27	F42
I/O	413	P70	AE21	AJ25	AK26	J39
I/O	414	P69	AD20	AH24	AM29	L37
GND	-	-	GND*	GND*	GND*	GND*
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	415	-	AF23	AL26	AM30	E41
I/O	416	-	AE22	AK26	AJ26	F40
I/O	417	-	AD21	AH25	AL28	C43
I/O	418	-	AC21	AL27	AK27	G39
I/O	419	-	-	AJ26	AL29	D42
I/O	420	-	-	AK27	AN31	H38
I/O	421	-	-	-	-	-
I/O	422	-	-	-	-	-
I/O	423	-	-	-	-	-
I/O	424	-	-	-	-	-
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	425	-	-	-	-	-
I/O	426	-	-	-	-	-
I/O (/LDC)	427	P68	AE23	AH26	AJ27	K36
I/O	428	P67	AD22	AL28	AM31	J37
I/O	429	P66	AF24	AJ27	AK28	B42
I/O	430	P65	AC22	AK28	AL30	D40
I/O (HDC)	431	P64	AD23	AH27	AK29	C41
I/O, GCK3	432	P63	AE24	AK29	AJ28	F38
I (M2)	-	P62	AC23	AJ28	AN32	H36
VCCIO	-	P61	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I (M0)	-	P60	AD24	AH28	AJ29	C39
GND	-	P59	GND*	GND*	GND*	GND*
O (M1)	-	P58	AB23	AH29	AK30	D38
I/O, GCK2	433	P57	AC24	AJ30	AH29	E37
I/O	434	P56	AD25	AH30	AJ30	B40

XC40150XV Pinout Table (Continued)

PAD NAME	EPIC PAD #	HQ240	BG352	BG432	BG560	PG559
VCCINT	-	P55	AB24	VCCINT*	VCCINT*	VCCINT*
I/O	435	-	-	-	-	H34
I/O	436	P54	AA23	AH31	AH30	G35
I/O	437	-	AC25	AG29	AL33	F36
I/O	438	-	AD26	AG30	AG29	D36
I/O	439	-	-	-	-	-
I/O	440	-	-	-	-	-
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	-	-	GND*	GND*	GND*
I/O	441	P53	AC26	AF28	AJ31	E35
I/O	442	P52	Y23	AG31	AK32	A41
I/O	443	-	-	AF29	AG30	G33
I/O	444	-	-	AF30	AH31	B38
I/O	445	-	-	-	-	-
I/O	446	-	-	-	-	-
I/O	447	-	-	-	-	-
I/O	448	-	-	-	-	-
I/O	449	-	AA24	AE28	AF29	D34
I/O	450	-	AB25	AF31	AJ32	E33
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	-	GND*	GND*	GND*	GND*
I/O	451	P51	AA25	AE29	AH32	F32
I/O	452	P50	Y24	AE30	AF30	G31
I/O	453	P49	Y25	AD28	AG31	A37
I/O	454	P48	AA26	AD29	AE29	H30
I/O	455	-	-	AD30	AH33	B36
I/O	456	-	-	AD31	AG33	C33
I/O	457	-	-	-	AE30	C35
I/O	458	-	-	-	AF31	D32
I/O	459	-	-	-	-	-
I/O	460	-	-	-	-	-
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	-	-	GND*	GND*	GND*
I/O	461	-	-	-	AD29	E31
I/O	462	-	-	-	AF32	G29
I/O	463	-	-	-	AE31	A35
I/O	464	-	-	-	AD30	H28
I/O	465	P47	V23	AC28	AE32	B34
I/O	466	P46	W24	AC29	AC29	C31
I/O	467	-	W25	AC30	AE33	A33
I/O	468	-	Y26	AB28	AD31	D30
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	P45	GND*	GND*	GND*	GND*
I/O, FCLK2	469	P44	U23	AB29	AC30	E29
I/O	470	-	-	-	-	C29
VCCINT	-	P43	V24	VCCINT*	VCCINT*	VCCINT*
I/O	471	P42	V25	AB31	AB29	B30
I/O	472	P41	U24	AA29	AC31	G27
VCCIO	-	P40	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	473	-	-	-	AC33	D28
I/O	474	-	-	-	AB30	A29
I/O	475	P39	V26	AA30	AB31	E27
I/O	476	P38	T23	Y28	AA29	F26
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	477	-	U25	Y29	AB32	C27

XC40150XV Pinout Table (Continued)

PAD NAME	EPIC PAD #	HQ240	BG352	BG432	BG560	PG559
I/O	478	-	T24	Y30	AA30	B28
I/O	479	-	-	Y31	AA31	G25
I/O	480	-	-	W28	AA32	A27
I/O	481	-	-	-	-	-
I/O	482	-	-	-	-	-
I/O	483	-	-	-	Y29	D26
I/O	484	-	-	-	AA33	B26
I/O	485	-	T25	W29	Y30	E25
I/O	486	-	T26	W30	Y31	F24
GND	-	P37	GND*	GND*	GND*	GND*
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	487	-	-	-	-	-
I/O	488	-	-	-	-	-
I/O	489	-	-	-	-	-
I/O	490	-	-	-	-	-
I/O	491	-	-	W31	Y32	H24
I/O	492	-	-	V28	W29	B24
I/O	493	-	R23	V29	W30	D24
I/O	494	-	R24	V30	W31	A23
I/O	495	P36	R25	U29	W33	C23
I/O	496	P35	R26	U28	V30	E23
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	497	P34	P24	U30	V29	G23
I/O	498	P33	P23	U31	V31	B22
I/O	499	-	-	-	V32	D22
I/O	500	-	-	-	U33	A21
I/O	501	-	-	-	-	-
I/O	502	-	-	-	-	-
I/O	503	P32	P25	T29	U30	F22
I/O	504	P31	N26	T30	U29	C21
VCCIO	-	P30	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	P29	GND*	GND*	GND*	GND*
I/O	505	P28	N25	T31	U31	E21
I/O	506	-	-	-	-	D20
VCCINT	-	P27	N24	VCCINT*	VCCINT*	VCCINT*
I/O	507	-	-	-	-	-
I/O	508	-	-	-	-	-
I/O	509	-	-	-	T32	C17
I/O	510	-	-	-	T30	G21
I/O	511	P26	M26	R28	T29	F20
I/O	512	P25	M25	R30	T31	D18
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	-	-	GND*	GND*	GND*
I/O	513	P24	M24	R31	R33	E19
I/O	514	P23	M23	P29	R31	B20
I/O	515	-	L26	P28	R30	H20
I/O	516	-	L25	P30	R29	B18
I/O	517	-	-	N30	P32	C15
I/O	518	-	-	N29	P31	D16
I/O	519	-	-	-	-	-
I/O	520	-	-	-	-	-
I/O	521	-	-	-	-	-
I/O	522	-	-	-	-	-
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
GND	-	P22	GND*	GND*	GND*	GND*

XC40150XV Pinout Table (Continued)

PAD NAME	EPIC PAD #	HQ240	BG352	BG432	BG560	PG559
I/O	523	-	K25	N28	N33	G19
I/O	524	-	L24	N31	P30	A17
VCCINT	-	-	-	-	-	-
I/O	525	-	L23	M31	P29	F18
I/O	526	-	J26	M29	M32	E17
I/O	527	-	-	-	-	-
I/O	528	-	-	-	-	-
I/O	529	-	-	-	N31	B16
I/O	530	-	-	-	N30	C13
I/O	531	-	-	M28	L33	A15
I/O	532	-	-	M30	N29	D14
VCCIO	-	-	-	VCCIO*	VCCIO*	-
GND	-	-	-	GND*	GND*	GND*
I/O	533	P21	J25	L30	M31	E15
I/O	534	P20	K24	L29	L32	G17
I/O	535	-	-	-	M30	B14
I/O	536	-	-	-	L31	C11
VCCIO	-	P19	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	537	P18	K23	K31	M29	D12
I/O (TMS)	538	P17	H25	K30	J33	A11
VCCINT	-	P16	J24	VCCINT*	VCCINT*	VCCINT*
I/O	539	-	-	-	-	E13
I/O, FCLK1	540	P15	J23	K28	L30	C9
GND	-	P14	GND*	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	541	-	G26	J30	K31	H16
I/O	542	-	G25	H31	L29	B10
I/O	543	P13	H24	J29	H33	G15
I/O	544	P12	H23	J28	K30	A9
I/O	545	-	-	-	J31	D10
I/O	546	-	-	-	H32	B8
I/O	547	-	-	-	K29	E11
I/O	548	-	-	-	H31	G13
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	549	P11	F26	-	J30	F12
I/O	550	P10	F25	-	G32	H14
I/O	551	P9	G24	H30	F33	G11
I/O	552	P8	D26	G30	J29	A7
I/O	553	-	-	H29	G31	E9
I/O	554	-	-	H28	H30	B6
I/O	555	-	-	F31	E33	D8
I/O	556	-	-	F30	E32	F8
I/O	557	-	-	-	-	-
I/O	558	-	-	-	-	-
GND	-	-	GND*	GND*	GND*	GND*
VCCIO	-	-	VCCIO*	VCCIO*	VCCIO*	VCCIO*
I/O	559	-	E25	G29	H29	G9
I/O	560	-	F24	G28	F31	H10
I/O	561	-	-	-	-	-
I/O	562	-	-	-	-	-
I/O	563	-	F23	E31	G30	B4
I/O	564	-	D25	E30	D32	E7
I/O	565	-	-	F29	E31	C5
I/O	566	-	-	F28	G29	D6
I/O	567	-	-	-	-	-

XC40150XV Pinout Table (Continued)

PAD NAME	EPIC PAD #	HQ240	BG352	BG432	BG560	PG559
I/O	568	-	-	-	-	-
GND	-	-	-	GND*	GND*	GND*
VCCIO	-	-	-	VCCIO*	VCCIO*	-
I/O	569	-	-	-	-	-
I/O	570	-	-	-	-	-
I/O (TCK)	571	P7	E24	D31	C33	D4
I/O (TDI)	572	P6	C26	D30	F30	H8
I/O	573	P5	E23	E29	D31	A3
I/O	574	-	-	-	-	F6
VCCINT	-	P4	D24	VCCINT*	VCCINT*	VCCINT*
I/O (A17)	575	P3	C25	C30	F29	C3
I/O, GCK1 (A16)	576	P2	D23	D29	B33	C1
GND	-	P1	GND*	GND*	GND*	GND*
VCCIO	-	-	A10	A1	A4	A13
VCCIO	-	-	A17	A11	A10	A31
VCCIO	-	-	AC14	A21	A16	A43
VCCIO	-	-	AC20	A31	A22	B2
VCCIO	-	-	AC8	D11	A26	C7
VCCIO	-	-	AF10	D21	A30	C19
VCCIO	-	-	AF17	L1	B2	C25
VCCIO	-	-	D7	L4	B13	C37
VCCIO	-	-	D13	L28	B19	F14
VCCIO	-	-	D19	L31	B32	F30
VCCIO	-	-	G23	AA1	C3	G3
VCCIO	-	-	H4	AA4	C31	G7
VCCIO	-	-	K1	AA28	C32	G37
VCCIO	-	-	K26	AA31	D1	G41
VCCIO	-	-	N23	AH11	D33	N1
VCCIO	-	-	P4	AH21	E5	N43
VCCIO	-	-	U1	AL1	H1	P6
VCCIO	-	-	U26	AL11	K33	P38
VCCIO	-	-	W23	AL21	M1	W3
VCCIO	-	-	Y4	AL31	N32	W41
VCCIO	-	-	B2	C3	R2	AE3
VCCIO	-	-	B25	C29	T33	AE41
VCCIO	-	-	AE2	AJ3	V1	AK6
VCCIO	-	-	AE25	AJ29	W32	AK38
VCCIO	-	-	-	-	AA2	AL1
VCCIO	-	-	-	-	AB33	AL43
VCCIO	-	-	-	-	AD1	AU3
VCCIO	-	-	-	-	AF33	AU7
VCCIO	-	-	-	-	AK1	AU37
VCCIO	-	-	-	-	AK4	AU41
VCCIO	-	-	-	-	AK33	AV14
VCCIO	-	-	-	-	AL2	AV30
VCCIO	-	-	-	-	AL3	BA7
VCCIO	-	-	-	-	AL31	BA19
VCCIO	-	-	-	-	AM2	BA25
VCCIO	-	-	-	-	AM15	BA37
VCCIO	-	-	-	-	AM21	BC1
VCCIO	-	-	-	-	AM32	BC13
VCCIO	-	-	-	-	AN4	BC31
VCCIO	-	-	-	-	AN8	BC43
VCCIO	-	-	-	-	AN12	-
VCCIO	-	-	-	-	AN18	-

XC40150XV Pinout Table (Continued)

PAD NAME	EPIC PAD #	HQ240	BG352	BG432	BG560	PG559
VCCIO	-	-	-	-	AN24	-
VCCIO	-	-	-	-	AN30	-
VCCINT	-	-	-	A10	E12	H12
VCCINT	-	-	-	AB2	AD2	H18
VCCINT	-	-	-	AB30	AD32	H26
VCCINT	-	-	-	AG28	AK31	H32
VCCINT	-	-	-	AH15	AM17	M8
VCCINT	-	-	-	AH5	AK5	M36
VCCINT	-	-	-	AJ10	AK11	V8
VCCINT	-	-	-	AK22	AN25	V36
VCCINT	-	-	-	B23	C24	AF8
VCCINT	-	-	-	B4	D6	AF36
VCCINT	-	-	-	C16	C17	AM8
VCCINT	-	-	-	E28	E30	AM36
VCCINT	-	-	-	K29	K32	AT12
VCCINT	-	-	-	K3	J1	AT18
VCCINT	-	-	-	R2	T3	AT26
VCCINT	-	-	-	R29	U32	AT32
GND	-	-	A1	A2	A7	A5
GND	-	-	A14	A3	A12	A19
GND	-	-	A19	A7	A14	A25
GND	-	-	A2	A9	A18	A39
GND	-	-	A22	A14	A20	B12
GND	-	-	A25	A18	A24	B32
GND	-	-	A26	A23	A29	E1
GND	-	-	A5	A25	A32	E5
GND	-	-	A8	A29	B1	E39
GND	-	-	AB1	A30	B6	E43
GND	-	-	AB26	B1	B9	F10
GND	-	-	AE1	B2	B15	F16
GND	-	-	AE26	B30	B23	F28
GND	-	-	AF1	B31	B27	F34
GND	-	-	AF13	C1	B31	H22
GND	-	-	AF19	C31	C2	K6
GND	-	-	AF2	D16	E1	K38
GND	-	-	AF22	G1	F32	M2
GND	-	-	AF25	G31	G2	M42
GND	-	-	AF26	J1	G33	T6
GND	-	-	AF5	J31	J32	T38
GND	-	-	AF8	P1	K1	W1
GND	-	-	B1	P31	L2	W43
GND	-	-	B26	T4	M33	AB8

XC40150XV Pinout Table (Continued)

PAD NAME	EPIC PAD #	HQ240	BG352	BG432	BG560	PG559
GND	-	-	E1	T28	P1	AB36
GND	-	-	E26	V1	P33	AE1
GND	-	-	H1	V31	R32	AE43
GND	-	-	H26	AC1	T1	AH6
GND	-	-	N1	AC31	V33	AH38
GND	-	-	P26	AE1	W2	AM2
GND	-	-	W1	AE31	Y1	AM42
GND	-	-	W26	AH16	Y33	AP6
GND	-	-	-	AJ1	AB1	AP38
GND	-	-	-	AJ31	AC32	AT22
GND	-	-	-	AK1	AD33	AV10
GND	-	-	-	AK2	AE2	AV16
GND	-	-	-	AK30	AG1	AV28
GND	-	-	-	AK31	AG32	AV34
GND	-	-	-	AL2	AH2	AW1
GND	-	-	-	AL3	AJ33	AW5
GND	-	-	-	AL7	AL32	AW39
GND	-	-	-	AL9	AM3	AW43
GND	-	-	-	AL14	AM11	BB12
GND	-	-	-	AL18	AM19	BB32
GND	-	-	-	AL23	AM25	BC5
GND	-	-	-	AL25	AM28	BC19
GND	-	-	-	AL29	AM33	BC25
GND	-	-	-	AL30	AM7	BC39
GND	-	-	-	-	AN2	-
GND	-	-	-	-	AN5	-
GND	-	-	-	-	AN10	-
GND	-	-	-	-	AN14	-
GND	-	-	-	-	AN16	-
GND	-	-	-	-	AN20	-
GND	-	-	-	-	AN22	-
GND	-	-	-	-	AN27	-
NC	-	P204	C8	C8	A1	-
NC	-	P219	-	-	A33	-
NC	-	-	-	-	AC2	-
NC	-	-	-	-	AN1	-
NC	-	-	-	-	AN33	-

12/21/98

Note: Pads labelled GND, VCCINT*, or VCCIO* are internally bonded to the corresponding power plane within the associated package. They have no direct connection to any specific package pin.

XC40200XV Pinout Table

Pad Name	EPIC Pad #	BG432	BG560	PG559
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O, GCK8 (A15	1	D28	E29	E3
I/O (A)14)	2	C28	D30	F4
I/O	3	B29	E28	J7
I/O	4	D27	D29	D2
I/O	5	B28	C30	K8
I/O	6	C27	D28	H6
I/O	7	-	-	-
I/O	8	-	-	-
I/O	9	-	-	-
I/O	10	-	-	-
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	11	-	-	-
I/O	12	-	-	-
I/O	13	-	-	-
I/O	14	-	-	-
I/O	15	D26	A31	G5
I/O	16	A28	E27	F2
I/O	17	B27	C29	H4
I/O	18	C26	B30	G1
I/O	19	D25	D27	J5
I/O	20	A27	C28	L7
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O (A13)	21	B26	E26	J3
I/O (A12)	22	D24	B29	K4
I/O	23	C25	B28	H2
I/O	24	A26	D26	L5
I/O	25	B25	C27	J1
I/O	26	D23	E25	M6
I/O	27	-	A28	K2
I/O	28	-	A27	N7
I/O	29	-	-	-
I/O	30	-	-	-
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	31	-	-	-
I/O	32	-	-	-
I/O	33	-	-	-
I/O	34	-	-	-
I/O	35	-	D25	P8
I/O	36	-	C26	L3
I/O	37	-	E24	L1
I/O	38	-	B26	M4
I/O	39	C24	C25	P2
I/O	40	B24	D24	N5
I/O	41	C23	B25	R1
I/O	42	D22	E23	N3
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	43	A24	A25	R7
I/O	44	-	-	P4
VCCINT	-	B23	C24	VCCINT*
I/O	45	C22	D23	T2

XC40200XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
I/O	46	B22	B24	T8
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	47	A22	E22	R5
I/O	48	C21	C23	R3
I/O	49	-	A23	U1
I/O	50	-	D22	T4
I/O	51	-	-	-
I/O	52	-	-	-
I/O	53	-	-	-
I/O	54	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	55	-	-	-
I/O	56	-	-	-
I/O	57	-	C22	U5
I/O	58	-	E21	V2
I/O	59	D20	B22	U7
I/O	60	B21	D21	U3
I/O	61	C20	C21	Y2
I/O	62	B20	B21	V4
I/O	63	A20	E20	V6
I/O	64	D19	A21	W5
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O (A11)	65	C19	D20	W7
I/O (A10)	66	B19	C20	Y4
I/O	67	A19	B20	AA1
I/O	68	B18	E19	Y6
I/O (A18)	69	D18	D19	AB2
I/O (A19)	70	C18	C19	Y8
I/O	71	-	-	-
I/O	72	-	-	-
I/O	73	-	-	-
I/O	74	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	75	-	-	-
I/O	76	-	-	-
I/O	77	-	-	-
I/O	78	-	-	-
I/O	79	-	A19	AA3
I/O	80	-	D18	AA5
I/O	81	B17	E18	AC1
I/O	82	C17	C18	AA7
I/O (A9)	83	A17	B18	AB4
I/O (A8)	84	D17	A17	AB6
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O (A7)	85	A16	D17	AC3
I/O (A6)	86	B16	E17	AC5
VCCINT	-	C16	C17	VCCINT*
I/O	87	-	-	AD2
I/O	88	A15	B17	AC7
I/O	89	-	B16	AF2
I/O	90	-	D16	AD4
I/O	91	-	-	-

XC40200XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
I/O	92	-	-	-
I/O	93	-	-	-
I/O	94	-	-	-
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	95	-	-	-
I/O	96	-	-	-
I/O	97	-	-	-
I/O	98	-	-	-
I/O (A20)	99	B15	E16	AD6
I/O (A21)	100	C15	C16	AE5
I/O	101	D15	A15	AF4
I/O	102	B14	C15	AG1
I/O (A5)	103	A13	D15	AD8
I/O (A4)	104	C14	E15	AG3
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	105	B13	B14	AH4
I/O	106	D14	C14	AE7
I/O	107	A12	D14	AH2
I/O	108	C13	A13	AF6
I/O	109	B12	E14	AJ1
I/O	110	D13	C13	AG5
I/O	111	-	D13	AJ3
I/O	112	-	B12	AK4
I/O	113	-	-	-
I/O	114	-	-	-
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	115	-	-	-
I/O	116	-	-	-
I/O	117	-	-	-
I/O	118	-	-	-
I/O	119	-	C12	AG7
I/O	120	-	E13	AK2
I/O	121	C12	A11	AJ5
I/O	122	B11	D12	AL3
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	123	D12	B11	AM4
I/O	124	C11	C11	AN1
VCCINT	-	A10	E12	VCCINT*
I/O	125	-	-	AL5
VCCINT	-	-	-	-
I/O	126	B10	B10	AH8
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO	VCCIO*	-
I/O	127	C10	D11	AJ7
I/O	128	B9	C10	AP2
I/O	129	C9	A9	AN3
I/O	130	D10	E11	AP4
I/O	131	-	C9	AR1
I/O	132	-	D10	AN5
I/O	133	-	A8	AM6
I/O	134	-	B8	AK8
I/O	135	-	-	-
I/O	136	-	-	-

XC40200XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
I/O	137	-	-	-
I/O	138	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	139	-	-	-
I/O	140	-	-	-
I/O	141	-	E10	AL7
I/O	142	-	C8	AT2
I/O	143	A8	D9	AR3
I/O	144	B8	B7	AU1
I/O	145	D9	A6	AT4
I/O	146	B7	E9	AV2
I/O	147	C7	C7	AR5
I/O	148	D8	D8	AN7
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	149	A6	A5	AW3
I/O	150	B6	B5	AV4
I/O (A3)	151	D7	E8	BA1
I/O, (CS1, A2)	152	A5	C6	AU5
I/O	153	C6	D7	AY2
I/O	154	B5	B4	AT6
I/O	155	-	-	-
I/O	156	-	-	-
I/O	157	-	-	-
I/O	158	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	159	-	-	-
I/O	160	-	-	-
I/O	161	-	-	-
I/O	162	-	-	-
I/O	163	D6	C5	AP8
I/O	164	A4	E7	AR7
I/O	165	C5	A3	AY4
I/O	166	-	-	BB2
I/O, GCK7 (A1)	167	D5	A2	AV6
I/O (A0, /WS)	168	B3	D5	AT8
GND	-	GND*	GND*	GND*
O, TDO	-	C4	E6	BA3
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
CCLK	-	D4	C4	BA5
I/O, GCK6 (DOUT)	169	D3	D4	BB4
I/O (D0, DIN)	170	C2	E4	AY6
I/O	171	D2	F5	BC3
I/O	172	E4	B3	AW7
I/O	173	D1	D3	BB6
I/O	174	E3	F4	AU9
I/O	176	-	-	-
I/O	177	-	-	-
I/O	178	-	-	-
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	179	-	-	-
I/O	180	-	-	-
I/O	181	E2	C1	AT10

XC40200XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
I/O	182	F4	G5	AV8
I/O	183	E1	E3	AY8
I/O	184	F3	D2	BC7
I/O	185	-	-	-
I/O	186	-	-	-
I/O (/RCK,RDY_/BUSY)	187	F2	G4	AW9
I/O (D1)	188	G4	F3	BA9
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	189	-	-	-
I/O	190	-	-	-
I/O	191	-	H5	AU11
I/O	192	-	E2	AY10
I/O	193	F1	F2	BB8
I/O	194	G3	H4	AW11
I/O	195	G2	G3	BC9
I/O	196	H4	J5	AV12
I/O	197	H3	F1	AU13
I/O	198	H2	G1	AT14
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	199	-	-	-
I/O	200	-	-	-
I/O	201	-	-	-
I/O	202	-	-	-
I/O	203	-	J4	BA11
I/O	204	-	H3	AY12
I/O	205	-	K5	BB10
I/O	206	-	H2	AW13
I/O	207	H1	J3	BC11
I/O	208	J4	K4	AU15
I/O	209	J3	J2	BB14
I/O	210	J2	L5	AT16
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	211	K4	K3	BA13
I/O	212	-	-	AY14
VCCINT	-	K3	J1	VCCINT*
I/O, FCLK4	213	K2	L4	BC15
I/O	214	K1	K2	AW15
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	215	-	-	-
I/O	216	-	-	-
I/O	217	-	-	-
I/O	218	-	-	-
I/O	219	-	M5	BA15
I/O	220	-	L3	AU17
I/O	221	L3	L1	BB16
I/O (D2)	222	L2	M4	AY16
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	223	M4	M3	AW17
I/O	224	M3	N5	AV18
I/O	225	-	M2	BA17
I/O	226	-	N4	BC17
I/O	227	-	-	-

XC40200XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
I/O	228	-	-	-
I/O	229	M2	N3	AU19
I/O	230	M1	N2	BB18
I/O	231	N4	P5	AY18
I/O	232	N3	N1	AW19
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	233	-	-	-
I/O	234	-	-	-
I/O	235	-	-	-
I/O	236	-	-	-
I/O	237	N2	P4	AV20
I/O	238	N1	P3	AT20
I/O	239	P4	P2	BB20
I/O	240	P3	R5	AY20
I/O	241	P2	R4	BC21
I/O	242	R3	R3	BA21
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	243	R4	R1	AW21
I/O	244	-	T4	AU21
I/O	245	-	T5	BB22
I/O	246	-	-	AY22
I/O	247	-	-	-
I/O	248	-	-	-
I/O	249	-	-	-
I/O	250	-	-	-
VCCINT	-	R2	T3	VCCINT*
I/O (/RS)	251	R1	T2	AV22
I/O (D3)	252	T3	U3	BA23
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	253	T2	U4	AW23
I/O (D4)	254	T1	U5	AY24
I/O	255	-	-	-
I/O	256	-	-	-
I/O	257	-	-	-
I/O	258	-	-	-
I/O	259	-	U1	BC23
I/O	260	-	U2	BA27
I/O	261	U3	V2	AU23
I/O	262	U4	V4	AV24
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	263	U2	V5	AY26
I/O	264	U1	V3	BB24
I/O	265	V3	W1	AW25
I/O	266	V4	W3	BB26
I/O	267	V2	W4	AT24
I/O	268	W2	W5	BA29
I/O	269	-	-	-
I/O	270	-	-	-
I/O	271	-	-	-
I/O	272	-	-	-
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*

XC40200XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
I/O	273	W3	Y2	AY28
I/O	274	W4	Y3	AU25
I/O	275	-	Y4	AV26
I/O	276	-	AA1	BC27
I/O	277	-	-	-
I/O	278	-	-	-
I/O	279	W1	Y5	AW27
I/O	280	Y1	AA3	BB28
I/O	281	Y3	AA4	BA31
I/O	282	Y4	AB2	AY30
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O (/CS0)	283	Y2	AB3	AW29
I/O (D5)	284	AA2	AA5	BC29
I/O	285	-	AC1	AU27
I/O	286	-	AB4	BA33
I/O	287	-	-	-
I/O	288	-	-	-
I/O	289	-	-	-
I/O	290	-	-	-
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	291	AA3	AC3	AY32
I/O, FCLK3	292	AB1	AB5	AW31
VCCINT	-	AB2	AD2	VCCINT*
I/O	293	-	-	BB30
I/O	294	AB3	AC4	BA35
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	295	AB4	AD3	AT28
I/O	296	AC2	AE1	AU29
I/O	297	AD1	AC5	BC33
I/O	298	AC3	AE3	AY34
I/O	299	-	AD4	BB34
I/O	300	-	AF1	AW33
I/O	301	-	AF2	AU31
I/O	302	-	AD5	AV32
I/O	303	-	-	-
I/O	304	-	-	-
I/O	305	-	-	-
I/O	306	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	307	-	-	-
I/O	308	-	-	-
I/O	309	-	AG2	AT30
I/O	310	-	AE4	AU33
I/O	311	AC4	AF3	AW35
I/O	312	AD2	AH1	BC35
I/O	313	AE2	AE5	AY36
I/O	314	AD3	AG3	BB36
I/O	315	AD4	AF4	AV36
I/O (D6)	316	AF1	AJ1	AU35
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	317	AF2	AJ2	AT34
I/O	318	AE3	AF5	AW37

XC40200XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
I/O	319	-	-	-
I/O	320	-	-	-
I/O	321	-	-	-
I/O	322	-	-	-
I/O	323	AE4	AH3	BC37
I/O	324	AG1	AG4	AY38
I/O	325	AG2	AK2	BB38
I/O	326	AF3	AJ3	BA41
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	327	-	-	-
I/O	328	-	-	-
I/O	329	-	-	-
I/O	330	-	-	-
I/O	331	AF4	AG5	AY40
I/O	332	AH1	AL1	BB40
I/O	333	AH2	AH4	AT36
I/O	334	AG3	AK3	BA39
I/O, GCK5	335	AG4	AJ4	AV38
I/O (D7)	336	AJ2	AH5	BC41
/PROGRAM	-	AH3	AM1	BB42
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
DONE	-	AH4	AJ5	AY42
GND	-	GND*	GND*	GND*
I/O, GCK4	337	AJ4	AL4	AW41
I/O	338	AK3	AJ6	AV40
VCCINT	-	AH5	AK5	VCCINT*
I/O	339	-	-	AV42
I/O	340	AK4	AN3	AR37
I/O	341	AJ5	AK6	AP36
I/O	342	AH6	AL5	AT38
I/O	343	-	-	-
I/O	344	-	-	-
I/O	345	-	-	-
I/O	346	-	-	-
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	347	-	-	-
I/O	348	-	-	-
I/O	349	-	-	-
I/O	350	-	-	-
I/O	351	AL4	AJ7	AU39
I/O	352	AK5	AM4	AU43
I/O	353	AJ6	AM5	BA43
I/O	354	AH7	AK7	AT42
I/O	355	AL5	AL6	AR39
I/O	356	AK6	AJ8	AN37
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	357	AH8	AM6	AT40
I/O	358	AJ7	AN6	AP40
I/O	359	AL6	AK8	AR43
I/O	360	AK7	AL7	AN39
I/O	361	AH9	AJ9	AP42
I/O	362	AJ8	AN7	AM38
I/O	363	-	AL8	AN43

XC40200XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
I/O	364	-	AK9	AL37
I/O	365	-	-	-
I/O	366	-	-	-
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	367	-	-	-
I/O	368	-	-	-
I/O	369	-	-	-
I/O	370	-	-	-
I/O	371	-	AM8	AK36
I/O	372	-	AJ10	AR41
I/O	373	-	AL9	AL41
I/O	374	-	AM9	AN41
I/O	375	AK8	AK10	AK42
I/O	376	AJ9	AN9	AM40
I/O	377	AH10	AJ11	AJ43
I/O	378	AL8	AL10	AJ37
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	379	AK9	AM10	AL39
I/O	380	-	-	AH36
VCCINT	-	AJ10	AK11	VCCINT*
I/O	381	AK10	AL11	AH42
I/O	382	AL10	AJ12	AJ39
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	383	AJ11	AN11	AK40
I/O	384	AH12	AK12	AG41
I/O	385	-	AL12	AJ41
I/O	386	-	AM12	AH40
I/O	387	-	-	-
I/O	388	-	-	-
I/O	389	-	-	-
I/O	390	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	391	-	-	-
I/O	392	-	-	-
I/O	393	-	AJ13	AG37
I/O	394	-	AK13	AG43
I/O	395	AK11	AL13	AG39
I/O	396	AJ12	AM13	AF38
I/O	397	AK12	AN13	AF42
I/O	398	AL12	AJ14	AD42
I/O	399	AH13	AK14	AF40
I/O	400	AJ13	AL14	AE37
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	401	AK13	AM14	AE39
I/O	402	AL13	AN15	AD40
I/O	403	AK14	AJ15	AC43
I/O	404	AH14	AK15	AD38
I/O	405	AJ14	AL15	AC41
I/O	406	AK15	AM16	AD36
I/O	407	-	-	-
I/O	408	-	-	-
I/O	409	-	-	-

XC40200XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
I/O	410	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	411	-	-	-
I/O	412	-	-	-
I/O	413	-	-	-
I/O	414	-	-	-
I/O	415	-	AL16	AC39
I/O	416	-	AJ16	AC37
I/O	417	AJ15	AK16	AB40
I/O	418	AL15	AN17	AB42
VCCINT	-	AH15	AM17	VCCINT*
I/O	419	-	-	AB38
I/O	420	AL16	AL17	AA41
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O (/INIT)	421	AK16	AJ17	AA39
I/O	422	AJ16	AK17	AA37
I/O	423	AL17	AM18	Y40
I/O	424	AK17	AL18	Y38
I/O	425	-	AK18	AA43
I/O	426	-	AJ18	W39
I/O	427	-	-	-
I/O	428	-	-	-
I/O	429	-	-	-
I/O	430	-	-	-
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	431	-	-	-
I/O	432	-	-	-
I/O	433	-	-	-
I/O	434	-	-	-
I/O	435	AJ17	AN19	V40
I/O	436	AH17	AL19	Y36
I/O	437	AK18	AK19	U41
I/O	438	AL19	AM20	Y42
I/O	439	AJ18	AJ19	T40
I/O	440	AK19	AL20	W37
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	441	AH18	AK20	V38
I/O	442	AL20	AN21	U39
I/O	443	AJ19	AL21	V42
I/O	444	AK20	AJ20	R41
I/O	445	AH19	AM22	U43
I/O	446	AJ20	AK21	P40
VCCIO	-	-	-	-
GND	-	-	-	-
I/O	447	-	AN23	T42
I/O	448	-	AL22	U37
I/O	449	-	-	-
I/O	450	-	-	-
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	451	-	-	-
I/O	452	-	-	-

XC40200XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
I/O	453	-	-	-
I/O	454	-	-	-
I/O	455	-	AJ21	R39
I/O	456	-	AM23	N41
I/O	457	AK21	AK22	R43
I/O	458	AH20	AM24	M40
VCCIO	-	VCCIO*	VCCIO*	-
I/O	459	AJ21	AL23	N39
I/O	460	AL22	AJ22	T36
VCCINT	-	AK22	AN25	VCCINT*
I/O	461	-	-	P42
I/O	462	AJ22	AK23	R37
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	463	AK23	AL24	L41
I/O	464	AJ23	AN26	L43
I/O	465	AH22	AJ23	K40
I/O	466	AL24	AL25	K42
I/O	467	-	AK24	L39
I/O	468	-	AM26	J43
I/O	469	-	AM27	M38
I/O	470	-	AJ24	P36
I/O	471	-	-	-
I/O	472	-	-	-
I/O	473	-	-	-
I/O	474	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	475	-	-	-
I/O	476	-	-	-
I/O	477	-	AL26	N37
I/O	478	-	AK25	H42
I/O	479	AK24	AN28	J41
I/O	480	AH23	AN29	G43
I/O	481	AJ24	AJ25	H40
I/O	482	AK25	AL27	F42
VCCINT	-	-	-	-
I/O	483	AJ25	AK26	J39
I/O	484	AH24	AM29	L37
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	485	AL26	AM30	E41
I/O	486	AK26	AJ26	F40
I/O	487	AH25	AL28	C43
I/O	488	AL27	AK27	G39
I/O	489	AJ26	AL29	D42
I/O	490	AK27	AN31	H38
I/O	491	-	-	-
I/O	492	-	-	-
I/O	493	-	-	-
I/O	494	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	495	-	-	-
I/O	496	-	-	-
I/O	497	-	-	-

XC40200XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
I/O	498	-	-	-
I/O (/LDC)	499	AH26	AJ27	K36
I/O	500	AL28	AM31	J37
I/O	501	AJ27	AK28	B42
I/O	502	AK28	AL30	D40
I/O (HDC)	503	AH27	AK29	C41
I/O, GCK3	504	AK29	AJ28	F38
I (M2)	-	AJ28	AN32	H36
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I (M0)	-	AH28	AJ29	C39
GND	-	GND*	GND*	GND*
O (M1)	-	AH29	AK30	D38
I/O, GCK2	505	AJ30	AH29	E37
I/O	506	AH30	AJ30	B40
VCCINT	-	AG28	AK31	VCCINT*
I/O	507	-	-	H34
I/O	508	AH31	AH30	G35
I/O	509	AG29	AL33	F36
I/O	510	AG30	AG29	D36
I/O	511	-	-	-
I/O	512	-	-	-
I/O	513	-	-	-
I/O	514	-	-	-
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	515	AF28	AJ31	E35
I/O	516	AG31	AK32	A41
I/O	517	AF29	AG30	G33
I/O	518	AF30	AH31	B38
I/O	519	-	-	-
I/O	520	-	-	-
I/O	521	-	-	-
I/O	522	-	-	-
I/O	523	AE28	AF29	D34
I/O	524	AF31	AJ32	E33
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	525	AE29	AH32	F32
I/O	526	AE30	AF30	G31
I/O	527	AD28	AG31	A37
I/O	528	AD29	AE29	H30
I/O	529	AD30	AH33	B36
I/O	530	AD31	AG33	C33
I/O	531	-	AE30	C35
I/O	532	-	AF31	D32
I/O	533	-	-	-
I/O	534	-	-	-
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	535	-	-	-
I/O	536	-	-	-
I/O	537	-	-	-
I/O	538	-	-	-
I/O	539	-	AD29	E31
I/O	540	-	AF32	G29
I/O	541	-	AE31	A35

XC40200XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
I/O	542	-	AD30	H28
I/O	543	AC28	AE32	B34
I/O	544	AC29	AC29	C31
I/O	545	AC30	AE33	A33
I/O	546	AB28	AD31	D30
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O, FCLK2	547	AB29	AC30	E29
I/O	548	-	-	C29
VCCINT	-	AB30	AD32	VCCINT*
I/O	549	AB31	AB29	B30
I/O	550	AA29	AC31	G27
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	551	-	-	-
I/O	552	-	-	-
I/O	553	-	-	-
I/O	554	-	-	-
I/O	555	-	AC33	D28
I/O	556	-	AB30	A29
I/O	557	AA30	AB31	E27
I/O	558	Y28	AA29	F26
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	559	Y29	AB32	C27
I/O	560	Y30	AA30	B28
I/O	561	Y31	AA31	G25
I/O	562	W28	AA32	A27
I/O	563	-	-	-
I/O	564	-	-	-
I/O	565	-	Y29	D26
I/O	566	-	AA33	B26
I/O	567	W29	Y30	E25
I/O	568	W30	Y31	F24
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	569	-	-	-
I/O	570	-	-	-
I/O	571	-	-	-
I/O	572	-	-	-
I/O	573	W31	Y32	H24
I/O	574	V28	W29	B24
I/O	575	V29	W30	D24
I/O	576	V30	W31	A23
I/O	577	U29	W33	C23
I/O	578	U28	V30	E23
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	579	U30	V29	G23
I/O	580	U31	V31	B22
I/O	581	-	V32	D22
I/O	582	-	U33	A21
I/O	583	-	-	-
I/O	584	-	-	-
I/O	585	-	-	-
I/O	586	-	-	-
I/O	587	T29	U30	F22

XC40200XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
I/O	588	T30	U29	C21
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	589	T31	U31	E21
I/O	590	-	-	D20
VCCINT	-	R29	U32	VCCINT*
I/O	591	-	-	-
I/O	592	-	-	-
I/O	593	-	-	-
I/O	594	-	-	-
I/O	595	-	T32	C17
I/O	596	-	T30	G21
I/O	597	R28	T29	F20
I/O	598	R30	T31	D18
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	599	R31	R33	E19
I/O	600	P29	R31	B20
I/O	601	P28	R30	H20
I/O	602	P30	R29	B18
I/O	603	N30	P32	C15
I/O	604	N29	P31	D16
I/O	605	-	-	-
I/O	606	-	-	-
I/O	607	-	-	-
I/O	608	-	-	-
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	609	N28	N33	G19
I/O	610	N31	P30	A17
I/O	611	M31	P29	F18
I/O	612	M29	M32	E17
I/O	613	-	-	-
I/O	614	-	-	-
I/O	615	-	N31	B16
I/O	616	-	N30	C13
I/O	617	M28	L33	A15
I/O	618	M30	N29	D14
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	619	L30	M31	E15
I/O	620	L29	L32	G17
I/O	621	-	M30	B14
I/O	622	-	L31	C11
I/O	623	-	-	-
I/O	624	-	-	-
I/O	625	-	-	-
I/O	626	-	-	-
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	627	K31	M29	D12
I/O (TMS)	628	K30	J33	A11
VCCINT	-	K29	K32	VCCINT*
I/O	629	-	-	E13
I/O, FCLK1	630	K28	L30	C9
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-

XC40200XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
I/O	631	J30	K31	H16
I/O	632	H31	L29	B10
I/O	633	J29	H33	G15
I/O	634	J28	K30	A9
I/O	635	-	J31	D10
I/O	636	-	H32	B8
I/O	637	-	K29	E11
I/O	638	-	H31	G13
I/O	639	-	-	-
I/O	640	-	-	-
I/O	641	-	-	-
I/O	642	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	643	H30	J30	F12
I/O	644	G30	G32	H14
I/O	645	H29	F33	G11
I/O	646	H28	J29	A7
I/O	647	F31	G31	E9
I/O	648	F30	H30	B6
I/O	649	-	E33	D8
I/O	650	-	E32	F8
I/O	651	-	-	-
I/O	652	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	653	G29	H29	G9
I/O	654	G28	F31	H10
I/O	655	-	-	-
I/O	656	-	-	-
I/O	657	E31	G30	B4
I/O	658	E30	D32	E7
I/O	659	F29	E31	C5
I/O	660	F28	G29	D6
I/O	661	-	-	-
I/O	662	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	663	-	-	-
I/O	664	-	-	-
I/O	665	-	-	-
I/O	666	-	-	-
GND	-	-	-	-
VCCIO	-	-	-	-
I/O (TCK)	667	D31	C33	D4
I/O (TDI)	668	D30	F30	H8
I/O	669	E29	D31	A3
I/O	670	-	-	F6
VCCINT	-	E28	E30	VCCINT*
I/O (A17)	671	C30	F29	C3
I/O, GCK1 (A16)	672	D29	B33	C1
GND	-	GND*	GND*	GND*
VCCIO	-	A1	A4	A13
VCCIO	-	A11	A10	A31
VCCIO	-	A21	A16	A43

XC40200XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
VCCIO	-	A31	A22	B2
VCCIO	-	D11	A26	C7
VCCIO	-	D21	A30	C19
VCCIO	-	L1	B2	C25
VCCIO	-	L4	B13	C37
VCCIO	-	L28	B19	F14
VCCIO	-	L31	B32	F30
VCCIO	-	AA1	C3	G3
VCCIO	-	AA4	C31	G7
VCCIO	-	AA28	C32	G37
VCCIO	-	AA31	D1	G41
VCCIO	-	AH11	D33	N1
VCCIO	-	AH21	E5	N43
VCCIO	-	AL1	H1	P6
VCCIO	-	AL11	K33	P38
VCCIO	-	AL21	M1	W3
VCCIO	-	AL31	N32	W41
VCCIO	-	C3	R2	AE3
VCCIO	-	C29	T33	AE41
VCCIO	-	AJ3	V1	AK6
VCCIO	-	AJ29	W32	AK38
VCCIO	-	-	AA2	AL1
VCCIO	-	-	AB33	AL43
VCCIO	-	-	AD1	AU3
VCCIO	-	-	AF33	AU7
VCCIO	-	-	AK1	AU37
VCCIO	-	-	AK4	AU41
VCCIO	-	-	AK33	AV14
VCCIO	-	-	AL2	AV30
VCCIO	-	-	AL3	BA7
VCCIO	-	-	AL31	BA19
VCCIO	-	-	AM2	BA25
VCCIO	-	-	AM15	BA37
VCCIO	-	-	AM21	BC1
VCCIO	-	-	AM32	BC13
VCCIO	-	-	AN4	BC31
VCCIO	-	-	AN8	BC43
VCCIO	-	-	AN12	-
VCCIO	-	-	AN18	-
VCCIO	-	-	AN24	-
VCCIO	-	-	AN30	-
VCCINT	-	-	-	H12
VCCINT	-	-	-	H18
VCCINT	-	-	-	H26
VCCINT	-	-	-	H32
VCCINT	-	-	-	M8
VCCINT	-	-	-	M36
VCCINT	-	-	-	V8
VCCINT	-	-	-	V36
VCCINT	-	-	-	AF8
VCCINT	-	-	-	AF36
VCCINT	-	-	-	AM8
VCCINT	-	-	-	AM36
VCCINT	-	-	-	AT12
VCCINT	-	-	-	AT18

XC40200XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
VCCINT	-	-	-	AT26
VCCINT	-	-	-	AT32
GND	-	A2	A7	A5
GND	-	A3	A12	A19
GND	-	A7	A14	A25
GND	-	A9	A18	A39
GND	-	A14	A20	B12
GND	-	A18	A24	B32
GND	-	A23	A29	E1
GND	-	A25	A32	E5
GND	-	A29	B1	E39
GND	-	A30	B6	E43
GND	-	B1	B9	F10
GND	-	B2	B15	F16
GND	-	B30	B23	F28
GND	-	B31	B27	F34
GND	-	C1	B31	H22
GND	-	C31	C2	K6
GND	-	D16	E1	K38
GND	-	G1	F32	M2
GND	-	G31	G2	M42
GND	-	J1	G33	T6
GND	-	J31	J32	T38
GND	-	P1	K1	W1
GND	-	P31	L2	W43
GND	-	T4	M33	AB8
GND	-	T28	P1	AB36
GND	-	V1	P33	AE1
GND	-	V31	R32	AE43
GND	-	AC1	T1	AH6
GND	-	AC31	V33	AH38
GND	-	AE1	W2	AM2
GND	-	AE31	Y1	AM42
GND	-	AH16	Y33	AP6

XC40200XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
GND	-	AJ1	AB1	AP38
GND	-	AJ31	AC32	AT22
GND	-	AK1	AD33	AV10
GND	-	AK2	AE2	AV16
GND	-	AK30	AG1	AV28
GND	-	AK31	AG32	AV34
GND	-	AL2	AH2	AW1
GND	-	AL3	AJ33	AW5
GND	-	AL7	AL32	AW39
GND	-	AL9	AM3	AW43
GND	-	AL14	AM11	BB12
GND	-	AL18	AM19	BB32
GND	-	AL23	AM25	BC5
GND	-	AL25	AM28	BC19
GND	-	AL29	AM33	BC25
GND	-	AL30	AM7	BC39
GND	-	-	AN2	-
GND	-	-	AN5	-
GND	-	-	AN10	-
GND	-	-	AN14	-
GND	-	-	AN16	-
GND	-	-	AN20	-
GND	-	-	AN22	-
GND	-	-	AN27	-
NC	-	C8	A1	-
NC	-	-	A33	-
NC	-	-	AC2	-
NC	-	-	AN1	-
NC	-	-	AN33	-

12/21/98

Note: Pads labelled GND, VCCINT*, or VCCIO* are internally bonded to the corresponding power plane within the associated package. They have no direct connection to any specific package pin.

XC40250XV Pinout Table

XC40250XV Pinout Table

Pad Name	EPIC Pad #	BG432	BG560	PG559
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O, GCK8 (A15)	1	D28	E29	E3
I/O (A14)	2	C28	D30	F4
I/O	3	B29	E28	J7
I/O	4	D27	D29	D2
I/O	5	B28	C30	K8
I/O	6	C27	D28	H6
I/O	7	-	-	-
I/O	8	-	-	-
I/O	9	-	-	-
I/O	10	-	-	-
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	11	-	-	-
I/O	12	-	-	-
I/O	13	-	-	-
I/O	14	-	-	-
I/O	15	-	-	-
I/O	16	-	-	-
I/O	17	D26	A31	G5
I/O	18	A28	E27	F2
I/O	19	B27	C29	H4
I/O	20	C26	B30	G1
I/O	21	D25	D27	J5
I/O	22	A27	C28	L7
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O (A13)	23	B26	E26	J3
I/O (A12)	24	D24	B29	K4
I/O	25	C25	B28	H2
I/O	26	A26	D26	L5
I/O	27	B25	C27	J1
I/O	28	D23	E25	M6
I/O	29	-	A28	K2
I/O	30	-	A27	N7
I/O	31	-	-	-
I/O	32	-	-	-
I/O	33	-	-	-
I/O	34	-	-	-
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	35	-	-	-
I/O	36	-	-	-
I/O	37	-	-	-
I/O	38	-	-	-
I/O	39	-	D25	P8
I/O	40	-	C26	L3
I/O	41	-	E24	L1
I/O	42	-	B26	M4
I/O	43	C24	C25	P2
I/O	44	B24	D24	N5
I/O	45	C23	B25	R1
I/O	46	D22	E23	N3
VCCIO	-	VCCIO*	VCCIO*	-

XC40250XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
GND	-	GND*	GND*	GND*
I/O	47	A24	A25	R7
I/O	48	-	-	P4
VCCINT	-	B23	C24	VCCINT*
I/O	49	C22	D23	T2
I/O	50	B22	B24	T8
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	51	A22	E22	R5
I/O	52	C21	C23	R3
I/O	53	-	A23	U1
I/O	54	-	D22	T4
I/O	55	-	-	-
I/O	56	-	-	-
I/O	57	-	-	-
I/O	58	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	59	-	-	-
I/O	60	-	-	-
I/O	61	-	-	-
I/O	62	-	-	-
I/O	63	-	C22	U5
I/O	64	-	E21	V2
I/O	65	D20	B22	U7
I/O	66	B21	D21	U3
I/O	67	C20	C21	Y2
I/O	68	B20	B21	V4
I/O	69	A20	E20	V6
I/O	70	D19	A21	W5
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O (A11)	71	C19	D20	W7
I/O (A10)	72	B19	C20	Y4
I/O	73	A19	B20	AA1
I/O	74	B18	E19	Y6
I/O (A18)	75	D18	D19	AB2
I/O (A19)	76	C18	C19	Y8
I/O	77	-	-	-
I/O	78	-	-	-
I/O	79	-	-	-
I/O	80	-	-	-
I/O	81	-	-	-
I/O	82	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	83	-	-	-
I/O	84	-	-	-
I/O	85	-	-	-
I/O	86	-	-	-
I/O	87	-	A19	AA3
I/O	88	-	D18	AA5
I/O	89	B17	E18	AC1
I/O	90	C17	C18	AA7
I/O (A9)	91	A17	B18	AB4
I/O (A8)	92	D17	A17	AB6
VCCIO	-	VCCIO*	VCCIO*	VCCIO*

XC40250XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
GND	-	GND*	GND*	GND*
I/O (A7)	93	A16	D17	AC3
I/O (A6)	94	B16	E17	AC5
VCCINT	-	C16	C17	VCCINT*
I/O	95	-	-	AD2
I/O	96	A15	B17	AC7
I/O	97	-	B16	AF2
I/O	98	-	D16	AD4
I/O	99	-	-	-
I/O	100	-	-	-
I/O	101	-	-	-
I/O	102	-	-	-
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	103	-	-	-
I/O	104	-	-	-
I/O	105	-	-	-
I/O	106	-	-	-
I/O	107	-	-	-
I/O	108	-	-	-
I/O (A20)	109	B15	E16	AD6
I/O (A21)	110	C15	C16	AE5
I/O	111	D15	A15	AF4
I/O	112	B14	C15	AG1
I/O (A5)	113	A13	D15	AD8
I/O (A4)	114	C14	E15	AG3
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	115	B13	B14	AH4
I/O	116	D14	C14	AE7
I/O	117	A12	D14	AH2
I/O	118	C13	A13	AF6
I/O	119	B12	E14	AJ1
I/O	120	D13	C13	AG5
I/O	121	-	D13	AJ3
I/O	122	-	B12	AK4
I/O	123	-	-	-
I/O	124	-	-	-
I/O	125	-	-	-
I/O	126	-	-	-
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	127	-	-	-
I/O	128	-	-	-
I/O	129	-	-	-
I/O	130	-	-	-
I/O	131	-	C12	AG7
I/O	132	-	E13	AK2
I/O	133	C12	A11	AJ5
I/O	134	B11	D12	AL3
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	135	D12	B11	AM4
I/O	136	C11	C11	AN1
VCCINT	-	A10	E12	VCCINT*
I/O	137	-	-	AL5
I/O	138	B10	B10	AH8

XC40250XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO	VCCIO*	-
I/O	139	C10	D11	AJ7
I/O	140	B9	C10	AP2
I/O	141	C9	A9	AN3
I/O	142	D10	E11	AP4
I/O	143	-	C9	AR1
I/O	144	-	D10	AN5
I/O	145	-	A8	AM6
I/O	146	-	B8	AK8
I/O	147	-	-	-
I/O	148	-	-	-
I/O	149	-	-	-
I/O	150	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	151	-	-	-
I/O	152	-	-	-
I/O	153	-	-	-
I/O	154	-	-	-
I/O	155	-	E10	AL7
I/O	156	-	C8	AT2
I/O	157	A8	D9	AR3
I/O	158	B8	B7	AU1
I/O	159	D9	A6	AT4
I/O	160	B7	E9	AV2
I/O	161	C7	C7	AR5
I/O	162	D8	D8	AN7
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	163	A6	A5	AW3
I/O	164	B6	B5	AV4
I/O (A3)	165	D7	E8	BA1
I/O,, (CS1, A2)	166	A5	C6	AU5
I/O	167	C6	D7	AY2
I/O	168	B5	B4	AT6
I/O	169	-	-	-
I/O	170	-	-	-
I/O	171	-	-	-
I/O	172	-	-	-
I/O	173	-	-	-
I/O	174	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	175	-	-	-
I/O	176	-	-	-
I/O	177	-	-	-
I/O	178	-	-	-
I/O	179	D6	C5	AP8
I/O	180	A4	E7	AR7
I/O	181	C5	A3	AY4
I/O	182	-	-	BB2
VCCINT	-	B4	D6	VCCINT*
I/O, GCK7 (A1)	183	D5	A2	AV6
I/O (A0, /WS)	184	B3	D5	AT8
GND	-	GND*	GND*	GND*

XC40250XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
O, TDO	-	C4	E6	BA3
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
CCLK	-	D4	C4	BA5
I/O,CK6 (DOUT)	185	D3	D4	BB4
I/O (D0, DIN)	186	C2	E4	AY6
I/O	187	D2	F5	BC3
I/O	188	E4	B3	AW7
I/O	189	D1	D3	BB6
I/O	190	E3	F4	AU9
I/O	191	-	-	-
I/O	192	-	-	-
I/O	193	-	-	-
I/O	194	-	-	-
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	195	-	-	-
I/O	196	-	-	-
I/O	197	-	-	-
I/O	198	-	-	-
I/O	199	E2	C1	AT10
I/O	200	F4	G5	AV8
I/O	201	E1	E3	AY8
I/O	202	F3	D2	BC7
I/O	203	-	-	-
I/O	204	-	-	-
I/O (/RCK, RDY_/BUSY)	205	F2	G4	AW9
I/O (D1)	206	G4	F3	BA9
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	207	-	-	-
I/O	208	-	-	-
I/O	209	-	H5	AU11
I/O	210	-	E2	AY10
I/O	211	F1	F2	BB8
I/O	212	G3	H4	AW11
I/O	213	G2	G3	BC9
I/O	214	H4	J5	AV12
I/O	215	H3	F1	AU13
I/O	216	H2	G1	AT14
I/O	217	-	-	-
I/O	218	-	-	-
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	219	-	-	-
I/O	220	-	-	-
I/O	221	-	-	-
I/O	222	-	-	-
I/O	223	-	J4	BA11
I/O	224	-	H3	AY12
I/O	225	-	K5	BB10
I/O	226	-	H2	AW13
I/O	227	H1	J3	BC11
I/O	228	J4	K4	AU15
I/O	229	J3	J2	BB14
I/O	230	J2	L5	AT16
VCCIO	-	VCCIO*	VCCIO*	-

XC40250XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
GND	-	GND*	GND*	GND*
I/O	231	K4	K3	BA13
I/O	232	-	-	AY14
VCCINT	-	K3	J1	VCCINT*
I/O, FCLK4	233	K2	L4	BC15
I/O	234	K1	K2	AW15
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	235	-	-	-
I/O	236	-	-	-
I/O	237	-	-	-
I/O	238	-	-	-
I/O	239	-	M5	BA15
I/O	240	-	L3	AU17
I/O	241	L3	L1	BB16
I/O (D2)	242	L2	M4	AY16
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	243	M4	M3	AW17
I/O	244	M3	N5	AV18
I/O	245	-	M2	BA17
I/O	246	-	N4	BC17
I/O	247	-	-	-
I/O	248	-	-	-
I/O	249	-	-	-
I/O	250	-	-	-
I/O	251	M2	N3	AU19
I/O	252	M1	N2	BB18
I/O	253	N4	P5	AY18
I/O	254	N3	N1	AW19
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	255	-	-	-
I/O	256	-	-	-
I/O	257	-	-	-
I/O	258	-	-	-
I/O	259	-	-	-
I/O	260	-	-	-
I/O	261	N2	P4	AV20
I/O	262	N1	P3	AT20
I/O	263	P4	P2	BB20
I/O	264	P3	R5	AY20
I/O	265	P2	R4	BC21
I/O	266	R3	R3	BA21
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	267	R4	R1	AW21
I/O	268	-	T4	AU21
I/O	269	-	T5	BB22
I/O	270	-	-	AY22
I/O	271	-	-	-
I/O	272	-	-	-
I/O	273	-	-	-
I/O	274	-	-	-
VCCINT	-	R2	T3	VCCINT*
I/O (/RS)	275	R1	T2	AV22
I/O (D3)	276	T3	U3	BA23

XC40250XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	277	T2	U4	AW23
I/O (D4)	278	T1	U5	AY24
I/O	279	-	-	-
I/O	280	-	-	-
I/O	281	-	-	-
I/O	282	-	-	-
I/O	283	-	U1	BC23
I/O	284	-	U2	BA27
I/O	285	U3	V2	AU23
I/O	286	U4	V4	AV24
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	287	U2	V5	AY26
I/O	288	U1	V3	BB24
I/O	289	V3	W1	AW25
I/O	290	V4	W3	BB26
I/O	291	V2	W4	AT24
I/O	292	W2	W5	BA29
I/O	293	-	-	-
I/O	294	-	-	-
I/O	295	-	-	-
I/O	296	-	-	-
I/O	297	-	-	-
I/O	298	-	-	-
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	299	W3	Y2	AY28
I/O	300	W4	Y3	AU25
I/O	301	-	Y4	AV26
I/O	302	-	AA1	BC27
I/O	303	-	-	-
I/O	304	-	-	-
I/O	305	-	-	-
I/O	306	-	-	-
I/O	307	W1	Y5	AW27
I/O	308	Y1	AA3	BB28
I/O	309	Y3	AA4	BA31
I/O	310	Y4	AB2	AY30
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O (/CS0)	311	Y2	AB3	AW29
I/O (D5)	312	AA2	AA5	BC29
I/O	313	-	AC1	AU27
I/O	314	-	AB4	BA33
I/O	315	-	-	-
I/O	316	-	-	-
I/O	317	-	-	-
I/O	318	-	-	-
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	319	AA3	AC3	AY32
I/O, FCLK3	320	AB1	AB5	AW31
VCCINT	-	AB2	AD2	VCCINT*
I/O	321	-	-	BB30
I/O	322	AB3	AC4	BA35

XC40250XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	323	AB4	AD3	AT28
I/O	324	AC2	AE1	AU29
I/O	325	AD1	AC5	BC33
I/O	326	AC3	AE3	AY34
I/O	327	-	AD4	BB34
I/O	328	-	AF1	AW33
I/O	329	-	AF2	AU31
I/O	330	-	AD5	AV32
I/O	331	-	-	-
I/O	332	-	-	-
I/O	333	-	-	-
I/O	334	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	335	-	-	-
I/O	336	-	-	-
I/O	337	-	-	-
I/O	338	-	-	-
I/O	339	-	AG2	AT30
I/O	340	-	AE4	AU33
I/O	341	AC4	AF3	AW35
I/O	342	AD2	AH1	BC35
I/O	343	AE2	AE5	AY36
I/O	344	AD3	AG3	BB36
I/O	345	AD4	AF4	AV36
I/O (D6)	346	AF1	AJ1	AU35
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	347	AF2	AJ2	AT34
I/O	348	AE3	AF5	AW37
I/O	349	-	-	-
I/O	350	-	-	-
I/O	351	-	-	-
I/O	352	-	-	-
I/O	353	AE4	AH3	BC37
I/O	354	AG1	AG4	AY38
I/O	355	AG2	AK2	BB38
I/O	356	AF3	AJ3	BA41
I/O	357	-	-	-
I/O	358	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	359	-	-	-
I/O	360	-	-	-
I/O	361	-	-	-
I/O	362	-	-	-
I/O	363	AF4	AG5	AY40
I/O	364	AH1	AL1	BB40
I/O	365	AH2	AH4	AT36
I/O	366	AG3	AK3	BA39
I/O, GCK5	367	AG4	AJ4	AV38
I/O (D7)	368	AJ2	AH5	BC41
/PROGRAM	-	AH3	AM1	BB42
VCCIO	-	VCCIO*	VCCIO*	VCCIO*

XC40250XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
DONE	-	AH4	AJ5	AY42
GND	-	GND*	GND*	GND*
I/O, GCK4	369	AJ4	AL4	AW41
I/O	370	AK3	AJ6	AV40
VCCINT	-	AH5	AK5	VCCINT*
I/O	371	-	-	AV42
I/O	372	AK4	AN3	AR37
I/O	373	AJ5	AK6	AP36
I/O	374	AH6	AL5	AT38
I/O	375	-	-	-
I/O	376	-	-	-
I/O	377	-	-	-
I/O	378	-	-	-
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	379	-	-	-
I/O	380	-	-	-
I/O	381	-	-	-
I/O	382	-	-	-
I/O	383	-	-	-
I/O	384	-	-	-
I/O	385	AL4	AJ7	AU39
I/O	386	AK5	AM4	AU43
I/O	387	AJ6	AM5	BA43
I/O	388	AH7	AK7	AT42
I/O	389	AL5	AL6	AR39
I/O	390	AK6	AJ8	AN37
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	391	AH8	AM6	AT40
I/O	392	AJ7	AN6	AP40
I/O	393	AL6	AK8	AR43
I/O	394	AK7	AL7	AN39
I/O	395	AH9	AJ9	AP42
I/O	396	AJ8	AN7	AM38
I/O	397	-	AL8	AN43
I/O	398	-	AK9	AL37
I/O	399	-	-	-
I/O	400	-	-	-
I/O	401	-	-	-
I/O	402	-	-	-
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	403	-	-	-
I/O	404	-	-	-
I/O	405	-	-	-
I/O	406	-	-	-
I/O	407	-	AM8	AK36
I/O	408	-	AJ10	AR41
I/O	409	-	AL9	AL41
I/O	410	-	AM9	AN41
I/O	411	AK8	AK10	AK42
I/O	412	AJ9	AN9	AM40
I/O	413	AH10	AJ11	AJ43
I/O	414	AL8	AL10	AJ37
VCCIO	-	VCCIO*	VCCIO*	-

XC40250XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
GND	-	GND*	GND*	GND*
I/O	415	AK9	AM10	AL39
I/O	416	-	-	AH36
VCCINT	-	AJ10	AK11	VCCINT*
I/O	417	AK10	AL11	AH42
I/O	418	AL10	AJ12	AJ39
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	419	AJ11	AN11	AK40
I/O	420	AH12	AK12	AG41
I/O	421	-	AL12	AJ41
I/O	422	-	AM12	AH40
I/O	423	-	-	-
I/O	424	-	-	-
I/O	425	-	-	-
I/O	426	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	427	-	-	-
I/O	428	-	-	-
I/O	429	-	-	-
I/O	430	-	-	-
I/O	431	-	AJ13	AG37
I/O	432	-	AK13	AG43
I/O	433	AK11	AL13	AG39
I/O	434	AJ12	AM13	AF38
I/O	435	AK12	AN13	AF42
I/O	436	AL12	AJ14	AD42
I/O	437	AH13	AK14	AF40
I/O	438	AJ13	AL14	AE37
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	439	AK13	AM14	AE39
I/O	440	AL13	AN15	AD40
I/O	441	AK14	AJ15	AC43
I/O	442	AH14	AK15	AD38
I/O	443	AJ14	AL15	AC41
I/O	444	AK15	AM16	AD36
I/O	445	-	-	-
I/O	446	-	-	-
I/O	447	-	-	-
I/O	448	-	-	-
I/O	449	-	-	-
I/O	450	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	451	-	-	-
I/O	452	-	-	-
I/O	453	-	-	-
I/O	454	-	-	-
I/O	455	-	AL16	AC39
I/O	456	-	AJ16	AC37
I/O	457	AJ15	AK16	AB40
I/O	458	AL15	AN17	AB42
VCCINT	-	AH15	AM17	VCCINT*
I/O	459	-	-	AB38
I/O	460	AL16	AL17	AA41

XC40250XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O (/INIT)	461	AK16	AJ17	AA39
I/O	462	AJ16	AK17	AA37
I/O	463	AL17	AM18	Y40
I/O	464	AK17	AL18	Y38
I/O	465	-	AK18	AA43
I/O	466	-	AJ18	W39
I/O	467	-	-	-
I/O	468	-	-	-
I/O	469	-	-	-
I/O	470	-	-	-
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	471	-	-	-
I/O	472	-	-	-
I/O	473	-	-	-
I/O	474	-	-	-
I/O	475	-	-	-
I/O	476	-	-	-
I/O	477	AJ17	AN19	V40
I/O	478	AH17	AL19	Y36
I/O	479	AK18	AK19	U41
I/O	480	AL19	AM20	Y42
I/O	481	AJ18	AJ19	T40
I/O	482	AK19	AL20	W37
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	483	AH18	AK20	V38
I/O	484	AL20	AN21	U39
I/O	485	AJ19	AL21	V42
I/O	486	AK20	AJ20	R41
I/O	487	AH19	AM22	U43
I/O	488	AJ20	AK21	P40
I/O	489	-	AN23	T42
I/O	490	-	AL22	U37
I/O	491	-	-	-
I/O	492	-	-	-
I/O	493	-	-	-
I/O	494	-	-	-
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	495	-	-	-
I/O	496	-	-	-
I/O	497	-	-	-
I/O	498	-	-	-
I/O	499	-	AJ21	R39
I/O	500	-	AM23	N41
I/O	501	AK21	AK22	R43
I/O	502	AH20	AM24	M40
VCCIO	-	VCCIO*	VCCIO*	-
I/O	503	AJ21	AL23	N39
I/O	504	AL22	AJ22	T36
VCCINT	-	AK22	AN25	VCCINT*
I/O	505	-	-	P42
I/O	506	AJ22	AK23	R37

XC40250XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	507	AK23	AL24	L41
I/O	508	AJ23	AN26	L43
I/O	509	AH22	AJ23	K40
I/O	510	AL24	AL25	K42
I/O	511	-	AK24	L39
I/O	512	-	AM26	J43
I/O	513	-	AM27	M38
I/O	514	-	AJ24	P36
I/O	515	-	-	-
I/O	516	-	-	-
I/O	517	-	-	-
I/O	518	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	519	-	-	-
I/O	520	-	-	-
I/O	521	-	-	-
I/O	522	-	-	-
I/O	523	-	AL26	N37
I/O	524	-	AK25	H42
I/O	525	AK24	AN28	J41
I/O	526	AH23	AN29	G43
I/O	527	AJ24	AJ25	H40
I/O	528	AK25	AL27	F42
I/O	529	AJ25	AK26	J39
I/O	530	AH24	AM29	L37
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	531	AL26	AM30	E41
I/O	532	AK26	AJ26	F40
I/O	533	AH25	AL28	C43
I/O	534	AL27	AK27	G39
I/O	535	AJ26	AL29	D42
I/O	536	AK27	AN31	H38
I/O	537	-	-	-
I/O	538	-	-	-
I/O	539	-	-	-
I/O	540	-	-	-
I/O	541	-	-	-
I/O	542	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	543	-	-	-
I/O	544	-	-	-
I/O	545	-	-	-
I/O	546	-	-	-
I/O (/LDC)	547	AH26	AJ27	K36
I/O	548	AL28	AM31	J37
I/O	549	AJ27	AK28	B42
I/O	550	AK28	AL30	D40
I/O (HDC)	551	AH27	AK29	C41
I/O, GCK3	552	AK29	AJ28	F38
I (M2)	-	AJ28	AN32	H36
VCCIO	-	VCCIO*	VCCIO*	VCCIO*

XC40250XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
I (M0)	-	AH28	AJ29	C39
GND	-	GND*	GND*	GND*
O (M1)	-	AH29	AK30	D38
I/O, GCK2	553	AJ30	AH29	E37
I/O	554	AH30	AJ30	B40
VCCINT	-	AG28	AK31	VCCINT*
I/O	555	-	-	H34
I/O	556	AH31	AH30	G35
I/O	557	AG29	AL33	F36
I/O	558	AG30	AG29	D36
I/O	559	-	-	-
I/O	560	-	-	-
I/O	561	-	-	-
I/O	562	-	-	-
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	563	AF28	AJ31	E35
I/O	564	AG31	AK32	A41
I/O	565	AF29	AG30	G33
I/O	566	AF30	AH31	B38
I/O	567	-	-	-
I/O	568	-	-	-
I/O	569	-	-	-
I/O	570	-	-	-
I/O	571	-	-	-
I/O	572	-	-	-
I/O	573	AE28	AF29	D34
I/O	574	AF31	AJ32	E33
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	575	AE29	AH32	F32
I/O	576	AE30	AF30	G31
I/O	577	AD28	AG31	A37
I/O	578	AD29	AE29	H30
I/O	579	AD30	AH33	B36
I/O	580	AD31	AG33	C33
I/O	581	-	AE30	C35
I/O	582	-	AF31	D32
I/O	583	-	-	-
I/O	584	-	-	-
I/O	585	-	-	-
I/O	586	-	-	-
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	587	-	-	-
I/O	588	-	-	-
I/O	589	-	-	-
I/O	590	-	-	-
I/O	591	-	AD29	E31
I/O	592	-	AF32	G29
I/O	593	-	AE31	A35
I/O	594	-	AD30	H28
I/O	595	AC28	AE32	B34
I/O	596	AC29	AC29	C31
I/O	597	AC30	AE33	A33
I/O	598	AB28	AD31	D30

XC40250XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O, FCLK2	599	AB29	AC30	E29
I/O	600	-	-	C29
VCCINT	-	AB30	AD32	VCCINT*
I/O	601	AB31	AB29	B30
I/O	602	AA29	AC31	G27
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	603	-	-	-
I/O	604	-	-	-
I/O	605	-	-	-
I/O	606	-	-	-
I/O	607	-	AC33	D28
I/O	608	-	AB30	A29
I/O	609	AA30	AB31	E27
I/O	610	Y28	AA29	F26
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	611	Y29	AB32	C27
I/O	612	Y30	AA30	B28
I/O	613	Y31	AA31	G25
I/O	614	W28	AA32	A27
I/O	615	-	-	-
I/O	616	-	-	-
I/O	617	-	-	-
I/O	618	-	-	-
I/O	619	-	Y29	D26
I/O	620	-	AA33	B26
I/O	621	W29	Y30	E25
I/O	622	W30	Y31	F24
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	623	-	-	-
I/O	624	-	-	-
I/O	625	-	-	-
I/O	626	-	-	-
I/O	627	-	-	-
I/O	628	-	-	-
I/O	629	W31	Y32	H24
I/O	630	V28	W29	B24
I/O	631	V29	W30	D24
I/O	632	V30	W31	A23
I/O	633	U29	W33	C23
I/O	634	U28	V30	E23
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	635	U30	V29	G23
I/O	636	U31	V31	B22
I/O	637	-	V32	D22
I/O	638	-	U33	A21
I/O	639	-	-	-
I/O	640	-	-	-
I/O	641	-	-	-
I/O	642	-	-	-
I/O	643	T29	U30	F22
I/O	644	T30	U29	C21

XC40250XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	645	T31	U31	E21
I/O	646	-	-	D20
VCCINT	-	R29	U32	VCCINT*
I/O	647	-	-	-
I/O	648	-	-	-
I/O	649	-	-	-
I/O	650	-	-	-
I/O	651	-	T32	C17
I/O	652	-	T30	G21
I/O	653	R28	T29	F20
I/O	654	R30	T31	D18
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	655	R31	R33	E19
I/O	656	P29	R31	B20
I/O	657	P28	R30	H20
I/O	658	P30	R29	B18
I/O	659	N30	P32	C15
I/O	660	N29	P31	D16
I/O	661	-	-	-
I/O	662	-	-	-
I/O	663	-	-	-
I/O	664	-	-	-
I/O	665	-	-	-
I/O	666	-	-	-
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
GND	-	GND*	GND*	GND*
I/O	667	N28	N33	G19
I/O	668	N31	P30	A17
I/O	669	M31	P29	F18
I/O	670	M29	M32	E17
I/O	671	-	-	-
I/O	672	-	-	-
I/O	673	-	-	-
I/O	674	-	-	-
I/O	675	-	N31	B16
I/O	676	-	N30	C13
I/O	677	M28	L33	A15
I/O	678	M30	N29	D14
VCCIO	-	VCCIO*	VCCIO*	-
GND	-	GND*	GND*	GND*
I/O	679	L30	M31	E15
I/O	680	L29	L32	G17
I/O	681	-	M30	B14
I/O	682	-	L31	C11
I/O	683	-	-	-
I/O	684	-	-	-
I/O	685	-	-	-
I/O	686	-	-	-
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	687	K31	M29	D12
I/O (TMS)	688	K30	J33	A11
VCCINT	-	K29	K32	VCCINT*
I/O	689	-	-	E13

XC40250XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
I/O, FCLK1	690	K28	L30	C9
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	691	J30	K31	H16
I/O	692	H31	L29	B10
I/O	693	J29	H33	G15
I/O	694	J28	K30	A9
I/O	695	-	J31	D10
I/O	696	-	H32	B8
I/O	697	-	K29	E11
I/O	698	-	H31	G13
I/O	699	-	-	-
I/O	700	-	-	-
I/O	701	-	-	-
I/O	702	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	703	-	-	-
I/O	704	-	-	-
I/O	705	H30	J30	F12
I/O	706	G30	G32	H14
I/O	707	H29	F33	G11
I/O	708	H28	J29	A7
I/O	709	F31	G31	E9
I/O	710	F30	H30	B6
I/O	711	-	E33	D8
I/O	712	-	E32	F8
I/O	713	-	-	-
I/O	714	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	VCCIO*
I/O	715	G29	H29	G9
I/O	716	G28	F31	H10
I/O	717	-	-	-
I/O	718	-	-	-
I/O	719	E31	G30	B4
I/O	720	E30	D32	E7
I/O	721	F29	E31	C5
I/O	722	F28	G29	D6
I/O	723	-	-	-
I/O	724	-	-	-
I/O	725	-	-	-
I/O	726	-	-	-
GND	-	GND*	GND*	GND*
VCCIO	-	VCCIO*	VCCIO*	-
I/O	727	-	-	-
I/O	728	-	-	-
I/O	729	-	-	-
I/O	730	-	-	-
I/O (TCK)	731	D31	C33	D4
I/O (TDI)	732	D30	F30	H8
I/O	733	E29	D31	A3
I/O	734	-	-	F6
VCCINT	-	E28	E30	VCCINT*
I/O (A17)	735	C30	F29	C3
I/O, GCK1 (A16)	736	D29	B33	C1

XC40250XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
GND	-	GND*	GND*	GND*
VCCIO	-	A1	A4	A13
VCCIO	-	A11	A10	A31
VCCIO	-	A21	A16	A43
VCCIO	-	A31	A22	B2
VCCIO	-	D11	A26	C7
VCCIO	-	D21	A30	C19
VCCIO	-	L1	B2	C25
VCCIO	-	L4	B13	C37
VCCIO	-	L28	B19	F14
VCCIO	-	L31	B32	F30
VCCIO	-	AA1	C3	G3
VCCIO	-	AA4	C31	G7
VCCIO	-	AA28	C32	G37
VCCIO	-	AA31	D1	G41
VCCIO	-	AH11	D33	N1
VCCIO	-	AH21	E5	N43
VCCIO	-	AL1	H1	P6
VCCIO	-	AL11	K33	P38
VCCIO	-	AL21	M1	W3
VCCIO	-	AL31	N32	W41
VCCIO	-	C3	R2	AE3
VCCIO	-	C29	T33	AE41
VCCIO	-	AJ3	V1	AK6
VCCIO	-	AJ29	W32	AK38
VCCIO	-	-	AA2	AL1
VCCIO	-	-	AB33	AL43
VCCIO	-	-	AD1	AU3
VCCIO	-	-	AF33	AU7
VCCIO	-	-	AK1	AU37
VCCIO	-	-	AK4	AU41
VCCIO	-	-	AK33	AV14
VCCIO	-	-	AL2	AV30
VCCIO	-	-	AL3	BA7
VCCIO	-	-	AL31	BA19
VCCIO	-	-	AM2	BA25
VCCIO	-	-	AM15	BA37
VCCIO	-	-	AM21	BC1
VCCIO	-	-	AM32	BC13
VCCIO	-	-	AN4	BC31
VCCIO	-	-	AN8	BC43
VCCIO	-	-	AN12	-
VCCIO	-	-	AN18	-
VCCIO	-	-	AN24	-
VCCIO	-	-	AN30	-
VCCINT	-	-	-	H12
VCCINT	-	-	-	H18
VCCINT	-	-	-	H26
VCCINT	-	-	-	H32
VCCINT	-	-	-	M8
VCCINT	-	-	-	M36
VCCINT	-	-	-	V8
VCCINT	-	-	-	V36
VCCINT	-	-	-	AF8

XC40250XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
VCCINT	-	-	-	AF36
VCCINT	-	-	-	AM8
VCCINT	-	-	-	AM36
VCCINT	-	-	-	AT12
VCCINT	-	-	-	AT18
VCCINT	-	-	-	AT26
VCCINT	-	-	-	AT32
GND	-	A2	A7	A5
GND	-	A3	A12	A19
GND	-	A7	A14	A25
GND	-	A9	A18	A39
GND	-	A14	A20	B12
GND	-	A18	A24	B32
GND	-	A23	A29	E1
GND	-	A25	A32	E5
GND	-	A29	B1	E39
GND	-	A30	B6	E43
GND	-	B1	B9	F10
GND	-	B2	B15	F16
GND	-	B30	B23	F28
GND	-	B31	B27	F34
GND	-	C1	B31	H22
GND	-	C31	C2	K6
GND	-	D16	E1	K38
GND	-	G1	F32	M2
GND	-	G31	G2	M42
GND	-	J1	G33	T6
GND	-	J31	J32	T38
GND	-	P1	K1	W1
GND	-	P31	L2	W43
GND	-	T4	M33	AB8
GND	-	T28	P1	AB36
GND	-	V1	P33	AE1
GND	-	V31	R32	AE43
GND	-	AC1	T1	AH6
GND	-	AC31	V33	AH38
GND	-	AE1	W2	AM2
GND	-	AE31	Y1	AM42
GND	-	AH16	Y33	AP6
GND	-	AJ1	AB1	AP38
GND	-	AJ31	AC32	AT22
GND	-	AK1	AD33	AV10
GND	-	AK2	AE2	AV16
GND	-	AK30	AG1	AV28
GND	-	AK31	AG32	AV34
GND	-	AL2	AH2	AW1
GND	-	AL3	AJ33	AW5
GND	-	AL7	AL32	AW39
GND	-	AL9	AM3	AW43
GND	-	AL14	AM11	BB12
GND	-	AL18	AM19	BB32
GND	-	AL23	AM25	BC5
GND	-	AL25	AM28	BC19
GND	-	AL29	AM33	BC25
GND	-	AL30	AM7	BC39

XC40250XV Pinout Table (Continued)

Pad Name	EPIC Pad #	BG432	BG560	PG559
GND	-	-	AN2	-
GND	-	-	AN5	-
GND	-	-	AN10	-
GND	-	-	AN14	-
GND	-	-	AN16	-
GND	-	-	AN20	-
GND	-	-	AN22	-
GND	-	-	AN27	-
NC	-	C8	A1	-
NC	-	-	A33	-
NC	-	-	AC2	-
NC	-	-	AN1	-
NC	-	-	AN33	-

12/21/98

Note: Pads labelled GND, VCCINT*, or VCCIO* are internally bonded to the corresponding power plane within the associated package. They have no direct connection to any specific package pin.