XC4000XLA/XV FPGAs

February 19, 1999 (Version 1.1) Product Specification

XC4000XLA/XV Family Features

Note: XC4000XLA devices are improved versions of XC4000XL devices. The XC4000XV devices have the same features as XLA devices, incorporate additional interconnect resources and extend gate capacity to 500,000 system gates. The XC4000XV devices require a separate 2.5V power supply for internal logic but maintain 5V I/O compatibility via a separate 3.3V I/O power supply. For additional information about the XC4000XLA/XV device architecture, refer to the XC4000E/X FPGA Series general and functional descriptions.

- System-featured Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - Synchronous write option
    - Dual-port RAM option
  - Flexible function generators and abundant flip-flops
  - Dedicated high-speed carry logic
  - Internal 3-state bus capability
  - Eight global low-skew clock or signal distribution networks
- Flexible Array Architecture
- Low-power Segmented Routing Architecture
- Systems-oriented Features
  - IEEE 1149.1-compatible boundary scan
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - Unlimited reprogrammability
- Read Back Capability
  - Program verification and internal node observability

Electrical Features

- XLA Devices Require 3.0 - 3.6 V (VCC)
- XV Devices Require 2.3- 2.7 V (VCCINT) and 3.0 - 3.6 V (VCCIO)
- 5.0 V TTL compatible I/O
- 3.3 V LVTTL, LVCMOS compliant I/O
- 5.0 V and 3.0 V PCI Compliant I/O
- 12 mA or 24 mA Current Sink Capability
- Safe under All Power-up Sequences
- XLA Consumes 40% Less Power than XL
- XV Consumes 65% Less Power than XL
- Optional Input Clamping to VCC (XLA) or VCCIO (XV)

Additional Features

- Footprint Compatible with XC4000XL FPGAs - Lower cost with improved performance and lower power
- Advanced Technology — 5 layer metal, 0.25 µm CMOS process (XV) or 0.35 µm CMOS process (XLA)
- Highest Performance — System erformance beyond 100 MHz
- High Capacity — Up to 500,000 system gates and 270,000 synchronous SRAM bits
- Low Power — 3.3 V/2.5 V technology plus segmented routing architecture
- Safe and Easy to Use — Interfaces to any combination of 3.3 V and 5.0 V TTL compatible devices

Table 1: XC4000XLA Series Field Programmable Gate Arrays

Device	Logic Cells	Max Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. User I/O	Required Configuration Bits
XC4013XLA	1,368	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	192	393,632
XC4020XLA	1,862	20,000	25,088	13,000 - 40,000	28 x 28	784	2,016	224	521,880
XC4028XLA	2,432	28,000	32,768	18,000 - 50,000	32 x 32	1,024	2,560	256	668,184
XC4036XLA	3,078	36,000	41,472	22,000 - 65,000	36 x 36	1,296	3,168	288	832,528
XC4044XLA	3,800	44,000	51,200	27,000 - 80,000	40 x 40	1,600	3,840	320	1,014,928
XC4052XLA	4,598	52,000	61,952	33,000 - 100,000	44 x 44	1,936	4,576	352	1,215,368
XC4062XLA	5,472	62,000	73,728	40,000 - 130,000	48 x 48	2,304	5,376	384	1,433,864
XC4085XLA	7,448	85,000	100,352	55,000 - 180,000	56 x 56	3,136	7,168	448	1,924,992
XC40110XV	9,728	110,000	131,072	75,000 - 235,000	64 x 64	4,096	9,216	448	2,686,136
XC40150XV	12,312	150,000	165,888	100,000 - 300,000	72 x 72	5,184	11,520	448	3,373,448
XC40200XV	16,758	200,000	225,792	130,000 - 400,000	84 x 84	7,056	15,456	448	4,551,056
XC40250XV	20,102	250,000	270,848	180,000 - 500,000	92 x 92	8,464	18,400	448	5,433,888

* Maximum values of gate range assume 20-30% of CLBs used as RAM

General Description

XC4000 Series high-performance, high-capacity Field Programmable Gate Arrays (FPGAs) provide the benefits of custom CMOS VLSI, while avoiding the initial cost, long development cycle, and inherent risk of a conventional masked gate array.

The result of fifteen years of FPGA design experience and feedback from thousands of customers, these FPGAs combine architectural versatility, increased speed, abundant routing resources, and new, sophisticated software to achieve fully automated implementation of complex, high-density, high-performance designs.

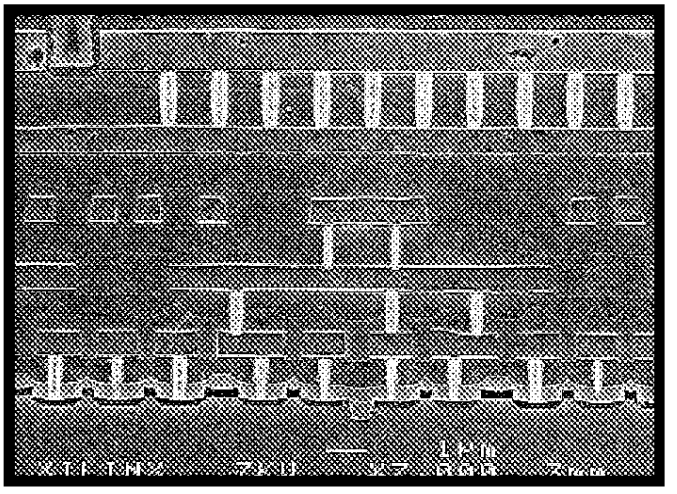


Figure 1: Cross Section of Xilinx 0.25 micron, 5 layer metal XC4000XV FPGA. Visible features are five layers of metallization, tungsten plug vias and trench isolation. The small gaps above the lowest layer are 0.25 micron polysilicon MOSFET gates. The excellent planarity of each metal layer is due to the use of "chemical-mechanical polishing" or CMP. In effect, each layer is ground flat before a new layer is added.

Technology Advantage

XC4000XLA/XV FPGAs use 5 layer metal silicon technology to improve performance while reducing device cost and power. In addition, IOB enhancements provide full PCI compliance and the JTAG functionality is expanded.

Low Power Internal Logic

XC4000XV FPGAs incorporate all the features of the XLA devices but require a separate 2.5V power supply for internal logic. I/O pads are still driven from a 3.3V power supply. The 2.5V logic supply is named VCCINT and the 3.3 V IO supply is named VCCIO.

The XV devices also incorporate additional routing resources in the form of 8 octal-length segmented routing channels vertically and horizontally per row and column.

XLA/XV and XL Family Differences

The XC4000XLA/XV families of FPGAs are logically identical to XC4000EX and XC4000XL FPGAs, however I/O, configuration logic, JTAG functionality, and performance have been enhanced. In addition, they deliver:

- **Improved Performance**
  XLA/XV devices benefit from advance processing technology and a reduction in interconnect capacitance which improves performance over XL devices by more than 30%.
- **Lower Power**
  XLA/XV devices have reduced power requirements compared to equivalent XL devices.
- **Shorter routing delays**
  The smaller die of XLA/XV devices directly reduces clock delays and the delay of high-fanout signals. The reduction in clock delay allows improved pin-to-pin I/O specifications.
- **Lower Cost**
  XLA/XV device cost is directly related to the die size and has been reduced significantly from that of equivalent XL devices.
- **Express mode configuration**
  Express mode configuration is available on the XLA and XV devices.

IOB Enhancements

- **12/24 mA Output Drive**
  The XLA/XV family of FPGAs allow individual IOBs to be configured as high drive outputs. Each output can be configured to have 24 mA drive strength as opposed to the standard default strength of 12 mA.
- **VCC Clamping Diode**
  XLA and XV FPGAs have an optional clamping diode connected from each output to VCC (VCCIO for XV). When enabled they clamp ringing transients back to the 3.3V supply rail. This clamping action is required in 3.3V PCI applications. VCC clamping is a global option affecting all I/O pins. If enabled, TTL I/O compatibility is maintained, but full 5.0 Volt I/O tolerance is sacrificed.
- **Enhanced ESD protection**
  An improved ESD structure allows XV devices to safely pass the stringent 5V PCI (4.2.1.3) ringing test. This test applies an 11V pulse to each IOB for 11 ns via a 55 ohm resistor.
- **Full 3.3V and 5.0V PCI compliance**
  The addition of 12/24 mA drive, optional 3.3V clamping and improved ESD provides full compliance with either 3.3V or 5.0V PCI specifications.

Three-State Register

XC4000XLA/XV devices incorporate an optional register controlling the three-state enable in the IOBs.The use of the three-state control register can significantly improve output enable and disable time.

FastCLK Clock Buffers

The XLA/XV devices incorporate FastCLK clock buffers. Two FastCLK buffers are available on each of the right and left edges of the die. Each FastCLK buffer can provide a fast clock signal (typically < 1.5 ns clock delay) to all the IOBs within the IOB octant containing the buffer. The FastCLK buffers can be instantiated by use of the BUFFCLK symbols. (In addition to FastCLK buffers, the Global Early BUFGE clock buffers #1, #2, #5, and #6 can also provide fast clock signals (typically < 1.5 ns clock delay) to IOBs on the top and bottom of the die.

XLA/XV Power Requirements

XC4000XLA devices require 40% less power per CLB than equivalent XL devices. XC4000XV devices require 42% less power per CLB than equivalent XLA devices and 65% less power than XL devices The representative K-Factor for the following families can be found in Table 2. The K-Factor predicts device current for typical user designs and is based on filling the FPGA with active 16-Bit counters and measuring the device current at 1 MHz. This technique is described in XBRF14 "A Simple Method of Estimating Power in XC4000XL/EX/E FPGAs". To predict device power (P) using the K-Factor use the following formula:

P=V*K*N*F; where:

P= Device Power
V= Power supply voltage
K= the Device K-Factor
N = number of active registers
F = Frequency in MHz

Table 2: K-Factor and Relative Power.

FPGA Family	K-Factor	Power Relative To XL	Power Relative To XLA
XC4000XL	28	1.00	1.65
XC4000XLA	17	0.60	1.00
XC4000XV	13	0.35	0.58

XLA/XV Logic Performance

XC4000XLA/XV devices feature 30% faster device speed than XL devices, and consistent performance is achieved across all family members. Table 3 illustrates the performance of the XLA devices. For details regarding the implementation of these benchmarks refer to XBRF15 "Speed Metrics for High Performance FPGAs".

Table 3: XLA/XV Estimated Benchmark Performance

Register - Register Benchmarks	Size	Maximum Frequency
Adder	8-Bit	172 MHz
	16-Bit	144 MHz
	32-Bit	108 MHz
2 Cascaded Adders	16-Bit	94 MHz
4 Cascaded Adders	16-Bit	57 MHz
Cascaded 4LUTs	1 Level	314 MHz
	2 Level	193 MHz
	4 Level	108 MHz
	6 Level	75 MHz
Interconnect (Manhattan Distance)	1 CLBs	325 MHz
	4 CLBs	260 MHz
	16 CLBs	185 MHz
	64 CLBs	108 MHz
	128 CLBs	81 MHz
Dual Port RAM (Pipelined)	8-Bits by 16	172 MHz
	8-Bits by 256	172 MHz

Using Fast I/O CLKS

There are several issues associated with implementing fast I/O clocks by using multiple FastCLK and BUFGE clock buffers for I/O transfers and a BUFGLS clock buffer for internal logic.

Reduced Clock to Out Period - When transferring data from a BUFGLS clocked register to an IOB output register which is clocked with a fast I/O clock, the total amount of time available for the transfer is reduced.

Using Fast Capture Latch in IOB input - It is necessary to transfer data captured with the fast I/O clock edge to a delayed BUFGLS clock without error. The use of the Fast Capture Latch in the IOBs provides this functionality.

Driving multiple clock inputs - Since each FastCLK input can only reach one octant of IOBs it will usually be necessary to drive multiple FastCLK and BUFGE input pads with a copy of the system clock. Xilinx recommends that systems which use multiple FastCLK and BUFGE input buffers use a "Zero Delay" clock buffer such as the Cypress CY2308 to drive up to 8 input pins. These devices contain a Phase locked loop to eliminate clock delay, and specify less than 250ps output jitter.

PCB layout - The recommended layout is to place the PLL underneath the FPGA on the reverse side of the PCB. All 8 clock lines should be of equal length. This arrangement will allow all the clock line to be less than 2 cm in length which will generally eliminate the need for clock termination.

Advancing the FPGAs clock - An additional advantage to using a PLL-equipped clock buffer is that it can advance the FPGA clocks relative to the system clock by incorporating additional board delay in the feedback path. Approximately 6 inches of trace length are necessary to delay the signal by 1 ns.

Advancing the FPGA's clock directly reduces input hold requirements and improves clock to out delay. FPGA clocks should not be advanced more than the guaranteed minimum Output Hold Time (minus any associated clock jitter) or the outputs may change state before the system clock edge. For XLA and XV FPGAs the Output Hold Time is specified as a minimum Clock to Output Delay in the tables on pages 21, 22, 35, and 36. The maximum recommended clock advance equals this value minus any clock jitter.

Instantiating I/O elements- Depending on the design environment, it may be necessary to instantiate the fast I/O elements. They are found in the libraries as:

- **BUFGE (I,O)** - The Global Early Buffer
- **BUFGLS (I,O)**- The Global Low Skew Buffer
- **BUFFCLK (I,O)** - The FastCLK Buffer
- **ILFFX (D, GF, CE, C, Q)** - The Fast Capture Latch Macro

Locating I/O elements - It is necessary to connect these elements to a particular I/O pad in order to select which buffer or fast capture latch will be used.

Restricted Clock Loading - Because the input hold requirement is a function of internal clock delay, it may be necessary to restrict the routing of BUFGE to IOBs along the top and bottom of the die to obtain sub-ns clock delays.

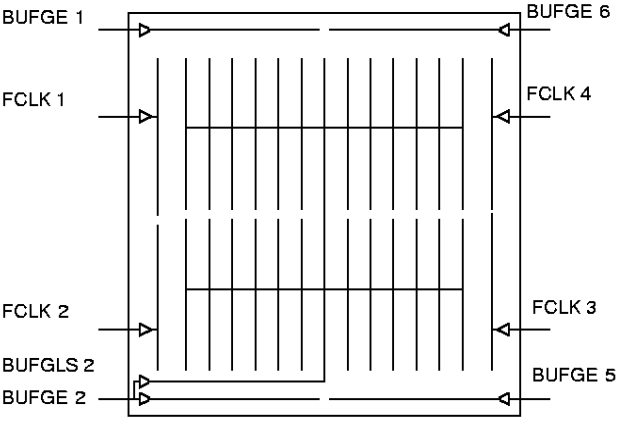


Figure 2: Location of FastCLK, BUFGE and BUFGLS Clock Buffers in XC4000XLA/XV FPGAs

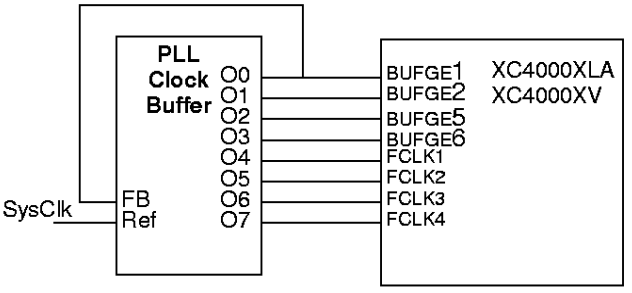


Figure 3: Diagram of XC4000XLA/XV FPGA Connected to PLL Clock Buffer Driving 4 BUFGE and 4 FastCLK Clock Buffers.

JTAG Enhancements

XC4000XLA/XV devices have improved JTAG functionality and performance in the following areas:

- **IDCODE** - The IDCODE register in JTAG is now supported. All future Xilinx FPGAs will support the IDCODE register. By using the IDCODE, the device connected to the JTAG port can be determined. The use of the IDCODE enables selective configuration dependent upon the FPGA found. The IDCODE register has the following binary format:
  `vvvv:ffff:fffa:aaaa:aaaa:cccc:cccc:ccc1`
  Where:
  c = the company code;
  a = the array dimension in CLBs;
  f = the Family code;
  v = the die version number

  Family Codes = 01 for XLA;
  = 02 for SpartanXL;
  = 03 for Virtex;
  = 07 for XV.

  Xilinx company code = 49 (hex)

Table 4: IDCODEs assigned to XC4000XLA/XV FPGAs

FPGA	IDCODE
XC4013XLA	0x00218093
XC4020XLA	0x0021c093
XC4028XLA	0x00220093
XC4036XLA	0x00224093
XC4044XLA	0x00228093
XC4052XLA	0x0022c093
XC4062XLA	0x00230093
XC4085XLA	0x00238093
XC40110XV	0x00e40093
XC40150XV	0x00e48093
XC40200XV	0x00e54093
XC40250XV	0x00e5c093

- **Configuration State** - The configuration state is available to JTAG controllers.
- **Configure Disable** - The JTAG port can be prevented from reconfiguring the FPGA
- **TCK Startup** - TCK can now be used to clock the start-up block in addition to other user clocks.
- **CCLK holdoff** - Changed the requirement for Boundary Scan Configure or EXTEST to be issued prior to the release of INIT pin and CCLK cycling.
- **Reissue configure** - The Boundary Scan Configure can be reissued to recover from an unfinished attempt to configure the device.
- **Bypass FF** - Bypass FF and IOB is modified to provide DRCLOCK only during BYPASS for the bypass flip-flop and during EXTEST or SAMPLE/PRELOAD for the IOB register.

XV and XLA Family Differences

The high density of the XC4000XV family FPGAs is achieved by using advanced 0.25 micron silicon technology. A 2.5 Volt power supply (VCCINT) is necessary to provide the reduced supply voltage required by 0.25 micron internal logic, however to maintain TTL compatibility a 3.3V power supply (VCCIO) is required by the I/O.

To accommodate the higher gate capacity of XV devices, additional interconnect has been added. These differences are detailed below.

- **VCCINT (2.5 Volt) Power Supply Pins**
  The XV family of FPGAs requires a 2.5V power supply for internal logic, which is named VCCINT. The pins assigned to the VCCINT supply are named in the pinout guide for the XC4000XV FPGAs and in Table 5 on page 6.
- **VCCIO (3.3 Volt) Power Supply Pins**
  Both the XV and XLA FPGAs use a 3.3V power supply to power the I/O pins. The I/O supply is named VCCIO in the XV family.
- **Octal-Length Interconnect Channels**
  The XC40110XV, XC40150XV, XC40200XV, and XC40250XV have enhanced routing. Eight routing channels of octal length have been added to each CLB in both vertical and horizontal dimensions.

XLA-to-XLSocket Compatibility

The XC4000XLA devices are generally available in the same packages as equivalent XL devices, however the range of packages available for the XC4085XLA has been extended to include smaller packages such as the HQ240.

XV-to-XL/XLA Socket Compatibility

XC4000XV devices are available in five package options, pin-grid PG599 and ball-grid BG560, BG432, and BG352 and quad-flatpack HQ240. With the exception of the VCCINT power pins, XC4000XV FPGAs are compatible with XL and XLA devices in these packages if the following guidelines are followed:

- Lay out the PCB for the XV pinout.
- When an XL or XLA device is installed disconnect the VCCINT (2.5 V) supply. For the PG599, VCCINT should be connected to 3.3V. For BG560, BG432 and BG352 and HQ240 packages, the VCCINT voltage source should be left unconnected. The unused I/O pins in the XL/XLA devices connected to VCCINT will be pulled up to 3.3V. Care must be taken to insure that these pins are not driven when the XL/XLA device is operative.
- When an XC4000XV is installed, the VCCINT pins must

be connected to a 2.5V power supply.

The differences between the XL and XV packages are detailed below:

PG559 - XLA and XL devices in the PG599 package have 56 VCC pins.The XC4000XV devices allocate 16 of these I/O pins to VCCINT (2.5V).

BG560 - XLA and XL devices in the BG560 package have 448 I/O pins.The XC4000XV devices allocate 16 of these I/O pins to VCCINT (2.5V).

BG432- XLA and XL devices in the BG432 package have 352 I/O pins. The XC4000XV devices allocate 16 of these I/O pins to VCCINT (2.5V).

BG352 - XLA and XL devices in the BG352 package have 289 I/O pins.The XC4000XV devices allocate 15 of these I/O pins to VCCINT (2.5V).

HQ240- XLA and XL devices in the HQ240 package have 193 I/O pins.The XC4000XV devices allocate 15 of these I/O pins to VCCINT (2.5V).

Table 5: VCCINT (2.5 V) Pins in XV Packages

HQ240	BG352	BG432	BG560	PG559
P198	D10	A10	E12	H12
P185	D5	AB2	AD2	H18
P164	K4	AB30	AD32	H26
P154	N3	AG28	AK31	H32
P137	W2	AH15	AM17	M8
P116	AE3	AH5	AK5	M36
P104	AC10	AJ10	AK11	V8
P93	AC13	AK22	AN25	V36
P77	AE19	B23	C24	AF8
P55	AB24	B4	D6	AF36
P43	V24	C16	C17	AM8
P27	N24	E28	E30	AM36
P16	J24	K29	K32	AT12
P4	D24	K3	J1	AT18
P225	A20	R2	T3	AT26
-	-	R29	U32	AT32

I/O Signalling Standards

XLA and XV devices are compatible with TTL, LVTTL, PCI 3V, PCI 5V and LVCMOS signalling. The various standards are illustrated in Table 6 and the signaling environment is illustrated in Figure 4.

VCC Clamping

XLA/XV devices are fully 5V TTL I/O compatible if VCC clamping is not enabled. The I/O pins can withstand input voltages up to 7V. With VCC clamping enabled, the XLA/XV devices will begin to clamp input voltages to one diode voltage drop above VCC. In both cases negative voltage is clamped to one diode voltage drop below ground.

XLA/XV devices maintain LVTTL I/O compatibility when VCC clamping is enabled, however full 5.0V TTL I/O compatibility is sacrificed.

Overshoot and Undershoot

Ringing wave forms are allowed on XLA/XV inputs as long as undershoot is limited to -2.0V and overshoot is limited to +7.0V and current is limited to 100 mA for less than 10 ns. If VCC clamping is enabled then overshoot will begin to be clamped at VCC/VCCIO plus one diode voltage drop and undershoot will be clamped to ground minus one diode voltage drop. In either case the current must be limited to 100 mA per pin for less than 10 ns.

Table 6: I/O Standards supported by XC4000XLA and XV FPGAs

Signaling Standard	VCC Clamping	Output Drive	V_{IH_MAX}	$V_{IH\ MIN}$	$V_{IL\ MAX}$	$V_{OH\ MIN}$	$V_{OL\ MAX}$
TTL	Not allowed	12/24 mA	5.5	2.0	0.8	2.4	0.4
LVTTL	OK	12/24 mA	3.6	2.0	0.8	2.4	0.4
PCI5V	Not allowed	24 mA	5.5	2.0	0.8	2.4	0.4
PCI3V	Required	12 mA	3.6	50% of VCC/VCCIO	30% of VCC/VCCIO	90% of VCC/VCCIO	10% of VCC/VCCIO
LVCMOS 3V	OK	12/24 mA	3.6	50% of VCC/VCCIO	30% of VCC/VCCIO	90% of VCC/VCCIO	10% of VCC/VCCIO

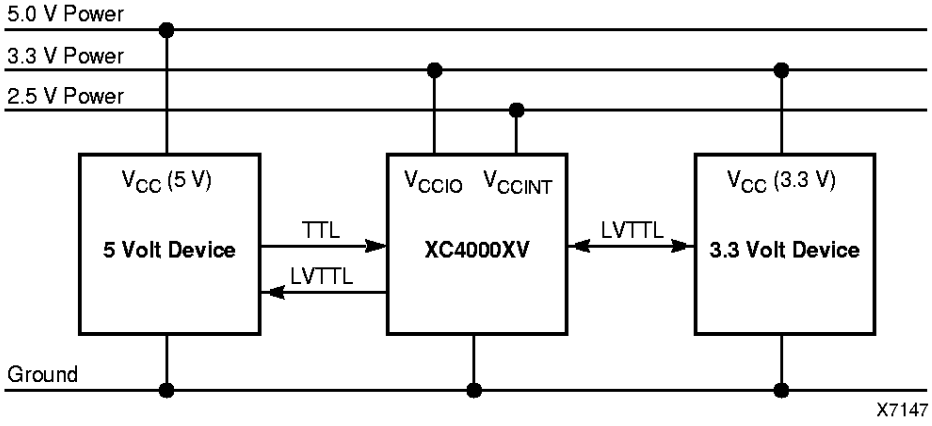


Figure 4: **The Signalling Environment for XLA/XV FPGAS.** For XLA devices the VCCIO and VCCINT supplies are replaced by a single 3.3 Volt VCC supply, however, all indicated I/O signalling is still supported.

Express Configuration Mode

Express configuration mode is similar to Slave Serial configuration mode, except that data is processed one byte per CCLK cycle instead of one bit per CCLK cycle. An external source is used to drive CCLK, while byte-wide data is loaded directly into the configuration data shift registers (Figure 5). A CCLK frequency of 10 MHz is equivalent to a 80 MHz serial rate, because eight bits of configuration data are loaded per CCLK cycle. Express mode does not sup-

port CRC error checking, but does support constant-field error checking. A length count is not used in Express mode.

Express mode must be specified as an option to the BitGen program, which generates the bitstream. The Express mode bitstream is not compatible with the other configuration modes. Express mode is selected by a <010> on the mode pins (M2, M1, M0).

The first byte of parallel configuration data must be available at the D inputs of the FPGA a short setup time before the second rising CCLK edge. Subsequent data bytes are clocked in on each consecutive rising CCLK edge (Figure 8).

Pseudo Daisy Chain

As illustrated in Figures 5 and 6, multiple devices with different configurations can be configured in a pseudo daisy chain provided that all of the devices are in Express mode. A single combined byte-wide data stream is used to configure the chain of Express mode devices. CCLK pins are tied together and D0-D7 pins are tied together as a data buss for all devices along the chain. A status signal is passed from DOUT of each device to the CS1 input of the device which follows it in the chain. Frame data is accepted only when CS1 is High and the device's configuration memory is not already full. The lead device in the chain has its CS1 input tied High (or floating, since there is an internal pullup). The status pin DOUT is initially High for all devices in the chain until the data stream header of seven bytes is loaded. This allows header data to be loaded into all devices in the chain simultaneously. After the header is loaded in all devices, their DOUT pins are pulled Low disabling configuration of all devices in the chain except the first device. As each device in the chain is filled, its DOUT goes High driving High the CS1 input of the next device, thereby enabling configuration of the next device in the pseudo daisy chain.

The requirement that all DONE pins in a daisy chain be wired together applies only to Express mode, and only if all devices in the chain are to become active simultaneously. All 4000XLA/XV devices in Express mode are synchronized to the DONE pin. User I/O for each device becomes active after the DONE pin for that device goes High (The exact timing is determined by BitGen options.)

Since the DONE pin is open-drain and does not drive a High value, tying the DONE pins of all devices together prevents all devices in the chain from going High until the last device in the chain has completed its configuration cycle. If the DONE pin of a device is left unconnected, the device becomes active as soon as that device has been configured.

Table 7: Pin Functions During Configuration (4000XLA/XV Express mode only)

CONFIGURATION MODE <M2:M1:M0>	USER OPERATION
EXPRESS MODE <0:1:0>	PIN FUNCTION
M2(LOW) (I)	M2
M1(HIGH) (I)	M1
M0(LOW) (I)	M0
HDC (HIGH)	I/O
$\overline{\text{LDC}}$ (LOW)	I/O
$\overline{\text{INIT}}$	I/O
DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
CCLK (I)	CCLK (I)
DATA 7 (I)	I/O
DATA 6 (I)	I/O
DATA 5 (I)	I/O
DATA 4 (I)	I/O
DATA 3 (I)	I/O
DATA 2 (I)	I/O
DATA 1 (I)	I/O
DATA 0 (I)	I/O
DOUT	SGCK4-I/O
TDI	TDI-I/O
TCK	TCK-I/O
TMS	TMS-I/O
TDO	TDO-(O)
CS1	I/O

Notes
1. A shaded table cell represents the internal pull-up used before and during configuration.
2. (I) represents an input; (O) represents an output.
3. $\overline{\text{INIT}}$ is an open-drain output during configuration.

Because only XC4000XLA/XV, SpartanXL, and XC5200 devices support Express mode, only these devices can be used to form an Express mode pseudo daisy chain.

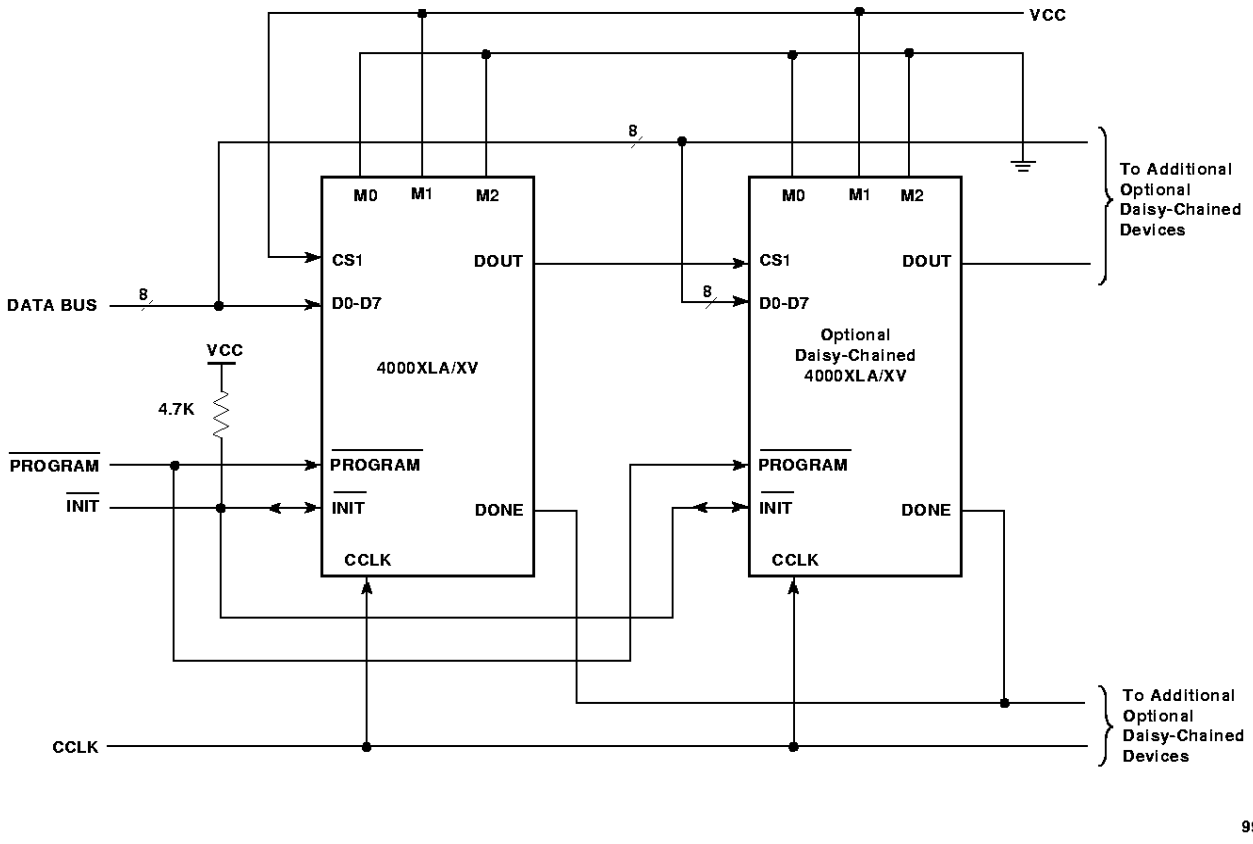
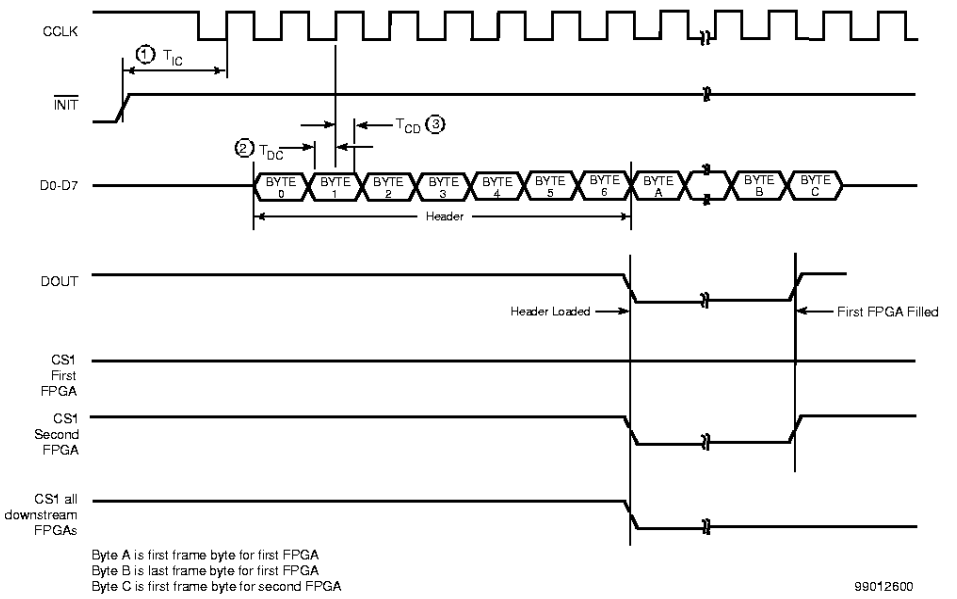


Figure 5: Express Mode Circuit Diagram

Table 8: Express Mode Programming Switching Characteristic

	Description	Symbol	Min	Max	Units
CCLK	$\overline{INIT}$ (High) setup time	T_{IC}	5		µs
	D0 - D7 setup time	T_{DC}	20		ns
	D0 - D7 hold time	T_{CD}	0		ns
	CCLK High time	T_{CCH}	45		ns
	CCLK Low time	T_{CCL}	45		ns
	CCLK Frequency	F_{CC}		10	MHz
			Preliminary		



Note: CS1 *must* remain High throughout loading of the configuration data stream. In the pseudo daisy chain of Figure 5, the 7 byte data stream header is loaded into all devices simultaneously. Each device's data frames are then loaded in turn when its CS1 pin is driven High by the DOUT of the preceding device in the chain.

Figure 6: Express Mode Circuit Diagram

Data Stream Format

The data stream ("bitstream") format is identical for all serial configuration modes, but different for the 4000XLA/XV Express mode. In Express mode, the device becomes active when DONE goes High, therefore no length count is required. Additionally, CRC error checking is not supported in Express mode. The data stream format is shown in Table 9. Express mode data is shown with D0 at the left and D7 at the right.

The configuration data stream begins with two bytes of eight ones each, a preamble code of one byte, followed by three bytes of eight ones each, and finally an end-of-header field check byte. This header of seven bytes is followed by the actual configuration data in frames. The length and number of frames depends on the device type. Each frame begins with a start field and ends with an end-of-frame field check byte. In all cases, additional start-up bytes of data are required to provide six, or more, clocks for the start-up sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All startup bytes are don't-cares; these bytes are not included in bitstreams created by the Xilinx software.

A selection of CRC or non-CRC error checking is allowed by the bitstream generation software. The 4000XLA Express mode only supports non-CRC error checking. The non-CRC error checking tests for a designated end-of-frame field check byte for each frame. non-CRC error checking tests for a designated end-of-frame field check byte for each frame.

Table 9: 4000XLA/XV Express Mode Data Stream Format

Data Type	Express Mode (D0-D7) (4000XLA only)
Fill Byte	FFFFh
Preamble Code	11110010b
Fill Byte	FFFFFFh
End-of-Header Field Check Byte	11010010b
Start Field	11111110b
Data Frame	DATA(n-1:0)
End-of-Frame Field Check Byte	11010010b
Extend Write Cycle	FFD2FFFFFFh
Start-Up Bytes	FFFFFFFFFFFFh

LEGEND:

Unshaded	Once per data stream
Light	Once per data frame

Detection of an error results in the suspension of data loading and the pulling down of the $\overline{INIT}$ pin. The user must detect $\overline{INIT}$ and initialize a new configuration by pulsing the $\overline{PROGRAM}$ pin Low or cycling VCC.

Serial PROM Recommendation

Table 10 shows the physical characteristics of each XLA/XV family member and the recommended Xilinx Serial PROM recommended for use as configuration storage.

Table 10: Physical Characteristics and Recommended Serial PROM

Device	Max. User I/O	CLB Matrix	Total CLBs	Logic Cells	Number of Flip-Flops	Max. RAM Bits (No Logic)	Required Configur-ation Bits	Serial PROM
XC4013XLA	192	24 x 24	576	1,368	1,536	18,432	393,632	XC17512L
XC4020XLA	224	28 x 28	784	1,862	2,016	25,088	521,880	XC17512L
XC4028XLA	256	32 x 32	1,024	2,432	2,560	32,768	668,184	XC1701L
XC4036XLA	288	36 x 36	1,296	3,078	3,168	41,472	832,528	XC1701L
XC4044XLA	320	40 x 40	1,600	3,800	3,840	51,200	1,014,928	XC1701L
XC4052XLA	352	44 x 44	1,936	4,598	4,576	61,952	1,215,368	XC1702L
XC4062XLA	384	48 x 48	2,304	5,472	5,376	73,728	1,433,864	XC1702L
XC4085XLA	448	56 x 56	3,136	7,448	7,168	100,352	1,924,992	XC1702L
XC40110XV	448	64 x 64	4,096	9,728	9,216	131,072	2,686,136	XC1704L
XC40150XV	448	72 x 72	5,184	12,312	11,520	165,888	3,373,448	XC1704L
XC40200XV	448	84 x 84	7,056	16,758	15,456	225,792	4,551,056	XC1704L+XC17512L
XC40250XV	448	92 x 92	8,464	20,102	18,400	270,848	5,433,888	XC1704L+XC1702L

User I/O Per Package

Table 11 shows the number of user I/Os available in each package for XC4000XLA/XV-Series devices. Call your local sales office for the latest availability information.

Table 11: User I/O Pins Available by Device and Package

		Maximum I/O Accessible per Package											
Device	Max I/O	HQ160	PQ160	HQ208	PQ208	HQ240	PQ240	BG256	HQ304	BG352	BG432	PG559	BG560
XC4013XLA	192		129		160		192	192					
XC4020XLA	224		129		160		193	205					
XC4028XLA	256	129		160		193		205	256	256			
XC4036XLA	288	129		160		193			256	288	288		
XC4044XLA	320	129		160		193			256	289	320		
XC4052XLA	352	129		160		193			256	289	352		352
XC4062XLA	384	129		160		193			256	289	352		384
XC4085XLA	448	129		160		193			256	289	352		448
XC40110XV	448					178				274	336		432
XC40150XV	448					178				274	336	448	432
XC40200XV	448										336		432
XC40250XV	448										336	448	432

Product Availability

XLA Family

Table 12 shows the current available package and speed grade combinations for XC4000XLA Series devices. Call your local sales office for the latest availability information, or see the Xilinx WEBLINX at http://www.xilinx.com for the latest revision of the specifications.

Table 12: Component Availability Chart for XC4000XLA FPGAs

	PINS	84	100	100	144	144	160	160	176	176	208	208	240	240	256	299	304	352	411	432	475	559	560
	TYPE	Plast. PLCC	Plast. PQFP	Plast. VQFP	Plast. TQFP	High-Perf. TQFP	High-Perf. QFP	Plast. PQFP	Plast. TQFP	High-Perf. TQFP	High-Perf. QFP	Plast. PQFP	High-Perf. QFP	Plast. PQFP	Plast. BGA	Ceram. PGA	High-Perf. QFP	Plast. BGA	Ceram. PGA	Plast. BGA	Ceram. PGA	Ceram. PGA	Plast. BGA
	CODE	PC84	PQ100	VQ100	TQ144	HT144	HQ160	PQ160	TQ176	HT176	HQ208	PQ208	HQ240	PQ240	BG256	PG299	HQ304	BG352	PG411	BG432	PG475	PG559	BG560
XC4013XLA	-09							C I				C I		C I	C I								
	-08							C I				C I		C I	C I								
	-07							C				C		C	C								
XC4020XLA	-09							C I				C I		C I	C I								
	-08							C I				C I		C I	C I								
	-07							C				C		C	C								
XC4028XLA	-09						C I				C I		C I		C I			C I					
	-08						C I				C I		C I		C I			C I					
	-07						C				C		C		C			C					
XC4036XLA	-09						C I				C I		C I					C I		C I			
	-08						C I				C I		C I					C I		C I			
	-07						C				C		C					C		C			
XC4044XLA	-09						C I				C I		C I				C I	C I		C I			
	-08						C I				C I		C I				C I	C I		C I			
	-07						C				C		C				C	C		C			
XC4052XLA	-09						C I				C I		C I				C I	C I		C I			C I
	-08						C I				C I		C I				C I	C I		C I			C I
	-07						C				C		C				C	C		C			C
XC4062XLA	-09						C I				C I		C I				C I	C I		C I			C I
	-08						C I				C I		C I				C I	C I		C I			C I
	-07						C				C		C				C	C		C			C
XC4085XLA	-09						C I				C I		C I				C I	C I		C I			C I
	-08						C I				C I		C I				C I	C I		C I			C I
	-07						C				C		C				C	C		C			C

1/25/99

C = Commercial T_J = 0° to +85°C

I= Industrial T_J = -40°C to +100°C

XV Family

Table 13 show the current available package and speed grade combinations for the XC4000XV Series devices. Call your local sales office for the latest availability information, or see the Xilinx WEBLINX at http://www.xilinx.com for the latest revision of the specifications.

Table 13: Component Availability Chart for XC4000XV FPGAs

	PINS	84	100	100	144	144	160	160	176	176	208	208	240	240	256	299	304	352	411	432	475	559	560
	TYPE	Plast. PLCC	Plast. PQFP	Plast. VQFP	Plast. TQFP	High-Perf. TQFP	High-Perf. QFP	Plast. PQFP	Plast. TQFP	High-Perf. TQFP	High-Perf. QFP	Plast. PQFP	High-Perf. QFP	Plast. PQFP	Plast. BGA	Ceram. PGA	High-Perf. QFP	Plast. BGA	Ceram. PGA	Plast. BGA	Ceram. PGA	Ceram. PGA	Plast. BGA
	CODE	PC84	PQ100	VQ100	TQ144	HT144	HQ160	PQ160	TQ176	HT176	HQ208	PQ208	HQ240	PQ240	BG256	PG299	HQ304	BG352	PG411	BG432	PG475	PG559	BG560
XC40110XV	-09												C I					C I		C I			C I
	-08												C I					C I		C I			C I
	-07												C					C		C			C
XC40150XV	-09												C I					C I		C I		C I	C I
	-08												C I					C I		C I		C I	C I
	-07												C					C		C		C	C
XC40200XV	-09																			C I			C I
	-08																			C I			C I
	-07																			C			C
XC40250XV	-09																			C I		C I	C I
	-08																			C I		C I	C I
	-07																			C		C	C

11/24/98

C = Commercial T_J = 0° to +85°C

I= Industrial T_J = -40°C to +100°C

6

XLA Specification Information

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered final.

Occasionally, values are of mixed classification. These are highlighted in bold face and the tables involved include a note explaining the nature of the bold face entries. All specifications are subject to change without notice.

Additional Specifications

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

XLA D.C. Characteristic Guidelines

Absolute Maximum Ratings

Symbol	Description		Values	Units
V_{CC}	Supply voltage relative to GND		-0.5 to 4.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to 5.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to 5.5	V
V_{CCt}	Longest Supply Voltage Rise Time from 1 V to 3V		50	ms
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Notes: 1. Maximum DC overshoot or undershoot above V_{cc} or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to + 7.0 V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device a

t these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	3.0	3.6	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	3.0	3.6	V
V_{IH}	High-level input voltage		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage		0	30% of V_{CC}	V
T_{IN}	Input signal transition time			250	ns

Note: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C. Input and output measurement threshold is ~50% of V_{CC}.

DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0 mA, V_{CC} min (LVTTL)		2.4		V
	High-level output voltage @ I_{OH} = -500 µA, (LVCMOS)		90% V_{CC}		V
V_{OL}	Low-level output voltage @ I_{OL} = 24.0 mA, V_{CC} min (LVTTL) (Note 1)			0.4	V
	Low-level output voltage @ I_{OL} = 1500 µA, (LVCMOS)			10% V_{CC}	V
V_{DR}	Data Retention Supply Voltage (below which configuration data may be lost)		2.5		V
I_{CCO}	Quiescent FPGA supply current (Note 2)			10	mA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, SBGA, PQ, HQ, MQ packages		10	pF
		PGA packages		16	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)		0.02	0.15	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.3	2.0	mA

Notes: 1. With up to 64 pins simultaneously sinking 24 mA
2. With no output current loads, no active input or Longline pull-up resistors, all I/O pins Tri-stated and floating

XLA AC Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature. Values apply to all XC4000XLA devices and expressed in nanoseconds unless otherwise noted.

Delay Via Global Low Skew Clock Buffer to Clock

		Speed Grade	All	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Max**	**Max**	
Delay from pad through Global Low Skew (GLS) clock buffer to any clock input, K.	T_{GLS}	XC4013XLA	0.7	2.4	2.1	1.9	ns
		XC4020XLA	0.7	2.6	2.3	2.1	ns
		XC4028XLA	0.8	2.9	2.6	2.3	ns
		XC4036XLA	0.8	3.2	2.8	2.5	ns
		XC4044XLA	0.9	3.6	3.1	2.8	ns
		XC4052XLA	1.0	3.9	3.4	3.1	ns
		XC4062XLA	1.1	4.2	3.7	3.3	ns
		XC4085XLA	1.2	5.0	4.4	3.9	ns
			Preliminary				

Delay Via FastCLK Buffer to IOB Clock

		Speed Grade	All	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Max**	**Max**	
Delay from pad through FastCLK buffer to any IOB clock input.	T_{FCLK}	XC4013XLA	0.4	1.5	1.3	1.1	ns
		XC4020XLA	0.5	1.5	1.3	1.2	ns
		XC4028XLA	0.5	1.6	1.4	1.3	ns
		XC4036XLA	0.5	1.7	1.5	1.4	ns
		XC4044XLA	0.5	1.8	1.6	1.4	ns
		XC4052XLA	0.6	1.9	1.7	1.5	ns
		XC4062XLA	0.6	2.0	1.8	1.6	ns
		XC4085XLA	0.6	2.3	2.0	1.8	ns
			Preliminary				

Note: Values in **bold face** are preliminary, all other values are advance.

Delay Via Global Early BUFGEs 1, 2, 5, 6 to IOB Clock

		Speed Grade	All	-09	-08	-07	Units
Description	Symbol	Device	Min	Max	Max	Max	
Delay from pad through Global Early (GE) clock buffer to any IOB clock input for BUFGEs 1, 2, 5, and 6.	T_{GE}	XC4013XLA	0.2	1.7	1.5	1.3	ns
		XC4020XLA	0.2	1.9	1.7	1.5	ns
		XC4028XLA	0.2	2.1	1.9	1.7	ns
		XC4036XLA	0.3	2.4	2.2	1.9	ns
		XC4044XLA	0.3	2.7	2.4	2.2	ns
		XC4052XLA	0.3	3.0	2.7	2.4	ns
		XC4062XLA	0.3	3.3	3.0	2.7	ns
		XC4085XLA	0.3	3.7	3.3	3.0	ns
			Preliminary				

Delay Via Global Early BUFGEs 3, 4, 7, 8 to IOB Clock

		Speed Grade	All	-09	-08	-07	Units
Description	Symbol	Device	Min	Max	Max	Max	
Delay from pad through Global Early (GE) clock buffer to any IOB clock input for BUFGEs 3, 4, 7, and 8.	T_{GE}	XC4013XLA	0.5	2.5	2.2	1.9	ns
		XC4020XLA	0.6	2.7	2.4	2.1	ns
		XC4028XLA	0.6	2.9	2.5	2.3	ns
		XC4036XLA	0.7	3.1	2.7	2.4	ns
		XC4044XLA	0.8	3.3	2.9	2.6	ns
		XC4052XLA	0.8	3.6	3.1	2.8	ns
		XC4062XLA	0.9	3.8	3.4	3.0	ns
		XC4085XLA	1.0	4.3	3.8	3.4	ns
			Preliminary				

CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XLA devices and expressed in nanoseconds unless otherwise noted.

	Speed Grade	-09		-08		-07		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Combinatorial Delays								
F/G inputs to X/Y outputs	T_{ILO}		1.1		1.0		0.9	ns
F/G inputs via H' to X/Y outputs	T_{IHO}		1.9		1.7		1.5	ns
F/G inputs via transparent latch to Q outputs	T_{ITO}		2.0		1.8		1.6	ns
C inputs via SR/H0 via H to X/Y outputs	T_{HH0O}		1.7		1.6		1.4	ns
C inputs via H1 via H to X/Y outputs	T_{HH1O}		1.6		1.4		1.3	ns
C inputs via DIN/H2 via H to X/Y outputs	T_{HH2O}		1.7		1.6		1.4	ns
C inputs via EC, DIN/H2 to YQ, XQ output (bypass)	T_{CBYP}		1.1		1.0		0.9	ns
CLB Fast Carry Logic								
Operand inputs (F1, F2, G1, G4) to C_{OUT}	T_{OPCY}		1.0		0.9		0.8	ns
Add/Subtract input (F3) to C_{OUT}	T_{ASCY}		1.2		1.1		1.0	ns
Initialization inputs (F1, F3) to C_{OUT}	T_{INCY}		0.8		0.7		0.6	ns
C_{IN} through function generators to X/Y outputs	T_{SUM}		1.7		1.5		1.3	ns
C_{IN} to C_{OUT}, bypass function generators	T_{BYP}		0.1		0.1		0.1	ns
Carry Net Delay, C_{OUT} to C_{IN}	T_{NET}		0.17		0.15		0.13	ns
Sequential Delays								
Clock K to Flip-Flop outputs Q	T_{CKO}		1.5		1.3		1.2	ns
Clock K to Latch outputs Q	T_{CKLO}		1.5		1.3		1.2	ns
Setup Time before Clock K								
F/G inputs	T_{ICK}	0.7		0.7		0.6		ns
F/G inputs via H	T_{IHCK}	1.4		1.3		1.2		ns
C inputs via H0 through H	T_{HH0CK}	1.3		1.2		1.1		ns
C inputs via H1 through H	T_{HH1CK}	1.2		1.1		1.0		ns
C inputs via H2 through H	T_{HH2CK}	1.3		1.2		1.1		ns
C inputs via DIN	T_{DICK}	0.6		0.6		0.5		ns
C inputs via EC	T_{ECCK}	0.7		0.6		0.5		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	0.5		0.4		0.4		ns
CIN input via F/G	T_{CCK}	1.2		1.1		1.0		ns
CIN input via F/G and H	T_{CHCK}	2.0		1.7		1.6		ns
Hold Time after Clock K								
All Hold Times		0.0		0.0		0.0		ns
Clock								
Clock High time	T_{CH}	2.2		1.9		1.7		ns
Clock Low time	T_{CL}	2.2		1.9		1.7		ns
Set/Reset Direct								
Width (High)	T_{RPW}	2.3		2.3		2.3		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		2.5		2.2		2.0	ns
Global Set/Reset								
Minimum GSR Pulse Width	T_{MRW}		12.8		11.4		10.2	ns
Delay from GSR input to any Q	T_{MRQ}	See page 27 for TRRI values per device.						
Toggle Frequency (MHz) (for export control)	F_{TOG}		227		263		294	MHz
		Preliminary						

CLB RAM Synchronous (Edge-Triggered) Read/Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XLA devices and are expressed in nanoseconds unless otherwise noted.

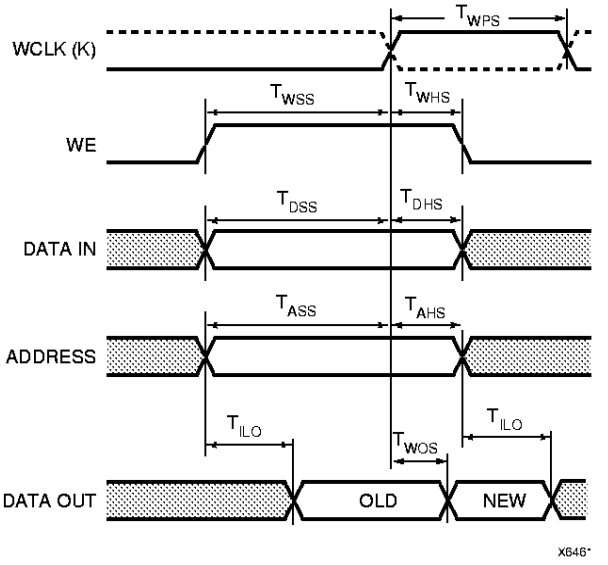
Single Port RAM	Speed Grade		-09		-08		-07		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	
Write Operation									
Address write cycle time (clock K period)	16x2 32x1	T_{WCS} T_{WCTS}	6.7 6.7		5.9 5.9		5.3 5.3		ns ns
Clock K pulse width (active edge)	16x2 32x1	T_{WPS} T_{WPTS}	3.4 3.4		3.0 3.0		2.7 2.7		ns ns
Address setup time before clock K	16x2 32x1	T_{ASS} T_{ASTS}	1.5 1.5		1.3 1.3		1.2 1.2		ns ns
Address hold time after clock K	16x2 32x1	T_{AHS} T_{AHTS}	0.0 0.0		0.0 0.0		0.0 0.0		ns ns
DIN setup time before clock K	16x2 32x1	T_{DSS} T_{DSTS}	1.5 1.8		1.3 1.6		1.2 1.5		ns ns
DIN hold time after clock K	16x2 32x1	T_{DHS} T_{DHTS}	0.0 0.0		0.0 0.0		0.0 0.0		ns ns
WE setup time before clock K	16x2 32x1	T_{WSS} T_{WSTS}	1.4 1.3		1.3 1.2		1.1 1.1		ns ns
WE hold time after clock K	16x2 32x1	T_{WHS} T_{WHTS}	0.0 0.0		0.0 0.0		0.0 0.0		ns ns
Data valid after clock K	16x2 32x1	T_{WOS} T_{WOTS}		5.0 5.8		4.4 5.2		4.0 4.7	ns ns
Read Operation									
Address read cycle time	16x2 32x1	T_{RC} T_{RCT}	2.6 3.8		2.6 3.8		2.6 3.8		ns ns
Data Valid after address change (no Write Enable)	16x2 32x1	T_{ILO} T_{IHO}		1.1 1.9		1.0 1.7		0.9 1.5	ns ns
Address setup time before clock K	16x2 32x1	T_{ICK} T_{IHCK}	0.7 1.4		0.7 1.3		0.6 1.2		ns ns
			Preliminary						

Dual Port RAM	Speed Grade		-09		-08		-07		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	
Address write cycle time (clock K period)	16x1	T_{WCDS}	6.7		5.9		5.3		ns
Clock K pulse width (active edge)	16x1	T_{WPDS}	3.4		3.0		2.7		ns
Address setup time before clock K	16x1	T_{ASDS}	1.5		1.3		1.2		ns
Address hold time after clock K	16x1	T_{AHDS}	0.0		0.0		0.0		ns
DIN setup time before clock K	16x1	T_{DSDS}	1.7		1.6		1.4		ns
DIN hold time after clock K	16x1	T_{DHDS}	0.0		0.0		0.0		ns
WE setup time before clock K	16x1	T_{WSDS}	1.4		1.3		1.1		ns
WE hold time after clock K	16x1	T_{WHDS}	0.0		0.0		0.0		ns
Data valid after clock K	16x1	T_{WODS}		5.7		5.1		4.6	ns

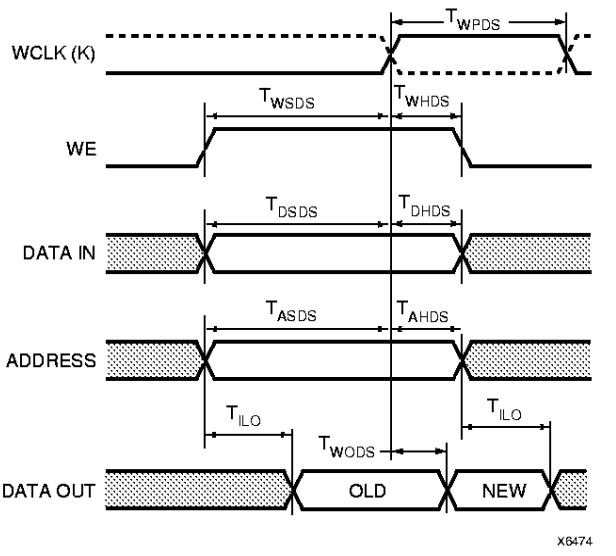
Note: Timing for 16x1 option is identical to 16x2 RAM.

Preliminary

CLB RAM Synchronous (Edge-Triggered) Write Timing



Single Port RAM



Dual Port RAM

XLA Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

Global Low Skew Clock Input to Output Delay

		Speed Grade	All	-09	-08	-07	Units
Description	Symbol	Device	Min	Max	Max	Max	
Global Low Skew (GLS) Clock Input to Output Delay using Output Flip-Flop	T_{ICKOF}	XC4013XLA	1.2	5.6	5.0	4.5	ns
		XC4020XLA	1.3	5.8	5.2	4.7	ns
		XC4028XLA	1.4	6.1	5.5	4.9	ns
		XC4036XLA	1.4	6.4	5.7	5.1	ns
		XC4044XLA	1.5	6.8	6.0	5.4	ns
		XC4052XLA	1.6	7.1	6.3	5.7	ns
		XC4062XLA	1.6	7.4	6.6	5.9	ns
		XC4085XLA	1.8	8.2	7.3	6.5	ns
For output SLOW option add	T_{SLOW}	All Devices	0.5	1.7	1.6	1.4	ns
			Preliminary				

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 7.

FastCLK Input to Output Delay for BUFNW, BUFSW, BUFNE, & BUFSE

		Speed Grade	All	-09	-08	-07	Units
Description	Symbol	Device	Min	Max	Max	Max	
FastCLK Input to Output Delay using Output Flip-Flop for FastCLK buffers BUFNW, BUFSW, BUFNE, and BUFSE.	T_{ICKFOF}	XC4013XLA	1.0	4.6	4.1	3.6	ns
		XC4020XLA	1.0	4.6	4.1	3.7	ns
		XC4028XLA	1.0	4.7	4.2	3.8	ns
		XC4036XLA	1.1	4.8	4.3	3.9	ns
		XC4044XLA	1.1	4.9	4.4	3.9	ns
		XC4052XLA	1.1	5.0	4.5	4.0	ns
		XC4062XLA	1.1	5.1	4.6	4.1	ns
		XC4085XLA	1.2	5.4	4.8	4.3	ns
			Preliminary				

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 7.

Global Early Clock Input to Output Delay for BUFGEs 1, 2, 5, and 6

		Speed Grade	All	-09	-08	-07	Units
Description	Symbol	Device	Min	Max	Max	Max	
Global Clock Signal Input to Output Delay using Global Early (GE) clock buffer to clock Output Flip-Flop for BUFGEs 1, 2, 5, & 6.	T_{ICKEOF}	XC4013XLA	0.8	4.9	4.4	3.9	ns
		XC4020XLA	0.8	5.1	4.6	4.1	ns
		XC4028XLA	0.8	5.3	4.8	4.3	ns
		XC4036XLA	0.8	5.6	5.1	4.5	ns
		XC4044XLA	0.9	5.9	5.3	4.8	ns
		XC4052XLA	0.9	6.2	5.6	5.0	ns
		XC4062XLA	0.9	6.5	5.9	5.3	ns
		XC4085XLA	0.9	6.9	6.2	5.6	ns
			Preliminary				

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 7.

Global Early Clock Input to Output Delay for BUFGEs 3, 4, 7, and 8

		Speed Grade	All	-09	-08	-07	Units
Description	Symbol	Device	Min	Max	Max	Max	
Global Clock Signal Input to Output Delay using Global Early (GE) clock buffer to clock Output Flip-Flop for BUFGEs 3, 4, 7, & 8.	T_{ICKEOF}	XC4013XLA	1.1	5.7	5.1	4.5	ns
		XC4020XLA	1.1	5.9	5.3	4.7	ns
		XC4028XLA	1.2	6.1	5.4	4.9	ns
		XC4036XLA	1.3	6.3	5.6	5.0	ns
		XC4044XLA	1.3	6.5	5.8	5.2	ns
		XC4052XLA	1.4	6.8	6.0	5.4	ns
		XC4062XLA	1.5	7.0	6.3	5.6	ns
		XC4085XLA	1.6	7.5	6.7	6.0	ns
			Preliminary				

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 7.

Capacitive Load Factor

Figure 7 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay.

Figure 7 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

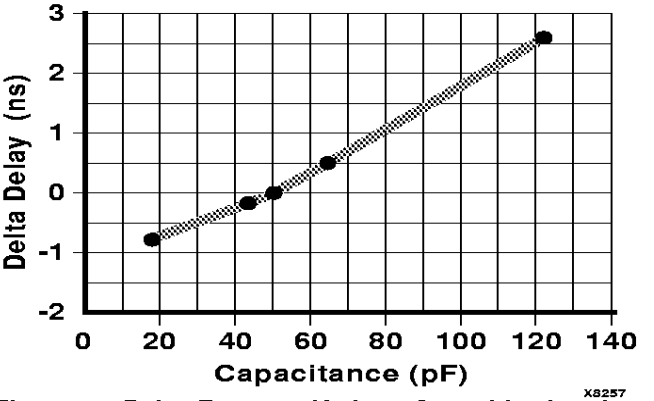


Figure 7: Delay Factor at Various Capacitive Loads

XLA Pin-to-Pin Set-up and Hold Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values are expressed in nanoseconds unless otherwise noted.

Global Low Skew Clock Set-Up and Hold

		Speed Grade	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Input Setup and Hold Time Relative to Global Clock Input Signal						
No Delay		XC4013XLA	1.0 / 3.0	0.8 / 2.6	0.2 / 2.5	ns
Global Low Skew Clock and IFF	T_{PSN}/T_{PHN}	XC4020XLA	0.9 / 3.2	0.7 / 2.9	0.1 / 2.7	ns
		XC4028XLA	0.8 / 3.8	0.6 / 3.3	0.0 / 3.0	ns
		XC4036XLA	0.6 / 4.0	0.4 / 3.5	0.0 / 3.3	ns
		XC4044XLA	0.4 / 4.4	0.2 / 3.9	0.0 / 3.6	ns
		XC4052XLA	0.3 / 4.6	0.2 / 4.1	0.0 / 3.9	ns
		XC4062XLA	0.2 / 5.0	0.1 / 4.5	0.0 / 4.2	ns
		XC4085XLA	0.0 / 5.4	0.0 / 4.8	0.0 / 4.5	ns
Partial Delay		XC4013XLA	4.4 / 0.5	4.1 / 0.3	3.7 / 0.0	ns
Global Low Skew Clock and IFF	T_{PSP}/T_{PHP}	XC4020XLA	4.5 / 0.6	4.1 / 0.3	3.7 / 0.0	ns
		XC4028XLA	4.6 / 0.7	4.2 / 0.4	3.7 / 0.0	ns
		XC4036XLA	4.6 / 0.8	4.2 / 0.4	3.7 / 0.0	ns
		XC4044XLA	4.7 / 0.9	4.3 / 0.5	3.8 / 0.0	ns
		XC4052XLA	4.8 / 1.0	4.3 / 0.6	3.8 / 0.2	ns
		XC4062XLA	5.0 / 1.0	4.4 / 0.7	3.8 / 0.4	ns
		XC4085XLA	5.5 / 1.2	4.7 / 0.9	3.8 / 0.6	ns
Full Delay		XC4013XLA	4.4 / 0.0	4.1 / 0.0	3.7 / 0.0	ns
Global Low Skew Clock and IFF	T_{PSD}/T_{PHD}	XC4020XLA	4.6 / 0.0	4.2 / 0.0	3.8 / 0.0	ns
		XC4028XLA	4.8 / 0.0	4.4 / 0.0	3.9 / 0.0	ns
		XC4036XLA	4.9 / 0.0	4.5 / 0.0	4.0 / 0.0	ns
		XC4044XLA	5.0 / 0.0	4.6 / 0.0	4.1 / 0.0	ns
		XC4052XLA	5.2 / 0.0	4.7 / 0.0	4.2 / 0.0	ns
		XC4062XLA	5.5 / 0.0	4.9 / 0.0	4.3 / 0.0	ns
		XC4085XLA	6.0 / 0.0	5.2 / 0.0	4.4 / 0.0	ns

IFF = Input Flip-Flop or Latch

Preliminary

Note: Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer (TRCE) to determine the setup and hold times under given design conditions.

FastCLK Input Set-Up and Hold for BUFNW, BUFSW, BUFNE, & BUFSE

Description	Symbol	Speed Grade / Device	-09 Min	-08 Min	-07 Min	Units
Input Setup and Hold Time Relative to FastCLK Input Signal						
No Delay		XC4013XLA	0.0 / 3.2	0.0 / 2.9	0.0 / 2.6	ns
FastCLK and IFF	T_{PSFN}/T_{PHFN}	XC4020XLA	0.0 / 3.3	0.0 / 3.0	0.0 / 2.7	ns
		XC4028XLA	0.0 / 3.4	0.0 / 3.1	0.0 / 2.8	ns
		XC4036XLA	0.0 / 3.5	0.0 / 3.2	0.0 / 2.9	ns
		XC4044XLA	0.0 / 3.6	0.0 / 3.3	0.0 / 3.0	ns
		XC4052XLA	0.0 / 3.7	0.0 / 3.4	0.0 / 3.1	ns
		XC4062XLA	0.0 / 3.8	0.0 / 3.5	0.0 / 3.2	ns
		XC4085XLA	0.0 / 3.9	0.0 / 3.6	0.0 / 3.3	ns
Partial Delay		XC4013XLA	3.5 / 0.6	3.2 / 0.3	2.9 / 0.0	ns
FastCLK and IFF	$T_{PSFP}T_{PHFP}$	XC4020XLA	3.7 / 0.4	3.4 / 0.2	3.1 / 0.0	ns
		XC4028XLA	3.9 / 0.2	3.6 / 0.1	3.3 / 0.0	ns
		XC4036XLA	4.1 / 0.0	3.8 / 0.0	3.5 / 0.0	ns
		XC4044XLA	4.3 / 0.0	4.0 / 0.0	3.7 / 0.0	ns
		XC4052XLA	4.5 / 0.0	4.2 / 0.0	3.9 / 0.0	ns
		XC4062XLA	4.7 / 0.0	4.4 / 0.0	4.1 / 0.0	ns
		XC4085XLA	5.1 / 0.0	4.8 / 0.0	4.5 / 0.0	ns
Full Delay		XC4013XLA	3.5 / 0.6	3.2 / 0.3	2.9 / 0.0	ns
FastCLK and IFF	T_{PSFD}/T_{PHFD}	XC4020XLA	3.8 / 0.4	3.5 / 0.2	3.2 / 0.0	ns
		XC4028XLA	4.0 / 0.2	3.7 / 0.1	3.4 / 0.0	ns
		XC4036XLA	4.3 / 0.0	4.0 / 0.0	3.7 / 0.0	ns
		XC4044XLA	4.6 / 0.0	4.3 / 0.0	4.0 / 0.0	ns
		XC4052XLA	4.9 / 0.0	4.6 / 0.0	4.3 / 0.0	ns
		XC4062XLA	5.3 / 0.0	5.0 / 0.0	4.7 / 0.0	ns
		XC4085XLA	6.1 / 0.0	5.8 / 0.0	5.5 / 0.0	ns

Preliminary

IFF = Input Flip-Flop

Note: Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer(TRCE) to determine the setup and hold times under given design conditions.

Global Early Clock Set-up and Hold, BUFGEs 1, 2, 5, and 6 for IFF and FCL

Description	Symbol	Speed Grade / Device	-09 Min	-08 Min	-07 Min	Units
Input Setup and Hold Time Relative to Global Clock Input Signal						
No Delay		XC4013XLA	1.0 / 3.2	0.8 / 2.6	0.5 / 1.8	ns
Global Early Clock and IFF	T_{PSEN}/T_{PHEN}	XC4020XLA	1.0 / 3.4	0.8 / 2.8	0.5 / 2.0	ns
Global Early Clock and FCL	T_{PFSEN}/T_{PFHEN}	XC4028XLA	1.0 / 3.5	0.8 / 3.0	0.5 / 2.2	ns
		XC4036XLA	1.0 / 3.6	0.8 / 3.1	0.5 / 2.4	ns
		XC4044XLA	1.0 / 3.8	0.8 / 3.3	0.5 / 2.6	ns
		XC4052XLA	1.0 / 4.0	0.8 / 3.5	0.5 / 2.8	ns
		XC4062XLA	1.0 / 4.2	0.8 / 3.7	0.5 / 3.0	ns
		XC4085XLA	1.0 / 4.6	0.8 / 4.0	0.5 / 3.2	ns
Partial Delay		XC4013XLA	4.6 / 0.0	4.2 / 0.0	3.9 / 0.0	ns
Global Early Clock and IFF	T_{PSEP}/T_{PHEP}	XC4020XLA	4.8 / 0.1	4.4 / 0.1	4.1 / 0.0	ns
Global Early Clock and FCL	T_{PFSEP}/T_{PFHEP}	XC4028XLA	4.9 / 0.1	4.6 / 0.1	4.4 / 0.0	ns
		XC4036XLA	5.0 / 0.2	4.7 / 0.1	4.5 / 0.0	ns
		XC4044XLA	5.5 / 0.3	5.1 / 0.2	4.8 / 0.0	ns
		XC4052XLA	5.8 / 0.3	5.3 / 0.2	5.0 / 0.0	ns
		XC4062XLA	6.2 / 0.4	5.6 / 0.2	5.2 / 0.0	ns
		XC4085XLA	6.5 / 0.5	5.9 / 0.3	5.4 / 0.0	ns
Full Delay		XC4013XLA	4.6 / 0.0	4.2 / 0.0	3.9 / 0.0	ns
Global Early Clock and IFF	T_{PSED}/T_{PHED}	XC4020XLA	4.9 / 0.0	4.5 / 0.0	4.1 / 0.0	ns
		XC4028XLA	5.1 / 0.0	4.7 / 0.0	4.4 / 0.0	ns
		XC4036XLA	5.3 / 0.0	4.9 / 0.0	4.5 / 0.0	ns
		XC4044XLA	5.8 / 0.0	5.3 / 0.0	5.0 / 0.0	ns
		XC4052XLA	6.2 / 0.0	5.7 / 0.0	5.3 / 0.0	ns
		XC4062XLA	6.7 / 0.0	6.1 / 0.0	5.6 / 0.0	ns
		XC4085XLA	7.0 / 0.0	6.4 / 0.0	6.0 / 0.0	ns

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Preliminary

Note: Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer (TRCE) to determine the setup and hold times under given design conditions.

Global Early Clock Set-up and Hold, BUFGEs 3, 4, 7, and 8 for IFF and FCL

		Speed Grade	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Input Setup and Hold Time Relative to Global Clock Input Signal						
No Delay		XC4013XLA	0.8 / 3.2	0.6 / 2.6	0.0 / 2.1	ns
Global Early Clock and IFF	T_{PSEN}/T_{PHEN}	XC4020XLA	0.8 / 3.4	0.6 / 2.8	0.0 / 2.3	ns
Global Early Clock and FCL	T_{PFSEN}/T_{PFHEN}	XC4028XLA	0.8 / 3.5	0.6 / 3.0	0.0 / 2.5	ns
		XC4036XLA	0.8 / 3.6	0.6 / 3.1	0.0 / 2.7	ns
		XC4044XLA	0.8 / 3.8	0.6 / 3.3	0.0 / 2.9	ns
		XC4052XLA	0.8 / 4.0	0.6 / 3.5	0.0 / 3.1	ns
		XC4062XLA	0.8 / 4.2	0.6 / 3.7	0.0 / 3.3	ns
		XC4085XLA	0.8 / 4.6	0.6 / 4.0	0.0 / 3.5	ns
Partial Delay		XC4013XLA	4.4 / 0.0	4.0 / 0.0	3.6 / 0.0	ns
Global Early Clock and IFF	T_{PSEP}/T_{PHEP}	XC4020XLA	4.6 / 0.1	4.2 / 0.1	3.8 / 0.0	ns
Global Early Clock and FCL	T_{PFSEP}/T_{PFHEP}	XC4028XLA	4.7 / 0.1	4.4 / 0.1	4.1 / 0.0	ns
		XC4036XLA	4.8 / 0.2	4.5 / 0.2	4.2 / 0.0	ns
		XC4044XLA	5.2 / 0.3	4.8 / 0.3	4.4 / 0.0	ns
		XC4052XLA	5.6 / 0.3	5.1 / 0.3	4.6 / 0.0	ns
		XC4062XLA	6.0 / 0.4	5.4 / 0.4	4.8 / 0.0	ns
		XC4085XLA	6.3 / 0.5	5.7 / 0.5	5.0 / 0.0	ns
Full Delay		XC4013XLA	4.4 / 0.0	4.0 / 0.0	3.6 / 0.0	ns
Global Early Clock and IFF	T_{PSED}/T_{PHED}	XC4020XLA	4.7 / 0.0	4.3 / 0.0	3.8 / 0.0	ns
		XC4028XLA	4.9 / 0.0	4.5 / 0.0	4.1 / 0.0	ns
		XC4036XLA	5.1 / 0.0	4.7 / 0.0	4.2 / 0.0	ns
		XC4044XLA	5.6 / 0.0	5.1 / 0.0	4.6 / 0.0	ns
		XC4052XLA	6.0 / 0.0	5.5 / 0.0	4.9 / 0.0	ns
		XC4062XLA	6.5 / 0.0	5.9 / 0.0	5.2 / 0.0	ns
		XC4085XLA	6.8 / 0.0	6.2 / 0.0	5.6 / 0.0	ns

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Preliminary

Note: Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer (TRCE) to determine the setup and hold times under given design conditions.

XLA IOB Switching Characteristics

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

IOB Input Delay Guidelines

		Speed Grade	-09		-08		-07		Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Clocks									
Clock Enable (EC) to Clock (IK)	T_{ECIK}	All devices	0.0		0.0		0.0		ns
Delay from FCL enable (OK) active edge to IFF clock (IK) active edge	T_{OKIK}	All Devices	1.4		1.3		1.2		ns
Setup Times									
Pad to Clock (IK), no delay	T_{PICK}	All Devices	1.2		1.0		0.9		ns
Pad to Clock (IK), via transparent Fast Capture Latch, no delay	T_{PICKF}	All Devices	1.6		1.4		1.3		ns
Pad to Fast Capture Latch Enable (OK), no delay	T_{POCK}	All Devices	0.8		0.7		0.6		ns
Hold Times									
All Hold Times		All Devices	0.0		0.0		0.0		ns
Global Set/Reset									
Minimum GSR Pulse Width	T_{MRW}	All devices	12.8		11.4		10.2		ns
Global Set/Reset									
Delay from GSR input to any Q	T_{RRI}*	XC4013XLA		11.4		10.2		9.1	ns
		XC4020XLA		13.3		11.9		10.6	ns
		XC4028XLA		14.3		12.8		11.4	ns
		XC4036XLA		16.2		14.5		12.9	ns
		XC4044XLA		18.1		16.2		14.4	ns
		XC4052XLA		19.5		17.4		15.6	ns
		XC4062XLA		20.9		18.7		16.7	ns
		XC4085XLA		24.7		22.1		19.7	ns
Propagation Delays									
Pad to I1, I2	T_{PID}	All devices		1.0		0.9		0.8	ns
Pad to I1, I2 via transparent input latch, no delay	T_{PLI}	All devices		2.1		1.9		1.7	ns
Pad to I1, I2 via transparent FCL and input latch, no delay	T_{PFLI}	All devices		2.5		2.2		2.0	ns
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}	All devices		1.1		1.0		0.9	ns
Clock (IK) to I1, I2 (latch enable, active Low)	T_{IKLI}	All devices		1.2		1.1		1.0	ns
FCL Enable (OK) active edge to I1, I2 (via transparent standard input latch)	T_{OKLI}	All devices		2.4		2.1		1.9	ns

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Preliminary

* Indicates Minimum Amount of Time to Assure Valid Data.

IOB Output Delay Guidelines

Description	Symbol	Device	-09		-08		-07		Units
			Min	Max	Min	Max	Min	Max	
Clocks									
Clock High	T_{CH}	All devices	2.2		1.9		1.7		ns
Clock Low	T_{CL}	All devices	2.2		1.9		1.7		ns
Propagation Delays									
Clock (OK) to Pad	T_{OKPOF}	All devices		3.2		2.9		2.6	ns
Output (O) to Pad	T_{OPF}	All devices		2.6		2.4		2.1	ns
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZ}	All devices		2.7		2.4		2.2	ns
3-state to Pad active and valid	T_{TSONF}	All devices		2.8		2.5		2.3	ns
Output (O) to Pad via Fast Output MUX	T_{OFPF}	All devices		3.6		3.2		2.9	ns
Select (OK) to Pad via Fast MUX	T_{OKFPF}	All devices		3.3		3.0		2.6	ns
Setup and Hold Times									
Output (O) to clock (OK) setup time	T_{OOK}	All devices	0.3		0.3		0.3		ns
Output (O) to clock (OK) hold time	T_{OKO}	All devices	0.0		0.0		0.0		ns
Clock Enable (EC) to clock (OK) setup time	T_{ECOK}	All devices	0.0		0.0		0.0		ns
Clock Enable (EC) to clock (OK) hold time	T_{OKEC}	All devices	0.0		0.0		0.0		ns
Global Set/Reset									
Minimum GSR pulse width	T_{MRW}		12.8		11.4		10.2		ns
Delay from GSR input to any Pad	T_{RPO*}	XC4013XLA		14.4		12.8		11.5	
		XC4020XLA		16.3		14.5		13.0	
		XC4028XLA		17.3		15.4		13.8	
		XC4036XLA		19.1		17.1		15.3	
		XC4044XLA		21.0		18.8		16.8	
		XC4052XLA		22.5		20.1		17.9	
		XC4062XLA		23.9		21.3		19.0	
		XC4085XLA		27.7		24.7		22.1	
Slew Rate Adjustment									
For output SLOW option add	T_{SLOW}			1.7		1.6		1.4	ns

* Indicates Minimum Amount of Time to Assure Valid Data

Preliminary

XV Specification Information

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

All specifications subject to change without notice.

Additional Speci

fications

Except for pin-to-pin input and output parameters, the a.c. parameter delay specifications included in this document are derived from measuring internal test patterns.All specifications are representative of worst- case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

XV DC Characteristic Guidelines

Absolute Maximum Ratings

Symbol	Description		Value	Units
V_{CCINT}	Supply voltage relative to GND		-0.5 to 3.0	V
V_{CCIO}	Supply voltage relative to GND		-0.5 to 4.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to 5.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to 5.5	V
V_{CC}	Longest Supply Voltage Rise Time from 1 V to 3V		50	ms
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Notes: Maximum DC overshoot or undershoot above V_{cc} or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to + 7.0 V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CCINT}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	2.3	2.7	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	2.3	2.7	V
V_{CCIO}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	3.0	3.6	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	3.0	3.6	V
V_{IH}	High-level input voltage		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage		0	30% of V_{CC}	V
T_{IN}	Input signal transition time			250	ns

Notes: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
Input and output measurement threshold is ~50% of V_{CC}.

DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0 mA, V_{CC} min (LVTTL)		2.4		V
	High-level output voltage @ I_{OH} = -500 µA, (LVCMOS)		90% V_{CC}		V
V_{OL}	Low-level output voltage @ I_{OL} = 24.0 mA, V_{CC} min (LVTTL) (Note 1)			0.4	V
	Low-level output voltage @ I_{OL} = 1500 µA, (LVCMOS)			10% V_{CC}	V
V_{DRINT}	V_{CCINT} Data Retention Supply Voltage (below which configuration data may be lost)		2.1		V
V_{DRIO}	V_{CCIO} Data Retention Supply Voltage (below which configuration data may be lost)		2.5		V
I_{CCO}	Quiescent FPGA supply current (Note 2)			10	mA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, SBGA, PQ, HQ, & MQ packages		10	pF
		PGA packages		16	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)		0.02	0.15	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.3	2.0	mA

Note 1: With up to 64 pins simultaneously sinking 24 mA.
Note 2: With no output current loads, no active input or Longline pull-up resistors, all I/O pins Tri-stated and floating.

XV AC Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Delay Via Clock Buffers to Clock

		Speed Grade	All	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Max**	**Max**	
Delay from pad through Global Low Skew (GLS) clock buffer to any clock input, K.	T_{GLS}	XC40110XV		7.2	6.3	5.4	ns
		XC40150XV		**7.3**	6.4	5.5	ns
		XC40200XV		8.8	7.7	6.6	ns
		XC40250XV		8.9	7.8	6.7	ns
Delay from pad through FastCLK buffer to any IOB clock input	T_{FCLK}	XC40110XV		2.5	2.2	1.8	ns
		XC40150XV		**2.6**	2.3	1.9	ns
		XC40200XV		2.9	2.6	2.2	ns
		XC40250XV		3.0	2.7	2.3	ns
Delay from pad through Global Early (GE) clock buffer to any IOB clock input for BUFGEs 1, 2, 5, and 6.	T_{GE_1256}	XC40110XV		5.1	4.5	3.8	ns
		XC40150XV		**5.2**	4.6	3.9	ns
		XC40200XV		5.6	4.9	4.2	ns
		XC40250XV		5.7	5.0	4.3	ns
Delay from pad through Global Early (GE) clock buffer to any IOB clock input for BUFGEs 3, 4, 7, and 8.	T_{GE_3478}	XC40110XV		5.1	4.5	3.8	ns
		XC40150XV		**5.2**	4.6	3.9	ns
		XC40200XV		5.6	4.9	4.2	ns
		XC40250XV		5.7	5.0	4.3	ns

Bold Face: Prelminary Values for the XC40150-09. All other values are Advance.

Advance

6

CLB Switching Characteristic Guidelines

Description	Symbol	Speed Grade -09 Min	-09 Max	-08 Min	-08 Max	-07 Min	-07 Max	Units
Combinatorial Delays								
F/G inputs to X/Y outputs	T_{ILO}		1.3		1.1		1.0	ns
F/G inputs via H' to X/Y outputs	T_{IHO}		2.0		1.7		1.5	ns
F/G inputs via transparent latch to Q outputs	T_{ITO}		2.1		1.8		1.6	ns
C inputs via SR/H0 via H to X/Y outputs	T_{HH0O}		1.9		1.6		1.4	ns
C inputs via H1 via H to X/Y outputs	T_{HH1O}		1.7		1.5		1.3	ns
C inputs via DIN/H2 via H to X/Y outputs	T_{HH2O}		1.9		1.6		1.4	ns
C inputs via EC, DIN/H2 to YQ, XQ output (bypass0	T_{CBYP}		1.2		1.0		0.9	ns
CLB Fast Carry Logic								
Operand inputs (F1, F2, G1, G4) to C_{OUT}	T_{OPCY}		2.2		1.9		1.7	ns
Add/Subtract input (F3) to C_{OUT}	T_{ASCY}		1.3		1.1		1.0	ns
Initialization inputs (F1, F3) to C_{OUT}	T_{INCY}		1.4		1.2		1.0	ns
C_{IN} through function generators to X/Y outputs	T_{SUM}		1.8		1.6		1.4	ns
C_{IN} to C_{OUT}, bypass function generators	T_{BYP}		0.3		0.2		0.2	ns
Carry Net Delay, C_{OUT} to C_{IN}	T_{NET}		0.4		0.3		0.3	ns
Sequential Delays								
Clock K to Flip-Flop outputs Q	T_{CKO}		1.6		1.4		1.2	ns
Clock K to Latch outputs Q	T_{CKLO}		1.6		1.4		1.2	ns
Setup Time before Clock K								
F/G inputs	T_{ICK}	0.8		0.7		0.6		ns
F/G inputs via H	T_{IHCK}	1.5		1.3		1.1		ns
C inputs via H0 through H	T_{HH0CK}	1.4		1.2		1.0		ns
C inputs via H1 through H	T_{HH1CK}	1.2		1.1		0.9		ns
C inputs via H2 through H	T_{HH2CK}	1.4		1.2		1.0		ns
C inputs via DIN	T_{DICK}	0.6		0.6		0.5		ns
C inputs via EC	T_{ECCK}	0.7		0.6		0.5		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	0.6		0.5		0.4		ns
CIN input via F/G	T_{CCK}	1.3		1.1		1.0		ns
CIN input via F/G and H	T_{CHCK}	2.0		1.7		1.5		ns
Hold Time after Clock K								
All Hold Times		0.0		0.0		0.0		ns
Clocks								
Clock High time	T_{CH}	2.3		2.0		1.7		ns
Clock Low time	T_{CL}	2.3		2.0		1.7		ns
Set/Reset Direct								
Width (High)	T_{RPW}	3.0		2.8		2.5		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		2.6		2.3		2.0	ns
Global Set/Reset								
Minimum GSR Pulse Width	T_{MRW}		13.4		11.7		10.2	ns
Delay from GSR input to any Q	T_{MRQ}	See page 39 for TRRI values per device						
Toggle Frequency (MHz) (for export control purposes)	F_{TOG}		225		258		296	MHz
		Advance						

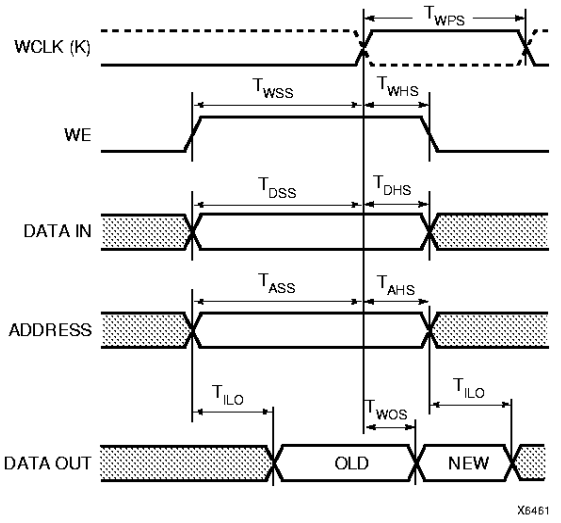
CLB RAM Synchronous (Edge-Triggered) Read/Write Operation Guidelines

Single Port RAM	Speed Grade		-09		-08		-07		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	
Write Operation									
Address write cycle time (clock K period)	16x2	T_{WCS}	7.0		6.1		5.3		ns
	32x1	T_{WCTS}	7.0		6.1		5.3		ns
Clock K pulse width (active edge)	16x2	T_{WPS}	3.5		3.1		2.7		ns
	32x1	T_{WPTS}	3.5		3.1		2.7		ns
Address setup time before clock K	16x2	T_{ASS}	1.5		1.3		1.2		ns
	32x1	T_{ASTS}	1.6		1.4		1.2		ns
Address hold time after clock K	16x2	T_{AHS}	0.0		0.0		0.0		ns
	32x1	T_{AHTS}	0.0		0.0		0.0		ns
DIN setup time before clock K	16x2	T_{DSS}	1.6		1.4		1.2		ns
	32x1	T_{DSTS}	2.0		1.7		1.5		ns
DIN hold time after clock K	16x2	T_{DHS}	0.0		0.0		0.0		ns
	32x1	T_{DHTS}	0.0		0.0		0.0		ns
WE setup time before clock K	16x2	T_{WSS}	1.5		1.3		1.2		ns
	32x1	T_{WSTS}	1.4		1.3		1.1		ns
WE hold time after clock K	16x2	T_{WHS}	0.0		0.0		0.0		ns
	32x1	T_{WHTS}	0.0		0.0		0.0		ns
Data valid after clock K	16x2	T_{WOS}		5.2		4.6		4.0	ns
	32x1	T_{WOTS}		6.2		5.4		4.7	ns
Read Operation									
Address read cycle time	16x2	T_{RC}	4.5		3.1		3.1		ns
	32x1	T_{RCT}	6.5		5.5		5.5		ns
Data Valid after address change (no Write Enable)	16x2	T_{ILO}		1.3		1.1		1.0	ns
	32x1	T_{IHO}		2.0		1.7		1.5	ns
Address setup time before clock K	16x2	T_{ICK}	0.8		0.7		0.6		ns
	32x1	T_{IHCK}	1.5		1.3		1.1		ns
			Advance						

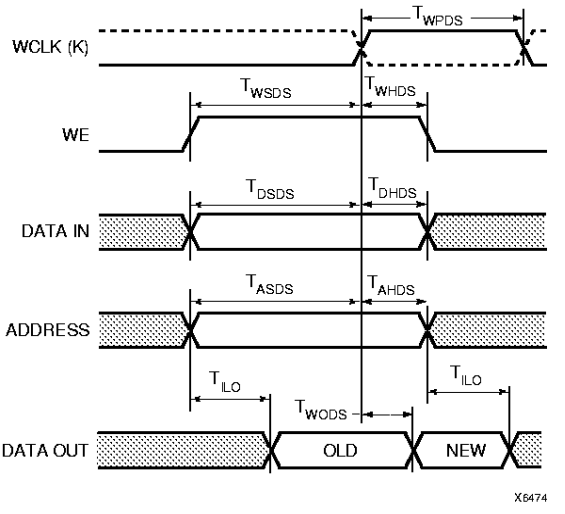
Dual Port RAM	Speed Grade		-09		-08		-07		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	
Address write cycle time (clock K period)	16x1	T_{WCDS}	7.0		6.1		5.3		ns
Clock K pulse width (active edge)	16x1	T_{WPDS}	3.5		3.1		2.7		ns
Address setup time before clock K	16x1	T_{ASDS}	1.5		1.3		1.2		ns
Address hold time after clock K	16x1	T_{AHDS}	0.0		0.0		0.0		ns
DIN setup time before clock K	16x1	T_{DSDS}	1.9		1.7		1.4		ns
DIN hold time after clock K	16x1	T_{DHDS}	0.0		0.0		0.0		ns
WE setup time before clock K	16x1	T_{WSDS}	1.5		1.3		1.2		ns
WE hold time after clock K	16x1	T_{WHDS}	0.0		0.0		0.0		ns
Data valid after clock K	16x1	T_{WODS}		6.0		5.3		4.6	ns
			Advance						

Note: Timing for 16x1 option is identical to 16x2 RAM.

CLB RAM Synchronous (Edge-Triggered) Write Timing



Single Port RAM



Dual Port RAM

XV Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

Global Low Skew Clock Input to Output Delay

		Speed Grade	All	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Max**	**Max**	
From pad through Global Low Skew buffer, to any clock K	T_{ICKOF}	XC40110XV		10.6	9.2	8.0	ns
		XC40150XV		**10.7**	9.3	8.1	ns
		XC40200XV		12.2	10.6	9.2	ns
		XC40250XV		12.3	10.7	9.3	ns
For output SLOW option add	T_{SLOW}	All Devices		2.3	2.0	1.7	ns
				Advance			

Bold Face: Prelminary Values for the XC40150-09. All other values are Advance.

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with fewer number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs in FAST mode specification.

Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 8.

FastCLK Input to Output Delay for BUFNW, BUFSW, BUFNE, and BUFSE

		Speed Grade	All	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Max**	**Max**	
FastCLK to Output using OFF for BUFNW, SW, NE, and SE	T_{ICKFOF}	XC40110XV		5.9	5.1	4.4	ns
		XC40150XV		**6.0**	5.2	4.5	ns
		XC40200XV		6.3	5.5	4.8	ns
		XC40250XV		6.4	5.6	4.9	ns
				Advance			

OFF = Output Flip Flop

Bold Face: Prelminary Values for the XC40150-09. All other values are Advance.

Notes: Listed above are representative values where one FastCLK input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the FastCLK net.

Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with fewer number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs in FAST slew mode specification.

Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 8.

Global Early Clock Input to Output Delay for BUFGEs 1, 2, 5, 6

		Speed Grade	All	-09	-08	-07	Units
Description	Symbol	Device	Min	Max	Max	Max	
Global Early Clock to Output via OFF for BUFGEs 1, 2, 5, 6	T_{ICKEOF_1256}	XC40110XV		8.5	7.4	6.4	ns
		XC40150XV		**8.6**	7.5	6.5	ns
		XC40200XV		9.0	7.8	6.8	ns
		XC40250XV		9.1	7.9	6.9	ns
OFF = Output Flip Flop			**Advance**				

Bold Face: Prelminary Values for the XC40150-09. All other values are Advance.

Notes: Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with fewer number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs in FAST mode specification.

Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 8.

Global Early Clock Input to Output Delay for BUFGEs 3, 4, 7, 8

		Speed Grade	All	-09	-08	-07	Units
Description	Symbol	Device	Min	Max	Max	Max	
Global Early Clock to Output via OFF for BUFGEs 3, 4, 7, 8	T_{ICKEOF_3478}	XC40110XV		8.5	7.4	6.4	ns
		XC40150XV		**8.6**	7.5	6.5	ns
		XC40200XV		9.0	7.8	6.8	ns
		XC40250XV		9.1	7.9	6.9	ns
OFF = Output Flip Flop			**Advance**				

Bold Face: Prelminary Values for the XC40150-09. All other values are Advance.

Notes: Clock-to-out minimum delay is measured with the fastest route and the lightest load, Clock-to-out maximum delay is measured using the farthest distance and a reference load of one clock pin (IK or OK) per IOB as well as driving all accessible CLB flip-flops. For designs with fewer number of clock loads, the pad-to-IOB clock pin delay as determined by the static timing analyzer (TRCE) can be added to the AC parameter Tokpof and used as a worst-case pin-to-pin clock-to-out delay for clocked outputs in FAST mode specification.

Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 8.

Capacitive Load Factor

Figure 8 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay.

Figure 8 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

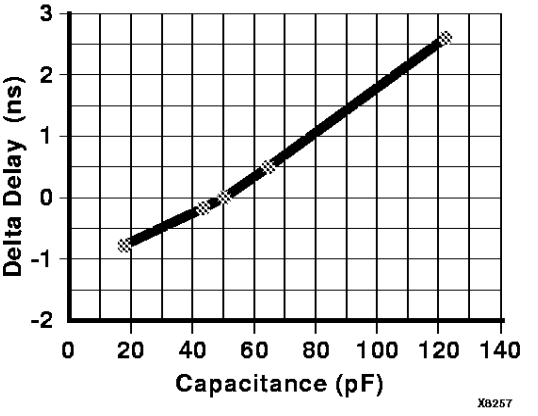


Figure 8: Delay Factor at Various Capacitive Loads

XV Set-up and Hold Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

Global Low Skew Clock Set-Up and Hold

		Speed Grade	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Input Setup and Hold Time Relative to Global Clock Input Signal						
No Delay		XC40110XV	0.0 / 6.8	0.0 / 5.9	0.0 / 5.1	ns
Global Low Skew Clock and IFF	T_{PSN}/T_{PHN}	XC40150XV	**0.0 / 7.5**	0.0 / 6.6	0.0 / 5.7	ns
Global Low Skew Clock and FCL		XC40200XV	0.0 / 8.8	0.0 / 6.7	0.0 / 6.7	ns
		XC40250XV	0.0 / 9.8	0.0 / 8.5	0.0 / 7.4	ns
Partial Delay		XC40110XV	5.5 / 0.5	4.8 / 0.5	4.1 / 0.4	ns
Global Low Skew Clock and IFF	T_{PSP}/T_{PHP}	XC40150XV	**6.1 / 0.5**	5.3 / 0.5	4.6 / 0.4	ns
Global Low Skew Clock and FCL		XC40200XV	7.9 / 0.3	6.8 / 0.2	5.9 / 0.2	ns
		XC40250XV	8.7 / 0.0	7.6 / 0.0	6.6 / 0.0	ns
Full Delay		XC40110XV	8.0 / 0.0	6.9 / 0.0	6.0 / 0.0	ns
Global Low Skew Clock and IFF	T_{PSD}/T_{PHD}	XC40150XV	**8.9 / 0.0**	7.7 / 0.0	6.7 / 0.0	ns
		XC40200XV	9.4 / 0.0	8.2 / 0.0	7.1 / 0.0	ns
		XC40250XV	9.7 / 0.0	8.4 / 0.0	7.3 / 0.0	ns
				Advance		

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Bold Face: Prelminary Values for the XC40150-09. All other values are Advance.

Notes: Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer (TRCE) to determine the setup and hold times under given design conditions.

FastCLK Input Set-Up and Hold for BUFNW, SW, NE, and SE

		Speed Grade	-09	-08	-07	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
No Delay		XC40110XV	0.8 / 4.2	0.7 / 3.7	0.6 / 3.2	ns
FastCLK and IFF	T_{PSFN}/T_{PHFN}	XC40150XV	**0.8 / 4.6**	0.7 / 4.0	0.6 / 3.5	ns
		XC40200XV	0.8 / 4.9	0.7 / 4.3	0.6 / 3.7	ns
		XC40250XV	0.8 / 5.3	0.7 / 4.6	0.6 / 4.0	ns
Partial Delay		XC40110XV	11.0 / 0.0	9.5 / 0.0	8.3 / 0.0	ns
FastCLK and IFF	T_{PSFP}/T_{PHFP}	XC40150XV	**11.1 / 0.0**	9.7 / 0.0	8.4 / 0.0	ns
		XC40200XV	11.4 / 0.0	9.9 / 0.0	8.6 / 0.0	ns
		XC40250XV	11.6 / 0.0	10.1 / 0.0	8.8 / 0.0	ns
Full Delay		XC40110XV	11.7 / 0.0	10.5 / 0.0	9.1 / 0.0	ns
FastCLK and IFF	T_{PSFD}/T_{PHFD}	XC40150XV	**11.8 / 0.0**	10.6 / 0.0	9.2 / 0.0	ns
		XC40200XV	12.4 / 0.0	10.8 / 0.0	9.4 / 0.0	ns
		XC40250XV	12.7 / 0.0	11.0 / 0.0	9.6 / 0.0	ns
				Advance		

IFF = Input Flip-Flop or Latch

Bold Face: Prelminary Values for the XC40150-09. All other values are Advance

Notes: Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer(TRCE) to determine the setup and hold times under given design conditions.

Global Early Clock Set-Up and Hold, BUFGEs 1, 2, 5, 6 for IFF and FCL

Description	Symbol	Speed Grade / Device	-09 Min	-08 Min	-07 Min	Units
Input Setup and Hold Time Relative to Global Clock Input Signal						
No Delay		XC40110XV	0.5 / 6.1	0.4 / 5.3	0.4 / 4.6	ns
Global Early Clock and IFF	T_{PSEN}/T_{PHEN}	**XC40150XV**	**0.6 / 6.2**	0.5 / 5.4	0.4 / 4.7	ns
Global Early Clock and FCL	T_{PFSEN}/T_{PFHEN}	XC40200XV	1.3 / 7.3	1.2 / 6.3	1.0 / 5.5	ns
		XC40250XV	1.5 / 7.5	1.3 / 6.6	1.1 / 5.7	ns
Partial Delay		XC40110XV	7.3 / 0.0	6.3 / 0.0	5.5 / 0.0	ns
Global Early Clock andIFF	T_{PSEP}/T_{PHEP}	XC40150XV	**8.1 / 0.0**	7.0 / 0.0	6.1 / 0.0	ns
Global Early Clock and FCL	T_{PFSEP}/T_{PFHEP}	XC40200XV	10.8 / 0.0	9.4 / 0.0	8.2 / 0.0	ns
		XC40250XV	12.0 / 0.0	10.5 / 0.0	9.1 / 0.0	ns
FullDelay		XC40110XV	10.6 / 0.0	9.2 / 0.0	8.0 / 0.0	ns
Global Early Clock and IFF	T_{PSED}/T_{PHED}	XC40150XV	**10.7 / 0.0**	9.3 / 0.0	8.1 / 0.0	ns
		XC40200XV	11.9 / 0.0	10.4 / 0.0	9.0 / 0.0	ns
		XC40250XV	13.1 / 0.0	11.4 / 0.0	9.9 / 0.0	ns
				Advance		

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Bold Face: Prelminary Values for the XC40150-09. All other values are Advance.

Notes: Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer(TRCE) to determine the setup and hold times under given design conditions.

Global Early Clock Set-Up and Hold, BUFGEs 3, 4, 7, 8 for IFF and FCL

Description	Symbol	Speed Grade / Device	-09 Min	-08 Min	-07 Min	Units
Input Setup and Hold Time Relative to Global Clock Input Signal						
No Delay		XC40110XV	0.4 / 5.2	0.3 / 4.5	0.3 / 3.9	ns
Global Early Clock and IFF	T_{PSEN}/T_{PHEN}	XC40150XV	**0.4 / 5.3**	0.4 / 4.6	0.3 / 4.0	ns
Global Early Clock and FCL	T_{PFSEN}/T_{PFHEN}	XC40200XV	0.9 / 6.2	0.8 / 5.4	0.7 / 4.7	ns
		XC40250XV	1.1 / 6.5	0.9 / 5.6	0.8 / 4.9	ns
Partial Delay		XC40110XV	7.4 / 0.0	6.5 / 0.0	5.6 / 0.0	ns
Global Early Clock and IFF	T_{PSEP}/T_{PHEP}	XC40150XV	**7.5 / 0.0**	6.6 / 0.0	5.7 / 0.0	ns
Global Early Clock and FCL	T_{PFSEP}/T_{PFHEP}	XC40200XV	9.7 / 0.0	8.4 / 0.0	7.3 / 0.0	ns
		XC40250XV	11.6 / 0.0	10.1 / 0.0	8.8 / 0.0	ns
FullDelay		XC40110XV	10.0 / 0.0	8.6 / 0.0	7.5 / 0.0	ns
Global Early Clock and IFF	T_{PSED}/T_{PHED}	XC40150XV	**10.1 / 0.0**	8.7 / 0.0	7.6 / 0.0	ns
		XC40200XV	10.7 / 0.0	9.3 / 0.0	8.1 / 0.0	ns
		XC40250XV	12.8 / 0.0	11.2 / 0.0	9.7 / 0.0	ns
				Advance		

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Bold Face: Prelminary Values for the XC40150-09. All other values are Advance.

Notes: Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal using the furthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer(TRCE) to determine the setup and hold times under given design conditions.

XV IOB Input Switching Characteristics

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

IOB Input Delay Guidelines

		Speed Grade	-09		-08		-07		Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Clocks									
Clock Enable (EC) to Clock (IK)	T_{ECIK}	All Devices	0.0		0.0		0.0		ns
Delay from Fast Capture Latch enable (OK) active edge to IFF clock (IK) active edge	T_{OKIK}	All Devices	1.3		1.2		1.0		ns
Setup Times									
Pad to Clock (IK), no delay	T_{PICK}	All Devices	1.3		1.1		1.0		ns
Pad to Clock (IK), via transparent Fast Capture Latch, no delay	T_{PICKF}	Al Devices	1.8		1.6		1.4		ns
Pad to Fast Capture Latch Enable (OK), no delay	T_{POCK}	All Devices	1.1		1.0		0.8		ns
Hold Times									
All Hold Times		All Devices	0.0		0.0		0.0		ns
Global Set/Reset									
Minimum GSR Pulse Width	T_{MRW}	All Devices	13.4		11.7		10.2		ns
Delay from GSR input to any Q	T_{RRI*}	XC40110XV	27.2		23.6		20.5		ns
		XC40150XV	29.1		25.3		22.0		ns
		XC40200XV	33.8		29.4		25.5		ns
		XC40250XV	35.8		31.1		27.0		ns
Propagation Delays									
Pad to I1, I2	T_{PID}	All devices		1.6		1.4		1.2	ns
Pad to I1, I2 via transparent input latch, no delay	T_{PLI}	All devices		2.7		2.3		2.0	ns
Pad to I1, I2 via transparent FCL and input latch, no delay	T_{PFLI}	All Devices		3.6		3.1		2.7	ns
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}	All Devices		1.4		1.2		1.1	ns
Clock (IK) to I1, I2 (latch enable, active Low)	T_{IKLI}	All Devices		1.6		1.4		1.2	ns
FCL Enable (OK) active edge to I1, I2 (via transparent standard input latch)	T_{OKLI}	All Devices		2.7		2.4		2.1	ns

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch.

Advance

Bold Face: Prelminary Values for the XC40150-09. All other values are Advance.

* Indicates Minimum Amount of Time to Assure Valid Data.

IOB Output Delay Guidelines

Description	Symbol	Speed Grade Device	-09 Min	-09 Max	-08 Min	-08 Max	-07 Min	-07 Max	Units
Clocks									
Clock High	T_{CH}		2.3		2.0		1.7		ns
Clock Low	T_{CL}		2.3		2.0		1.7		ns
Propagation Delays (See Note 1)									
Clock (OK) to Pad	T_{OKPOF}			3.5		3.0		2.7	ns
Output (O) to Pad	T_{OPF}			3.0		2.6		2.3	ns
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZ}			3.0		2.6		2.2	ns
3-state to Pad active and valid	T_{TSONF}			3.1		2.7		2.3	ns
Output (O) to Pad via Fast Output MUX	T_{OFPF}			4.4		3.8		3.3	ns
Select (OK) to Pad via Fast MUX	T_{OKFPF}			4.0		3.5		3.0	ns
Setup and Hold Times									
Output (O) to clock (OK) setup time	T_{OOK}		0.4		0.4		0.3		ns
Output (O) to clock (OK) hold time	T_{OKO}		0.0		0.0		0.0		ns
Clock Enable (EC) to clock (OK) setup time	T_{ECOK}		0.0		0.0		0.0		ns
Clock Enable (EC) to clock (OK) hold time	T_{OKEC}		0.3		0.2		0.1		ns
Global Set/Reset									
Minimum GSR pulse width	T_{MRW}		13.4		11.7		10.2		ns
Delay from GSR input to any Pad	T_{RPO*}	XC40110XV		30.5		26.6		23.1	ns
		XC40150XV		32.5		28.3		24.6	ns
		XC40200XV		37.1		32.3		28.1	ns
		XC40250XV		39.1		34.0		29.6	ns
Slew Rate Adjustment									
For output SLOW option add	T_{SLOW}			2.3		2.0		1.7	ns
			Advance						

IFF = Input Flip-Flop or Latch, FCL = Fast Capture Latch

Bold Face: Prelminary Values for the XC40150-09. All other values are Advance.

Note: Output timing is measured at ~50% V_{CC} threshold, with 50 pF external capacitive loads.

* Indicates Minimum Amount of Time to Assure Valid Data.