XC4300 HardWire™ Array Family

Product Specification

Features

- Mask-programmed versions of Programmable Logic Cell Arrays FPGA
  - Specifically designed for easy XC4000 series FPGA conversions
  - Significant cost reduction for high volume applications
  - Transparent conversion from FPGA device
  - On-chip scan-path test latches
  - High performance deep submicron CMOS process
  - Meets XC4000 series -4 speeds (system clock rates of 60-70 MHz)
  - On-chip ultra-fast RAM
  - 5 volt operation
- Easy conversion with guaranteed results
  - No customer engineering resource required
  - Fully pin-for-pin compatible
  - Supports most popular package types
  - Same specifications and architecture as programmable XC4000 FPGA devices
  - Up to 13,000 gate complexity
  - All nets and CLBs preserved
  - FPGA Design File used to generate production ready prototypes
  - Prototypes built on production fab line, fully tested to production specification

Description

The XC4300 HardWire Array are mask-programmed versions of the XC4000 programmable devices. In volume applications where the design is stable, the programmable FPGA devices used for prototyping and initial production can be replaced by their HardWire Array equivalents. This offers a significant cost reduction with virtually no risk or engineering resources required.

In a programmable array device, the logic functions and interconnections are determined by the configuration program data, loaded and stored in internal static-memory cells. The HardWire Array has the identical architecture as the programmable FPGA device it replaces. All CLBs, IOBs, interconnect topology, power distribution and so on are the same. In the HardWire Array, the memory cells and the logic they control are replaced by metal connections. Thus the HardWire array is a semicustom device manufactured to provide a customer specific function, yet is completely compatible with the programmable FPGA device it replaces.

Xilinx manufactures the HardWire Array using the information from the programmable array design file. Since the HardWire device is both pinout and architecturally identical to the programmable array device, it is easily created without all the costly and time-consuming engineering activity that other semicustom solutions would require – no redesign time, no expensive and time-consuming simulation runs, no place and route, no test-vector generation. The combination of the programmable FPGA device and the HardWire Array offers the fastest and easiest way to get a new product to market, while ensuring low cost, low risk, and high-volume cost reduction.

Table 1. Summary of HardWire Product Availability For Each Member of the XC4000 Family

HardWire Device	Replacement FPGA	Speed Grade Supported up to 240*	Packages								
			PC 84	PQ 100	VQ 100	TQ 144	PQ 160	PQ 208	BG 225	PG 191	PQ 240
XC4303	XC4002A, XC4003/A	-4	√	√	√						
XC4305	XC4004A, XC4005/A	-4	√	√		√	√	√			
XC4310	XC4006, XC4008, XC4010	-4	√				√	√	√	√	
XC4313	XC4013	-4					√	√	√		√

* Consult factory for information if faster speed grades are required.

X7094

Electrical Characteristics

The XC4300 HardWire Array family is form, fit and function compatible with the XC4000 FPGA family (for XC4000E designs utilizing Select-RAM™ features, Xilinx offers the XC4400 HardWire devices for lower cost solutions for high volume products). Accordingly, all XC4300 HardWire devices meet the electrical specifications of the respective XC4000 FPGA device for the -4 Speed Grade. For specific data, please see the XC4000 section of the Xilinx Programmable Logic Data Book. Absolute Maximum Ratings, Operating Conditions, DC Characteristics, Input to Output Parameters (Pin-to-Pin) and Switching Characteristics of the -4 Speed Grade of the appropriate device type apply.

XC4300 Features

CLB has two **independent** 4-input function generators.
A **third** function generator combines the outputs of the two other function generators with a ninth input.
All function inputs are swappable, all have full access; none are mutually exclusive.
CLB has **very fast arithmetic carry** capability.
CLB function generator look-up table can also be used as high-speed **RAM.**
CLB flip-flops have asynchronous set **or** reset.
CLB has **four outputs**, two flip-flops, two combinatorial.
CLB connections symmetrically located on all **four** edges.

IOB has more versatile clocking polarity options.
IOB has programmable input set-up time:
long to avoid potential hold time problems,
short to improve performance.
IOB has Long Line access through its own TBUF.
Outputs are **n-channel only**, lower V_{OH} increases speed, outputs do not clamp to V_{CC}.

XC4303 and XC4305 can sink 24 mA per output; XC4310 12 mA per output

IEEE 1149.1-type **boundary scan** is supported in the I/O.

Wide decoders on all four edges of the array.

Increased **number of interconnect resources.**
All CLB inputs and outputs have **access to most interconnect lines.**
Switch Matrices are simplified to increase speed.
Eight global nets can be used for clocking or distributing logic signals.
TBUF output configuration is more versatile and 3-state control less confined.

Program is single-function input pin, overrides everything.
INIT pin also acts as Configuration Error output.

Start-up can be **synchronized** to any user clock (this is a configuration option).
No Powerdown, but instead a **Global 3-state input** that does not reset any flip-flops.
No on-chip **crystal oscillator** amplifier.

Configuration Bit Stream includes **CRC error checking.**
Configuration Clock can be increased to **>8 MHz.**
Configuration Clock is **fully static**, no constraint on the maximum Low time.

Table 2. Three Generations of Xilinx HardWire LCA Families

Parameter	XC4300	XC3300	XC2300
Max number of flip-flops	2280	928	174
Max number of user I/O	240	144	74
Max number of RAM bits	28,800	0	0
Function generators per CLB	3	2	2
Number of logic inputs per CLB	9	5	4
Number of logic outputs per CLB	4	2	2
Number of low-skew global nets	8	2	2
Dedicated decoders	yes	no	no
Fast carry logic	yes	no	no
Internal 3-state drivers	yes	yes	no
Output slew-rate control	yes	yes	no
Power-down option	no	yes	yes
Crystal oscillator circuit	no	yes	yes

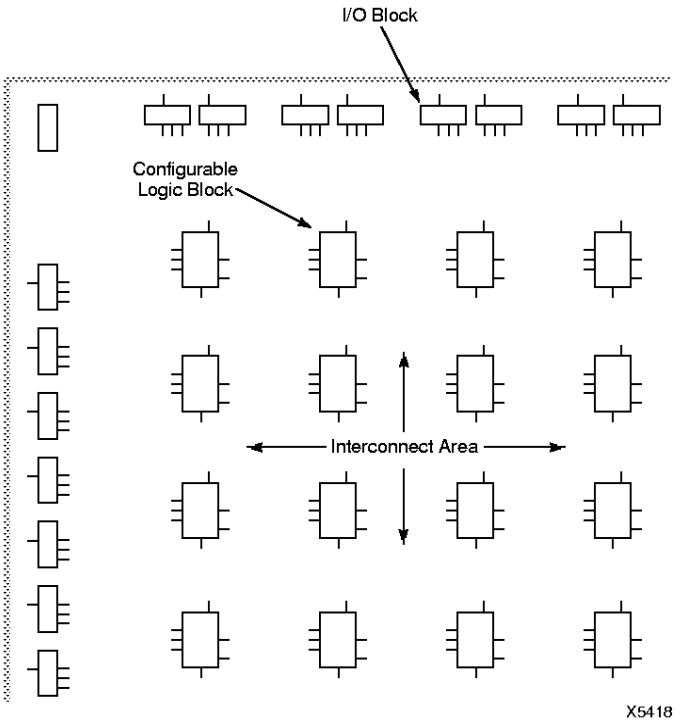


Figure 1. Logic Cell Array Structure

Architectural Overview

As shown in Figure 1, the HardWire Array has the same architecture as the programmable FPGA device it replaces. The perimeter of I/O Blocks (IOBs) provides an interface between the internal logic array and the device package pins. The array of Configurable Logic Blocks (CLBs) performs user-specified logic functions. The interconnect resources are programmed to form networks carrying logic signals among blocks, analogous to printed-circuit-board traces connecting SSI/MSI packages.

The logic functions of the blocks are implemented by look-up tables. Functional options are implemented by user-defined multiplexers. Interconnecting networks between blocks are implemented with user-defined fixed metal connections.

I/O Block

Each user-defined IOB, shown in Figure 5, provides an interface between the external package pin and the internal user logic. It can be defined for input, output or bidirectional signals. The IOB is identical to that used in the programmable array device. There are a wide variety of I/O options available to the user.

Summary of I/O Options

Inputs

- Direct
- Latched/Registered
- Programmable pull-up/pull-down resistor

Outputs

- Direct/registered
- Inverted/not inverted
- 3-state/on/off
- Full speed/slew limited
- 3-state/output enable (inverse)

See *The XC4000 Data Book* for more details on IOB operation.

Configurable Logic Block

The array of Configurable Logic Blocks (CLBs) provides the functional elements from which the user's logic is constructed. The powerful and flexible XC4000/4300 CLB provides more capability than previous generations of array devices, resulting in more "effective gates per CLB."

The XC4300 CLB is identical to that used in the XC4000 family of FPGA devices. Each CLB has two flip-flops and two independent 4-input function generators. A total of thirteen CLB inputs and four CLB outputs provide access to the function generators and flip-flops. These inputs and outputs connect to the user-defined fixed metal interconnects.

The versatility of the CLB function generators improves system speed significantly. In addition, the CLB can pass the combinatorial outputs to the interconnect network, and can also store the combinatorial results or other incoming data in one or two flip-flops, and connect their outputs to the interconnect network as well. The flip-flops can be used as registers or shift registers without blocking the function generators from performing a different, perhaps unrelated, task. This increases the functional density of the device.

See The Xilinx *Programmable Logic Data Book* for more information on Configurable Logic Blocks.

Interconnect

User-defined interconnect resources in the array provide routing paths to connect inputs and outputs of the I/O and logic blocks into logic networks. Three types of metal interconnects are provided to accommodate various network-interconnect requirements:

- General purpose
- Direct connect
- LongLines.

The topology of all these interconnect resources is identical with that of the FPGA, but the speed of the interconnect paths is significantly faster, since all interconnections are fixed metal connections.

Architectural Enhancements

The XC4300 HardWire arrays provide the system features below, incorporated to improve system speed, device flexibility, and ease of use.

- On-Chip Memory
  The XC4000/XC4300 family provides very fast on-chip RAM/ROM capability. Each CLB can be configured as a small memory block that can be combined with as many other CLBs as desired. This reduces the cost of distributed memory dramatically.

- Wide Decoding
  The XC4300 family has 16 very fast programmable decoders located at the chip periphery, four on each chip edge. They accept I/O signals and internal signals as input and generate a very fast decoded output. This fast-decoding feature makes designing with FPGAs easier in many applications.

- Fast Carry Logic
  Each CLB includes high-speed carry logic. The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods, like carry generate/propagate, are meaningless even at the 16-bit level, and are of marginal benefit at the 32-bit level.

  The fast-carry logic opens the door to many new applications involving arithmetic operation where the previous generations of FPGAs were not fast or efficient enough. High-speed address offset calculations in microprocessors or graphics systems, and high-speed addition in digital-signal processing are two typical applications.

- JTAG Boundary Scan
  The XC4000/XC4300 family implements IEEE 1149.1 Boundary-scan methodology. This technique permits systems manufacturers to test their PC boards more safely, thoroughly, and efficiently, at significantly lower cost than using the traditional bed-of-nails test.

Configuration and Start-up

The XC4300 family of HardWire arrays are designed to be fully compatible with their XC4000 programmable array-device equivalents. While the HardWire arrays do not require the loading of configuration data, they support a wide variety of configuration modes.

Configuration

The XC4300 HardWire Array can be used as a stand-alone device or in a daisy chain with other array or HardWire-array devices. It is designed to emulate the configuration sequence of the XC4000 array device for most configuration modes. The HardWire Array cannot act as the first device in a daisy-chain in Master Parallel or Peripheral Mode; however it can operate downstream from an array device operating in these modes. Stand-alone array designs using these modes are also acceptable, since the HardWire Array provides an "instant-on" option. The "instant-on" option bypasses the normal configuration emulation sequence. This mode can also be used for systems where the normal configuration delay is not acceptable.

If "instant-on" is not selected, the user can select either the "bit-swallowing" or "no-data" option. With the bit-swallowing option, the device fully supports Serial Configuration Modes, and may be used anywhere in a daisy chain of array devices with no change to the configuration bitstream

required. With the no-data option, the HardWire Array does not "swallow" its own configuration data. Whatever bits are fed into the DIN pin will appear at the DOUT pin after a delay "TDIO". This mode is useful for a stand-alone HardWire array, or in a daisy chain where the designer wants to reduce the total number of required configuration bits.

Start-Up Sequence

The XC4300 HardWire Arrays are designed to emulate the start-up sequence of the FPGA devices as closely as possible, however, multiple options are available. The start-up sequence may be thought of as three stages: power-on-reset; internal clear; and configuration. There are three basic sequence options:

- Standard configuration
- Rapid reset
- Instant-on

Standard Configuration Sequence

An internal power-on reset circuit is triggered when power is applied. When V_{CC} reaches approximately 3 V, the device generates a POR (power-on reset) pulse. During the reset, the I/O output buffers are disabled and all inputs are pulled High. The POR pulse has a nominal delay of 22 ms. If the M0 pin is held Low during the POR cycle, (see chart) the POR pulse is extended to four times its nominal delay. This ensures that all daisy-chained slave devices will have sufficient time to power up.

Following the POR cycle, the HardWire Array enters a "clearing" state. This state emulates the memory clear performed by a FPGA upon power-up. The length of the clear cycle is nominally 250 µs.

At the completion of the clear cycle the INIT pin is sampled. If the INIT pin is held Low, the "configuration" is delayed until INIT is driven High and the value of the Mode pins is latched. If the device is in Master Mode (see chart) it begins to produce CCLKs. If the device is in Slave Mode it requires CCLKs to be supplied from another device.

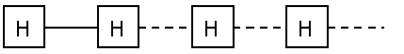
If "no-data" is chosen after four CCLK cycles the part is "configured" and the Done pin is released. (If the device is in a daisy chain with the DONE pins tied together the DONE pin will remain Low until all devices have completed configuration.)

Table 3. Configuration Modes

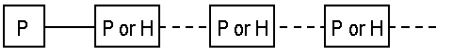
M0	M1	POR	CCLK
0	X	4X	Mstr
1	0	1X	Mstr
1	1	1X	Slv

Example 1. As a stand alone HardWire Array.

Example 2. As a daisy chain of all HardWire Arrays.



Example 3. As a HardWire Array or programmable slave in a daisy chain with a Programmable device as a master.



Example 4. As a HardWire Array device acting as a Serial Master with any combination of Programmable and HardWire Arrays as slaves.

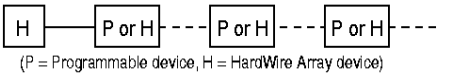


Figure 2.

One CCLK after the DONE pin goes High the I/Os will become active. The internal global reset is user-defined to release either one CCLK cycle before or after the I/O pins become active. A HardWire Array operating in Master Mode will stop producing CCLKs one cycle after the I/Os become active.

If "bit-swallowing" is chosen, the device will behave exactly like a serial mode XC4000. A complete bit stream is required to configure the array. The full range of start-up options offered by the XC4000 are available.

Rapid Reset

The rapid-reset cycle follows the same three stages as the standard configuration sequence, however the time delays are significantly reduced. The POR pulse is shortened and is nominally 1 µs. The clearing-state delay is also reduced to approximately 1 µs. Following the clearing state, the configuration stage is the same as for the standard configuration sequence.

Instant-On

When the Instant-On option is selected, the HardWire Array has a short POR delay of nominally 1 µs. If the INIT pin is not held Low, the array goes active within an additional 1 µs. The DONE pin goes High, the I/Os become active, and the internal global set/reset signal goes inactive. Holding the INIT pin Low delays start-up until the INIT pin is released, at which time the device goes active within 1 µs. The CCLK pin is disabled during the entire power-up and start-up sequence.

Performance

The XC4300 family of HardWire Arrays is manufactured using the same high-performance submicron CMOS technology. Actual array performance is determined by the timing of critical paths, including the timing for the logic and storage elements in that path and the timing of the associated interconnect. HardWire Array logic-block performance is equal to or slightly faster than the equivalent FPGA performance, while the interconnect performance is significantly faster.

All HardWire Arrays are specified and tested for operation at the fastest equivalent FPGA speed available at the time the HardWire device is introduced. For the XC4300 family, this means all parts are guaranteed to the -4 speed grade. Since the finished HardWire product is customized for a specific customer and application, speed grading is not available.

Power

Power for the HardWire Array is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the device, dedicated V_{CC} and ground rings surround the logic array and provide power to the I/O drivers. An independent matrix of V_{CC} and ground lines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically a 0.1-µF capacitor connected near the V_{CC} and ground pins will provide adequate decoupling.

Output buffers capable of driving the specified 12-mA/ 24-mA loads under worst-case conditions may be capable of driving many times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads. The I/O Block output buffers have a slew-limited mode which should be used where output rise and fall times are not speed critical. Slew-limited outputs maintain their dc drive capability, but generate less external reflections and internal noise. A maximum total external capacitive load for simultaneous fast-mode switching in the same direction is 200 pF per power/ground pin pair. For slew-rate limited outputs this total is four times larger.

XC4000/XC4300-Family Pin Assignments

Xilinx offers members of the XC4300 family in a variety of surface-mount and through-hole package types, with pin counts from 84 to 225.

Each chip is offered in several package types to accommodate the available PC-board space and manufacturing technology. Most package types are also offered with different chips to accommodate design changes without requiring PC-board changes.

3 V/5 V Considerations

The XC4300 HardWire Array operates as 5 volt device only. See table 4.

Table 4. 5 Volt Operation

	5 Volt Operation			
	Vil (max)	Vih (min)	Vol (max)	Voh (min)
XC4300	0.80	2.00	0.40	V_{CC} -0.4

X7115

HardWire Array Testability

The HardWire Array products contain significant on-chip logic to facilitate manufacturability and testing. This logic, combined with Xilinx's internal Automatic Test Generation (ATG) software, assures 100% functionality. In fact, the HardWire array can be 100% functionally tested by Xilinx without the need for customer generated test vectors (as is required with custom gate arrays).

This section examines the two basic block structures and the special test circuitry in the HardWire Array.

Test Architecture

The HardWire Array contains two types of internal blocks: the Input/Output Block (IOB) and the Configurable Logic Block (CLB). To accomplish 100% functional testing, special test circuitry is designed into the device. This circuitry allows testing of each block (CLB and IOB) in a synchronized procedure known as "Scan Test". Special dedicated test latches (called TBLKs) are included on all HardWire devices. They are completely transparent to the normal operation of the circuit. Scan testing allows the contents of all internal flip-flops to be serially shifted off-chip, and for Xilinx generated test vectors to be shifted into the device, thus enabling all flip-flops to be initialized to any desired state.

These special dedicated test latches are placed into each CLB and IOB. Each CLB has four internal test latches, (placed at the CLB outputs), while each IOB contains four test latches (placed at the IOB inputs) as shown in Figures 3 and 4. The placement of these test latches is very important, since each CLB output or IOB input can fanout to multiple destinations. All sources and destinations of logic blocks come from other logic blocks. Therefore, this placement of the latches provides complete access to all nets and synchronized control of all CLBs and IOBs.

The test latches are connected into a daisy chain which passes through every flip-flop in the array. Figure 5 shows an overview of the scan path. The path begins at the Scan In pin, sequences through each CLB, then through the IOBs, and finally exits at the Scan Out pin. This scan path can be seen in more detail in Figure 4, which shows the precise sequence with which the CLB and IOB internal test latches are loaded or read.

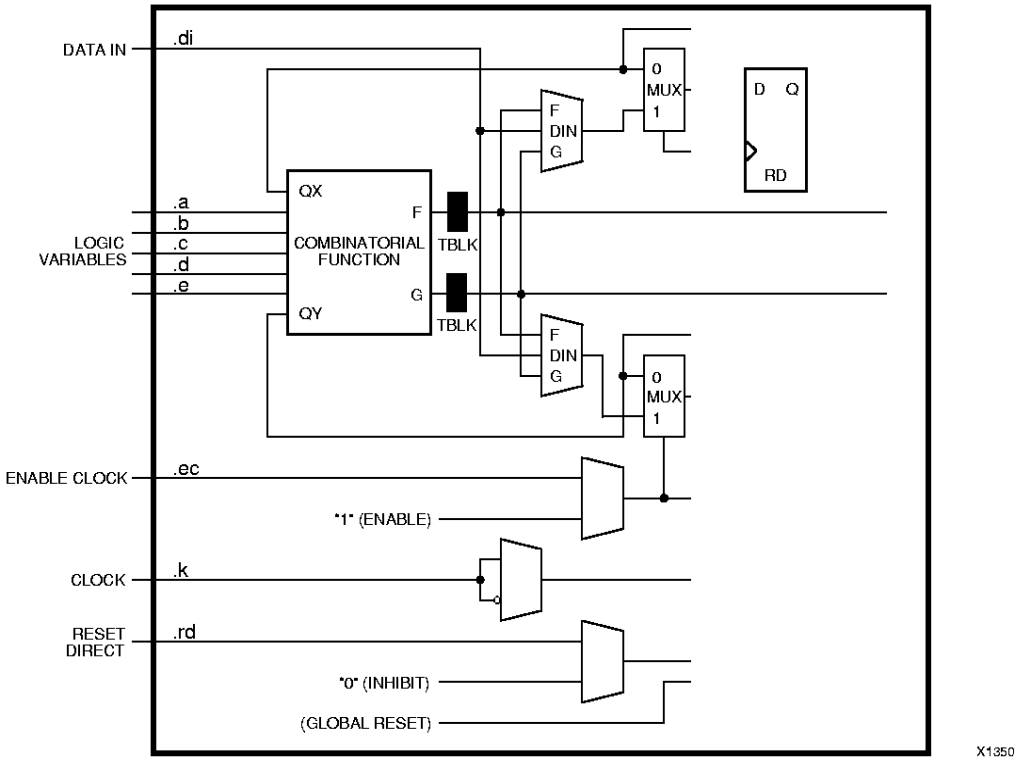


Figure 3. HardWire CLB Test Latch Locations

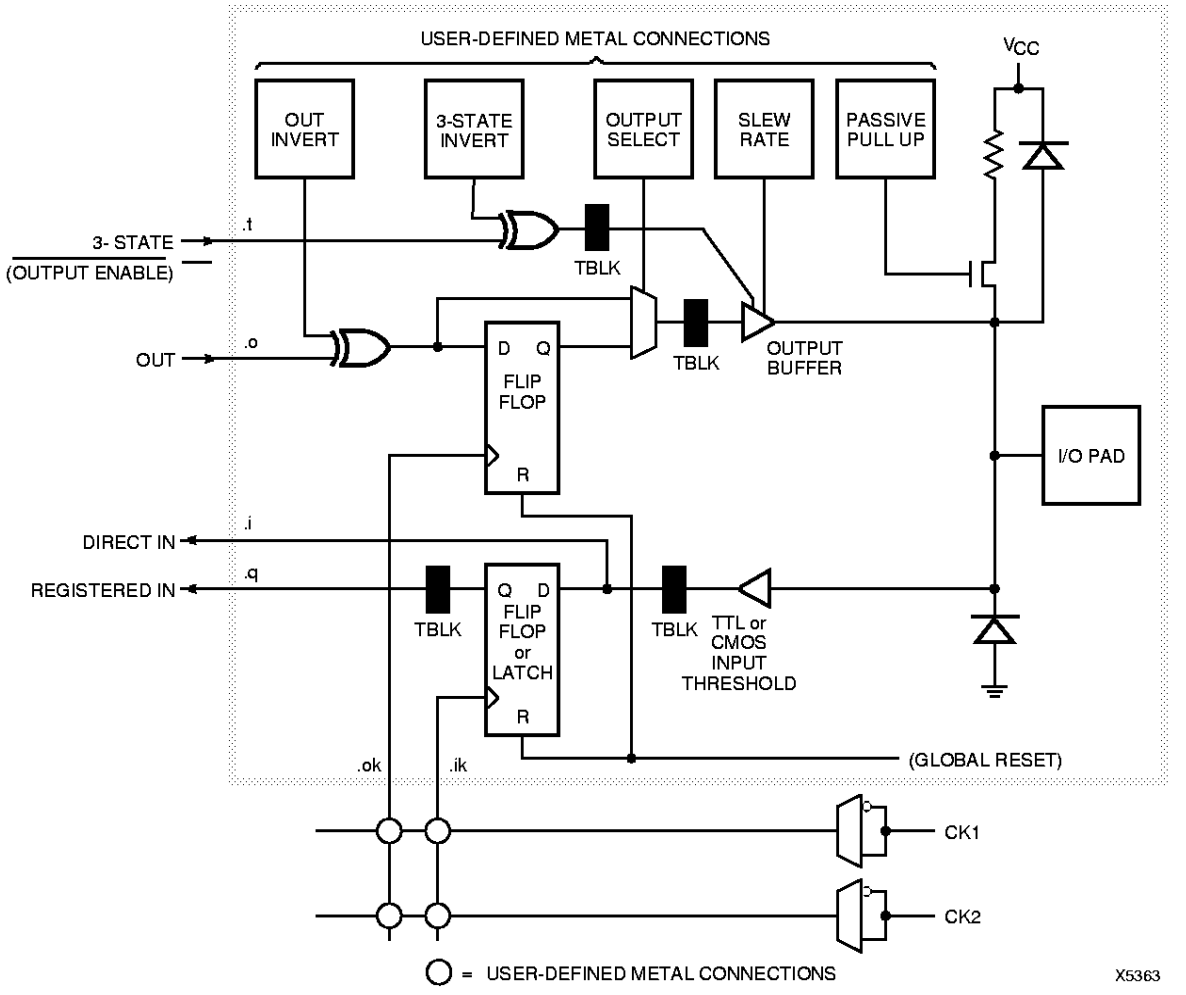


Figure 4. HardWire IOB Test Latch Location

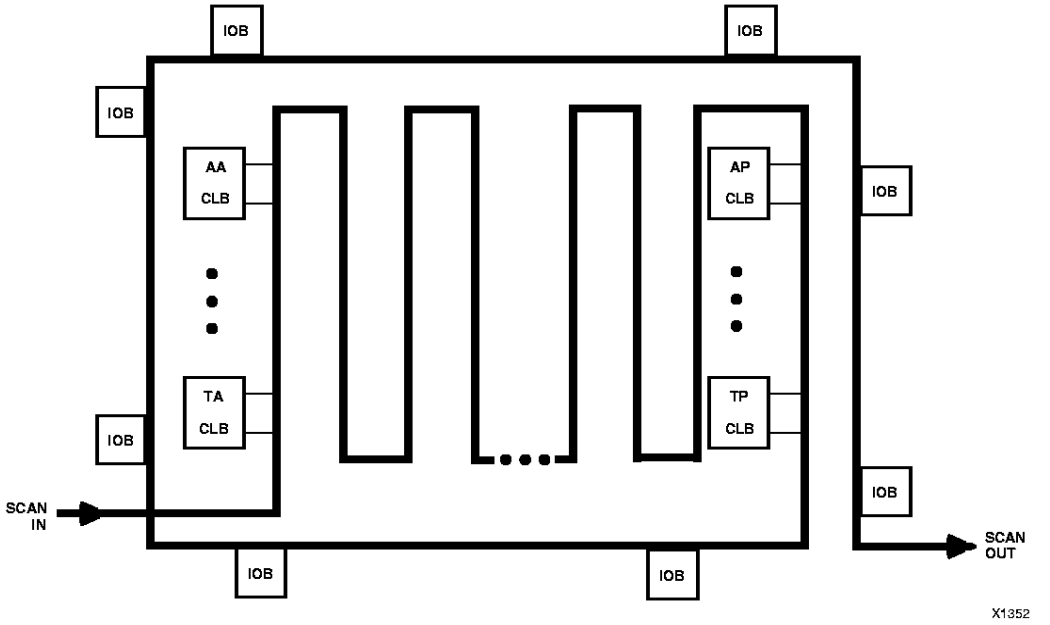


Figure 5. Scan Path Overview

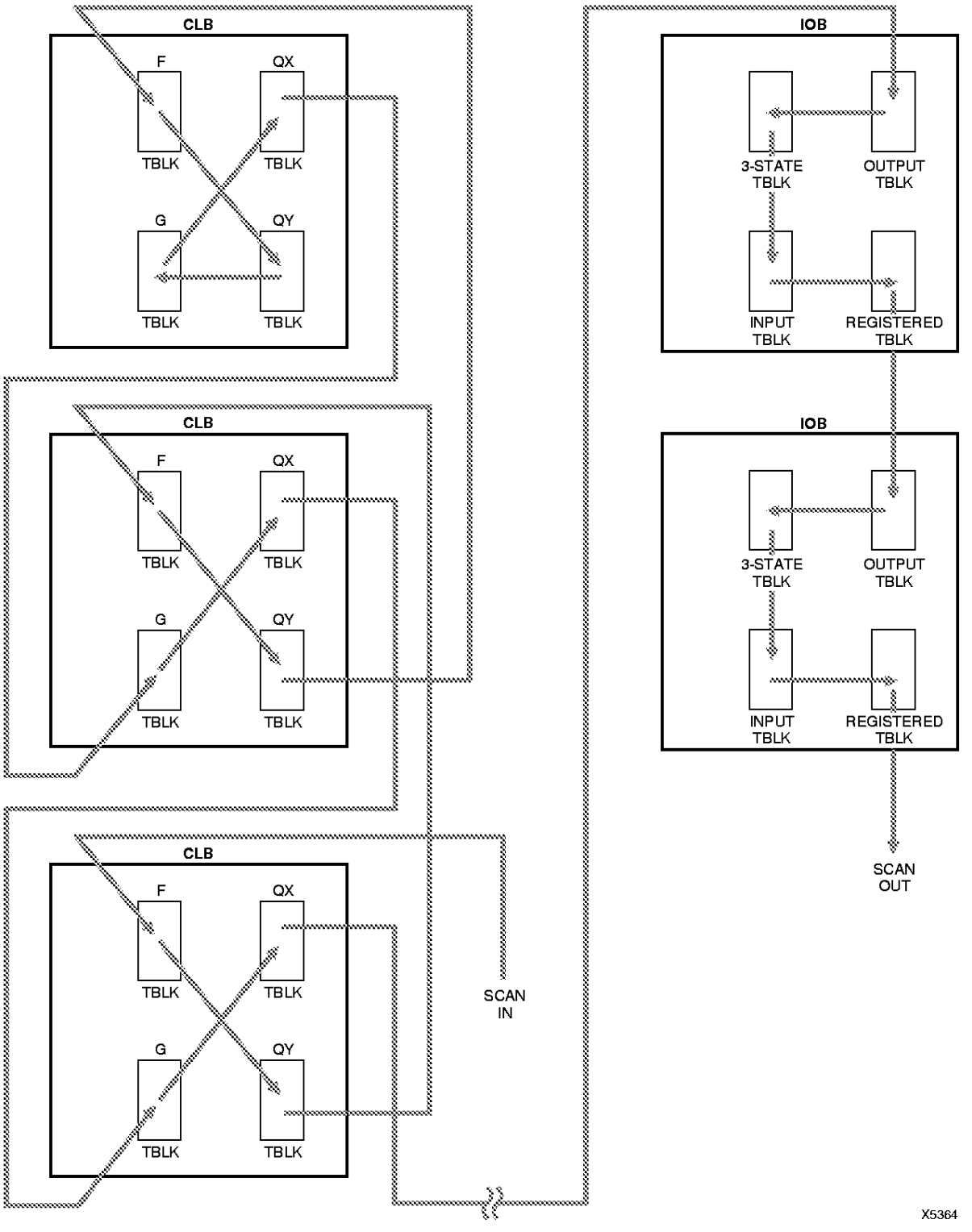


Figure 6. Detailed Scan Path

The internal architecture of a TBLK is shown in Figure 7. In the normal operation mode of the HardWire array, SW1 is in position A and all the test latches are bypassed completely. The HardWire array device is set into Test Mode (SW1 = position B) by Xilinx ATG software. This software inputs unique conditions on several control pins while serially loading a "password" into the device. For this reason, it is not possible for a customer design to inadvertently place the HardWire array into Test Mode. When SW1 is in position B (Test Mode) all the latches can receive data from either the CLB output or the previous latch in the daisy chain (SQn).

Synchronized together by a special test clock, all the test latches operate in two phases. The first phase serially loads all the latches to place a specific vector at the inputs of the logic block to be tested. The second phase is a parallel load of all latches, storing the expected output data of the logic block being tested (SW2 = A). At this point testing returns to phase one and serially clocks out the results, while simultaneously clocking in a new input vector.

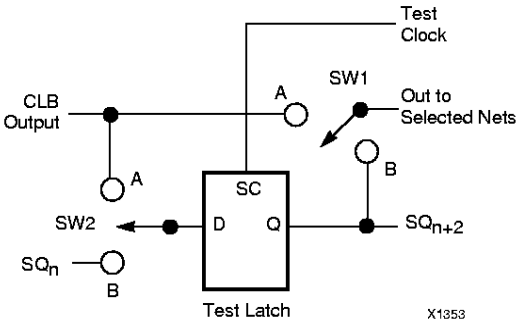


Figure 7. TBLK Block Diagram

Scan Test

To see how scan testing can be used to provide complete functional test coverage, consider the logic shown in Figure 8. This diagram shows a CLB (CLB2) with two inputs being driven by two different CLBs and the other two inputs being driven by two different IOBs. If we apply every possible combination of inputs to CLB2 and all expected output conditions are met, then CLB2 has been 100% functionally tested. The input conditions applied also include any register control signals (such as Clock, Reset, or Clock Enable). The same procedure is used for testing IOBs.

Looking again at Figure 8, CLB2 is tested by first serially loading the X output latches of CLB1 and CLB3 and the input latches of IOB1 and IOB2. Note that the latches on CLB2's outputs are also loaded in this first phase. Not all CLBs and IOBs can be tested at once, due to signal dependencies. To position the correct data into the latches all unused latches still need "don't cares" loaded. Regardless of which CLBs and IOBs are being tested by a particular scan vector, the complete scan path is always shifted in and out for testing and verification. The state of CLB2's output latches will be opposite to their expected results in phase two. This guarantees that CLB2's input data changed the state of its output latches and therefore, is current data.

CLB or IOB data registers using a synchronous or asynchronous clock are not a problem during this special test mode. All customer-used registers are clock inhibited during the phase one load. The inhibit of register clocking is accomplished by logically "ANDing" the register clocks with the global inhibit control line.

The test vectors needed to perform this thorough testing are created by Xilinx. No additional effort or engineering time is required from the user to ensure proper device performance. The customer design file used to create the HardWire array is used in conjunction with specially developed Xilinx Automatic Test Generation software. This creates the complete set of test vectors required to perform 100% functional testing. This software creates the data for all possible input conditions and corresponding output data for each CLB and IOB used in the customer design. This data is then compiled into the test vectors used to perform the actual testing.

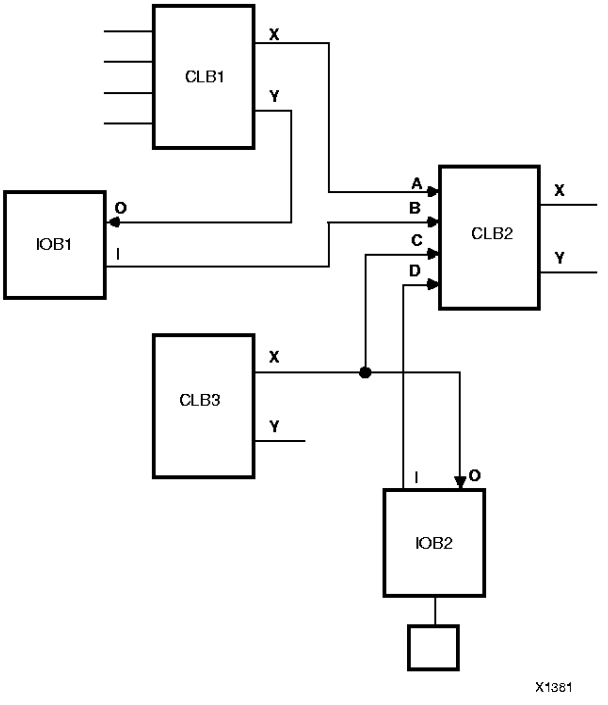


Figure 8. Four Input CLB (CLB2) Driven by Two Different CLB Outputs and Two different IOB Outputs

XC4303 Pinouts

Pin Description	PC84	PQ100	Bound Scan
VCC	2	92	–
I/O (A8)	3	93	32
I/O (A9)	4	94	35
I/O	–	95	38
I/O	–	96	41
I/O (A10)	5	97	44
I/O (A11)	6	98	47
–	–	–	–
I/O (A12)	7	99	50
I/O (A13)	8	100	53
–	–	–	–
–	–	–	–
I/O (A14)	9	1	56
SGCK1 (A15,I/O)	10	2	59
VCC	11	3	–
GND	12	4	–
PGCK1 (A16, I/O)	13	5	62
I/O (A17)	14	6	65
–	–	–	–
–	–	–	–
I/O (TDI)	15	7	68
I/O (TCK)	16	8	71
–	–	–	–
I/O (TMS)	17	9	74
I/O	18	10	77
I/O	–	–	80
I/O	–	11	83
I/O	19	12	86
I/O	20	13	89
GND	21	14	–
VCC	22	15	–
I/O	23	16	92
I/O	24	17	95
I/O	–	18	98
I/O	–	–	101
I/O	25	19	104
I/O	26	20	107
I/O	27	21	110
I/O	–	22	113
–	–	–	–
I/O	28	23	116
SGCK2 (I/O)	29	24	119
O (M1)	30	25	122
GND	31	26	–
I (M0)	32	27	125†
VCC	33	28	–
I (M2)	34	29	126†
PGCK2 (I/O)	35	30	127
I/O (HDC)	36	31	130
–	–	–	–
–	–	–	–
I/O	–	32	133
I/O ($\overline{LDC}$)	37	33	136
I/O	38	34	139
I/O	39	35	142
I/O	–	36	145
I/O	–	37	148
I/O	40	38	151
I/O ($\overline{ERR}$, $\overline{INIT}$)	41	39	154
VCC	42	40	–

Pin Description	PC84	PQ100	Bound Scan
GND	43	41	–
I/O	44	42	157
I/O	45	43	160
I/O	–	44	163
I/O	–	45	166
I/O	46	46	169
I/O	47	47	172
I/O	48	48	175
I/O	49	49	178
–	–	–	–
–	–	–	–
I/O	50	50	181
SGCK3 (I/O)	51	51	184
GND	52	52	–
DONE	53	53	–
VCC	54	54	–
$\overline{PROG}$	55	55	–
I/O (D7)	56	56	187
PGCK3 (I/O)	57	57	190
–	–	–	–
–	–	–	–
I/O (D6)	58	58	193
I/O	–	59	196
I/O (D5)	59	60	199
I/O ($\overline{CS0}$)	60	61	202
I/O	–	62	205
I/O	–	63	208
I/O (D4)	61	64	211
I/O	62	65	214
VCC	63	66	–
GND	64	67	–
I/O (D3)	65	68	217
I/O ($\overline{RS}$)	66	69	220
I/O	–	70	223
I/O	–	–	226
I/O (D2)	67	71	229
I/O	68	72	232
I/O (D1)	69	73	235
I/O (RCLK-$\overline{BUSY}$/RDY)	70	74	238
–	–	–	–
–	–	–	–
I/O (D0, DIN)	71	75	241
SGCK4 (DOUT, I/O)	72	76	244
CCLK	73	77	–
VCC	74	78	–
O (TDO)	75	79	–
GND	76	80	–
I/O (A0, $\overline{WS}$)	77	81	2
PGCK4 (A1, I/O)	78	82	5
–	–	–	–
–	–	–	–
I/O (CS1, A2)	79	83	8
I/O (A3)	80	84	11
I/O (A4)	81	85	14
I/O (A5)	82	86	17
I/O	–	87	20
I/O	–	88	23
I/O (A6)	83	89	26
I/O (A7)	84	90	29
GND	1	91	–

* Indicates unconnected package pins.
† Contributes only one bit (.i) to the boundary scan register.
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 247 = BSCANT.UPD

XC4305 Pinouts

Pin Description	PC84	PQ160	PQ208	Bound Scan
VCC	2	142	183	–
I/O (A8)	3	143	184	44
I/O (A9)	4	144	185	47
I/O	–	145	186	50
I/O	–	146	187	53
–	–	–	188*	–
–	–	–	189*	–
I/O (A10)	5	147	190	56
I/O (A11)	6	148	191	59
I/O	–	149	192	62
I/O	–	150	193	65
GND	–	151	194	–
–	–	–	195*	–
–	–	–	196*	–
–	–	152*	197*	–
–	–	153*	198*	–
I/O (A12)	7	154	199	68
I/O (A13)	8	155	200	71
–	–	–	–	–
I/O	–	156	201	74
I/O	–	157	202	77
I/O (A14)	9	158	203	80
SGCK1 (A15, I/O)	10	159	204	83
VCC	11	160	205	–
–	–	–	206*	–
–	–	–	207*	–
–	–	–	208*	–
–	–	–	1*	–
GND	12	1	2	–
–	–	–	3*	–
PGCK1 (A16, I/O)	13	2	4	86
I/O (A17)	14	3	5	89
I/O	–	4	6	92
I/O	–	5	7	95
–	–	–	–	–
I/O (TDI)	15	6	8	98
I/O (TCK)	16	7	9	101
–	–	8*	10*	–
–	–	9*	11*	–
–	–	–	12*	–
–	–	–	13*	–
GND	–	10	14	–
I/O	–	11	15	104
I/O	–	12	16	107
I/O (TMS)	17	13	17	110
I/O	18	14	18	113
–	–	–	19*	–
–	–	–	20*	–
I/O	–	15	21	116
I/O	–	16	22	119
I/O	19	17	23	122
I/O	20	18	24	125
GND	21	19	25	–
VCC	22	20	26	–
I/O	23	21	27	128
I/O	24	22	28	131
I/O	–	23	29	134
I/O	–	24	30	137
–	–	–	31*	–
–	–	–	32*	–
I/O	25	25	33	140
I/O	26	26	34	143
I/O	–	27	35	146
I/O	–	28	36	149
GND	–	29	37	–
–	–	–	38*	–
–	–	–	39*	–
–	–	30*	40*	–
–	–	31*	41*	–
I/O	27	32	42	152
I/O	–	33	43	155
I/O	–	34	44	158

Pin Description	PC84	PQ160	PQ208	Bound Scan
I/O	–	35	45	161
–	–	–	–	–
I/O	28	36	46	164
SGCK2 (I/O)	29	37	47	167
O (M1)	30	38	48	170
GND	31	39	49	–
I (M0)	32	40	50	173†
–	–	–	51*	–
–	–	–	52*	–
–	–	–	53*	–
–	–	–	54*	–
VCC	33	41	55	–
I (M2)	34	42	56	174†
PGCK2 (I/O)	35	43	57	175
I/O (HDC)	36	44	58	178
I/O	–	45	59	181
–	–	–	–	–
I/O	–	46	60	184
I/O	–	47	61	187
I/O ($\overline{LDC}$)	37	48	62	190
–	–	49*	63*	–
–	–	50*	64*	–
–	–	–	65*	–
–	–	–	66*	–
GND	–	51	67	–
I/O	–	52	68	193
I/O	–	53	69	196
I/O	38	54	70	199
I/O	39	55	71	202
–	–	–	72*	–
–	–	–	73*	–
I/O	–	56	74	205
I/O	–	57	75	208
I/O	40	58	76	211
I/O ($\overline{ERR}$, $\overline{INIT}$)	41	59	77	214
VCC	42	60	78	–
GND	43	61	79	–
I/O	44	62	80	217
I/O	45	63	81	220
I/O	–	64	82	223
I/O	–	65	83	226
–	–	–	84*	–
–	–	–	85*	–
I/O	46	66	86	229
I/O	47	67	87	232
I/O	–	68	88	235
I/O	–	69	89	238
GND	–	70	90	–
–	–	–	91*	–
–	–	–	92*	–
–	–	71*	93*	–
–	–	72*	94*	–
I/O	48	73	95	241
I/O	49	74	96	244
I/O	–	75	97	247
I/O	–	76	98	250
I/O	50	77	99	253
SGCK3 (I/O)	51	78	100	256
GND	52	79	101	–
–	–	–	102*	–
DONE	53	80	103	–
–	–	–	104*	–
–	–	–	105*	–
VCC	54	81	106	–
–	–	–	107*	–
$\overline{PROG}$	55	82	108	–
I/O (D7)	56	83	109	259
PGCK3 (I/O)	57	84	110	262
I/O	–	85	111	265
–	–	–	–	–
I/O	–	86	112	268
I/O (D6)	58	87	113	271

Pin Description	PC84	PQ160	PQ208	Bound Scan
I/O	–	88	114	274
–	–	89*	115*	–
–	–	89*	115*	–
–	–	90†	116*	–
–	–	–	117*	–
–	–	–	118*	–
GND	–	91	119	–
I/O	–	92	120	277
I/O	–	93	121	280
I/O (D5)	59	94	122	283
I/O (CS0)	60	95	123	286
–	–	–	124*	–
–	–	–	125*	–
I/O	–	96	126	289
I/O	–	97	127	292
I/O (D4)	61	98	128	295
I/O	62	99	129	298
VCC	63	100	130	–
GND	64	101	131	–
I/O (D3)	65	102	132	301
I/O ($\overline{RS}$)	66	103	133	304
I/O	–	104	134	307
I/O	–	105	135	310
–	–	–	136*	–
–	–	–	137*	–
I/O (D2)	67	106	138	313
I/O	68	107	139	316
I/O	–	108	140	319
I/O	–	109	141	322
GND	–	110	142	–
–	–	–	143*	–
–	–	–	144*	–
–	–	111*	145*	–
–	–	112*	146*	–
I/O (D1)	69	113	147	325
I/O (RCLK-$\overline{BUSY}$/RDY)	70	114	148	328
I/O	–	115	149	331
–	–	–	–	–
I/O	–	116	150	334
I/O (D0, DIN)	71	117	151	337
SGCK4 (DOUT, I/O)	72	118	152	340
CCLK	73	119	153	–
VCC	74	120	154	–
–	–	–	155*	–
–	–	–	156*	–
–	–	–	157*	–
–	–	–	158*	–
O (TDO)	75	121	159	–
GND	76	122	160	–
I/O (A0,$\overline{WS}$)	77	123	161	2
PGCK4 (A1,I/O)	78	124	162	5
I/O	–	125	163	8
–	–	–	–	–
I/O	–	126	164	11
I/O (CS1,A2)	79	127	165	14
I/O (A3)	80	128	166	17
–	–	129*	167*	–
–	–	130*	168*	–
–	–	–	169*	–
–	–	–	170*	–
GND	–	131	171	–
I/O	–	132	172	20
I/O	–	133	173	23
I/O (A4)	81	134	174	26
I/O (A5)	82	135	175	29
–	–	–	176*	–
–	–	136*	177*	–
I/O	–	137	178	32
I/O	–	138	179	35
I/O (A6)	83	139	180	38
I/O (A7)	84	140	181	41
GND	1	141	182	–

* Indicates unconnected package pins.

† Contributes only one bit (.i) to the boundary scan register.

Boundary Scan Bit 0 = TDO.T

Boundary Scan Bit 1 = TDO.O

XC4310 Pinouts

Pin Description	PQ160	PG191	PQ208	Boundary Scan Order
VCC	142	J4	183	-
I/O (A8)	143	J3	184	62
I/O (A9)	144	J2	185	65
I/O	145	J1	186	68
I/O	146	H1	187	71
I/O	-	H2	188	74
I/O	-	H3	189	77
I/O (A10)	147	G1	190	80
I/O (A11)	148	G2	191	83
I/O	149	F1	192	86
I/O	150	E1	193	89
GND	151	G3	194	-
I/O	-	F2	195	92
I/O	-	D1	196	96
I/O	152	C1	197	98
I/O	153	E2	198	101
I/O (A12)	154	F3	199	104
I/O (A13)	155	D2	200	107
I/O	156	B1	201	110
I/O	157	E3	202	113
I/O (A14)	158	C2	203	116
SGCK1 (A15, I/O)	159	B2	204	119
VCC	160	D3	205	-
-	-	-	206*	-
-	-	-	207*	-
-	-	-	208*	-
-	-	-	1*	-
GND	1	D4	2	-
-	-	-	3*	-
PGCK1 (A16, I/O)	2	C3	4	122
I/O (A17)	3	C4	5	125
I/O	4	B3	6	128
I/O	5	C5	7	131
I/O (TDI)	6	A2	8	134
I/O (TCK)	7	B4	9	137
I/O	8	C6	10	140
I/O	9	A3	11	143
I/O	-	B5	12	146
I/O	-	B6	13	149
GND	10	C7	14	-
I/O	11	A4	15	152
I/O	12	A5	16	155
I/O (TMS)	13	B7	17	158
I/O	14	A6	18	161
I/O	-	C8	19	164
I/O	-	A7	20	167
I/O	15	B8	21	170
I/O	16	A8	22	173
I/O	17	B9	23	176
I/O	18	C9	24	179
GND	19	D9	25	-
VCC	20	D10	26	-
I/O	21	C10	27	182
I/O	22	B10	28	185
I/O	23	A9	29	188

Pin Description	PQ160	PG191	PQ208	Boundary Scan Order
I/O	24	A10	30	191
I/O	-	A11	31	194
I/O	-	C11	32	197
I/O	25	B11	33	200
I/O	26	A12	34	203
I/O	27	B12	35	206
I/O	28	A13	36	209
GND	29	C12	37	-
I/O	-	B13	38	212
I/O	-	A14	39	215
I/O	30	A15	40	218
I/O	31	C13	41	221
I/O	32	B14	42	224
I/O	33	A16	43	227
I/O	34	B15	44	230
I/O	35	C14	45	233
I/O	36	A17	46	236
SGCK2 (I/O)	37	B16	47	239
M1	38	C15	48	242
GND	39	D15	49	-
M0	40	A18	50	245†
-	-	-	51*	-
-	-	-	52*	-
-	-	-	53*	-
-	-	-	54*	-
VCC	41	D16	55	-
M2	42	C16	56	246†
PGCK2 (I/O)	43	B17	57	247
I/O (HDC)	44	E16	58	250
I/O	45	C17	59	253
I/O	46	D17	60	256
I/O	47	B18	61	259
I/O (LDC)	48	E17	62	262
I/O	49	F16	63	265
I/O	50	C18	64	268
I/O	-	D18	65	271
I/O	-	F17	66	274
GND	51	G16	67	-
I/O	52	E18	68	277
I/O	53	F18	69	280
I/O	54	G17	70	283
I/O	55	G18	71	286
I/O	-	H16	72	289
I/O	-	H17	73	291
I/O	56	H18	74	295
I/O	57	J18	75	298
I/O	58	J17	76	301
I/O ($\overline{ERR}$, $\overline{INIT}$)	59	J16	77	304
VCC	60	J15	78	-
GND	61	K15	79	-
I/O	62	K16	80	307
I/O	63	K17	81	310
I/O	64	K18	82	313
I/O	65	L18	83	316
I/O	-	L17	84	319
I/O	-	L16	85	322
I/O	66	M18	86	325

* Indicates unconnected package pins.

† Contributes only one bit (.i) to the boundary scan register.

XC4310 Pinouts (continued)

Pin Description	PQ160	PG191	PQ208	Boundary Scan Order
I/O	67	M17	87	328
I/O	68	N18	88	331
I/O	69	P18	89	334
GND	70	M16	90	-
I/O	-	N17	91	337
I/O	-	R18	92	340
I/O	71	T18	93	343
I/O	72	P17	94	346
I/O	73	N16	95	349
I/O	74	T17	96	352
I/O	75	R17	97	355
I/O	76	P16	98	358
I/O	77	U18	99	361
SGCK3 (I/O)	78	T16	100	364
GND	79	R16	101	-
-	-	-	102*	-
DONE	80	U17	103	-
-	-	-	104*	-
-	-	-	105*	-
VCC	81	R15	106	-
-	-	-	107*	-
$\overline{\text{PROG}}$	82	V18	108	-
I/O (D7)	83	T15	109	367
PGCK3 (I/O)	84	U16	110	370
I/O	85	T14	111	373
I/O	86	U15	112	376
I/O (D6)	87	V17	113	379
I/O	88	V16	114	382
I/O	89	T13	115	385
I/O	90	U14	116	388
I/O	-	V15	117	391
I/O	-	V14	118	394
GND	91	T12	119	-
I/O	92	U13	120	397
I/O	93	V13	121	400
I/O (D5)	94	U12	122	403
I/O ($\overline{\text{CSO}}$)	95	V12	123	406
I/O	-	T11	124	409
I/O	-	U11	125	412
I/O	96	V11	126	415
I/O	97	V10	127	418
I/O (D4)	98	U10	128	421
I/O	99	T10	129	424
VCC	100	R10	130	-
GND	101	R9	131	-
I/O (D3)	102	T9	132	427
I/O ($\overline{\text{RS}}$)	103	U9	133	430
I/O	104	V9	134	433
I/O	105	V8	135	436
I/O	-	U8	136	439
I/O	-	T8	137	442
I/O (D2)	106	V7	138	445
I/O	107	U7	139	448
I/O	108	V6	140	451
I/O	109	U6	141	454
GND	110	T7	142	-
I/O	-	V5	143	457

* Indicates unconnected package pins.

Pin Description	PQ160	PG191	PQ208	Boundary Scan Order
I/O	-	V4	144	460
I/O	111	U5	145	463
I/O	112	T6	146	466
I/O (D1)	113	V3	147	469
I/O ($\overline{\text{RCLK}}$-$\overline{\text{BUSY}}$/RDY)	114	V2	148	472
I/O	115	U4	149	475
I/O	116	T5	150	478
I/O (D0, DIN)	117	U3	151	481
SGCK4 (I/O)	118	T4	152	484
CCLK	119	V1	153	-
VCC	120	R4	154	-
-	-	-	155*	-
-	-	-	156*	-
-	-	-	157*	-
-	-	-	158*	-
TD0	121	U2	159	-
GND	122	R3	160	-
I/O (A0, $\overline{\text{WS}}$)	123	T3	161	2
PGCK4 (I/O, A1)	124	U1	162	5
I/O	125	P3	163	8
I/O	126	R2	164	11
I/O (CS1, A2)	127	T2	165	14
I/O (A3)	128	N3	166	17
I/O	129	P2	167	20
I/O	130	T1	168	23
I/O	-	R1	169	26
I/O	-	N2	170	29
GND	131	M3	171	-
I/O	132	P1	172	32
I/O	133	N1	173	35
I/O (A4)	134	M2	174	38
I/O (A5)	135	M1	175	41
I/O	-	L3	176	44
I/O	136	L2	177	47
I/O	137	L1	178	50
I/O	138	K1	179	53
I/O (A6)	139	K2	180	56
I/O (A7)	140	K3	181	59
GND	141	K4	182	-

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 487 = BSCAN.UPD

XC4313 Pinouts

Pin Description	PQ208	BG225	PQ240	Boundary Scan Orde
VCC	183	A10	212	-
I/O (A8)	184	E8	213	74
I/O (A9)	185	F8	214	77
I/O	186	B7	215	80
I/O	187	A7	216	83
I/O	188	G7	217	86
I/O	189	E7	218	89
-	-	-	219*	-
I/O (A10)	190	F7	220	92
I/O (A11)	191	C7	221	95
VCC	-	-	222	-
I/O	-	B6	223	98
I/O	-	E6	224	101
I/O	192	D7	225	104
I/O	193	F6	226	107
GND	194	A5	227	-
I/O	195	B5	228	110
I/O	196	D5	229	113
I/O	197	C5	230	116
I/O	198	C6	231	119
I/O (A12)	199	A4	232	122
I/O (A13)	200	D4	233	125
I/O	-	B4	234	128
I/O	-	C3	235	131
I/O	201	A3	236	134
I/O	202	C2	237	137
I/O (A14)	203	D6	238	140
SGCK1 (A15, I/O)	204	A2	239	143
VCC	205	A6	240	-
-	206*	-	-	-
-	207*	-	-	-
-	208*	-	-	-
-	1*	-	-	-
GND	2	A1	1	-
-	3*	-	-	-
PGCK1 (A16,I/O)	4	B1	2	146
I/O (A17)	5	B3	3	149
I/O	6	C4	4	152
I/O	7	B2	5	155
I/O (TDI)	8	C1	6	158
I/O (TCK)	9	E3	7	161
I/O	10	D2	8	164
I/O	11	D3	9	167
I/O	12	D1	10	170
I/O	13	E5	11	173
I/O	-	F4	12	176
I/O	-	E2	13	179
GND	14	E1	14	-
I/O	15	E4	15	182
I/O	16	F3	16	185
I/O (TMS)	17	F2	17	188
I/O	18	F5	18	191
VCC	-	F1	19	-
I/O	-	G4	20	194
I/O	-	G2	21	197
-	-	-	22*	-
I/O	19	G3	23	200
I/O	20	G6	24	203
I/O	21	G5	25	206
I/O	22	G1	26	209
I/O	23	H5	27	212
I/O	24	H7	28	215
GND	25	H1	29	-
VCC	26	H2	30	-

Pin Description	PQ208	BG225	PQ240	Boundary Scan Orde
I/O	27	H6	31	218
I/O	28	H3	32	221
I/O	29	J6	33	224
I/O	30	H4	34	227
I/O	31	J1	35	230
I/O	32	J5	36	233
-	-	-	37*	-
I/O	-	J2	38	236
I/O	-	J7	39	239
VCC	-	K1	40	-
I/O	33	J3	41	242
I/O	34	K2	42	245
I/O	35	K5	43	248
I/O	36	K3	44	251
GND	37	L1	45	-
I/O	-	K6	46	254
I/O	-	L2	47	257
I/O	38	J4	48	260
I/O	39	M2	49	263
I/O	40	L5	50	266
I/O	41	M1	51	269
I/O	42	H3	52	272
I/O	43	L3	53	275
I/O	44	M4	54	278
I/O	45	N1	55	281
I/O	46	N2	56	284
SGCK2 (I/O)	47	K4	57	287
M1	48	L4	58	290
GND	49	41	59	-
M0	50	P1	60	293†
-	51*	-	-	-
-	52*	-	-	-
-	53*	-	-	-
-	54*	-	-	-
VCC	55	R6	61	-
M2	56	R2	62	294†
PGCK2 (I/O)	57	P3	63	295
I/O (HDC)	58	M6	64	298
I/O	59	P2	65	301
I/O	60	R3	66	304
I/O	61	N3	67	307
I/O (LDC)	62	N5	68	310
I/O	63	N4	69	313
I/O	64	R4	70	316
I/O	65	P4	71	319
I/O	66	N6	72	322
I/O	-	P5	73	325
I/O	-	M5	74	328
GND	67	R5	75	-
I/O	68	M7	76	331
I/O	69	P6	77	334
I/O	70	L6	78	337
I/O	71	N7	79	340
VCC	-	-	80	-
I/O	72	P7	81	343
I/O	73	M8	82	346
-	-	-	83*	-
I/O	-	K7	84	349
I/O	-	L7	85	352
I/O	74	R7	86	355
I/O	75	N8	87	358
I/O	76	J8	88	361
I/O ($\overline{ERR}$, $\overline{INIT}$)	77	P8	89	364
VCC	78	R10	90	-

* Indicates unconnected package pins.

† Contributes only one bit (.i) to the boundary scan register.

XC4313 Pinouts (continued)

Pin Description	PQ208	BG225	PQ240	Boundary Scan Orde
GND	79	R8	91	-
I/O	80	L8	92	367
I/O	81	M9	93	370
I/O	82	P9	94	373
I/O	83	R9	95	376
I/O	84	K8	96	379
I/O	85	L9	97	382
-	-	-	98*	-
I/O	-	K9	99	385
I/O	-	N9	100	388
VCC	-	-	101	-
I/O	86	P10	102	391
I/O	87	L10	103	394
I/O	88	N10	104	397
I/O	89	K10	105	400
GND	90	R11	106	-
I/O	-	N11	107	403
I/O	-	P11	108	406
I/O	91	M10	109	409
I/O	92	P12	110	412
I/O	93	R12	111	415
I/O	94	N12	112	418
I/O	95	K12	113	421
I/O	96	P13	114	424
I/O	97	R13	115	427
I/O	98	P14	116	430
I/O	99	K13	117	433
SGCK3 (I/O)	100	M13	118	0
GND	101	R15	119	-
-	102*	-	-	-
DONE	103	R14	120	-
-	104*	-	-	-
-	105*	-	-	-
VCC	106	K15	121	-
-	107*	-	-	-
$\overline{\text{PROG}}$	108	P15	122	-
I/O (D7)	109	N14	123	439
PGCK3 (I/O)	110	L13	124	442
I/O	111	N13	125	445
I/O	112	N15	126	448
I/O	-	M11	127	451
I/O	-	M14	128	454
I/O (D6)	113	M12	129	457
I/O	114	M15	130	460
I/O	115	L11	131	463
I/O	116	J12	132	466
I/O	117	L14	133	469
I/O	118	L12	134	472
GND	119	L15	135	-
I/O	-	J13	136	475
I/O	-	K14	137	478
I/O	120	K11	138	481
I/O	121	H11	139	484
VCC	-	-	140	-
I/O (D5)	122	J14	141	487
I/O ($\overline{\text{CSO}}$)	123	H12	142	490
-	-	-	143*	-
I/O	124	J10	144	493
I/O	125	J11	145	496
I/O	126	J15	146	499
I/O	127	H13	147	502
I/O (D4)	128	J9	148	505
I/O	129	H9	149	508
VCC	130	H14	150	-

Pin Description	PQ208	BG225	PQ240	Boundary Scan Orde
GND	131	H15	151	-
I/O (D3)	132	H10	152	511
I/O ($\overline{\text{RS}}$)	133	G12	153	514
I/O	134	G14	154	517
I/O	135	G15	155	520
I/O	136	G9	156	523
I/O	137	G11	157	526
-	-	-	158*	-
I/O (D2)	138	G10	159	529
I/O	139	G13	160	532
VCC	-	-	161	-
I/O	140	F14	162	535
I/O	141	F11	163	538
I/O	-	F13	164	541
I/O	-	F10	165	544
GND	142	E15	166	-
I/O	-	E14	167	547
I/O	-	F12	168	550
I/O	143	D14	169	553
I/O	144	E12	170	556
I/O	145	D15	171	559
I/O	146	D13	172	562
I/O (D1)	147	E13	173	565
I/O ($\overline{\text{RCLK}}$-$\overline{\text{BUSY}}$/RDY)	148	C13	174	568
I/O	149	C15	175	571
I/O	150	C14	176	574
I/O (D0, DIN)	151	D10	177	577
SGCK4 (DOUT, I/O)	152	C11	178	580
CCLK	153	B15	179	-
VCC	154	F15	180	-
-	155*	-	-	-
-	156*	-	-	-
-	157*	-	-	-
-	158*	-	-	-
TDO	159	A14	181	-
GND	160	A15	182	-
I/O (A0, $\overline{\text{WS}}$)	161	C12	183	2
PGCK4 (I/O, A1)	162	C10	184	5
I/O	163	B14	185	8
I/O	164	A13	186	11
I/O (CS1, A2)	165	B13	187	14
I/O (A3)	166	B12	188	17
I/O	-	D12	189	20
I/O	-	A12	190	23
I/O	167	E11	191	26
I/O	168	D9	192	29
I/O	169	B11	193	32
I/O	170	D11	194	35
-	-	-	195*	-
GND	171	A11	196	-
I/O	172	C9	197	38
I/O	173	B10	198	41
I/O	-	E10	199	44
I/O	-	D8	200	47
VCC	-	-	201	-
I/O (A4)	174	B9	202	50
I/O (A5)	175	C8	203	53
-	-	-	204*	-
I/O	176	F9	205	56
I/O	177	E9	206	59
I/O	178	A9	207	62
I/O	179	B8	208	65
I/O (A6)	180	H8	209	68
I/O (A7)	181	G8	210	71
GND	182	A8	211	-

* Indicates unconnected package pins.
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 583 = BSCAN.UPD