XC4400 HardWire™ Array Family

Preliminary

Product Specification

Features

- Mask-programmed versions of Programmable Logic Cell Arrays FPGA
  - Specifically designed for easy XC4000/E series FPGA conversions
  - Significant cost reduction for high volume applications
  - Transparent conversion from FPGA device
  - On-chip scan-path test registers
  - High performance CMOS process
  - Meets XC4000/E series -3 speeds
  - Supports all XC4000E Select-RAM™ features
  - Low voltage versions available for 3.3 V operation
- Easy conversion with guaranteed results
  - No customer engineering resource required
  - Fully pin-for-pin compatible
  - Supports most popular package types
  - Same specifications and architecture as programmable FPGA devices
  - All nets and CLBs preserved
  - FPGA Design File used to generate production ready prototypes
  - Prototypes built on production fab line, fully tested to production specification
  - Greater than 95% fault coverage

Description

The XC4400 Series HardWire Arrays are advanced mask-programmed versions of the XC4000 programmable devices. In high-volume applications where the design is stable, the programmable FPGA devices used for prototyping and initial production can be replaced by their HardWire Array equivalents. This offers a significant cost reduction with virtually no risk or engineering resources required.

In a programmable FPGA device, the logic functions and interconnections are determined by the configuration program data, loaded and stored in internal static-memory cells. The HardWire device has the identical functional architecture as the programmed FPGA device it replaces. In the HardWire device, the logic is optimized for area but maintains the relative timing relationship.

Xilinx manufactures the HardWire device using the information from the programmed FPGA design file. Since the HardWire device is both pinout and architecturally identical to the programmable FPGA device, it is easily created without all the costly and time-consuming customer engineering activity that other semicustom solutions would require – no redesign time, no expensive and time-consuming simulation runs, no place and route, no test-vector generation. Xilinx proprietary software checks the design and maintains timing relationships as well as automatically generating test vectors.The combination of the program-

Table 1. Summary of HardWire Product Availability For Each Member of the XC4000 FPGA Family

HardWire Device	Replacement FPGA	Speed Grade	Packages*									
			PC 84	PQ 100	VQ 100	TQ 144	PQ 160	PQ 208	BG 225	PQ 240	PG 299	HQ 304
XC4403	XC4003/E	-3	√	√	√							
XC4405	XC4005/E	-3	√	√		√	√	√				
XC4406	XC4006/E	-3	√			√	√	√				
XC4408	XC4008/E	-3	√				√	√				
XC4410	XC4010/E	-3	√				√	√	√			
XC4413	XC4013/E	-3					√	√	√	√		
XC4420	XC4020/E	-3						√		√		
XC4425	XC4025/E	-3								√	√	√

* Consult factory for information if different packages or faster speed grades are required.

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mable FPGA device and the HardWire array offers the fastest and easiest way to get a new product to market, while ensuring low cost, low risk, and high-volume cost reduction.

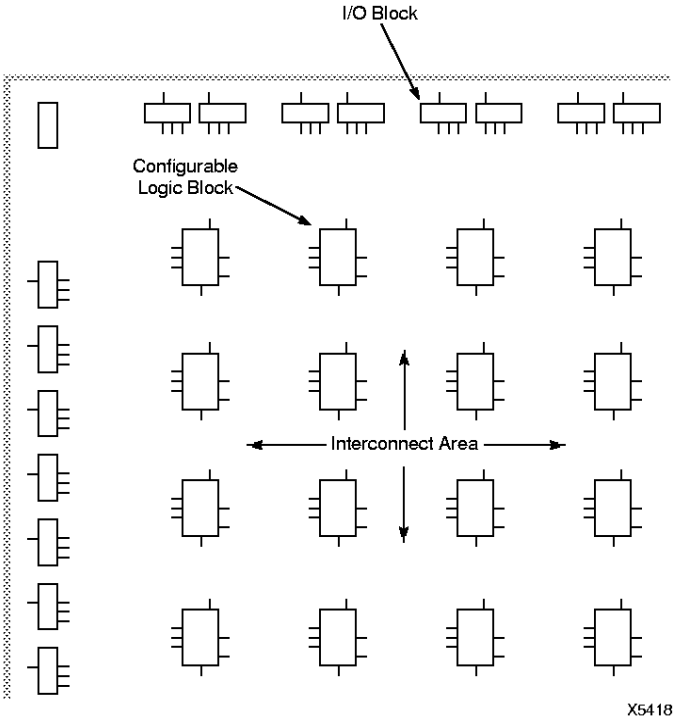

Figure 1. Logic Cell Array Structure

Architectural Overview

As shown in Figure 1, the HardWire Array has the same architecture as the programmable FPGA device it replaces. The perimeter of I/O Blocks (IOBs) provides an interface between the internal logic array and the device package pins. The array of Configurable Logic Blocks (CLBs) performs user-specified logic functions. The interconnect resources are programmed to form networks carrying logic signals among blocks, analogous to printed-circuit-board traces connecting SSI/MSI packages.

The XC4400 HardWire technology further optimizes silicon area by removing all unused logic in a CLB, and removing any unused CLBs and routing resources. In fact, all unused FPGA features are eliminated in the XC4400. However, using our DesignLock™ technology, the implementation of the CLB (including placement and routing) are maintained. This unique conversion process also eliminates the need for timing simulation. Timing is guaranteed through our Design Review process with the aid of our proprietary software.

See The Xilinx *Data Book* for more information on the XC4000 architecture.

Interconnect

User-defined interconnect resources in the device provide routing paths to connect inputs and outputs of the I/O and logic blocks into logic networks.

The speed of the interconnect paths of the HardWire Array is significantly faster, since all interconnections are fixed metal connections.

Architectural Enhancements

Compared to older array families, XC4400 HardWire arrays provide significant enhancements. Powerful system features, as listed below, are incorporated to improve system speed, device flexibility, and ease of use.

- JTAG Boundary Scan IEEE 1149.1 Boundary-scan
- Select-RAM Memory: on chip RAM with:
  – Synchronous write option
  – Dual-port RAM option

STARTUP

The STARTUP User Logic block is completely supported in the XH4400. The input pins for GSR and GTS can be tied anywhere in the design. Each of these pins can also be inverted, as in the XC4000 FPGA. Refer to Figure 1 for a detailed block diagram of the STARTUP User Logic block. Xilinx recommends the use of the STARTUP block for FPGA designs. By utilizing the GSR pin, all flip-flops in the design may be cleared. It is further recommended that the GSR input be driven directly from a device pin rather than from internal logic. This permits the design to be fully reset from an external device pin, resulting in greater testability.

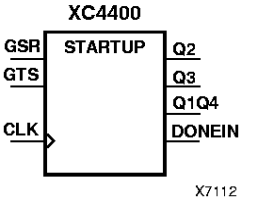

Figure 1. STARTUP User Logic Block

Similary, the GTS pin should also be connected to an external device pin so that the FPGA/HardWire may have all I/O pins at a three-state condition. This condition is often necessary for printed circuit board level manufacturing testing and is therefore a recommended design practice.

BSCAN

The XC4400 BSCAN User Logic supports most XC4000 BSCAN User Logic modes. (Since the re-programmable elements of the XC4400 have been removed from the HardWire device, the Configuration and Readback modes are not supported.) The XC4000 BSCAN macro also supports the ability to connect two additional data streams

corresponding to the USER1 and USER2 Boundary Scan instruction decodes. The HardWire Array supports this feature fully and automatically.

If Boundary Scan is intended to be used after the configuration process, then the BSCAN User logic must be instantiated in the FPGA. For more information on the usage of the BSCAN User Logic, refer to the XC4000E data sheet and the Xilinx Libraries Guide.The BSCAN User Logic block is shown in Figure 2.

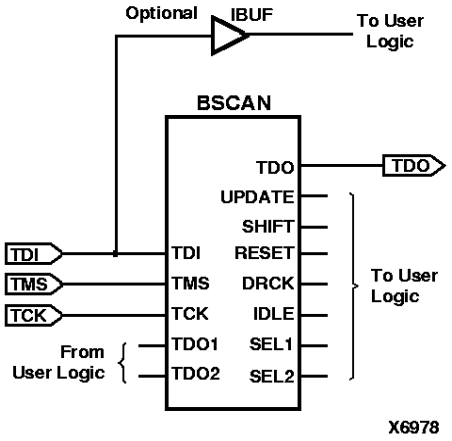

Figure 2. XC4000 BSCAN User Logic Block

Configuration Modes

XC4000E devices have six configuration modes. These modes are selected by a 3-bit input code applied to the M2, M1, and M0 inputs. These are three self-loading Master modes, two Peripheral modes, and a Serial Slave mode, which is used primarily for dasiy-chain devices.

Table 2. Configuration Modes

Mode	M2	M1	M0	CCLK	Data
Master Serial	0	0	0	output	Bit-Serial
Slave Serial	1	1	1	input	Bit-Serial
Master Parallel Up	1	0	0	output	Byte-Wide, increment from 00000
Master Parallel Down	1	1	0	output increment	Byte-Wide, from 3FFFF
Peripheral Synchronous*	0	1	1	input	Byte-Wide
Peripheral Asynchronous*	1	0	1	output	Byte-Wide
Reserved	0	1	0	–	–
Reserved	0	0	1	–	–

Note: * Synchronous Peripheral can be considered byte-wide Slave Parallel

A detailed description of each configuration mode, with timing information, is included in the XC4000 data sheet. For more information on Configuration Emulation, refer to the Design Considerations section of this Data Book.

Power Distribution

Power for the HardWire Array is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the device, dedicated V_{CC} and ground rings surround the logic array and provide power to the I/O drivers. An independent matrix of V_{CC} and ground lines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically a 0.1-µF capacitor connected near the V_{CC} and ground pins will provide adequate decoupling.

Output buffers capable of driving the specified 12-mA/24-mA loads under worst-case conditions may be capable of driving many times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads. The I/O Block output buffers have a slew-limited mode which should be used where output rise and fall times are not speed critical. Slew-limited outputs maintain their dc drive capability, but generate less external reflections and internal noise. A maximum total external capacitive load for simultaneous fast-mode switching in the same direction is 100 pF per power/ground pin pair. For slew-rate limited outputs this total is four times larger.

XC4400 Family Pin Assignments

Xilinx offers members of the XC4400 family in a variety of surface-mount package types, with pin counts from 84 to 304.

Each chip is offered in several package types to accommodate the available PC-board space and manufacturing technology. Most package types are also offered with different chips to accommodate design changes without requiring PC-board changes.

Unrestricted User-Programmable I/O Pins.

An I/O pin may be programmed by the user to be an Input or an Output pin following configuration. Before configuration is completed, these pins have an internal high-value pull-up resistor that defines the logic level as High.

Table 3. Dedicated or Special Pins on XC4400 HardWire Array

Pin Function		
	Configuration Emulation Mode	
Pin Name	**During Configuration**	**During Operation**
M0	M0	User Input (1,2)
M1	M1	User Output (1,2)
M2	M2	User Input (1,2)
CCLK	Master: Output, Slave; Input	HIGH - Internal Pull-up
$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$ Input	Global Reset Device - "Reconfigure"
DONE	DONE Output	HIGH - Internal Pull-up
HDC	HDC Output	User I/O
$\overline{\text{LDC}}$	$\overline{\text{LDC}}$ Output	User I/O
$\overline{\text{INIT}}$	Master: $\overline{\text{INIT}}$ Input	Open Drain
DIN	DIN Pin	User I/O
DOUT	DOUT Pin	User I/O

Notes:
1. User Pin is only accessible through special schematic I/O Macros
2. Pin does not have an associated IOB register(s)

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Production Test Methodology

The Xilinx XC4400 utilizes a Production Test Methodology which permits total testability of all testable faults. This is achieved through high fault coverage vectors generated by an Automatic Test Vector Generator (ATPG). The vectors are fed via both a serial and a parallel data path for the highest degree of fault observation.

One major advantage of Xilinx's test methodology is that the customer is not required to generate any production test vectors. Since this can often consume a great deal of time, Xilinx HardWire can save valuable customer engineering resources.

The user flip-flops in the design are converted into scannable elements. All flip-flops in the dedicated logic such as Configuration Emulation or Boundary Scan are also converted into scannable elements. These elements are then combined to form full-scan chains. Up to eight chains are used in order to reduce the total required test time. By using a combination of random and deterministic fault alogrithms, high fault coverage is achieved resulting in total testability of all testable faults.

ESD Considerations

The XC4400 has similar ESD protection as the XC4000 FPGA, and is able to withstand ESD up to 2,000 volts. The HardWire is manufactured in CMOS process technology, and appropriate Electro-Static Discharge (ESD) handling precautions should be followed.

3 V/5 V Considerations

The XC4400 HardWire Array can operate either as 5 volt only, or as a 3.3 volt device (part number XC4400L). See Table 4.

Table 4. 5 Volt and 3.3 Volt Operation

	Type	5 Volt Operation				3.3 Volt Operation			
		Vil (max)	Vih (min)	Vol (max)	Voh (min)	Vil (max)	Vih (min)	Vol (max)	Voh (min)
XC4400	TTL	0.80	2.00	0.40	V_{CC} -0.4				
	CMOS	1.00	3.50	0.40	V_{DD} -0.4	0.80	2.20	0.30	V_{DD} -0.3

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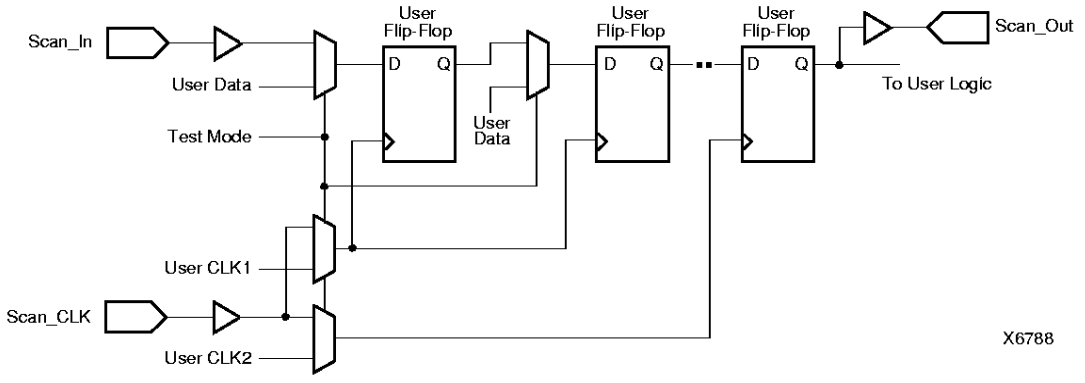

Figure 2. XC4400 Scan Chain Example

XC4403 Pinouts

Pin Description	PC84	PQ100	Bound Scan
VCC	2	92	–
I/O (A8)	3	93	32
I/O (A9)	4	94	35
I/O	–	95	38
I/O	–	96	41
I/O (A10)	5	97	44
I/O (A11)	6	98	47
–	–	–	–
I/O (A12)	7	99	50
I/O (A13)	8	100	53
–	–	–	–
–	–	–	–
I/O (A14)	9	1	56
SGCK1 (A15,I/O)	10	2	59
VCC	11	3	–
GND	12	4	–
PGCK1 (A16, I/O)	13	5	62
I/O (A17)	14	6	65
–	–	–	–
–	–	–	–
I/O (TDI)	15	7	68
I/O (TCK)	16	8	71
–	–	–	–
I/O (TMS)	17	9	74
I/O	18	10	77
I/O	–	–	80
I/O	–	11	83
I/O	19	12	86
I/O	20	13	89
GND	21	14	–
VCC	22	15	–
I/O	23	16	92
I/O	24	17	95
I/O	–	18	98
I/O	–	–	101
I/O	25	19	104
I/O	26	20	107
I/O	27	21	110
I/O	–	22	113
–	–	–	–
I/O	28	23	116
SGCK2 (I/O)	29	24	119
O (M1)	30	25	122
GND	31	26	–
I (M0)	32	27	125†
VCC	33	28	–
I (M2)	34	29	126†
PGCK2 (I/O)	35	30	127
I/O (HDC)	36	31	130
–	–	–	–
–	–	–	–
I/O	–	32	133
I/O ($\overline{\text{LDC}}$)	37	33	136
I/O	38	34	139
I/O	39	35	142
I/O	–	36	145
I/O	–	37	148
I/O	40	38	151
I/O ($\overline{\text{ERR}}$, $\overline{\text{INIT}}$)	41	39	154
VCC	42	40	–

Pin Description	PC84	PQ100	Bound Scan
GND	43	41	–
I/O	44	42	157
I/O	45	43	160
I/O	–	44	163
I/O	–	45	166
I/O	46	46	169
I/O	47	47	172
I/O	48	48	175
I/O	49	49	178
–	–	–	–
–	–	–	–
I/O	50	50	181
SGCK3 (I/O)	51	51	184
GND	52	52	–
DONE	53	53	–
VCC	54	54	–
$\overline{\text{PROG}}$	55	55	–
I/O (D7)	56	56	187
PGCK3 (I/O)	57	57	190
–	–	–	–
–	–	–	–
I/O (D6)	58	58	193
I/O	–	59	196
I/O (D5)	59	60	199
I/O ($\overline{\text{CS0}}$)	60	61	202
I/O	–	62	205
I/O	–	63	208
I/O (D4)	61	64	211
I/O	62	65	214
VCC	63	66	–
GND	64	67	–
I/O (D3)	65	68	217
I/O ($\overline{\text{RS}}$)	66	69	220
I/O	–	70	223
I/O	–	–	226
I/O (D2)	67	71	229
I/O	68	72	232
I/O (D1)	69	73	235
I/O (RCLK-$\overline{\text{BUSY}}$/RDY)	70	74	238
–	–	–	–
–	–	–	–
I/O (D0, DIN)	71	75	241
SGCK4 (DOUT, I/O)	72	76	244
CCLK	73	77	–
VCC	74	78	–
O (TDO)	75	79	–
GND	76	80	–
I/O (A0, $\overline{\text{WS}}$)	77	81	2
PGCK4 (A1, I/O)	78	82	5
–	–	–	–
–	–	–	–
I/O (CS1, A2)	79	83	8
I/O (A3)	80	84	11
I/O (A4)	81	85	14
I/O (A5)	82	86	17
I/O	–	87	20
I/O	–	88	23
I/O (A6)	83	89	26
I/O (A7)	84	90	29
GND	1	91	–

* Indicates unconnected package pins.
† Contributes only one bit (.i) to the boundary scan register.
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 247 = BSCANT.UPD

XC4405 Pinouts

Pin Description	PC84	PQ160	PQ208	Bound Scan
VCC	2	142	183	–
I/O (A8)	3	143	184	44
I/O (A9)	4	144	185	47
I/O	–	145	186	50
I/O	–	146	187	53
–	–	–	188*	–
–	–	–	189*	–
I/O (A10)	5	147	190	56
I/O (A11)	6	148	191	59
I/O	–	149	192	62
I/O	–	150	193	65
GND	–	151	194	–
–	–	–	195*	–
–	–	–	196*	–
–	–	152*	197*	–
–	–	153*	198*	–
I/O (A12)	7	154	199	68
I/O (A13)	8	155	200	71
–	–	–	–	–
I/O	–	156	201	74
I/O	–	157	202	77
I/O (A14)	9	158	203	80
SGCK1 (A15, I/O)	10	159	204	83
VCC	11	160	205	–
–	–	–	206*	–
–	–	–	207*	–
–	–	–	208*	–
–	–	–	1*	–
GND	12	1	2	–
–	–	–	3*	–
PGCK1 (A16, I/O)	13	2	4	86
I/O (A17)	14	3	5	89
I/O	–	4	6	92
I/O	–	5	7	95
–	–	–	–	–
I/O (TDI)	15	6	8	98
I/O (TCK)	16	7	9	101
–	–	8*	10*	–
–	–	9*	11*	–
–	–	–	12*	–
–	–	–	13*	–
GND	–	10	14	–
I/O	–	11	15	104
I/O	–	12	16	107
I/O (TMS)	17	13	17	110
I/O	18	14	18	113
–	–	–	19*	–
–	–	–	20*	–
I/O	–	15	21	116
I/O	–	16	22	119
I/O	19	17	23	122
I/O	20	18	24	125
GND	21	19	25	–
VCC	22	20	26	–
I/O	23	21	27	128
I/O	24	22	28	131
I/O	–	23	29	134
I/O	–	24	30	137
–	–	–	31*	–
–	–	–	32*	–
I/O	25	25	33	140
I/O	26	26	34	143
I/O	–	27	35	146
I/O	–	28	36	149
GND	–	29	37	–
–	–	–	38*	–
–	–	–	39*	–
–	–	30*	40*	–
–	–	31*	41*	–
I/O	27	32	42	152
I/O	–	33	43	155
I/O	–	34	44	158
I/O	–	35	45	161
–	–	–	–	–
I/O	28	36	46	164
SGCK2 (I/O)	29	37	47	167
O (M1)	30	38	48	170
GND	31	39	49	–
I (M0)	32	40	50	173†
–	–	–	51*	–
–	–	–	52*	–
–	–	–	53*	–
–	–	–	54*	–
VCC	33	41	55	–
I (M2)	34	42	56	174†
PGCK2 (I/O)	35	43	57	175
I/O (HDC)	36	44	58	178
I/O	–	45	59	181
–	–	–	–	–
I/O	–	46	60	184
I/O	–	47	61	187
I/O ($\overline{LDC}$)	37	48	62	190
–	–	49*	63*	–
–	–	50*	64*	–
–	–	–	65*	–
–	–	–	66*	–
GND	–	51	67	–
I/O	–	52	68	193
I/O	–	53	69	196
I/O	38	54	70	199
I/O	39	55	71	202
–	–	–	72*	–
–	–	–	73*	–
I/O	–	56	74	205
I/O	–	57	75	208
I/O	40	58	76	211
I/O ($\overline{ERR}$, $\overline{INIT}$)	41	59	77	214
VCC	42	60	78	–
GND	43	61	79	–
I/O	44	62	80	217
I/O	45	63	81	220
I/O	–	64	82	223
I/O	–	65	83	226
–	–	–	84*	–
–	–	–	85*	–
I/O	46	66	86	229
I/O	47	67	87	232
I/O	–	68	88	235
I/O	–	69	89	238
GND	–	70	90	–
–	–	–	91*	–
–	–	–	92*	–
–	–	71*	93*	–
–	–	72*	94*	–
I/O	48	73	95	241
I/O	49	74	96	244
I/O	–	75	97	247
I/O	–	76	98	250
I/O	50	77	99	253
SGCK3 (I/O)	51	78	100	256
GND	52	79	101	–
–	–	–	102*	–
DONE	53	80	103	–
–	–	–	104*	–
–	–	–	105*	–
VCC	54	81	106	–
–	–	–	107*	–
$\overline{PROG}$	55	82	108	–
I/O (D7)	56	83	109	259
PGCK3 (I/O)	57	84	110	262
I/O	–	85	111	265
–	–	–	–	–
I/O	–	86	112	268
I/O (D6)	58	87	113	271
I/O	–	88	114	274
–	–	89*	115*	–
–	–	89*	115*	–
–	–	90†	116*	–
–	–	–	117*	–
–	–	–	118*	–
GND	–	91	119	–
I/O	–	92	120	277
I/O	–	93	121	280
I/O (D5)	59	94	122	283
I/O (CS0)	60	95	123	286
–	–	–	124*	–
–	–	–	125*	–
I/O	–	96	126	289
I/O	–	97	127	292
I/O (D4)	61	98	128	295
I/O	62	99	129	298
VCC	63	100	130	–
GND	64	101	131	–
I/O (D3)	65	102	132	301
I/O ($\overline{RS}$)	66	103	133	304
I/O	–	104	134	307
I/O	–	105	135	310
–	–	–	136*	–
–	–	–	137*	–
I/O (D2)	67	106	138	313
I/O	68	107	139	316
I/O	–	108	140	319
I/O	–	109	141	322
GND	–	110	142	–
–	–	–	143*	–
–	–	–	144*	–
–	–	111*	145*	–
–	–	112*	146*	–
I/O (D1)	69	113	147	325
I/O (RCLK-$\overline{BUSY}$/RDY)	70	114	148	328
I/O	–	115	149	331
–	–	–	–	–
I/O	–	116	150	334
I/O (D0, DIN)	71	117	151	337
SGCK4 (DOUT, I/O)	72	118	152	340
CCLK	73	119	153	–
VCC	74	120	154	–
–	–	–	155*	–
–	–	–	156*	–
–	–	–	157*	–
–	–	–	158*	–
O (TDO)	75	121	159	–
GND	76	122	160	–
I/O (A0, $\overline{WS}$)	77	123	161	2
PGCK4 (A1, I/O)	78	124	162	5
I/O	–	125	163	8
–	–	–	–	–
I/O	–	126	164	11
I/O (CS1, A2)	79	127	165	14
I/O (A3)	80	128	166	17
–	–	129*	167*	–
–	–	130*	168*	–
–	–	–	169*	–
–	–	–	170*	–
GND	–	131	171	–
I/O	–	132	172	20
I/O	–	133	173	23
I/O (A4)	81	134	174	26
I/O (A5)	82	135	175	29
–	–	–	176*	–
–	–	136*	177*	–
I/O	–	137	178	32
I/O	–	138	179	35
I/O (A6)	83	139	180	38
I/O (A7)	84	140	181	41
GND	1	141	182	–

* Indicates unconnected package pins.

† Contributes only one bit (.i) to the boundary scan register.

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 343 = BSCANT.UPD

XC4406 Pinouts

Pin Description	PC84	PQ160	PQ208	Boundary Scan Order
VCC	2	142	183	-
I/O (A8)	3	143	184	50
I/O (A9)	4	144	185	53
I/O	-	145	186	56
I/O	-	146	187	59
-	-	-	188*	-
-	-	-	189*	-
I/O (A10)	5	147	190	62
I/O (A11)	6	148	191	65
I/O	-	149	192	68
I/O	-	150	193	71
GND	-	151	194	-
-	-	-	195*	-
-	-	-	196*	-
I/O	-	152	197	74
I/O	-	153	198	77
I/O (A12)	7	154	199	80
I/O (A13)	8	155	200	83
I/O	-	156	201	86
I/O	-	157	202	89
I/O (A14)	9	158	203	92
SGCK1 (A15, I/O)	10	159	204	95
VCC	11	160	205	-
-	-	-	206*	-
-	-	-	207*	-
-	-	-	208*	-
-	-	-	1*	-
GND	12	1	2	-
-	-	-	3*	-
PGCK1 (A16, I/O)	13	2	4	98
I/O (A17)	14	3	5	101
I/O	-	4	6	104
I/O	-	5	7	107
I/O (TDI)	15	6	8	110
I/O (TCK)	16	7	9	113
I/O	-	8	10	116
I/O	-	9	11	119
-	-	-	12*	-
-	-	-	13*	-
GND	-	10	14	-
I/O	-	11	15	122
I/O	-	12	16	125
I/O (TMS)	17	13	17	128
I/O	18	14	18	131
-	-	-	19*	-
-	-	-	20*	-
I/O	-	15	21	134
I/O	-	16	22	137
I/O	19	17	23	140
I/O	20	18	24	143
GND	21	19	25	-
VCC	22	20	26	-

Pin Description	PC84	PQ160	PQ208	Boundary Scan Order
I/O	23	21	27	146
I/O	24	22	28	149
I/O	-	23	29	152
I/O	-	24	30	155
-	-	-	31*	-
-	-	-	32*	-
I/O	25	25	33	158
I/O	26	26	34	161
I/O	-	27	35	164
I/O	-	28	36	167
GND	-	29	37	-
-	-	-	38*	-
-	-	-	39*	-
I/O	-	30	40	170
I/O	-	31	41	173
I/O	27	32	42	176
I/O	-	33	43	179
I/O	-	34	44	182
I/O	-	35	45	185
I/O	28	36	46	188
SGCK2 (I/O)	29	37	47	191
M1	30	38	48	194
GND	31	39	49	-
M0	32	40	50	197†
-	-	-	51*	-
-	-	-	52*	-
-	-	-	53*	-
-	-	-	54*	-
VCC	33	41	55	-
M2	34	42	56	198†
PGCK2 (I/O)	35	43	57	199
I/O (HDC)	36	44	58	202
I/O	-	45	59	205
I/O	-	46	60	208
I/O	-	47	61	211
I/O ($\overline{\text{LDC}}$)	37	48	62	214
I/O	-	49	63	217
I/O	-	50	64	220
-	-	-	65*	-
-	-	-	66*	-
GND	-	51	67	-
I/O	-	52	68	223
I/O	-	53	69	226
I/O	38	54	70	229
I/O	39	55	71	232
-	-	-	72*	-
-	-	-	73*	-
I/O	-	56	74	235
I/O	-	57	75	238
I/O	40	58	76	241
I/O ($\overline{\text{ERR}}$,$\overline{\text{INIT}}$)	41	59	77	244
VCC	42	60	78	-

* Indicates unconnected package pins.

†Contributes only one bit (.i) to the boundary scan register.

XC4406 Pinouts (continued)

Pin Description	PC84	PQ160	PQ208	Boundary Scan Order
GND	43	61	79	-
I/O	44	62	80	247
I/O	45	63	81	250
I/O	-	64	82	253
I/O	-	65	83	256
-	-	-	84*	-
-	-	-	85*	-
I/O	46	66	86	259
I/O	47	67	87	262
I/O	-	68	88	265
I/O	-	69	89	268
GND	-	70	90	-
-	-	-	91*	-
-	-	-	92*	-
I/O	-	71	93	271
I/O	-	72	94	274
I/O	48	73	95	277
I/O	49	74	96	280
I/O	-	75	97	283
I/O	-	76	98	286
I/O	50	77	99	289
SGCK3 (I/O)	51	78	100	292
GND	52	79	101	-
-	-	-	102*	-
DONE	53	80	103	-
-	-	-	104*	-
-	-	-	105*	-
VCC	54	81	106	-
-	-	-	107*	-
$\overline{\text{PROG}}$	55	82	108	-
I/O (D7)	56	83	109	295
PGCK3 (I/O)	57	84	110	298
I/O	-	85	111	301
I/O	-	86	112	304
I/O (D6)	58	87	113	307
I/O	-	88	114	310
I/O	-	89	115	313
I/O	-	90	116	316
-	-	-	117*	-
-	-	-	118*	-
GND	-	91	119	-
I/O	-	92	120	319
I/O	-	93	121	322
I/O (D5)	59	94	122	325
I/O ($\overline{\text{CS0}}$)	60	95	123	328
-	-	-	124*	-
-	-	-	125*	-
I/O	-	96	126	331
I/O	-	97	127	334
I/O (D4)	61	98	128	337
I/O	62	99	129	340
VCC	63	100	130	-

* Indicates unconnected package pins.

Pin Description	PC84	PQ160	PQ208	Boundary Scan Order
GND	64	101	131	-
I/O (D3)	65	102	132	343
I/O ($\overline{\text{RS}}$)	66	103	133	346
I/O	-	104	134	349
I/O	-	105	135	352
-	-	-	136*	-
-	-	-	137*	-
I/O (D2)	67	106	138	355
I/O	68	107	139	358
I/O	-	108	140	361
I/O	-	109	141	364
GND	-	110	142	-
-	-	-	143*	-
-	-	-	144*	-
I/O	-	111	145	367
I/O	-	112	146	370
I/O (D1)	69	113	147	373
I/O (RCLK-BUSY/$\overline{\text{RDY}}$)	70	114	148	376
I/O	-	115	149	379
I/O	-	116	150	382
I/O (D0, DIN)	71	117	151	385
SGCK4 (DOUT, I/O)	72	118	152	388
CCLK	73	119	153	-
VCC	74	120	154	-
-	-	-	155*	-
-	-	-	156*	-
-	-	-	157*	-
-	-	-	158*	-
TDO	75	121	159	-
GND	76	122	160	-
I/O (A0, $\overline{\text{WS}}$)	77	123	161	2
PGCK4 (I/O, A1)	78	124	162	5
I/O	-	125	163	8
I/O	-	126	164	11
I/O (CS1,A2)	79	127	165	14
I/O (A3)	80	128	166	17
I/O	-	129	167	20
I/O	-	130	168	23
-	-	-	169*	-
-	-	-	170*	-
GND	-	131	171	-
I/O	-	132	172	26
I/O	-	133	173	29
I/O (A4)	81	134	174	32
I/O (A5)	82	135	175	35
-	-	-	176*	-
-	-	136*	177*	-
I/O	-	137	178	38
I/O	-	138	179	41
I/O (A6)	83	139	180	44
I/O (A7)	84	140	181	47
GND	1	141	182	-

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 0 = TDO.O
Boundary Scan Bit 391 = BSCAN.UPD

XC4408 Pinouts

Pin Description	PC84	PQ160	PQ208	Boundary Scan Order
VCC	2	142	183	–
I/O (A8)	3	143	184	56
I/O (A9)	4	144	185	59
I/O	–	145	186	62
I/O	–	146	187	65
I/O	–	–	188	68
I/O	–	–	189	71
I/O (A10)	5	147	190	74
I/O (A11)	6	148	191	77
I/O	–	149	192	80
I/O	–	150	193	83
GND	–	151	194	–
–	–	–	195*	–
–	–	–	196*	–
I/O	–	152	197	86
I/O	–	153	198	89
I/O (A12)	7	154	199	92
I/O (A13)	8	155	200	95
I/O	–	156	201	98
–	–	–	–	–
I/O	–	157	202	101
I/O (A14)	9	158	203	104
SGCK1 (A15, I/O)	10	159	204	107
VCC	11	160	205	–
–	–	–	206*	–
–	–	–	207*	–
–	–	–	208*	–
–	–	–	1*	–
GND	12	1	2	–
–	–	–	3*	–
PGCK1 (A16, I/O)	13	2	4	110
I/O (A17)	14	3	5	113
I/O	–	4	6	116
–	–	–	–	–
I/O	–	5	7	119
I/O (TDI)	15	6	8	122
I/O (TCK)	16	7	9	125
I/O	–	8	10	128
I/O	–	9	11	131
–	–	–	12*	–
–	–	–	13*	–
GND	–	10	14	–
I/O	–	11	15	134
I/O	–	12	16	137
I/O (TMS)	17	13	17	140
I/O	18	14	18	143
I/O	–	–	19	146
I/O	–	–	20	149
I/O	–	15	21	152
I/O	–	16	22	155
I/O	19	17	23	158
I/O	20	18	24	161
GND	21	19	25	–

Pin Description	PC84	PC160	PQ208	Boundary Scan Order
VCC	22	20	26	–
I/O	23	21	27	164
I/O	24	22	28	167
I/O	–	23	29	170
I/O	–	24	30	173
I/O	–	–	31	176
I/O	–	–	32	179
I/O	25	25	33	182
I/O	26	26	34	185
I/O	–	27	35	188
I/O	–	28	36	191
GND	–	29	37	–
–	–	–	38*	–
–	–	–	39*	–
I/O	–	30	40	194
I/O	–	31	41	197
I/O	27	32	42	200
I/O	–	33	43	203
I/O	–	34	44	206
I/O	–	35	45	209
I/O	28	36	46	212
SGCK2 (I/O)	29	37	47	215
M1	30	38	48	218
GND	31	39	49	–
M0	32	40	50	221†
–	–	–	51*	–
–	–	–	52*	–
–	–	–	53*	–
–	–	–	54*	–
VCC	33	41	55	–
M2	34	42	56	222†
PGCK2 (I/O)	35	43	57	223
I/O (HDC)	36	44	58	226
–	–	–	–	–
I/O	–	45	59	229
I/O	–	46	60	232
I/O	–	47	61	235
I/O (LDC)	37	48	62	238
I/O	–	49	63	241
I/O	–	50	64	244
–	–	–	65*	–
–	–	–	66*	–
GND	–	51	67	–
I/O	–	52	68	247
I/O	–	53	69	250
I/O	38	54	70	253
I/O	39	55	71	256
I/O	–	–	72	259
I/O	–	–	73	262
I/O	–	56	74	265
I/O	–	57	75	268
I/O	40	58	76	271
I/O ($\overline{ERR}$, $\overline{INIT}$)	41	59	77	274
VCC	42	60	78	–

* Indicates unconnected package pins.

† Contributes only one bit (.i) to the boundary scan register.

XC4408 Pinouts (continued)

Pin Description	PC84	PQ160	PQ208	Boundary Scan Order
GND	43	61	79	–
I/O	44	62	80	277
I/O	45	63	81	280
I/O	–	64	82	283
I/O	–	65	83	286
I/O	–	–	84	289
I/O	–	–	85	292
I/O	46	66	86	295
I/O	47	67	87	298
I/O	–	68	88	301
I/O	–	69	89	304
GND	–	70	90	–
–	–	–	91*	–
–	–	–	92*	–
I/O	–	71	93	307
I/O	–	72	94	310
I/O	48	73	95	313
I/O	49	74	96	316
I/O	–	75	97	319
I/O	–	76	98	322
I/O	50	77	99	325
SGCK3 (I/O)	51	78	100	328
GND	52	79	101	–
–	–	–	102*	–
DONE	53	80	103	–
–	–	–	104*	–
–	–	–	105*	–
VCC	54	81	106	–
–	–	–	107*	–
$\overline{\text{PROG}}$	55	82	108	–
I/O (D7)	56	83	109	331
PGCK3 (I/O)	57	84	110	334
–	–	–	–	–
I/O	–	85	111	337
I/O	–	86	112	340
I/O (D6)	58	87	113	343
I/O	–	88	114	346
I/O	–	89	115	349
I/O	–	90	116	352
–	–	–	117*	–
–	–	–	118*	–
GND	–	91	119	–
I/O	–	92	120	355
I/O	–	93	121	358
I/O (D5)	59	94	122	361
I/O ($\overline{\text{CSO}}$)	60	95	123	364
I/O	–	–	124	367
I/O	–	–	125	370
I/O	–	96	126	373
I/O	–	97	127	376
I/O (D4)	61	98	128	379
I/O	62	99	129	382
VCC	63	100	130	
GND	64	101	131	

Pin Description	PC84	PQ160	PQ208	Boundary Scan Order
I/O (D3)	65	102	132	385
I/O ($\overline{\text{RS}}$)	66	103	133	388
I/O	–	104	134	391
I/O	–	105	135	394
I/O	–	–	136	397
I/O	–	–	137	400
I/O (D2)	67	106	138	403
I/O	68	107	139	406
I/O	–	108	140	409
I/O	–	109	141	412
GND	–	110	142	–
–	–	–	143*	–
–	–	–	144*	–
I/O	–	111	145	415
I/O	–	112	146	418
I/O (D1)	69	113	147	421
I/O (RCLK-$\overline{\text{BUSY}}$/RDY)	70	114	148	424
I/O	–	115	149	427
I/O	–	116	150	430
I/O (D0, DIN)	71	117	151	433
SGCK4 (DOUT, I/O)	72	118	152	436
CCLK	73	119	153	–
VCC	74	120	154	–
–	–	–	155*	–
–	–	–	156*	–
–	–	–	157*	–
–	–	–	158*	–
TDO	75	121	159	–
GND	76	122	160	–
I/O (A0, $\overline{\text{WS}}$)	77	123	161	2
PGCK4 (I/O,A1)	78	124	162	5
–	–	–	–	–
I/O	–	125	163	8
I/O	–	126	164	11
I/O (CS1, A2)	79	127	165	14
I/O (A3)	80	128	166	17
I/O	–	129	167	20
I/O	–	130	168	23
–	–	–	169*	–
–	–	–	170*	–
GND	–	131	171	–
I/O	–	132	172	26
I/O	–	133	173	29
I/O (A4)	81	134	174	32
I/O (A5)	82	135	175	35
I/O	–	–	176	38
I/O	–	136	177	41
I/O	–	137	178	44
I/O	–	138	179	47
I/O (A6)	83	139	180	50
I/O (A7)	84	140	181	53
GND	1	141	182	–

* Indicates unconnected package pins.

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 0 = TDO.O
Boundary Scan Bit 391 = BSCAN.UPD

XC4410 Pinouts

Pin Description	PC84	PQ160	PQ208	Boundary Scan Order
VCC	2	142	183	-
I/O (A8)	3	143	184	62
I/O (A9)	4	144	185	65
I/O	-	145	186	68
I/O	-	146	187	71
I/O	-	-	188	74
I/O	-	-	189	77
I/O (A10)	5	147	190	80
I/O (A11)	6	148	191	83
I/O	-	149	192	86
I/O	-	150	193	89
GND	-	151	194	-
I/O	-	-	195	92
I/O	-	-	196	96
I/O	-	152	197	98
I/O	-	153	198	101
I/O (A12)	7	154	199	104
I/O (A13)	8	155	200	107
I/O	-	156	201	110
I/O	-	157	202	113
I/O (A14)	9	158	203	116
SGCK1 (A15, I/O)	10	159	204	119
VCC	11	160	205	-
-	-	-	206*	-
-	-	-	207*	-
-	-	-	208*	-
-	-	-	1*	-
GND	12	1	2	-
-	-	-	3*	-
PGCK1 (A16, I/O)	13	2	4	122
I/O (A17)	14	3	5	125
I/O	-	4	6	128
I/O	-	5	7	131
I/O (TDI)	15	6	8	134
I/O (TCK)	16	7	9	137
I/O	-	8	10	140
I/O	-	9	11	143
I/O	-	-	12	146
I/O	-	-	13	149
GND	-	10	14	-
I/O	-	11	15	152
I/O	-	12	16	155
I/O (TMS)	17	13	17	158
I/O	18	14	18	161
I/O	-	-	19	164
I/O	-	-	20	167
I/O	-	15	21	170
I/O	-	16	22	173
I/O	19	17	23	176
I/O	20	18	24	179
GND	21	19	25	-
VCC	22	20	26	-
I/O	23	21	27	182
I/O	24	22	28	185
I/O	-	23	29	188
I/O	-	24	30	191
I/O	-	-	31	194
I/O	-	-	32	197
I/O	25	25	33	200
I/O	26	26	34	203
I/O	-	27	35	206
I/O	-	28	36	209
GND	-	29	37	-
I/O	-	-	38	212
I/O	-	-	39	215
I/O	-	30	40	218
I/O	-	31	41	221
I/O	27	32	42	224
I/O	-	33	43	227
I/O	-	34	44	230
I/O	-	35	45	233
I/O	28	36	46	236
SGCK2 (I/O)	29	37	47	239
M1	30	38	48	242
GND	31	39	49	-
M0	32	40	50	245†
-	-	-	51*	-
-	-	-	52*	-
-	-	-	53*	-
-	-	-	54*	-
VCC	33	41	55	-
M2	34	42	56	246†
PGCK2 (I/O)	35	43	57	247
I/O (HDC)	36	44	58	250
I/O	-	45	59	253
I/O	-	46	60	256
I/O	-	47	61	259
I/O (LDC)	37	48	62	262
I/O	-	49	63	265
I/O	-	50	64	268
I/O	-	-	65	271
I/O	-	-	66	274
GND	-	51	67	-
I/O	-	52	68	277
I/O	-	53	69	280
I/O	38	54	70	283
I/O	39	55	71	286
I/O	-	-	72	289
I/O	-	-	73	291
I/O	-	56	74	295
I/O	-	57	75	298
I/O	40	58	76	301
I/O ($\overline{\text{ERR}}$, $\overline{\text{INIT}}$)	41	59	77	304
VCC	42	60	78	-
GND	43	61	79	-
I/O	44	62	80	307
I/O	45	63	81	310
I/O	-	64	82	313
I/O	-	65	83	316
I/O	-	-	84	319
I/O	-	-	85	322
I/O	46	66	86	325

* Indicates unconnected package pins.

† Contributes only one bit (.i) to the boundary scan register.

XC4410 Pinouts (continued)

Pin Description	PC84	PQ160	PQ208	Boundary Scan Order
I/O	47	67	87	328
I/O	-	68	88	331
I/O	-	69	89	334
GND	-	70	90	-
I/O	-	-	91	337
I/O	-	-	92	340
I/O	-	71	93	343
I/O	-	72	94	346
I/O	48	73	95	349
I/O	49	74	96	352
I/O	-	75	97	355
I/O	-	76	98	358
I/O	50	77	99	361
SGCK3 (I/O)	51	78	100	364
GND	52	79	101	-
-	-	-	102*	-
DONE	53	80	103	-
-	-	-	104*	-
-	-	-	105*	-
VCC	54	81	106	-
-	-	-	107*	-
$\overline{\text{PROG}}$	55	82	108	-
I/O (D7)	56	83	109	367
PGCK3 (I/O)	57	84	110	370
I/O	-	85	111	373
I/O	-	86	112	376
I/O (D6)	58	87	113	379
I/O	-	88	114	382
I/O	-	89	115	385
I/O	-	90	116	388
I/O	-	-	117	391
I/O	-	-	118	394
GND	-	91	119	-
I/O	-	92	120	397
I/O	-	93	121	400
I/O (D5)	59	94	122	403
I/O ($\overline{\text{CSO}}$)	60	95	123	406
I/O	-	-	124	409
I/O	-	-	125	412
I/O	-	96	126	415
I/O	-	97	127	418
I/O (D4)	61	98	128	421
I/O	62	99	129	424
VCC	63	100	130	-
GND	64	101	131	-
I/O (D3)	65	102	132	427
I/O ($\overline{\text{RS}}$)	66	103	133	430
I/O	-	104	134	433
I/O	-	105	135	436
I/O	-	-	136	439
I/O	-	-	137	442
I/O (D2)	67	106	138	445
I/O	68	107	139	448
I/O	-	108	140	451
I/O	-	109	141	454
GND	-	110	142	-
I/O	-	-	143	457

Pin Description	PC84	PQ160	PQ208	Boundary Scam Order
I/O	-	-	144	460
I/O	-	111	145	463
I/O	-	112	146	466
I/O (D1)	69	113	147	469
I/O ($\overline{\text{RCLK}}$-$\overline{\text{BUSY}}$/RDY)	70	114	148	472
I/O	-	115	149	475
I/O	-	116	150	478
I/O (D0, DIN)	71	117	151	481
SGCK4 (DOUT, I/O)	72	118	152	484
CCLK	73	119	153	-
VCC	74	120	154	-
-	-	-	155*	-
-	-	-	156*	-
-	-	-	157*	-
-	-	-	158*	-
TD0	75	121	159	-
GND	76	122	160	-
I/O (A0, $\overline{\text{WS}}$)	77	123	161	2
PGCK4 (I/O, A1)	78	124	162	5
I/O	-	125	163	8
I/O	-	126	164	11
I/O (CS1, A2)	79	127	165	14
I/O (A3)	80	128	166	17
I/O	-	129	167	20
I/O	-	130	168	23
I/O	-	-	169	26
I/O	-	-	170	29
GND	-	131	171	-
I/O	-	132	172	32
I/O	-	133	173	35
I/O (A4)	81	134	174	38
I/O (A5)	82	135	175	41
I/O	-	-	176	44
I/O	-	136	177	47
I/O	-	137	178	50
I/O	-	138	179	53
I/O (A6)	83	139	180	56
I/O (A7)	84	140	181	59
GND	1	141	182	-

* Indicates unconnected package pins.
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 0 = TDO.O
Boundary Scan Bit 391 = BSCAN.UPD

BG225 Pinouts

BG225 Pin	XC4410	XC4413
R1	VCC	VCC
R2	I/O, PGCK2	I/O, PGCK2
R3	I/O	I/O
R4	I/O	I/O
R5	I/O	I/O
R6	I/O	I/O
R7	I/O	I/O
R8	VCC	I/O
R9	I/O	I/O
R10	N.C.	I/O
R11	I/O	I/O
R12	I/O	I/O
R13	I/O	I/O
R14	I/O	I/O
R15	VCC	VCC
P1	I/O, SCGK2	I/O, SCGK2
P2	I (M0)	I (M0)
P3	I/O,(HDC)	I/O,(HDC)
P4	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)
P5	N.C.	I/O
P6	I/O	I/O
P7	N.C.	I/O
P8	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)
P9	I/O	I/O
P10	N.C.	I/O
P11	I/O	I/O
P12	I/O	I/O
P13	I/O	I/O
P14	DONE	DONE
P15	I/O (D7)	I/O (D7)
N1	I/O	I/O
N2	I/O	I/O
N3	O (M1)	O (M1)
N4	I/O	I/O
N5	I/O	I/O
N6	I/O	I/O
N7	N.C.	I/O
N8	I/O	I/O
N9	I/O	I/O
N10	I/O	I/O
N11	N.C.	I/O
N12	I/O	I/O
N13	I/O, SGCK3	I/O, SGCK3
N14	I/O, PGCK3	I/O, PGCK3
N15	N.C.	I/O
M1	I/O	I/O
M2	I/O	I/O
M3	I/O	I/O
M4	I (M2)	I (M2)
M5	I/O	I/O
M6	I/O	I/O
M7	I/O	I/O
M8	GND	GND
M9	I/O	I/O
M10	N.C.	I/O
M11	I/O	I/O
M12	$\overline{PROGRAM}$	$\overline{PROGRAM}$
M13	I/O	I/O
M14	N.C.	I/O

BG225 Pin	XC4410	XC4413
M15	I/O	I/O
L1	I/O	I/O
L2	N.C.	I/O
L3	I/O	I/O
L4	I/O	I/O
L5	I/O	I/O
L6	N.C.	I/O
L7	I/O	I/O
L8	I/O	I/O
L9	I/O	I/O
L10	I/O	I/O
L11	I/O	I/O
L12	I/O	I/O
L13	I/O	I/O
L14	I/O	I/O
L15	N.C.	I/O
K1	N.C.	I/O
K2	I/O	I/O
K3	I/O	I/O
K4	N.C.	I/O
K5	I/O	I/O
K6	I/O	I/O
K7	I/O	I/O
K8	GND	GND
K9	I/O	I/O
K10	I/O	I/O
K11	I/O	I/O
K12	N.C.	I/O
K13	I/O	I/O
K14	I/O	I/O
K15	I/O (D5)	I/O (D5)
J1	I/O	I/O
J2	I/O	I/O
J3	I/O	I/O
J4	I/O	I/O
J5	N.C.	I/O
J6	I/O	I/O
J7	GND	GND
J8	GND	GND
J9	GND	GND
J10	I/O (D6)	I/O (D6)
J11	I/O	I/O
J12	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)
J13	I/O	I/O
J14	I/O	I/O
J15	I/O	I/O
H1	VCC	VCC
H2	GND	GND
H3	I/O	I/O
H4	I/O	I/O
H5	I/O	I/O
H6	GND	GND
H7	GND	GND
H8	GND	GND
H9	GND	GND
H10	GND	GND
H11	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)
H12	I/O (D3)	I/O (D3)
L1	I/O (D4)	I/O (D4)

BG225 Pinouts (continued)

BG225 Pin	XC4410	XC4413
H14	I/O	I/O
H15	VCC	VCC
G1	I/O	I/O
G2	I/O	I/O
G3	I/O	I/O
G4	I/O	I/O
G5	I/O	I/O
G6	I/O	I/O
G7	I/O	I/O
G8	I/O	I/O
G9	I/O	I/O
G10	N.C.	N.C.
G11	I/O (D2)	I/O (D2)
G12	I/O	I/O
G13	I/O	I/O
G14	I/O	I/O
G15	I/O	I/O
F1	N.C.	N.C.
F2	N.C.	N.C.
F3	I/O	I/O
F4	I/O, TMS	I/O, TMS
F5	I/O	I/O
F6	I/O	I/O
F7	N.C.	N.C.
F8	GND	GND
F9	N.C.	N.C.
F10	I/O (D0, DIN)	I/O (D0, DIN)
F11	I/O	I/O
F12	N.C.	N.C.
F13	I/O	I/O
F14	I/O	I/O
F15	I/O	I/O
E1	I/O	I/O
E2	N.C.	N.C.
E3	N.C.	N.C.
E4	I/O	I/O
E5	I/O	I/O
E6	I/O	I/O
E7	I/O	I/O
E8	I/O (A8)	I/O (A8)
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O (D1)	I/O (D1)
E13	I/O	I/O
E14	N.C.	N.C.
E15	N.C.	N.C.
D1	I/O	I/O
D2	I/O	I/O
D3	I/O, TDI	I/O, TDI
D4	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
D5	I/O (A13)	I/O (A13)
D6	I/O	I/O
D7	I/O	I/O
D8	VCC	VCC
D9	I/O (A5)	I/O (A5)
D10	I/O	I/O
D11	N.C.	N.C.
D12	GND	GND
D13	I/O	I/O
D14	I/O	I/O
C1	I/O, TCK	I/O, TCK
C2	I/O	I/O
C3	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)
C4	N.C.	I/O
C5	I/O	I/O
C6	N.C.	I/O
C7	I/O	I/O
C8	I/O (A6)	I/O (A6)
C9	I/O	I/O
C10	N.C.	I/O
C11	I/O	I/O
C12	I/O	I/O
C13	CCLK	CCLK
C14	I/O	I/O
C15	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)
B1	I/O (A17)	I/O (A17)
B2	VCC	VCC
B3	I/O	I/O
B4	I/O (A12)	I/O (A12)
B5	I/O	I/O
B6	I/O (A11)	I/O (A11)
B7	I/O (A9)	I/O (A9)
B8	I/O (A7)	I/O (A7)
B9	I/O	I/O
B10	N.C.	I/O
B11	I/O	I/O
B12	I/O (A3)	I/O (A3)
B13	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)
B14	VCC	VCC
B15	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)
A1	GND	GND
A2	I/O (A14)	I/O (A14)
A3	N.C.	I/O
A4	I/O	I/O
A5	I/O	I/O
A6	I/O (A10)	I/O (A10)
A7	I/O	I/O
A8	GND	GND
A9	I/O	I/O
A10	I/O (A4)	I/O (A4)
A11	I/O	I/O
A12	I/O	I/O
A13	I/O (CS1, A2)	I/O (CS1, A2)
A14	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)
A15	0, TDO	0, TDO

2/28/96

Note: Shade should be taken into account when designing PC boards, in case of future replacement by different devices.

Note: Viewed from bottom side, the package pins start at the top row and go from the left edge to the right edge. Viewed from the top side, the pins start at the top row and go from the right edge to the left edge.

BG225 Pinouts (continued)

BG225 Pin	XC4410E	XC4413E/L
R1	VCC	VCC
R2	I/O, PGCK2	I/O, PGCK2
R3	I/O	I/O
R4	I/O	I/O
R5	I/O	I/O
R6	I/O	I/O
R7	I/O	I/O
R8	VCC	I/O
R9	I/O	I/O
R10	N.C.	I/O
R11	I/O	I/O
R12	I/O	I/O
R13	I/O	I/O
R14	I/O	I/O
R15	VCC	VCC
P1	I/O, SCGK2	I/O, SCGK2
P2	I (M0)	I (M0)
P3	I/O,(HDC)	I/O,(HDC)
P4	I/O ($\overline{LDC}$)	I/O ($\overline{LDC}$)
P5	N.C.	I/O
P6	I/O	I/O
P7	N.C.	I/O
P8	I/O ($\overline{INIT}$)	I/O ($\overline{INIT}$)
P9	I/O	I/O
P10	N.C.	I/O
P11	I/O	I/O
P12	I/O	I/O
P13	I/O	I/O
P14	DONE	DONE
P15	I/O (D7)	I/O (D7)
N1	I/O	I/O
N2	I/O	I/O
N3	O (M1)	O (M1)
N4	I/O	I/O
N5	I/O	I/O
N6	I/O	I/O
N7	N.C.	I/O
N8	I/O	I/O
N9	I/O	I/O
N10	I/O	I/O
N11	N.C.	I/O
N12	I/O	I/O
N13	I/O, SGCK3	I/O, SGCK3
N14	I/O, PGCK3	I/O, PGCK3
N15	N.C.	I/O
M1	I/O	I/O
M2	I/O	I/O
M3	I/O	I/O
M4	I (M2)	I (M2)
M5	I/O	I/O
M6	I/O	I/O
M7	I/O	I/O
M8	GND	GND
M9	I/O	I/O
M10	N.C.	I/O
M11	I/O	I/O
M12	$\overline{PROGRAM}$	$\overline{PROGRAM}$
M13	I/O	I/O
M14	N.C.	I/O

BG225 Pin	XC4410E	XC4413E/L
M15	I/O	I/O
L1	I/O	I/O
L2	N.C.	I/O
L3	I/O	I/O
L4	I/O	I/O
L5	I/O	I/O
L6	N.C.	I/O
L7	I/O	I/O
L8	I/O	I/O
L9	I/O	I/O
L10	I/O	I/O
L11	I/O	I/O
L12	I/O	I/O
L13	I/O	I/O
L14	I/O	I/O
L15	N.C.	I/O
K1	N.C.	I/O
K2	I/O	I/O
K3	I/O	I/O
K4	N.C.	I/O
K5	I/O	I/O
K6	I/O	I/O
K7	I/O	I/O
K8	GND	GND
K9	I/O	I/O
K10	I/O	I/O
K11	I/O	I/O
K12	N.C.	I/O
K13	I/O	I/O
K14	I/O	I/O
K15	I/O (D5)	I/O (D5)
J1	I/O	I/O
J2	I/O	I/O
J3	I/O	I/O
J4	I/O	I/O
J5	N.C.	I/O
J6	I/O	I/O
J7	GND	GND
J8	GND	GND
J9	GND	GND
J10	I/O (D6)	I/O (D6)
J11	I/O	I/O
J12	I/O ($\overline{CS0}$)	I/O ($\overline{CS0}$)
J13	I/O	I/O
J14	I/O	I/O
J15	I/O	I/O
H1	VCC	VCC
H2	GND	GND
H3	I/O	I/O
H4	I/O	I/O
H5	I/O	I/O
H6	GND	GND
H7	GND	GND
H8	GND	GND
H9	GND	GND
H10	GND	GND
H11	I/O ($\overline{RS}$)	I/O ($\overline{RS}$)
H12	I/O (D3)	I/O (D3)
L1	I/O (D4)	I/O (D4)

BG225 Pinouts (continued)

BG225 Pin	XC4410E	XC4413E/L
H14	I/O	I/O
H15	VCC	VCC
G1	I/O	I/O
G2	I/O	I/O
G3	I/O	I/O
G4	I/O	I/O
G5	I/O	I/O
G6	I/O	I/O
G7	I/O	I/O
G8	I/O	I/O
G9	I/O	I/O
G10	N.C.	N.C.
G11	I/O (D2)	I/O (D2)
G12	I/O	I/O
G13	I/O	I/O
G14	I/O	I/O
G15	I/O	I/O
F1	N.C.	N.C.
F2	N.C.	N.C.
F3	I/O	I/O
F4	I/O, TMS	I/O, TMS
F5	I/O	I/O
F6	I/O	I/O
F7	N.C.	N.C.
F8	GND	GND
F9	N.C.	N.C.
F10	I/O (D0, DIN)	I/O (D0, DIN)
F11	I/O	I/O
F12	N.C.	N.C.
F13	I/O	I/O
F14	I/O	I/O
F15	I/O	I/O
E1	I/O	I/O
E2	N.C.	N.C.
E3	N.C.	N.C.
E4	I/O	I/O
E5	I/O	I/O
E6	I/O	I/O
E7	I/O	I/O
E8	I/O (A8)	I/O (A8)
E9	I/O	I/O
E10	I/O	I/O
E11	I/O	I/O
E12	I/O (D1)	I/O (D1)
E13	I/O	I/O
E14	N.C.	N.C.
E15	N.C.	N.C.
D1	I/O	I/O
D2	I/O	I/O
D3	I/O, TDI	I/O, TDI
D4	I/O, PGCK1 (A16)	I/O, PGCK1 (A16)
D5	I/O (A13)	I/O (A13)
D6	I/O	I/O
D7	I/O	I/O
D8	VCC	VCC
D9	I/O (A5)	I/O (A5)
D10	I/O	I/O
D11	N.C.	N.C.
D12	GND	GND
D13	I/O	I/O
D14	I/O	I/O
C1	I/O, TCK	I/O, TCK
C2	I/O	I/O
C3	I/O, SGCK1 (A15)	I/O, SGCK1 (A15)
C4	N.C.	I/O
C5	I/O	I/O
C6	N.C.	I/O
C7	I/O	I/O
C8	I/O (A6)	I/O (A6)
C9	I/O	I/O
C10	N.C.	I/O
C11	I/O	I/O
C12	I/O	I/O
C13	CCLK	CCLK
C14	I/O	I/O
C15	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)	I/O ($\overline{\text{RCLK}}$, RDY/ $\overline{\text{BUSY}}$)
B1	I/O (A17)	I/O (A17)
B2	VCC	VCC
B3	I/O	I/O
B4	I/O (A12)	I/O (A12)
B5	I/O	I/O
B6	I/O (A11)	I/O (A11)
B7	I/O (A9)	I/O (A9)
B8	I/O (A7)	I/O (A7)
B9	I/O	I/O
B10	N.C.	I/O
B11	I/O	I/O
B12	I/O (A3)	I/O (A3)
B13	I/O, PGCK4 (A1)	I/O, PGCK4 (A1)
B14	VCC	VCC
B15	I/O, SGCK4 (DOUT)	I/O, SGCK4 (DOUT)
A1	GND	GND
A2	I/O (A14)	I/O (A14)
A3	N.C.	I/O
A4	I/O	I/O
A5	I/O	I/O
A6	I/O (A10)	I/O (A10)
A7	I/O	I/O
A8	GND	GND
A9	I/O	I/O
A10	I/O (A4)	I/O (A4)
A11	I/O	I/O
A12	I/O	I/O
A13	I/O (CS1, A2)	I/O (CS1, A2)
A14	I/O (A0, $\overline{\text{WS}}$)	I/O (A0, $\overline{\text{WS}}$)
A15	0, TDO	0, TDO

2/28/96

Note: Shade should be taken into account when designing PC boards, in case of future replacement by different devices.

Note: Viewed from bottom side, the package pins start at the top row and go from the left edge to the right edge. Viewed from the top side, the pins start at the top row and go from the right edge to the left edge.

XC4413 Pinouts

Description	PQ208	PQ240	Boundary Scan Order
VCC	183	212	-
I/O (A8)	184	213	74
I/O (A9)	185	214	77
I/O	186	215	80
I/O	187	216	83
I/O	188	217	86
I/O	189	218	89
-	-	219*	-
I/O (A10)	190	220	92
I/O (A11)	191	221	95
VCC	-	222	-
I/O	-	223	98
I/O	-	224	101
I/O	192	225	104
I/O	193	226	107
GND	194	227	-
I/O	195	228	110
I/O	196	229	113
I/O	197	230	116
I/O	198	231	119
I/O (A12)	199	232	122
I/O (A13)	200	233	125
I/O	-	234	128
I/O	-	235	131
I/O	201	236	134
I/O	202	237	137
I/O (A14)	203	238	140
SGCK1 (A15, I/O)	204	239	143
VCC	205	240	-
-	206*	-	-
-	207*	-	-
-	208*	-	-
-	1*	-	-
GND	2	1	-
-	3*	-	-
PGCK1 (A16,I/O)	4	2	146
I/O (A17)	5	3	149
I/O	6	4	152
I/O	7	5	155
I/O (TDI)	8	6	158
I/O (TCK)	9	7	161
I/O	10	8	164
I/O	11	9	167
I/O	12	10	170
I/O	13	11	173
I/O	-	12	176
I/O	-	13	179
GND	14	14	-
I/O	15	15	182
I/O	16	16	185
I/O (TMS)	17	17	188
I/O	18	18	191
VCC	-	19	-
I/O	-	20	194
I/O	-	21	197
-	-	22*	-
I/O	19	23	200
I/O	20	24	203
I/O	21	25	206
I/O	22	26	209
I/O	23	27	212
I/O	24	28	215
GND	25	29	-
VCC	26	30	-

Pin Description	PQ208	PQ240	Boundary Scan Order
I/O	27	31	218
I/O	28	32	221
I/O	29	33	224
I/O	30	34	227
I/O	31	35	230
I/O	32	36	233
-	-	37*	-
I/O	-	38	236
I/O	-	39	239
VCC	-	40	-
I/O	33	41	242
I/O	34	42	245
I/O	35	43	248
I/O	36	44	251
GND	37	45	-
I/O	-	46	254
I/O	-	47	257
I/O	38	48	260
I/O	39	49	263
I/O	40	50	266
I/O	41	51	269
I/O	42	52	272
I/O	43	53	275
I/O	44	54	278
I/O	45	55	281
I/O	46	56	284
SGCK2 (I/O)	47	57	287
M1	48	58	290
GND	49	59	-
M0	50	60	293†
-	51*	-	-
-	52*	-	-
-	53*	-	-
-	54*	-	-
VCC	55	61	-
M2	56	62	294†
PGCK2 (I/O)	57	63	295
I/O (HDC)	58	64	298
I/O	59	65	301
I/O	60	66	304
I/O	61	67	307
I/O (LDC)	62	68	310
I/O	63	69	313
I/O	64	70	316
I/O	65	71	319
I/O	66	72	322
I/O	-	73	325
I/O	-	74	328
GND	67	75	-
I/O	68	76	331
I/O	69	77	334
I/O	70	78	337
I/O	71	79	340
VCC	-	80	-
I/O	72	81	343
I/O	73	82	346
-	-	83*	-
I/O	-	84	349
I/O	-	85	352
I/O	74	86	355
I/O	75	87	358
I/O	76	88	361
I/O ($\overline{ERR}$, $\overline{INIT}$)	77	89	364
VCC	78	90	-

* Indicates unconnected package pins.

† Contributes only one bit (.i) to the boundary scan register.

XC4413 Pinouts (continued)

Pin Description	PQ208	PQ240	Boundary Scan Order
GND	79	91	-
I/O	80	92	367
I/O	81	93	370
I/O	82	94	373
I/O	83	95	376
I/O	84	96	379
I/O	85	97	382
-	-	98*	-
I/O	-	99	385
I/O	-	100	388
VCC	-	101	-
I/O	86	102	391
I/O	87	103	394
I/O	88	104	397
I/O	89	105	400
GND	90	106	-
I/O	-	107	403
I/O	-	108	406
I/O	91	109	409
I/O	92	110	412
I/O	93	111	415
I/O	94	112	418
I/O	95	113	421
I/O	96	114	424
I/O	97	115	427
I/O	98	116	430
I/O	99	117	433
SGCK3 (I/O)	100	118	436
GND	101	119	-
-	102*	-	-
DONE	103	120	-
-	104*	-	-
-	105*	-	-
VCC	106	121	-
-	107*	-	-
$\overline{PROG}$	108	122	-
I/O (D7)	109	123	439
PGCK3 (I/O)	110	124	442
I/O	111	125	445
I/O	112	126	448
I/O	-	127	451
I/O	-	128	454
I/O (D6)	113	129	457
I/O	114	130	460
I/O	115	131	463
I/O	116	132	466
I/O	117	133	469
I/O	118	134	472
GND	119	135	-
I/O	-	136	475
I/O	-	137	478
I/O	120	138	481
I/O	121	139	484
VCC	-	140	-
I/O (D5)	122	141	487
I/O ($\overline{CSO}$)	123	142	490
-	-	143*	-
I/O	124	144	493
I/O	125	145	496
I/O	126	146	499
I/O	127	147	502
I/O (D4)	128	148	505
I/O	129	149	508
VCC	130	150	-

Pin Description	PQ208	PQ240	Boundary Scan Order
GND	131	151	-
I/O (D3)	132	152	511
I/O ($\overline{RS}$)	133	153	514
I/O	134	154	517
I/O	135	155	520
I/O	136	156	523
I/O	137	157	526
-	-	158*	-
I/O (D2)	138	159	529
I/O	139	160	532
VCC	-	161	-
I/O	140	162	535
I/O	141	163	538
I/O	-	164	541
I/O	-	165	544
GND	142	166	-
I/O	-	167	547
I/O	-	168	550
I/O	143	169	553
I/O	144	170	556
I/O	145	171	559
I/O	146	172	562
I/O (D1)	147	173	565
I/O ($\overline{RCLK}$-$\overline{BUSY}$/RDY)	148	174	568
I/O	149	175	571
I/O	150	176	574
I/O (D0, DIN)	151	177	577
SGCK4 (DOUT, I/O)	152	178	580
CCLK	153	179	-
VCC	154	180	-
-	155*	-	-
-	156*	-	-
-	157*	-	-
-	158*	-	-
TD0	159	181	-
GND	160	182	-
I/O (A0, $\overline{WS}$)	161	183	2
PGCK4 (I/O, A1)	162	184	5
I/O	163	185	8
I/O	164	186	11
I/O (CS1, A2)	165	187	14
I/O (A3)	166	188	17
I/O	-	189	20
I/O	-	190	23
I/O	167	191	26
I/O	168	192	29
I/O	169	193	32
I/O	170	194	35
-	-	195*	-
GND	171	196	-
I/O	172	197	38
I/O	173	198	41
I/O	-	199	44
I/O	-	200	47
VCC	-	201	-
I/O (A4)	174	202	50
I/O (A5)	175	203	53
-	-	204*	-
I/O	176	205	56
I/O	177	206	59
I/O	178	207	62
I/O	179	208	65
I/O (A6)	180	209	68
I/O (A7)	181	210	71
GND	182	211	-

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 0 = TDO.O
Boundary Scan Bit 391 = BSCAN.UPD

* Indicates unconnected package pins.

XC4420 Pinouts

Pin Description	HQ208	PG223	HQ240	Bound Scan
VCC	P183	J4	P212	–
I/O (A8)	P184	J3	P213	86
I/O (A9)	P185	J2	P214	69
I/O	P186	J1	P215	92
I/O	P187	H1	P216	95
I/O	P188	H2	P217	98
I/O	P189	H3	P218	101
I/O (A10)	P190	G1	P220	104
I/O (A11)	P191	G2	P221	107
I/O	–	–	–	110
I/O	–	–	–	113
VCC	–	–	P222	–
I/O	–	H4	P223	116
I/O	–	G4	P224	119
I/O	P192	F1	P225	122
I/O	P193	E1	P226	125
GND	P194	G3	P227	–
I/O	P195	F2	P228	128
I/O	P196	D1	P229	131
I/O	P197	C1	P230	134
I/O	P198	E2	P231	137
I/O (A12)	P199	F3	P232	140
I/O (A13)	P200	D2	P233	143
I/O	–	–	–	146
I/O	–	–	–	149
I/O	–	F4	P234	152
I/O	–	E4	P235	155
I/O	P201	B1	P236	158
I/O	P202	E3	P237	161
I/O (A14)	P203	C2	P238	164
I/O, SGCK1 (A15)	P204	B2	P239	167
VCC	P205	D3	P240	–
GND	P2	D4	P1	–
I/O, PGCK1 (A16)	P4	C3	P2	170
I/O (A17)	P5	C4	P3	173
I/O	P6	B3	P4	176
I/O	P7	C5	P5	179
I/O, TDI	P8	A2	P6	182
I/O, TCK	P9	B4	P7	185
I/O	–	–	–	188
I/O	–	–	–	191
I/O	P10	C6	P8	194
I/O	P11	A3	P9	197
I/O	P12	B5	P10	200
I/O	P13	B6	P11	203
I/O	–	D5	P12	206
I/O	–	D6	P13	209
GND	P14	C7	P14	–
I/O	P15	A4	P15	212
I/O	P16	A5	P16	215
I/O, TMS	P17	B7	P17	218

Pin Description	HQ208	PG223	HQ240	Bound Scan
I/O	P18	A6	P18	221
VCC	–	–	P19	–
I/O	–	D7	P20	224
I/O	–	D8	P21	227
I/O	–	–	–	230
I/O	–	–	–	233
I/O	P19	C8	P23	236
I/O	P20	A7	P24	238
I/O	P21	B8	P25	242
I/O	P22	A8	P26	245
I/O	P23	B9	P27	248
I/O	P24	C9	P28	251
GND	P25	D9	P29	–
VCC	P26	D10	P30	–
I/O	P27	C10	P31	254
I/O	P28	B10	P32	257
I/O	P29	A9	P33	260
I/O	P30	A10	P34	263
I/O	P31	A11	P35	266
I/O	P32	C11	P36	269
I/O	–	–	–	272
I/O	–	–	–	275
I/O	–	D11	P38	278
I/O	–	D12	P39	281
VCC	–	–	P40	–
I/O	P33	B11	P41	284
I/O	P34	A12	P42	287
I/O	P35	B12	P43	290
I/O	P36	A13	P44	293
GND	P37	C12	P45	–
I/O	–	D13	P46	296
I/O	–	D14	P47	299
I/O	P38	B13	P48	302
I/O	P39	A14	P49	305
I/O	P40	A15	P50	308
I/O	P41	C13	P51	311
I/O	–	–	–	314
I/O	–	–	–	317
I/O	P42	B14	P52	320
I/O	P43	A16	P53	323
I/O	P44	B15	P54	326
I/O	P45	C14	P55	329
I/O	P46	A17	P56	332
I/O, SCGK2	P47	B16	P57	335
O (M1)	P48	C15	P58	338
GND	P49	D15	P59	–
I (M0)	P50	A18	P60	341
VCC	P55	D16	P61	–
I (M2)	P56	C16	P62	342
I/O PGCK2	P57	B17	P63	343
I/O (HDC)	P58	E16	P64	346

XC4420 Pinouts (continued)

Pin Description	HQ208	PG223	HQ240	Bound Scan
I/O	P59	C17	P65	349
I/O	P60	D17	P66	352
I/O	P61	B18	P67	355
I/O (LDC)	P62	E17	P68	358
I/O	–	–	–	361
I/O	–	–	–	364
I/O	P63	F16	P69	367
I/O	P64	C18	P70	370
I/O	P65	D18	P71	373
I/O	P66	F17	P72	376
I/O	–	E15	P73	379
I/O	–	F15	P74	382
GND	P67	G16	P75	–
I/O	P68	E18	P76	385
I/O	P69	F18	P77	388
I/O	P70	G17	P78	391
I/O	P71	G18	P79	394
VCC	–	–	P80	–
I/O	P72	H16	P81	397
I/O	P73	H17	P82	400
I/O	–	–	–	403
I/O	–	–	–	406
I/O	–	G15	P84	409
I/O	–	H15	P85	412
I/O	P74	H18	P86	415
I/O	P75	J18	P87	418
I/O	P76	J17	P88	421
I/O ($\overline{\text{INIT}}$)	P77	J16	P89	424
VCC	P78	J15	P90	–
GND	P79	K15	P91	–
I/O	P80	K16	P92	427
I/O	P81	K17	P93	430
I/O	P82	K18	P94	433
I/O	P83	L18	P95	436
I/O	P84	L17	P96	439
I/O	P85	L16	P97	442
I/O	–	–	–	445
I/O	–	–	–	448
I/O	–	L15	P99	451
I/O	–	M15	P100	454
VCC	–	–	P101	–
I/O	P86	M18	P102	457
I/O	P87	M17	P103	460
I/O	P88	N18	P104	463
I/O	P89	P18	P105	466
GND	P90	M16	P106	–
I/O	–	N15	P107	469
I/O	–	P15	P108	472
I/O	P91	N17	P109	475
I/O	P92	R18	P110	478
I/O	P93	T18	P111	481
I/O	P94	P17	P112	484

Pin Description	HQ208	PG223	HQ240	Bound Scan
I/O	–	–	–	487
I/O	–	–	–	490
I/O	P95	N16	P113	493
I/O	P96	T17	P114	496
I/O	P97	R17	P115	499
I/O	P98	P16	P116	502
I/O	P99	U18	P117	505
I/O,SGCK3	P100	T16	P118	508
GND	P101	R16	P119	–
DONE	P103	U17	P120	–
VCC	P106	R15	P121	–
$\overline{\text{PROGRAM}}$	P108	V18	P122	–
I/O (D7)	P109	T15	P123	511
I/O, PGCK3	P110	U16	P124	514
I/O	P111	T14	P125	517
I/O	P112	U15	P126	520
I/O	–	R14	P127	523
I/O	–	R13	P128	526
I/O	–	–	–	529
I/O	–	–	–	532
I/O (D6)	P113	V17	P129	535
I/O	P114	V16	P130	538
I/O	P115	T13	P131	541
I/O	P116	U14	P132	544
I/O	P117	V15	P133	547
I/O	P118	V14	P134	550
GND	P119	T12	P135	–
I/O	–	R12	P136	553
I/O	–	R11	P137	556
I/O	P120	U13	P138	559
I/O	P121	V13	P139	562
VCC	–	–	P140	–
I/O (D5)	P122	U12	P141	565
I/O ($\overline{\text{CS0}}$)	P123	V12	P142	568
I/O	–	–	–	571
I/O	–	–	–	574
I/O	P124	T11	P144	577
I/O	P125	U11	P145	580
I/O	P126	V11	P146	583
I/O	P127	V10	P147	586
I/O (D4)	P128	U10	P148	598
I/O	P129	T10	P149	592
VCC	P130	R10	P150	–
GND	P131	R9	P151	–
I/O (D3)	P132	T9	P152	595
I/O ($\overline{\text{RS}}$)	P133	U9	P153	598
I/O	P134	V9	P154	601
I/O	P135	V8	P155	604
I/O	P136	U8	P156	607
I/O	P137	T8	P157	610
I/O	–	–	–	613
I/O	–	–	–	616

XC4420 Pinouts (continued)

Pin Description	HQ208	PG223	HQ240	Bound Scan
I/O (D2)	P138	V7	P159	619
I/O	P139	U7	P160	622
VCC	–	–	P161	–
I/O	P140	V6	P162	625
I/O	P141	U6	P163	628
I/O	–	R8	P164	631
I/O	–	R7	P165	634
GND	P142	T7	P166	–
I/O	–	R6	P167	637
I/O	–	R5	P168	640
I/O	P143	V5	P169	643
I/O	P144	V4	P170	646
I/O	P145	U5	P171	649
I/O	P146	T6	P172	652
I/O (D1)	P147	V3	P173	655
I/O ($\overline{\text{RCLK}}$, RDY/$\overline{\text{BUSY}}$)	P148	V2	P174	658
I/O	–	–	–	661
I/O	–	–	–	664
I/O	P149	U4	P175	667
I/O	P150	T5	P176	670
I/O (D0, DIN)	P151	U3	P177	673
I/O, SGCK4 (DOUT)	P152	T4	P178	676
CCLK	P153	V1	P179	–
VCC	P154	R4	P180	–
O, TDO	P159	U2	P181	0
GND	P160	R3	P182	–
I/O (A0, $\overline{\text{WS}}$)	P161	T3	P183	2
I/O, PGCK4 (A1)	P162	U1	P184	5
I/O	P163	P3	P185	8
I/O	P164	R2	P186	11
I/O (CS1, A2)	P165	T2	P187	14
I/O (A3)	P166	N3	P188	17
I/O	–	–	–	20
I/O	–	–	–	23
I/O	–	P4	P189	26
I/O	–	N4	P190	29
I/O	P167	P2	P191	32
I/O	P168	T1	P192	35
I/O	P169	R1	P193	38
I/O	P170	N2	P194	41
GND	P171	M3	P196	–
I/O	P172	P1	P197	44
I/O	P173	N1	P198	47
I/O	–	M4	P199	50
I/O	–	L4	P200	53
VCC	–	–	P201	–
I/O	–	–	–	56
I/O	–	–	–	59
I/O (A4)	P174	M2	P202	62
I/O (A5)	P175	M1	P203	65
I/O	P176	L3	P205	68
I/O	P177	L2	P206	71
I/O	P178	L1	P207	74
I/O	P179	K1	P208	77
I/O (A6)	P180	K2	P209	80
I/O (A7)	P181	K3	P210	83
GND	P182	K4	P211	–

4/2/96

Additional No Connect (N.C.) Connections on HQ208 & HQ240 Packages

HQ208	HQ240
P1	P22‡
P3	P37‡
P51	P83‡
P52	P98‡
P53	P143‡
P54	P158‡
P102	P195
P104	P204‡
P105	P219‡
P107	
P155	
P156	
P157	
P158	
P206	
P207	
P208	

3/20/96

‡ Pins marked with this symbol are reserved for Ground connections on future revisions of the device. These pins do not physically connect to anything on the current device revision. However, they should be externally connected to Ground, if possible.

XC4425 Pinouts

Pin Description	PQ240	PG299	Bound Scan
VCC	212	K1	-
I/O (A8)	213	K2	98
I/O (A9)	214	K3	101
I/O	215	K5	104
I/O	216	K4	107
I/O	217	J1	110
I/O	218	J2	113
GND	219	-	-
I/O (A10)	220	H1	116
I/O (A11)	221	J3	119
I/O	-	J4	122
I/O	-	J5	125
I/O	-	H2	128
I/O	-	G1	131
VCC	222	E1	-
I/O	223	H3	134
I/O	224	G2	137
I/O	225	H4	140
I/O	226	F2	143
GND	227	F1	-
I/O	-	H5	146
I/O	-	G3	149
I/O	228	D1	152
I/O	229	G4	155
I/O	230	E2	158
I/O	231	F3	161
I/O (A12)	232	G5	164
I/O (A13)	233	C1	167
I/O	-	F4	170
I/O	-	E3	173
I/O	234	D2	176
I/O	235	C2	179
I/O	236	F5	182
I/O	237	E4	185
I/O (A14)	238	D3	188
SGCK1 (A15, I/O)	239	C3	191
VCC	240	A2	-
GND	1	B1	-
PGCK1 (A16, I/O)	2	D4	194
VCC	-	E5	-
I/O (A17)	3	B2	197
I/O	4	B3	200
I/O	5	E6	203
I/O (TDI)	6	D5	206
I/O (TCK)	7	C4	209
I/O	-	A3	212
I/O	-	D6	215
I/O	8	E7	218
I/O	9	B4	221
I/O	10	C5	224
I/O	11	A4	227
I/O	12	D7	230
I/O	13	C6	233
I/O	-	E8	236
I/O	-	B5	239
GND	14	A5	-
I/O	15	B6	242
I/O	16	D8	245
I/O (TMS)	17	C7	248
I/O	18	B7	251
VCC	19	A6	-
I/O	20	C8	254
I/O	21	E9	257
GND	22	-	-
I/O	-	A7	260
I/O	-	D9	263
I/O	-	B8	266
I/O	-	A8	269
I/O	23	C9	272
I/O	24	B9	275
I/O	25	E10	278
I/O	26	A9	281
I/O	27	D10	284
I/O	28	C10	287
GND	29	A10	-
VCC	30	A11	-
I/O	31	B10	290

Pin Description	PQ240	PG299	Bound Scan
I/O	32	B11	293
I/O	33	C11	296
I/O	34	E11	299
I/O	35	D11	302
I/O	36	A12	305
I/O	-	B12	308
I/O	-	A13	311
I/O	-	C12	314
I/O	-	D12	317
GND	37	-	-
I/O	38	E12	320
I/O	39	B13	323
VCC	40	A16	-
I/O	41	A14	326
I/O	42	C13	329
I/O	43	B14	332
I/O	44	D13	335
GND	45	A15	-
I/O	-	B15	338
I/O	-	E13	341
I/O	46	C14	344
I/O	47	A17	347
I/O	48	D14	350
I/O	49	B16	353
I/O	50	C15	356
I/O	51	E14	359
I/O	-	A18	362
I/O	-	D15	365
I/O	52	C16	368
I/O	53	B17	371
I/O	54	B18	374
I/O	55	E15	377
I/O	56	D16	380
SCGK2 (I/O)	57	C17	383
M1	58	A20	386
GND	59	A19	-
M0	60	C18	389†
VCC	61	B20	-
M2	62	D17	390†
PGCK2 (I/O)	63	B19	391
I/O (HDC)	64	C19	394
GND	-	E16	-
I/O	65	F16	397
I/O	66	E17	400
I/O	67	D18	403
I/O (LDC)	68	C20	406
I/O	-	F17	409
I/O	-	G16	412
I/O	69	D19	415
I/O	70	E18	418
I/O	71	D20	421
I/O	72	G17	424
I/O	73	F18	427
I/O	74	H16	430
I/O	-	E19	433
I/O	-	F19	436
GND	75	E20	-
I/O	76	H17	439
I/O	77	G18	442
I/O	78	G19	445
I/O	79	H18	448
VCC	80	F20	-
I/O	81	J16	451
I/O	82	G20	454
GND	83	-	-
I/O	-	J17	457
I/O	-	H19	460
I/O	-	H20	463
I/O	-	J18	466
I/O	84	J19	469
I/O	85	K16	472
I/O	86	J20	475
I/O	87	K17	478
I/O	88	K18	481
I/O ($\overline{\text{ERR}}$, $\overline{\text{INIT}}$)	89	K19	484
VCC	90	L20	-
GND	91	K20	-

† Contributes only one bit (.i) to the boundary scan register.

XC4425 Pinouts (continued)

Pin Description	PQ240	PG299	Bound Scan
I/O	92	L19	487
I/O	93	L18	490
I/O	94	L16	493
I/O	95	L17	496
I/O	96	M20	499
I/O	97	M19	502
I/O	-	N20	505
I/O	-	M18	508
I/O	-	M17	511
I/O	-	M16	514
GND	98	-	-
I/O	99	N19	517
I/O	100	P20	520
VCC	101	T20	-
I/O	102	N18	523
I/O	103	P19	526
I/O	104	N17	529
I/O	105	R19	532
GND	106	R20	-
I/O	-	N16	535
I/O	-	P18	538
I/O	107	U20	541
I/O	108	P17	544
I/O	109	T19	547
I/O	110	R18	550
I/O	111	P16	553
I/O	112	V20	556
I/O	-	R17	559
I/O	-	T18	562
I/O	113	U19	565
I/O	114	V19	568
I/O	115	R16	571
I/O	116	T17	574
I/O	117	U18	577
SGCK3 (I/O)	118	X20	580
VCC	-	T16	-
GND	119	W20	-
DONE	120	V18	-
VCC	121	X19	-
$\overline{\text{PROG}}$	122	U17	-
I/O (D7)	123	W19	583
PGCK3 (I/O)	124	W18	586
I/O	125	T15	589
I/O	126	U16	592
I/O	127	V17	595
I/O	128	X18	598
I/O	-	U15	601
I/O	-	T14	604
I/O (D6)	129	W17	607
I/O	130	V16	610
I/O	131	X17	613
I/O	132	U14	616
I/O	133	V15	619
I/O	134	T13	622
I/O	-	W16	625
I/O	-	W15	628
GND	135	X16	-
I/O	136	U13	631
I/O	137	V14	634
I/O	138	W14	637
I/O	139	V13	640
VCC	140	X15	-
I/O (D5)	141	T12	643
I/O ($\overline{\text{CS0}}$)	142	X14	646
GND	143	-	-
I/O	-	U12	649
I/O	-	W13	652
I/O	-	X13	655
I/O	-	V12	658
I/O	144	W12	661
I/O	145	T11	664
I/O	146	X12	667
I/O	147	U11	670
I/O (D4)	148	V11	673
I/O	149	W11	676
VCC	150	X10	-
GND	151	X11	-

Pin Description	PQ240	PG299	Bound Scan
I/O (D3)	152	W10	679
I/O ($\overline{\text{RS}}$)	153	V10	682
I/O	154	T10	685
I/O	155	U10	688
I/O	156	X9	691
I/O	157	W9	694
I/O	-	X8	697
I/O	-	V9	700
I/O	-	U9	703
I/O	-	T9	706
GND	158	-	-
I/O (D2)	159	W8	709
I/O	160	X7	712
VCC	161	X5	-
I/O	162	V8	715
I/O	163	W7	718
I/O	164	U8	721
I/O	165	W6	724
GND	166	X6	-
I/O	-	T8	727
I/O	-	V7	730
I/O	167	X4	733
I/O	168	U7	736
I/O	169	W5	739
I/O	170	V6	742
I/O	171	T7	745
I/O	172	X3	748
I/O (D1)	173	U6	751
I/O (RCLK-$\overline{\text{BUSY}}$/RDY)	174	V5	754
I/O	-	W4	757
I/O	-	W3	760
I/O	175	T6	763
I/O	176	U5	766
I/O (D0, DIN)	177	V4	769
SGCK4 (DOUT, I/O)	178	X1	772
CCLK	179	V3	-
GND	-	T5	-
VCC	180	W1	-
TDO	181	U4	
GND	182	X2	-
I/O (A0, $\overline{\text{WS}}$)	183	W2	2
PGCK4 (I/O, A1)	184	V2	5
I/O	185	R5	8
I/O	186	T4	11
I/O (CS1, A2)	187	U3	14
I/O (A3)	188	V1	17
I/O	-	R4	20
I/O	-	P5	23
I/O	189	U2	26
I/O	190	T3	29
I/O	191	U1	32
I/O	192	P4	35
I/O	193	R3	38
I/O	194	N5	41
I/O	195	T2	44
I/O	-	R2	47
GND	196	T1	-
I/O	197	N4	50
I/O	198	P3	53
I/O	199	P2	56
I/O	200	N3	59
VCC	201	R1	-
I/O	-	M5	62
I/O	-	P1	65
I/O	-	M4	68
I/O	-	N2	71
I/O (A4)	202	N1	74
I/O (A5)	203	M3	77
GND	204	-	-
I/O	205	M2	80
I/O	206	L5	83
I/O	207	M1	86
I/O	208	L4	89
I/O (A6)	209	L3	92
I/O (A7)	210	L2	95
GND	211	L1	-

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 0 = TDO.O
Boundary Scan Bit 391 = BSCAN.UPD