SECTION 2

SPECIFICATIONS

INTRODUCTION

The DSP56303 is fabricated in high density CMOS with Transistor-Transistor Logic (TTL) compatible inputs and outputs. The DSP56303 specifications are preliminary and are from design simulations, and may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after full characterization and device qualifications are complete.

MAXIMUM RATINGS

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Note: In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification will never occur in the same device that has a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2-1 Maximum Ratings

Rating[1]	Symbol	Value[1, 2]	Unit
Supply Voltage	V_{CC}	−0.3 to +4.0	V
All input voltages excluding "5 V tolerant" inputs[3]	V_{IN}	GND − 0.3 to V_{CC} + 0.3	V
All "5 V tolerant" input voltages[3]	V_{IN5}	GND − 0.3 to V_{CC} + 3.95	V
Current drain per pin excluding V_{CC} and GND	I	10	mA
Operating temperature range	T_J	−40 to +100	°C
Storage temperature	T_{STG}	−55 to +150	°C

Notes:
1. GND = 0 V, V_{CC} = 3.3 V ± 0.3 V, T_J = −40°C to +100°C, CL = 50 pF + 2 TTL Loads
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.
3. **CAUTION**: All "5 V Tolerant" input voltages cannot be more than 3.95 V greater than the supply voltage; this restriction applies to "power on", as well as during normal operation. In any case, the input voltages can not be more than 5.75 V. "5 V Tolerant" inputs are inputs that tolerate 5 V.

THERMAL CHARACTERISTICS

Table 2-2 Thermal Characteristics

Characteristic	Symbol	TQFP Value	PBGA[3] Value	PBGA[4] Value	Unit
Junction-to-ambient thermal resistance	$R_{\theta JA}$ or θ_{JA}	55.7	57	28	°C/W
Junction-to-case thermal resistance	$R_{\theta JC}$ or θ_{JC}	11.4	15	—	°C/W
Thermal characterization parameter	Ψ_{JT}	6.8	8	—	°C/W

Notes:
1. Junction-to-ambient thermal resistance is based on measurements on a horizontal single-sided printed circuit board per SEMI G38-87 in natural convection.(SEMI is Semiconductor Equipment and Materials International, 805 East Middlefield Rd., Mountain View, CA 94043, (415) 964-5111)
2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88, with the exception that the cold plate temperature is used for the case temperature.
3. These are simulated values; testing is not complete. See note 1 for test board conditions.
4. These are simulated values; testing is not complete. The test board has two, 2-ounce signal layers and two 1-ounce solid ground planes internal to the test board.

DC ELECTRICAL CHARACTERISTICS

Table 2-3 DC Electrical Characteristics[6]

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input high voltage • D(0:23), $\overline{BG}$, $\overline{BB}$, $\overline{TA}$ • MOD[1]/$\overline{IRQ}$[1], $\overline{RESET}$, PINIT/$\overline{NMI}$ and all JTAG/ESSI/SCI/Timer/HI08 pins • EXTAL[8]	 V_{IH} V_{IHP} V_{IHX}	 2.0 2.0 $0.8 \times V_{CC}$	 — — —	 V_{CC} $V_{CC} + 3.95$ V_{CC}	 V V V
Input low voltage • D(0:23), $\overline{BG}$, $\overline{BB}$, $\overline{TA}$, MOD[1]/$\overline{IRQ}$[1], $\overline{RESET}$, PINIT • All JTAG/ESSI/SCI/Timer/HI08 pins • EXTAL[8]	 V_{IL} V_{ILP} V_{ILX}	 –0.3 –0.3 –0.3	 — — —	 0.8 0.8 $0.2 \times V_{CC}$	 V V V
Input leakage current	I_{IN}	–10	—	10	µA
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I_{TSI}	–10	—	10	µA
Output high voltage • TTL (I_{OH} = –0.4 mA)[5,7] • CMOS (I_{OH} = –10 µA)[5]	V_{OH} 	 $V_{CC} - 0.4$ $V_{CC} - 0.01$	 — —	 — —	 V V
Output low voltage • TTL (I_{OL} = 3.0 mA, open-drain pins I_{OL} = 6.7 mA)[5,7] • CMOS (I_{OL} = 10 µA)[5]	V_{OL} 	 — —	 — —	 0.4 0.01	 V V
Internal supply current[2]: • In Normal mode • In Wait mode[3] • In Stop mode[4]	 I_{CCI} I_{CCW} I_{CCS}	 — — —	 **66 MHz:** 84 **80 MHz:** 102 **100 MHz:** 127 **66 MHz:** 5 **80 MHz:** 6 **100 MHz:** 7. 5 **66 MHz:** 100 **80 MHz:** 100 **100 MHz:** 100	 **66 MHz:** 120 **80 MHz:** 145 **100 MHz:** 181 **66 MHz:** 7 **80 MHz:** 9 **100 MHz:** 11 **66 MHz:** 150 **80 MHz:** 150 **100 MHz:** 150	 mA mA mA mA mA mA µA µA µA
PLL supply current in Stop mode[5]		—	1	2.5	mA
Input capacitance[5]	C_{IN}	—	—	10	pF

Table 2-3 DC Electrical Characteristics[6] (Continued)

Characteristics	Symbol	Min	Typ	Max	Unit

Notes:
1. Refers to MODA/$\overline{\text{IRQA}}$, MODB/$\overline{\text{IRQB}}$, MODC/$\overline{\text{IRQC}}$, and MODD/$\overline{\text{IRQD}}$ pins
2. **Power Consumption Considerations** on page 4-4 provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). Measurements are based on synthetic intensive DSP benchmarks (see **Appendix A**). The power consumption numbers in this specification are 90% of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CC} = 3.0 V at T_J = 100°C. Maximum internal supply current is measured with V_{CC} = 3.6 V at T_J = 100°C.
3. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). PLL and XTAL signals are disabled during Stop state.
4. In order to obtain these results, all inputs, which are not disconnected at Stop mode, must be terminated (i.e., not allowed to float).
5. Periodically sampled and not 100% tested
6. V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100 °C, C_L = 50 pF + 2 TTL Loads
7. This characteristic does not apply to XTAL and PCAP.
8. Driving EXTAL to the low V_{IHX} or the high V_{ILX} value may cause additional power consumption (DC current). To minimize power consumption, the minimum V_{IHX} should be no lower than $0.9 \times V_{CC}$ and the maximum V_{ILX} should be no higher than $0.1 \times V_{CC}$.

AC ELECTRICAL CHARACTERISTICS

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.3 V and a V_{IH} minimum of 2.4 V for all pins except EXTAL, which is tested using the input levels shown in **Note 6** of the previous table. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. DSP56303 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively.

INTERNAL CLOCKS

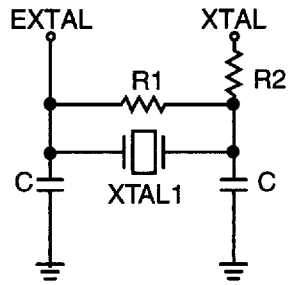
Table 2-4 Internal Clocks, CLKOUT

Characteristics	Symbol	Expression[1, 2]		
		Min	Typ	Max
Internal operation frequency and CLKOUT with PLL enabled	f	—	(Ef × MF)/ (PDF × DF)	—
Internal operation frequency and CLKOUT with PLL disabled	f	—	Ef/2	—
Internal clock and CLKOUT high period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_H	— 0.49 × ET_C × PDF × DF/MF 0.47 × ET_C × PDF × DF/MF	ET_C — —	— 0.51 × ET_C × PDF × DF/MF 0.53 × ET_C × PDF × DF/MF
Internal clock and CLKOUT low period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_L	— 0.49 × ET_C × PDF × DF/MF 0.47 × ET_C × PDF × DF/MF	ET_C — —	— 0.51 × ET_C × PDF × DF/MF 0.53 × ET_C × PDF × DF/MF
Internal clock and CLKOUT cycle time with PLL enabled	T_C	—	ET_C × PDF × DF/MF	—
Internal clock and CLKOUT cycle time with PLL disabled	T_C	—	2 × ET_C	—
Instruction cycle time	I_{CYC}	—	T_C	—

Notes: 1. DF = Division Factor
Ef = External frequency
ET_C = External clock cycle
MF = Multiplication Factor
PDF = Predivision Factor
T_C = internal clock cycle
2. See the **PLL and Clock Generation** section in the *DSP56300 Family Manual* for a detailed discussion of the PLL.

EXTERNAL CLOCK OPERATION

The DSP56303 system clock may be derived from the on–chip crystal oscillator, as shown in **Figure 1** on the cover page, or it may be externally supplied. An externally supplied square wave voltage source should be connected to EXTAL (see **Figure 2-2**), leaving XTAL physically not connected to the board or socket.

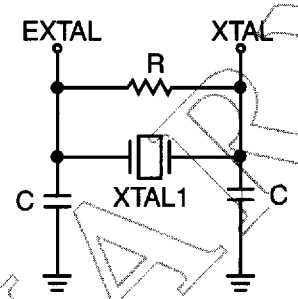


Fundamental Frequency Fork Crystal Oscillator

Suggested Component Values:

f_{OSC} = 32.768 kHz
R1 = 3.9 MΩ ± 10%
C = 22 pF ± 20%
R2 = 200 kΩ ± 10%

Calculations were done for a 32.768 kHz crystal with the following parameters:
a load capacitance (C_L) of 12.5 pF,
a shunt capacitance (C_0) of 1.8 pF,
a series resistance of 40 kΩ, and
a drive level of 1 μW.



Fundamental Frequency Crystal Oscillator

Suggested Component Values:

f_{OSC} = 4 MHz	f_{OSC} = 20 MHz
R = 680 kΩ ± 10%	R = 680 kΩ ± 10%
C = 56 pF ± 20%	C = 22 pF ± 20%

Calculations were done for a 4/20 MHz crystal with the following parameters:
a C_L of 30/20 pF,
a C_0 of 7/6 pF,
a series resistance of 100/20 Ω, and
a drive level of 2 mW.

AA1071

Figure 2-1 Crystal Oscillator Circuits

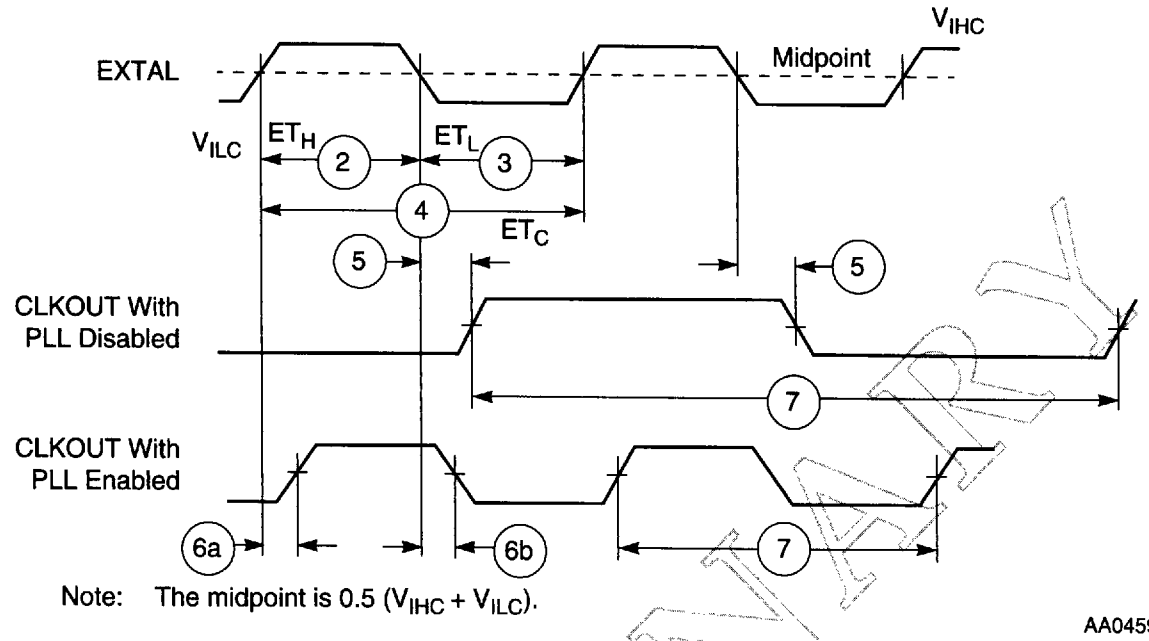


Figure 2-2 External Clock Timing

Table 2-5 Clock Operation

No.	Characteristics	Symbol	66 MHz		80 MHz		100 MHz	
			Min	Max	Min	Max	Min	Max
1	Frequency of EXTAL (EXTAL Pin Frequency) The rise and fall time of this external clock should be 3 ns maximum.	Ef	0	66.0	0	80.0	0	100.0
2	EXTAL input high[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[6]) • With PLL enabled (42.5%–57.5% duty cycle[6])	ET_H	7.08 ns 6.44 ns	∞ 157.0 µs	5.84 ns 5.31 ns	∞ 157.0 µs	4.67 ns 4.25 ns	∞ 157.0 µs
3	EXTAL input low[1, 2] • With PLL disabled (46.7%–53.3% duty cycle[6]) • With PLL enabled (42.5%–57.5% duty cycle[6])	ET_L	7.08 ns 6.44 ns	∞ 157.0 µs	5.84 ns 5.31 ns	∞ 157.0 µs	4.67 ns 4.25 ns	∞ 157.0 µs

Table 2-5 Clock Operation (Continued)

No.	Characteristics	Symbol	66 MHz		80 MHz		100 MHz	
			Min	Max	Min	Max	Min	Max
4	EXTAL cycle time[2] • With PLL disabled • With PLL enabled	ET_C	15.15 ns 15.15 ns	∞ 273.1 µs	12.50 ns 12.50 ns	∞ 273.1 µs	10.00 ns 10.00 ns	∞ 273.1 µs
5	CLKOUT change from EXTAL fall with PLL disabled		4.3 ns	11.0 ns	4.3 ns	11.0 ns	4.3 ns	11.0 ns
6	CLKOUT rising edge from EXTAL rising edge with PLL enabled (MF = 1, PDF = 1, Ef > 15 MHz)[3,5]		0.0 ns	1.8 ns	0.0 ns	1.8 ns	0.0 ns	1.8 ns
	CLKOUT falling edge from EXTAL rising edge with PLL enabled (MF = 2 or 4, PDF = 1, Ef > 15 MHz)[3,5]		0.0 ns	1.8 ns	0.0 ns	1.8 ns	0.0 ns	1.8 ns
	CLKOUT falling edge from EXTAL falling edge with PLL enabled (MF ≤ 4, PDF ≠ 1, Ef / PDF > 15 MHz)[3,5]		0.0 ns	1.8 ns	0.0 ns	1.8 ns	0.0 ns	1.8 ns
7	Instruction cycle time = $I_{CYC} = T_C$[4] (see **Table 2-4**) (46.7%–53.3% duty cycle) • With PLL disabled • With PLL enabled	I_{CYC}	30.3 ns 15.15 ns	∞ 8.53 µs	25.0 ns 12.50 ns	∞ 8.53 µs	20.0 ns 10.00 ns	∞ 8.53 µs

Notes:
1. Measured at 50% of the input transition
2. The maximum value for PLL enabled is given for minimum V_{CO} and maximum MF.
3. Periodically sampled and not 100% tested
4. The maximum value for PLL enabled is given for minimum V_{CO} and maximum DF.
5. The skew is not guaranteed for any other MF value.
6. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correction operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

PHASE LOCK LOOP (PLL) CHARACTERISTICS

Table 2-6 PLL Characteristics

Characteristics	66 MHz		80 MHz		100 MHz		Unit
	Min	Max	Min	Max	Min	Max	
V_{CO} frequency when PLL enabled ($MF \times E_f \times 2/PDF$)	30	132	30	160	30	200	MHz
PLL external capacitor (PCAP pin to V_{CCP}) (C_{PCAP}[1])							
• @ MF ≤ 4	(MF × 425) – 125	(MF × 590) – 175	(MF × 425) – 125	(MF × 590) – 175	(MF × 425) – 125	(MF × 590) – 175	pF
• @ MF > 4	MF × 520	MF × 920	MF × 520	MF × 920	MF × 520	MF × 920	pF

Note: C_{PCAP} is the value of the PLL capacitor (connected between the PCAP pin and V_{CCP}). The recommended value in pF for C_{PCAP} can be computed from one of the following equations:
$(500 \times MF) - 150$, for $MF \leq 4$, or
$690 \times MF$, for $MF > 4$.

RESET, STOP, MODE SELECT, AND INTERRUPT TIMING

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing[6]

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
8	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[3]	—	—	26.0	—	26.0	—	26.0	ns
9	Required $\overline{\text{RESET}}$ duration[4]								
	• Power on, external clock generator, PLL disabled	$50 \times ET_C$	760.0	—	625.0	—	500.0	—	ns
	• Power on, external clock generator, PLL enabled	$1000 \times ET_C$	15.2	—	12.5	—	10.0	—	µs
	• Power on, internal oscillator	$75000 \times ET_C$	1.14	—	1.0	—	0.75	—	ms
	• During STOP, XTAL disabled (PCTL Bit 16 = 0)	$75000 \times ET_C$	1.14	—	1.0	—	0.75	—	ms
	• During STOP, XTAL enabled (PCTL Bit 16 = 1)	$2.5 \times T_C$	38.0	—	31.3	—	25.0	—	ns
	• During normal operation	$2.5 \times T_C$	38.0	—	31.3	—	25.0	—	ns
10	Delay from asynchronous $\overline{\text{RESET}}$ deassertion to first external address output (internal reset deassertion)[5]								
	• Minimum	**66 MHz:** $3.25 \times T_C + 2.0$	51.0	—	—	—	—	—	ns
		80 MHz: $3.25 \times T_C + 2.0$	—	—	42.6	—	—	—	ns
		100 MHz: $3.25 \times T_C + 2.0$	—	—	—	—	34.5	—	ns
	• Maximum	**66 MHz:** $20.25\ T_C + 11.0$	—	318.0	—	—	—	—	ns
		80 MHz: $20.25\ T_C + 9.95$	—	—	—	263.1	—	—	ns
		100 MHz: $20.25\ T_C + 7.50$	—	—	—	—	—	211.5	ns

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
11	Synchronous reset setup time from $\overline{\text{RESET}}$ deassertion to CLKOUT Transition 1								
	• Minimum	T_C	9.0	—	7.4	—	5.9	—	ns
	• Maximum		—	15.2	—	12.5	—	10.0	ns
12	Synchronous reset deasserted, delay time from the CLKOUT Transition 1 to the first external address output								
	• Minimum	$3.25 \times T_C + 1.0$	50.0	—	41.6	—	33.5	—	ns
	• Maximum	$20.25\ T_C + 5.0$	—	312.0	—	258.1	—	207.5	ns
13	Mode select setup time		30.0	—	30.0	—	30.0	—	ns
14	Mode select hold time		0.0	—	0.0	—	0.0	—	ns
15	Minimum edge-triggered interrupt request assertion width		10.0	—	8.25	—	6.6	—	ns
16	Minimum edge-triggered interrupt request deassertion width		10.0	—	8.25	—	6.6	—	ns
17	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory access address out valid								
	• Caused by first interrupt instruction fetch	$4.25 \times T_C + 2.0$	66.0	—	55.1	—	44.5	—	ns
	• Caused by first interrupt instruction execution	$7.25 \times T_C + 2.0$	112.0	—	92.6	—	74.5	—	ns

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
18	Delay from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{NMI}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution	$10 \times T_C + 5.0$	157.0	—	130.0	—	105.0	—	ns
19	Delay from address output valid caused by first interrupt instruction execute to interrupt request deassertion for level sensitive fast interrupts[1]	**66 MHz**[8]: $3.75 \times T_C + WS \times T_C - 14$ **80 MHz**[8]: $3.75 \times T_C + WS \times T_C - 12.4$ **100 MHz**[8]: $3.75 \times T_C + WS \times T_C - 10.94$	—		—		—		ns ns ns
20	Delay from $\overline{RD}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1]	**66 MHz**[8]: $3.25 \times T_C + WS \times T_C - 14$ **80 MHz**[8]: $3.25 \times T_C + WS \times T_C - 12.4$ **100 MHz**[8]: $3.25 \times T_C + WS \times T_C - 10.94$	—		—		—		ns ns ns

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
21	Delay from $\overline{WR}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1]								
	• DRAM for all WS	**66 MHz**[8]: $(WS + 3.5) \times T_C - 14$	—						ns
		80 MHz[8]: $(WS + 3.5) \times T_C - 12.4$			—				ns
		100 MHz[8]: $(WS + 3.5) \times T_C - 10.94$					—		ns
	• SRAM WS = 1	**66 MHz**[8]: $(WS + 3.5) \times T_C - 14$	—						ns
		80 MHz[8]: $(WS + 3.5) \times T_C - 12.4$			—				ns
		100 MHz[8]: $(WS + 3.5) \times T_C - 10.94$					—		ns
	• SRAM WS = 2, 3	**66 MHz**[8]: $(WS + 3) \times T_C - 14$	—						ns
		80 MHz[8]: $(WS + 3) \times T_C - 12.4$			—				ns
		100 MHz[8]: $(WS + 3) \times T_C - 10.94$					—		ns
	• SRAM WS ≥ 4	**66 MHz**[8]: $(WS + 2.5) \times T_C - 14$	—						ns
		80 MHz[8]: $(WS + 2.5) \times T_C - 12.4$			—				ns
		100 MHz[8]: $(WS + 2.5) \times T_C - 10.94$					—		ns
22	Synchronous interrupt setup time from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{NMI}$ assertion to the CLKOUT Transition 2		9.0	T_C	7.4	T_C	5.9	T_C	ns

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
23	Synchronous interrupt delay time from the CLKOUT Transition 2 to the first external address output valid caused by the first instruction fetch after coming out of Wait Processing state								
	• Minimum	$9.25 \times T_C + 1.0$	141.0	—	116.6	—	93.5	—	ns
	• Maximum	$24.75 \times T_C + 5.0$	—	380.0	—	314.4	—	252.5	ns
24	Duration for $\overline{IRQA}$ assertion to recover from Stop state		9.0	—	7.4	—	5.9	—	ns
25	Delay from $\overline{IRQA}$ assertion to fetch of first instruction (when exiting Stop)[2, 3]								
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (OMR Bit 6 = 0)	$PLC \times ET_C \times PDF + (128\ K - PLC/2) \times T_C$	2.0	64.1	1.6	17.0	1.3	13.6	ms
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (OMR Bit 6 = 1)	$PLC \times ET_C \times PDF + (23.75 \pm 0.5) \times T_C$	352.3 ns	62.1 ms	290.6 ns	15.4 ms	232.5 ns	12.3 ms	
	• PLL is active during Stop (PCTL Bit 17 = 1) (Implies No Stop Delay)	$(8.25 \pm 0.5) \times T_C$	117.4	132.6	96.9	109.4	77.5	87.5	ns

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
26	Duration of level sensitive $\overline{IRQA}$ assertion to ensure interrupt service (when exiting Stop)[2, 3]								
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (OMR Bit 6 = 0)	$PLC \times ET_C \times PDF + (128K - PLC/2) \times T_C$	64.1	—	17.0	—	13.6	—	ms
	• PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (OMR Bit 6 = 1)	$PLC \times ET_C \times PDF + (20.5 \pm 0.5) \times T_C$	62.1	—	15.4	—	12.3	—	ms
	• PLL is active during Stop (PCTL Bit 17 = 1) (implies no Stop delay)	$5.5 \times T_C$	83.4	—	68.8	—	55.0	—	ns
27	Interrupt Requests Rate								
	• HI08, ESSI, SCI, Timer	$12T_C$	—	181.8	—	150.0	—	120.0	ns
	• DMA	$8T_C$	—	121.2	—	100.0	—	80.0	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	$8T_C$	—	121.2	—	100.0	—	80.0	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (level trigger)	$12T_C$	—	181.8	—	150.0	—	120.0	ns
28	DMA Requests Rate								
	• Data read from HI08, ESSI, SCI	$6T_C$	—	90.9	—	75.0	—	60.0	ns
	• Data write to HI08, ESSI, SCI	$7T_C$	—	106.1	—	87.5	—	70.0	ns
	• Timer	$2T_C$	—	30.3	—	25.0	—	20.0	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	$3T_C$	—	45.5	—	37.5	—	30.0	ns

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
29	Delay from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{NMI}$ assertion to external memory (DMA source) access address out valid	$4.25 \times T_C + 2.0$	66.0	—	55.1	—	44.0	—	ns

Notes:

1. When using fast interrupts and $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, and $\overline{IRQD}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.
2. This timing depends on several settings:

   For PLL disable, using internal oscillator (PLL Control Register (PCTL) Bit 16 = 0) and oscillator disabled during Stop (PCTL Bit 17 = 0), a stabilization delay is required to assure the oscillator is stable before executing programs. In that case, resetting the Stop delay (OMR Bit 6 = 0) will provide the proper delay. While it is possible to set OMR Bit 6 = 1, it is not recommended and these specifications do not guarantee timings for that case.

   For PLL disable, using internal oscillator (PCTL Bit 16 = 0) and oscillator enabled during Stop (PCTL Bit 17=1), no stabilization delay is required and recovery time will be minimal (OMR Bit 6 setting is ignored).

   For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time will be defined by the PCTL Bit 17 and OMR Bit 6 settings.

   For PLL enable, if PCTL Bit 17 is 0, the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0 to 1000 cycles. This procedure occurs in parallel with the stop delay counter, and stop recovery will end when the last of these two events occurs. The stop delay counter completes count or PLL lock procedure completion.

   PLC value for PLL disable is 0.

   The maximum value for ET_C is 4096 (maximum MF) divided by the desired internal frequency (i.e., for 66 MHz it is 4096/66 MHz = 62 µs). During the stabilization period, T_C, T_H, and T_L will not be constant, and their width may vary, so timing may vary as well.
3. Periodically sampled and not 100% tested

Table 2-7 Reset, Stop, Mode Select, and Interrupt Timing[6] (Continued)

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	

4. For an external clock generator, $\overline{\text{RESET}}$ duration is measured during the time in which $\overline{\text{RESET}}$ is asserted, V_{CC} is valid, and the EXTAL input is active and valid.

   For internal oscillator, $\overline{\text{RESET}}$ duration is measured during the time in which $\overline{\text{RESET}}$ is asserted and V_{CC} is valid. The specified timing reflects the crystal oscillator stabilization time after power-up. This number is affected both by the specifications of the crystal and other components connected to the oscillator and reflects worst case conditions.

   When the V_{CC} is valid, but the other "required $\overline{\text{RESET}}$ duration" conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.
5. If PLL does not lose lock
6. V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100°C, C_L = 50 pF + 2 TTL Loads
7. WS = number of wait states (measured in clock cycles, number of T_C)
8. Use expression to compute maximum value.

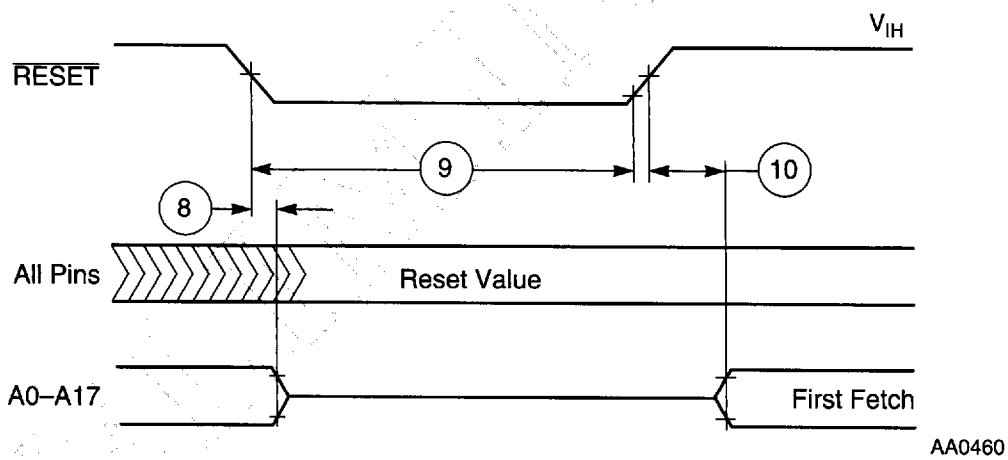


Figure 2-3 Reset Timing

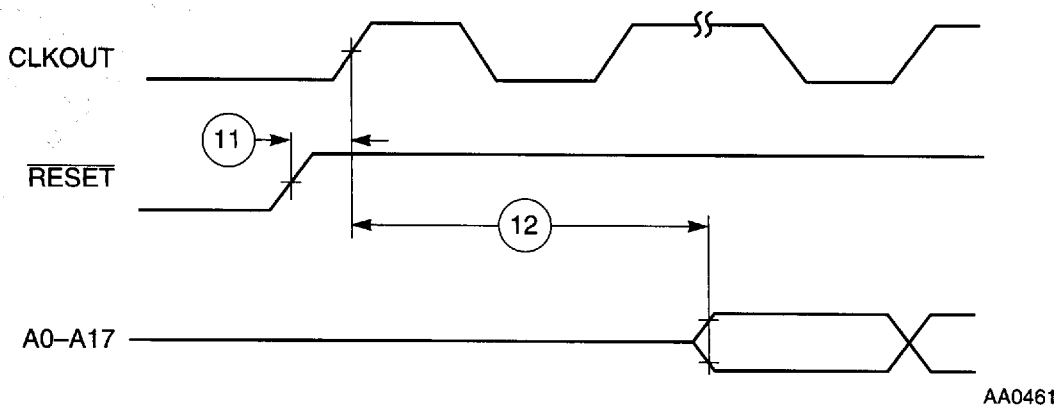
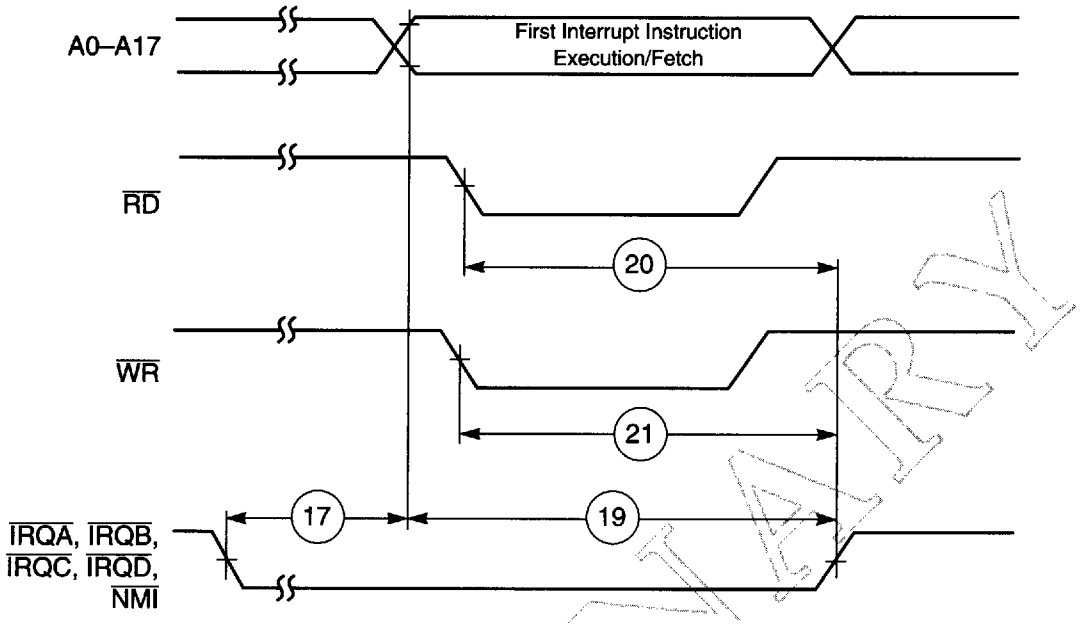
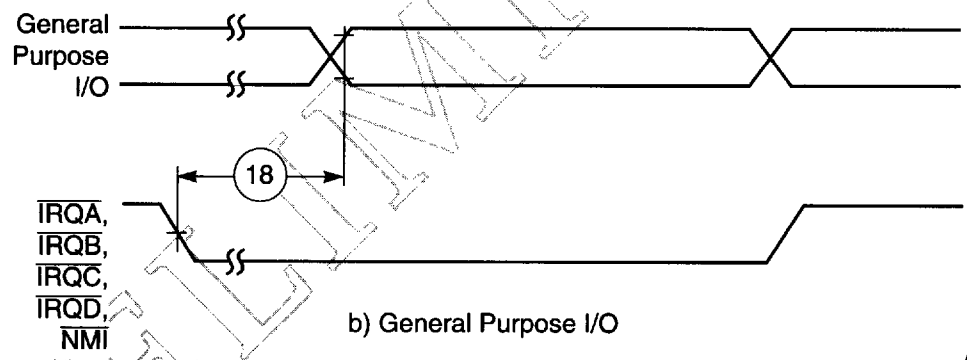


Figure 2-4 Synchronous Reset Timing



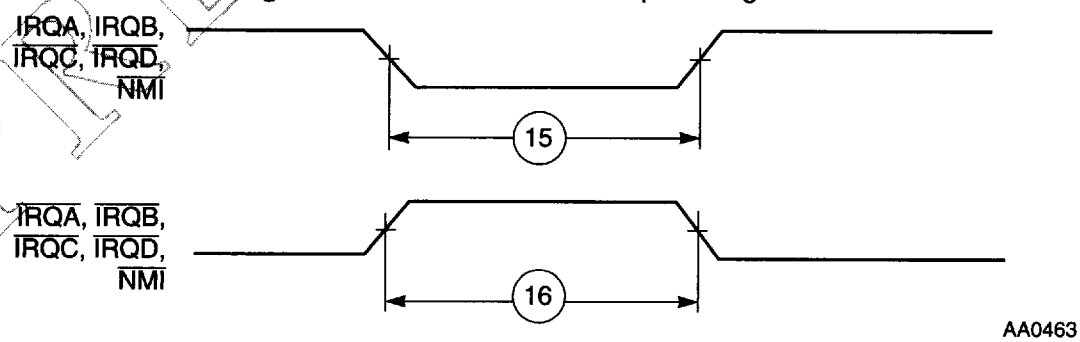
a) First Interrupt Instruction Execution



b) General Purpose I/O

AA0462

Figure 2-5 External Fast Interrupt Timing



AA0463

Figure 2-6 External Interrupt Timing (Negative Edge-Triggered)

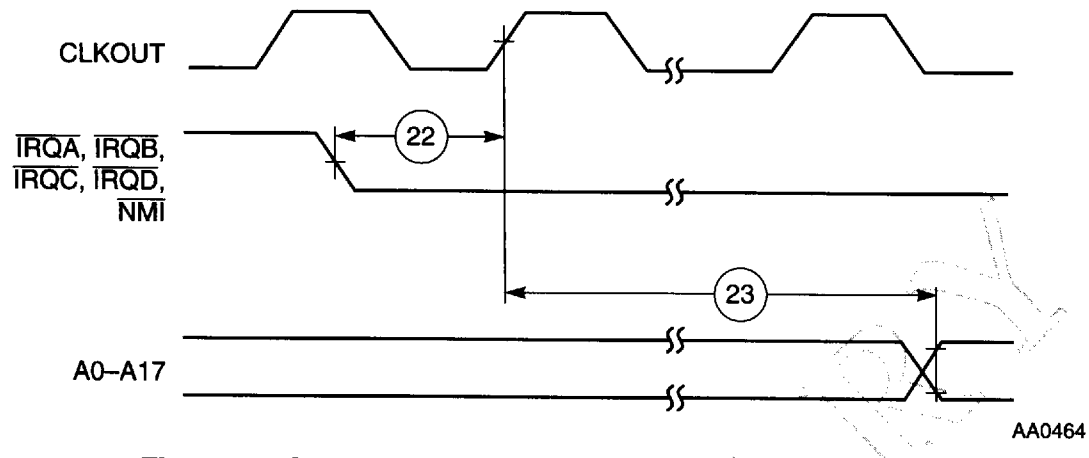


Figure 2-7 Synchronous Interrupt from Wait State Timing

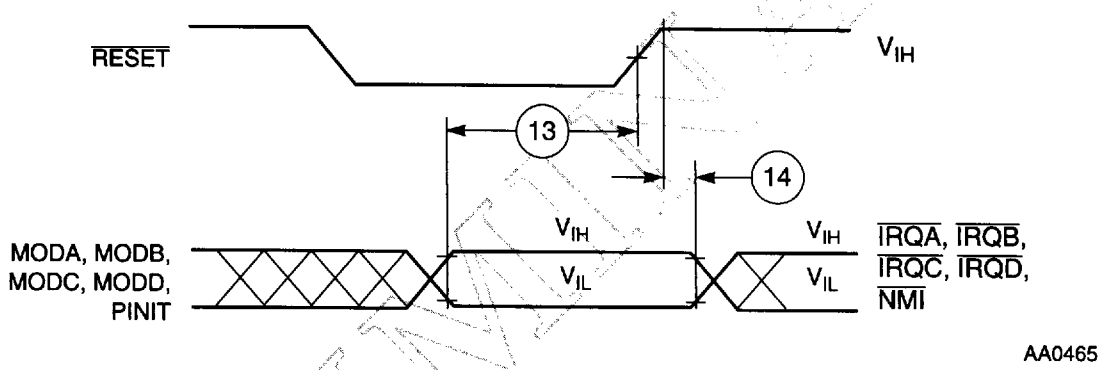


Figure 2-8 Operating Mode Select Timing

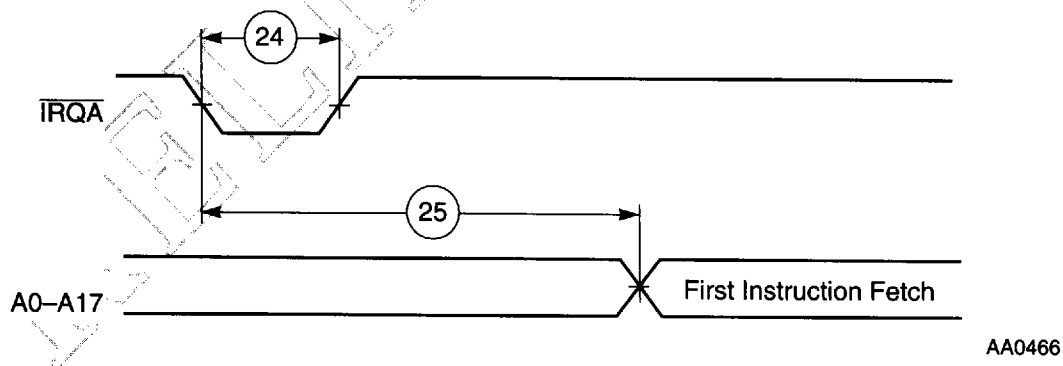


Figure 2-9 Recovery from Stop State Using IRQA

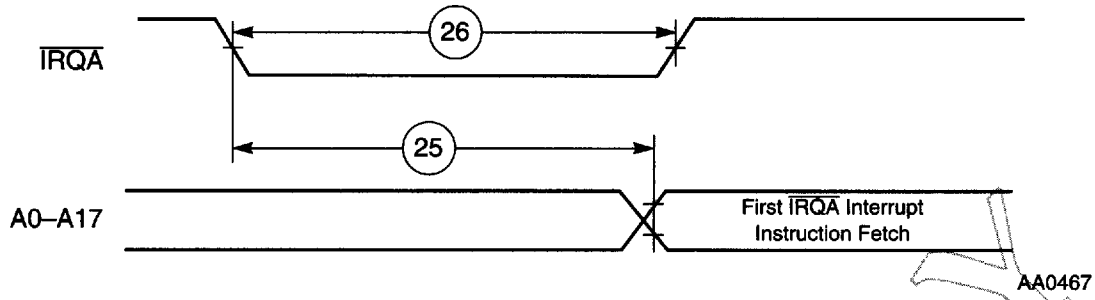


Figure 2-10 Recovery from Stop State Using IRQA Interrupt Service

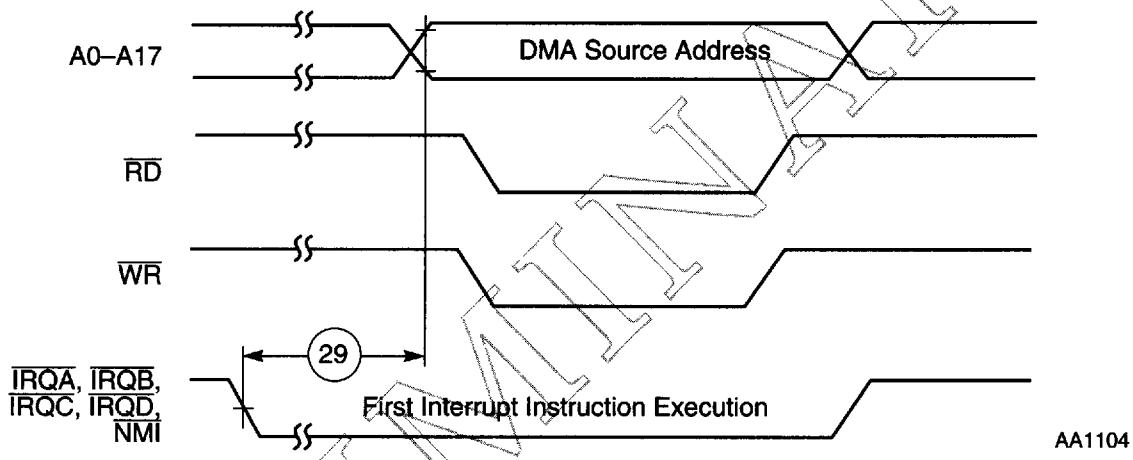


Figure 2-11 External Memory Access (DMA Source) Timing

EXTERNAL MEMORY EXPANSION PORT (PORT A)

SRAM Timing

Table 2-8 SRAM Read and Write Accesses

No.	Characteristics	Symbol	Expression[1]	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
100	Address valid and AA assertion pulse width	t_{RC}, t_{WC}	$(WS + 1) \times T_C - 4.0$ [$1 \le WS \le 3$]	26.3	—	21.0	—	16.0	—	ns
			$(WS + 2) \times T_C - 4.0$ [$4 \le WS \le 7$]	86.9	—	71.0	—	56.0	—	ns
			$(WS + 3) \times T_C - 4.0$ [$WS \ge 8$]	162.7	—	133.5	—	106.0	—	ns
101	Address and AA valid to $\overline{WR}$ assertion	t_{AS}	**66 MHz:** $0.25 \times T_C - 3.7$ [$WS = 1$]	0.1	—	—	—	—	—	ns
			80 MHz: $0.25 \times T_C - 3.0$ [$WS = 1$]	—	—	0.1	—	—	—	ns
			100 MHz: $0.25 \times T_C - 2.4$ [$WS = 1$]	—	—	—	—	0.1	—	ns
			All frequencies: $0.75 \times T_C - 4.0$ [$2 \le WS \le 3$]	7.4	—	5.4	—	3.5	—	ns
			$1.25 \times T_C - 4.0$ [$WS \ge 4$]	14.9	—	11.6	—	8.5	—	ns
102	$\overline{WR}$ assertion pulse width	t_{WP}	$1.5 \times T_C - 4.5$ [$WS = 1$]	18.2	—	14.3	—	10.5	—	ns
			$WS \times T_C - 4.0$ [$2 \le WS \le 3$]	26.3	—	21.0	—	16.0	—	ns
			$(WS - 0.5) \times T_C - 4.0$ [$WS \ge 4$]	49.0	—	39.8	—	31.0	—	ns

Table 2-8 SRAM Read and Write Accesses (Continued)

No.	Characteristics	Symbol	Expression[1]	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
103	$\overline{WR}$ deassertion to address not valid	t_{WR}	**66 MHz:** $0.25 \times T_C - 3.8$ $[1 \le WS \le 3]$	0.1	—	—	—	—	—	ns
			80 MHz: $0.25 \times T_C - 3.0$ $[1 \le WS \le 3]$	—	—	0.1	—	—	—	ns
			100 MHz: $0.25 \times T_C - 2.4$ $[1 \le WS \le 3]$	—	—	—	—	0.1	—	ns
			All frequencies: $1.25 \times T_C - 4.0$ $[4 \le WS \le 7]$	14.9	—	11.6	—	8.5	—	ns
			$2.25 \times T_C - 4.0$ $[WS \ge 8]$	30.1	—	24.1	—	18.5	—	ns
104	Address and AA valid to input data valid	t_{AA}, t_{AC}	**66 MHz:** $(WS + 0.75) \times T_C - 11.0$ $[WS \ge 1]$	—	15.5	—	—	—	—	ns
			80 MHz: $(WS + 0.75) \times T_C - 9.5$ $[WS \ge 1]$	—	—	—	12.4	—	—	ns
			100 MHz: $(WS + 0.75) \times T_C - 8.0$ $[WS \ge 1]$	—	—	—	—	—	9.5	ns
105	$\overline{RD}$ assertion to input data valid	t_{OE}	**66 MHz:** $(WS + 0.25) \times T_C - 11.0$ $[WS \ge 1]$	—	7.9	—	—	—	—	ns
			80 MHz: $(WS + 0.25) \times T_C - 9.5$ $[WS \ge 1]$	—	—	—	6.1	—	—	ns
			100 MHz: $(WS + 0.25) \times T_C - 8.0$ $[WS \ge 1]$	—	—	—	—	—	4.5	ns
106	$\overline{RD}$ deassertion to data not valid (data hold time)	t_{OHZ}		0.0	—	0.0	—	0.0	—	ns
107	Address valid to $\overline{WR}$ deassertion	t_{AW}	$(WS + 0.75) \times T_C - 4.0$ $[WS \ge 1]$	22.5	—	17.9	—	13.5	—	ns

Table 2-8 SRAM Read and Write Accesses (Continued)

No.	Characteristics	Symbol	Expression[1]	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
108	Data valid to $\overline{WR}$ deassertion (data setup time)	t_{DS} (t_{DW})	**66 MHz:** $(WS - 0.25) \times T_C - 3.9$ $[WS \geq 1]$	7.5	—	—	—	—	—	ns
			80 MHz: $(WS - 0.25) \times T_C - 3.3$ $[WS \geq 1]$	—	—	6.1	—	—	—	ns
			100 MHz: $(WS - 0.25) \times T_C - 2.75$ $[WS \geq 1]$	—	—	—	—	4.8	—	ns
109	Data hold time from $\overline{WR}$ deassertion	t_{DH}	**66 MHz:** $0.25 \times T_C - 3.7$ $[1 \leq WS \leq 3]$	0.1	—	—	—	—	—	ns
			80 MHz: $0.25 \times T_C - 3.0$ $[1 \leq WS \leq 3]$	—	—	0.1	—	—	—	ns
			100 MHz: $0.25 \times T_C - 2.4$ $[1 \leq WS \leq 3]$	—	—	—	—	0.1	—	ns
			All frequencies: $1.25 \times T_C - 3.8$ $[4 \leq WS \leq 7]$	15.2	—	11.8	—	8.7	—	ns
			$2.25 \times T_C - 3.8$ $[WS \geq 8]$	30.4	—	24.3	—	18.7	—	ns
110	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 3.7$ $[WS = 1]$	7.7	—	5.7	—	3.8	—	ns
			$0.25 \times T_C - 3.7$ $[2 \leq WS \leq 3]$	0.1	—	–0.6	—	–1.2	—	ns
			$-0.25 \times T_C - 3.7$ $[WS \geq 4]$	–7.5	—	–6.8	—	–6.2	—	ns
111	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C + 0.2$ $[1 \leq WS \leq 3]$	—	4.0	—	3.3	—	2.7	ns
			$1.25 \times T_C + 0.2$ $[4 \leq WS \leq 7]$	—	19.1	—	15.8	—	12.7	ns
			$2.25 \times T_C + 0.2$ $[WS \geq 8]$	—	34.3	—	28.3	—	22.7	ns
112	Previous $\overline{RD}$ deassertion to data active (write)		$1.25 \times T_C - 4.0$ $[1 \leq WS \leq 3]$	14.9	—	11.6	—	8.5	—	ns
			$2.25 \times T_C - 4.0$ $[4 \leq WS \leq 7]$	30.1	—	24.1	—	18.5	—	ns
			$3.25 \times T_C - 4.0$ $[WS \geq 8]$	45.2	—	36.6	—	28.5	—	ns

Table 2-8 SRAM Read and Write Accesses (Continued)

No.	Characteristics	Symbol	Expression[1]	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
113	$\overline{RD}$ deassertion time		$0.75 \times T_C - 4.0$ [$1 \le WS \le 3$]	7.4	—	5.4	—	3.5	—	ns
			$1.75 \times T_C - 4.0$ [$4 \le WS \le 7$]	22.5	—	17.9	—	13.5	—	ns
			$2.75 \times T_C - 4.0$ [$WS \ge 8$]	37.7	—	30.4	—	23.5	—	ns
114	$\overline{WR}$ deassertion time		$0.5 \times T_C - 3.5$ [$WS = 1$]	4.1	—	2.8	—	1.5	—	ns
			$T_C - 3.5$ [$2 \le WS \le 3$]	11.7	—	9.0	—	6.5	—	ns
			$2.5 \times T_C - 3.5$ [$4 \le WS \le 7$]	34.4	—	27.8	—	21.5	—	ns
			$3.5 \times T_C - 3.5$ [$WS \ge 8$]	49.5	—	40.3	—	31.5	—	ns
115	Address valid to $\overline{RD}$ assertion		$0.5 \times T_C - 4$	3.5	—	2.3	—	1.0	—	ns
116	$\overline{RD}$ assertion pulse width		$(WS + 0.25) \times T_C - 3.8$	15.1	—	11.8	—	8.7	—	ns
117	$\overline{RD}$ deassertion to address not valid		$0.25 \times T_C - 3.0$ [$1 \le WS \le 3$]	0.7	—	0.1	—	0.0	—	ns
			$1.25 \times T_C - 3.0$ [$4 \le WS \le 7$]	15.9	—	12.6	—	9.5	—	ns
			$2.25 \times T_C - 3.0$ [$WS \ge 8$]	31.0	—	25.1	—	19.5	—	ns

Notes: 1. WS is the number of wait states specified in the BCR.
2. $V_{CC} = 3.3\ V \pm 0.3\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF + 2$ TTL Loads

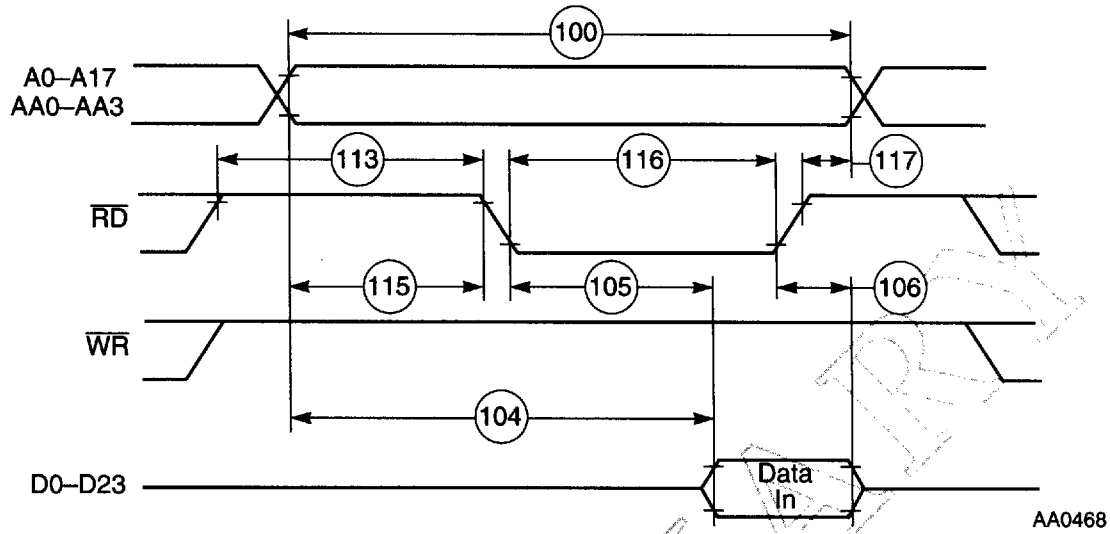


Figure 2-12 SRAM Read Access

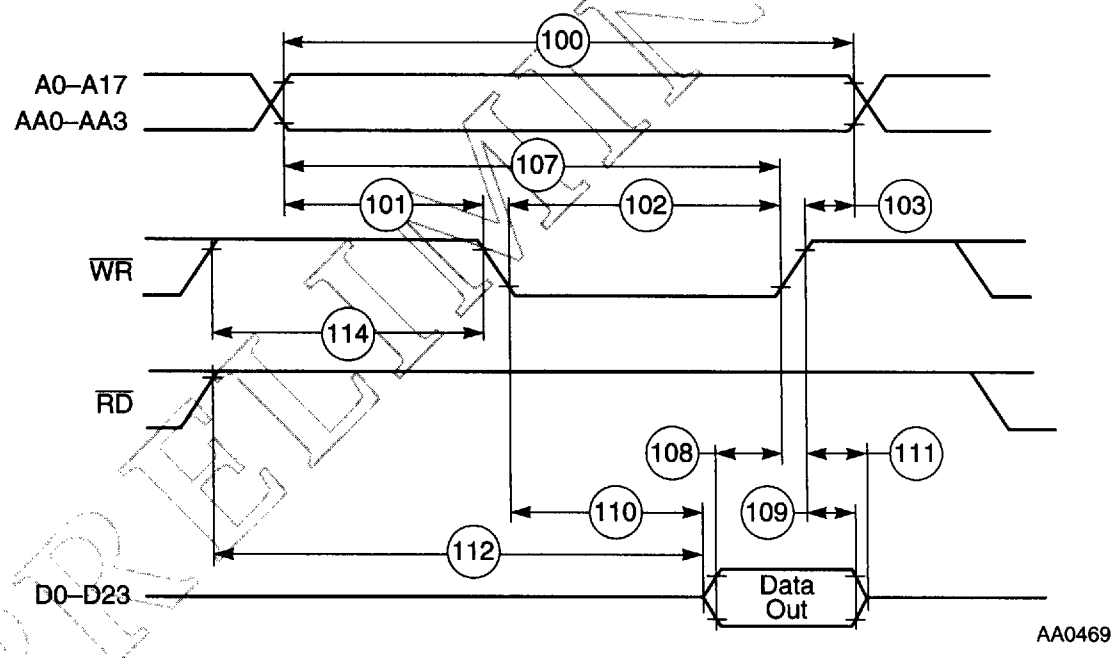


Figure 2-13 SRAM Write Access

DRAM Timing

The selection guides provided in **Figure 2-14** and **Figure 2-17** on page 2-37 should be used for primary selection only. Final selection should be based on the timing provided in the following tables. As an example, the selection guide suggests that 4 wait states must be used for 100 MHz operation when using Page Mode DRAM. However, by using the information in the appropriate table, a designer may choose to evaluate whether fewer wait states might be used by determining which timing prevents operation at 100 MHz, running the chip at a slightly lower frequency (e.g., 95 MHz), using faster DRAM (if it becomes available), and control factors such as capacitive and resistive load to improve overall system performance.

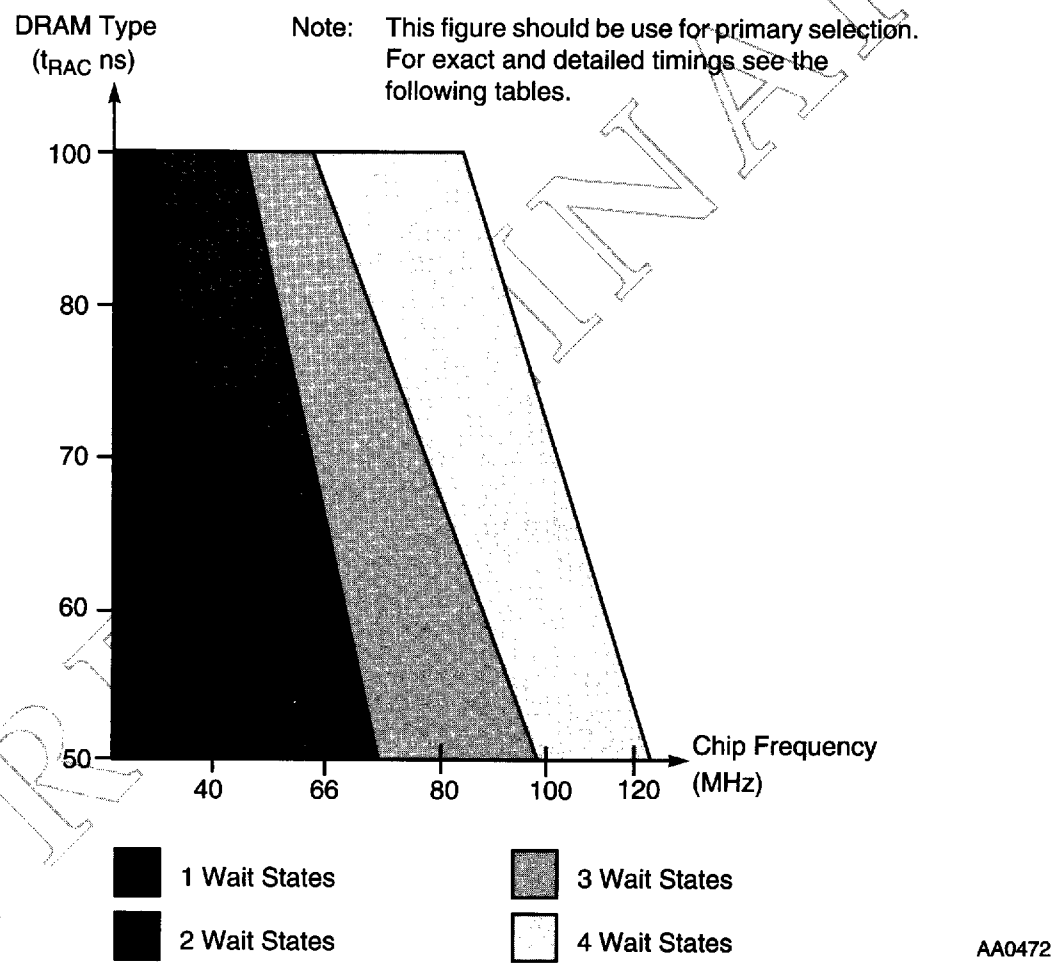


Figure 2-14 DRAM Page Mode Wait States Selection Guide

Table 2-9 DRAM Page Mode Timings, One Wait State (Low-Power Applications)[1, 2, 3]

No.	Characteristics	Symbol	Expression	20 MHz[6]		30 MHz[6]		Unit
				Min	Max	Min	Max	
131	Page mode cycle time	t_{PC}	$1.25 \times T_C$	62.5	—	41.7	—	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$T_C - 7.5$	—	42.5	—	25.8	ns
133	Column address valid to data valid (read)	t_{AA}	$1.5 \times T_C - 7.5$	—	67.5	—	42.5	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$2 \times T_C - 4.0$	96.0	—	62.7	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion[4]	t_{CRP}						
	• BRW[1:0] = 00		$1.75 \times T_C - 6.0$	81.5	—	52.3	—	ns
	• BRW[1:0] = 01		$3.25 \times T_C - 6.0$	156.5	—	102.2	—	ns
	• BRW[1:0] = 10		$4.25 \times T_C - 6.0$	206.5	—	135.5	—	ns
	• BRW[1:0] = 11		$6.25 \times T_C - 6.0$	306.5	—	202.1	—	ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$0.5 \times T_C - 4.0$	21.0	—	12.7	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.5 \times T_C - 4.0$	21.0	—	12.7	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$2 \times T_C - 4.0$	96.0	—	62.7	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$0.75 \times T_C - 3.8$	33.7	—	21.2	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.25 \times T_C - 3.7$	8.8	—	4.6	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$0.5 \times T_C - 4.2$	20.8	—	12.5	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$1.5 \times T_C - 4.5$	70.5	—	45.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$1.75 \times T_C - 4.3$	83.2	—	54.0	—	ns

Table 2-9 DRAM Page Mode Timings, One Wait State (Low-Power Applications)[1, 2, 3]

No.	Characteristics	Symbol	Expression	20 MHz[6]		30 MHz[6]		Unit
				Min	Max	Min	Max	
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$1.75 \times T_C - 4.3$	83.2	—	54.0	—	ns
149	Data valid to $\overline{CAS}$ assertion (Write)	t_{DS}	$0.25 \times T_C - 4.0$	8.5	—	4.3	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$0.75 \times T_C - 4.0$	33.5	—	21.0	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$T_C - 4.3$	45.7	—	29.0	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$1.5 \times T_C - 4.0$	71.0	—	46.0	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	$T_C - 7.5$	—	42.5	—	25.8	ns
154	$\overline{RD}$ deassertion to data not valid [5]	t_{GZ}		0.0	—	0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	37.2	—	24.7	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	12.5	—	8.3	ns

Notes:
1. The number of wait states for Page mode access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $2 \times T_C$ for read-after-read or write-after-write sequences).
4. BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
5. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
6. Reduced DSP clock speed allows use of Page Mode DRAM with one Wait state (see **Figure 2-14**).

Table 2-10 DRAM Page Mode Timings, Two Wait States[1, 2, 3, 7]

No.	Characteristics	Symbol	Expression	66 MHz		80 MHz		Unit
				Min	Max	Min	Max	
131	Page mode cycle time	t_{PC}	$2.75 \times T_C$	41.7	—	34.4	—	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	**66 MHz:** $1.5 \times T_C - 7.5$	—	15.2	—	—	ns
			80 MHz: $1.5 \times T_C - 6.5$	—	—	—	12.3	ns
133	Column address valid to data valid (read)	t_{AA}	**66 MHz:** $2.5 \times T_C - 7.5$	—	30.4	—	—	ns
			80 MHz: $2.5 \times T_C - 6.5$	—	—	—	24.8	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$1.75 \times T_C - 4.0$	22.5	—	17.9	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$3.25 \times T_C - 4.0$	45.2	—	36.6	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$1.5 \times T_C - 4.0$	18.7	—	14.8	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion[5]	t_{CRP}						
	• BRW[1:0] = 00		$2.0 \times T_C - 6.0$	24.4	—	19.0	—	ns
	• BRW[1:0] = 01		$3.5 \times T_C - 6.0$	47.2	—	37.8	—	ns
	• BRW[1:0] = 10		$4.5 \times T_C - 6.0$	62.4	—	50.3	—	ns
	• BRW[1:0] = 11		$6.5 \times T_C - 6.0$	92.8	—	75.3	—	ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.25 \times T_C - 4.0$	14.9	—	11.6	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	11.2	—	8.5	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$1.75 \times T_C - 4.0$	22.5	—	17.9	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$3 \times T_C - 4.0$	41.5	—	33.5	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 3.8$	15.1	—	11.8	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.5 \times T_C - 3.7$	3.9	—	2.6	—	ns
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$1.5 \times T_C - 4.2$	18.5	—	14.6	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$2.5 \times T_C - 4.5$	33.4	—	26.8	—	ns

Table 2-10 DRAM Page Mode Timings, Two Wait States[1, 2, 3, 7] (Continued)

No.	Characteristics	Symbol	Expression	66 MHz		80 MHz		Unit
				Min	Max	Min	Max	
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$2.75 \times T_C - 4.3$	37.4	—	30.1	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$2.5 \times T_C - 4.3$	33.6	—	27.0	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	**66 MHz:** $0.25 \times T_C - 3.7$ **80 MHz:** $0.25 \times T_C - 3.0$	0.1 —	— —	— 0.1	— —	ns ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$1.75 \times T_C - 4.0$	22.5	—	17.9	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$T_C - 4.3$	10.9	—	8.2	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$2.5 \times T_C - 4.0$	33.9	—	27.3	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	**66 MHz:** $1.75 \times T_C - 7.5$ **80 MHz:** $1.75 \times T_C - 6.5$	— —	19.0 —	— —	— 15.4	ns ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	11.1	—	9.1	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.8	—	3.1	ns

Notes:
1. The number of wait states for Page mode access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56303.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $3 \times T_C$ for read-after-read or write-after-write sequences).
5. BRW[1:0] (DRAM Control Register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
6. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
7. There are not any fast enough DRAMs to fit to two wait states Page mode @ 100MHz (see **Figure 2-14**)

Table 2-11 DRAM Page Mode Timings, Three Wait States[1, 2, 3]

No.	Characteristics	Symbol	Expression	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
131	Page mode cycle time	t_{PC}	$3.5 \times T_C$	53.0	—	43.8	—	35.0	—	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	**66 MHz:** $2 \times T_C - 7.5$	—	22.8	—	—	—	—	ns
			80 MHz: $2 \times T_C - 6.5$	—	—	—	18.5	—	—	ns
			100 MHz: $2 \times T_C - 5.7$	—	—	—	—	—	14.3	ns
133	Column address valid to data valid (read)	t_{AA}	**66 MHz:** $3 \times T_C - 7.5$	—	37.9	—	—	—	—	ns
			80 MHz: $3 \times T_C - 6.5$	—	—	—	31.0	—	—	ns
			100 MHz: $3 \times T_C - 5.7$	—	—	—	—	—	24.3	ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$2.5 \times T_C - 4.0$	33.9	—	27.3	—	21.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$4.5 \times T_C - 4.0$	64.2	—	52.3	—	41.0	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2 \times T_C - 4.0$	26.3	—	21.0	—	16.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion[5]	t_{CRP}								
	• BRW[1:0] = 00		$2.25 \times T_C - 6.0$	28.2	—	22.2	—	16.5	—	ns
	• BRW[1:0] = 01		$3.75 \times T_C - 6.0$	51.0	—	40.9	—	31.5	—	ns
	• BRW[1:0] = 10		$4.75 \times T_C - 6.0$	66.2	—	53.4	—	41.5	—	ns
	• BRW[1:0] = 11		$6.75 \times T_C - 6.0$	96.6	—	78.4	—	61.5	—	ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.5 \times T_C - 4.0$	18.7	—	14.8	—	11.0	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	11.2	—	8.5	—	6.0	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$2.5 \times T_C - 4.0$	33.9	—	27.3	—	21.0	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$4 \times T_C - 4.0$	56.6	—	46.0	—	36.0	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 3.8$	15.1	—	11.8	—	8.7	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.75 \times T_C - 3.7$	7.7	—	5.7	—	3.8	—	ns

Table 2-11 DRAM Page Mode Timings, Three Wait States[1, 2, 3] (Continued)

No.	Characteristics	Symbol	Expression	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$2.25 \times T_C - 4.2$	29.9	—	23.9	—	18.3	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$3.5 \times T_C - 4.5$	48.5	—	39.3	—	30.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$3.75 \times T_C - 4.3$	52.5	—	42.6	—	33.2	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$3.25 \times T_C - 4.3$	44.9	—	36.3	—	28.2	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.0$	3.6	—	2.3	—	1.0	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$2.5 \times T_C - 4.0$	33.9	—	27.3	—	21.0	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$1.25 \times T_C - 4.3$	14.6	—	11.3	—	8.2	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$3.5 \times T_C - 4.0$	49.0	—	39.8	—	31.0	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	**66 MHz:** $2.5 \times T_C - 7.5$	—	30.4	—	—	—	—	ns
			80 MHz: $2.5 \times T_C - 6.5$	—	—	—	24.8	—	—	ns
			100 MHz: $2.5 \times T_C - 5.7$	—	—	—	—	—	19.3	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	0.0	—	0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	11.1	—	9.1	—	7.2	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.8	—	3.1	—	2.5	ns

Notes:
1. The number of wait states for Page mode access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56303.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $4 \times T_C$ for read-after-read or write-after-write sequences).
5. BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of page-access.
6. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

Table 2-12 DRAM Page Mode Timings, Four Wait States[1, 2, 3]

No.	Characteristics	Symbol	Expression	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
131	Page mode cycle time	t_{PC}	$4.5 \times T_C$	68.2	—	56.3	—	45.0	—	ns
132	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	**66 MHz:** $2.75 \times T_C - 7.5$ **80 MHz:** $2.75 \times T_C - 6.5$ **100 MHz:** $2.75 \times T_C - 5.7$	 — — —	 34.2 — —	 — — —	 — 27.9 —	 — — —	 — — 21.8	 ns ns ns
133	Column address valid to data valid (read)	t_{AA}	**66 MHz:** $3.75 \times T_C - 7.5$ **80 MHz:** $3.75 \times T_C - 6.5$ **100 MHz:** $3.75 \times T_C - 5.7$	 — — —	 49.3 — —	 — — —	 — 40.4 —	 — — —	 — — 31.8	 ns ns ns
134	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	0.0	—	ns
135	Last $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$3.5 \times T_C - 4.0$	49.0	—	39.8	—	31.0	—	ns
136	Previous $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion	t_{RHCP}	$6 \times T_C - 4.0$	86.9	—	71.0	—	56.0	—	ns
137	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2.5 \times T_C - 4.0$	33.9	—	27.3	—	21.0	—	ns
138	Last $\overline{CAS}$ deassertion to $\overline{RAS}$ deassertion[5] • BRW[1:0] = 00 • BRW[1:0] = 01 • BRW[1:0] = 10 • BRW[1:0] = 11	t_{CRP}	 $2.75 \times T_C - 6.0$ $4.25 \times T_C - 6.0$ $5.25 \times T_C - 6.0$ $6.25 \times T_C - 6.0$	 35.8 58.6 73.8 89.0	 — — — —	 28.4 47.2 59.7 72.2	 — — — —	 21.5 36.5 46.5 56.5	 — — — —	 ns ns ns ns
139	$\overline{CAS}$ deassertion pulse width	t_{CP}	$2 \times T_C - 4.0$	26.3	—	21.0	—	16.0	—	ns
140	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$T_C - 4.0$	11.2	—	8.5	—	6.0	—	ns
141	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$3.5 \times T_C - 4.0$	49.0	—	39.8	—	31.0	—	ns
142	Last column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$5 \times T_C - 4.0$	71.8	—	58.5	—	46.0	—	ns
143	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.25 \times T_C - 3.8$	15.1	—	11.8	—	8.7	—	ns
144	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$1.25 \times T_C - 3.7$	15.2	—	11.9	—	8.8	—	ns

Table 2-12 DRAM Page Mode Timings, Four Wait States[1, 2, 3] (Continued)

No.	Characteristics	Symbol	Expression	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
145	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$3.25 \times T_C - 4.2$	45.0	—	36.4	—	28.3	—	ns
146	$\overline{WR}$ assertion pulse width	t_{WP}	$4.5 \times T_C - 4.5$	63.7	—	51.8	—	40.5	—	ns
147	Last $\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$4.75 \times T_C - 4.3$	67.7	—	55.1	—	43.2	—	ns
148	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$3.75 \times T_C - 4.3$	52.5	—	42.6	—	33.2	—	ns
149	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$0.5 \times T_C - 4.0$	3.6	—	2.3	—	1.0	—	ns
150	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$3.5 \times T_C - 4.0$	49.0	—	39.8	—	31.0	—	ns
151	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$1.25 \times T_C - 4.3$	14.6	—	11.3	—	8.2	—	ns
152	Last $\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$4.5 \times T_C - 4.0$	64.2	—	52.3	—	41.0	—	ns
153	$\overline{RD}$ assertion to data valid	t_{GA}	**66 MHz:** $3.25 \times T_C - 7.5$	—	41.7	—	—	—	—	ns
			80 MHz: $3.25 \times T_C - 6.5$	—	—	—	34.1	—	—	ns
			100 MHz: $3.25 \times T_C - 5.7$	—	—	—	—	—	26.8	ns
154	$\overline{RD}$ deassertion to data not valid[6]	t_{GZ}		0.0	—	0.0	—	0.0	—	ns
155	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	11.1	—	9.1	—	7.2	—	ns
156	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.8	—	3.1	—	2.5	ns

Notes:
1. The number of wait states for Page mode access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56303.
4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (e.g., t_{PC} equals $3 \times T_C$ for read-after-read or write-after-write sequences).
5. BRW[1:0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
6. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.

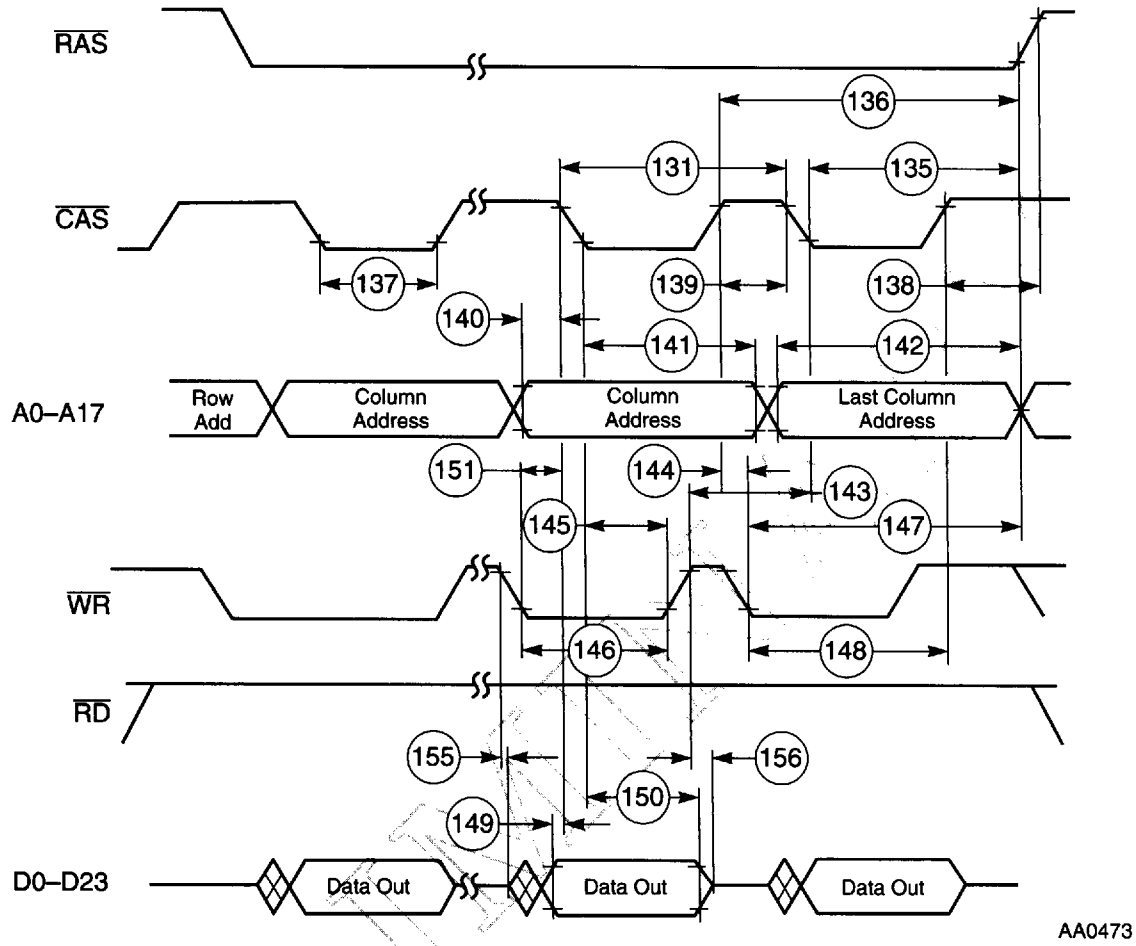


Figure 2-15 DRAM Page Mode Write Accesses

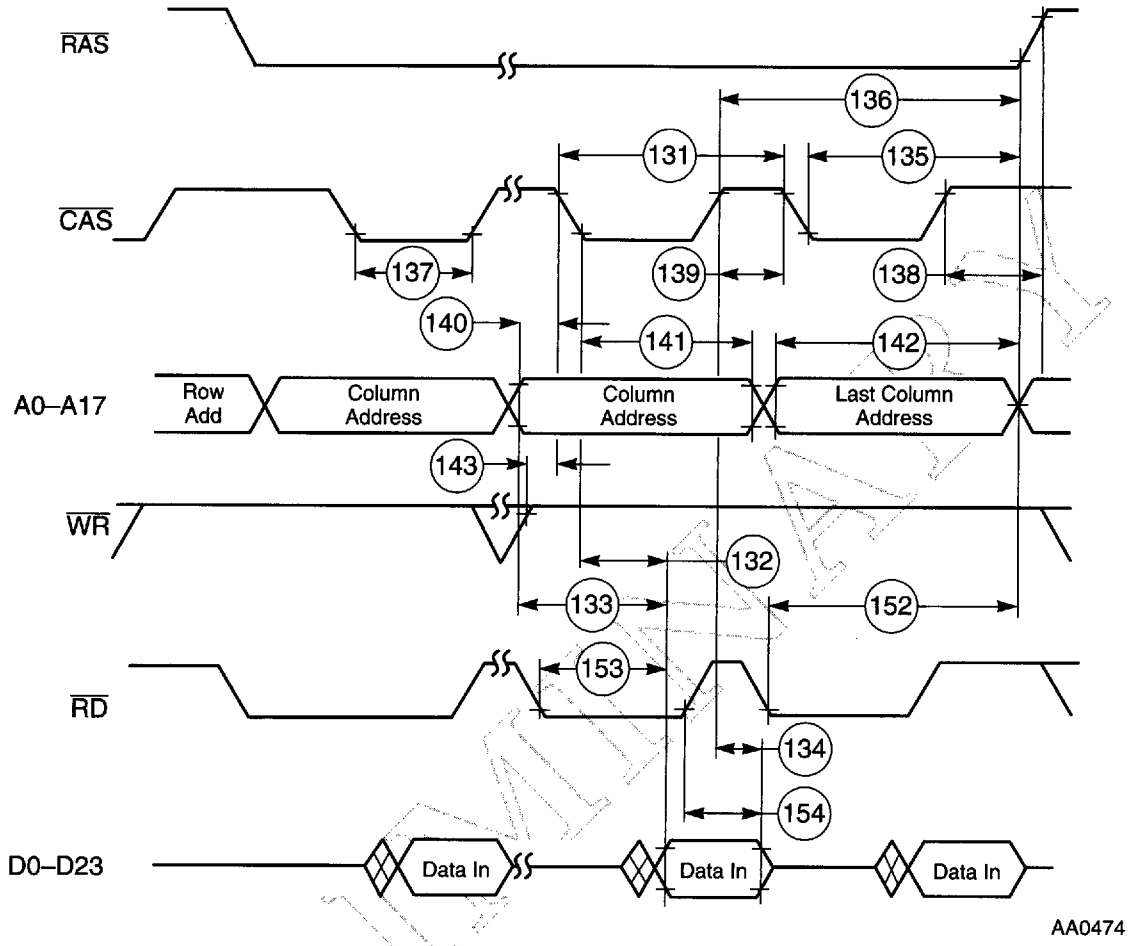


Figure 2-16 DRAM Page Mode Read Accesses

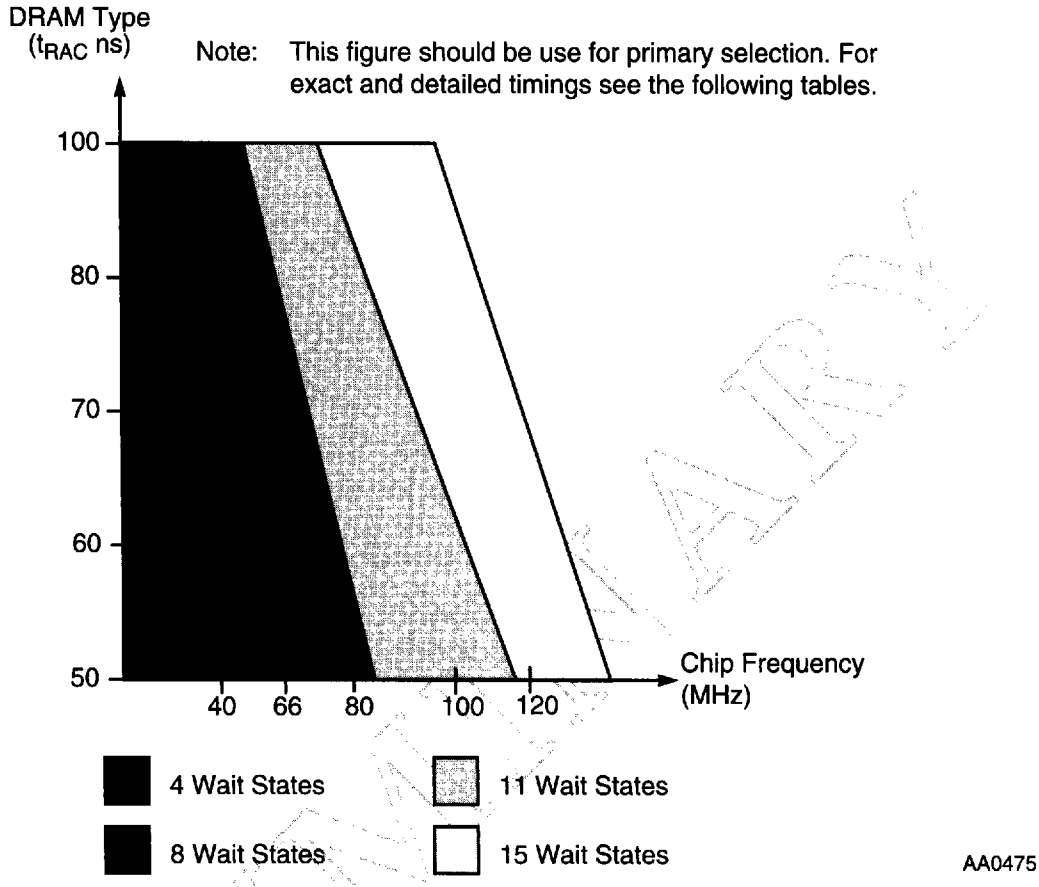


Figure 2-17 DRAM Out-of-Page Wait States Selection Guide

Table 2-13 DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2]

No.	Characteristics[3]	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
157	Random read or write cycle time	t_{RC}	$5 \times T_C$	250.0	—	166.7	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	$2.75 \times T_C - 7.5$	—	130.0	—	84.2	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	$1.25 \times T_C - 7.5$	—	55.0	—	34.2	ns
160	Column address valid to data valid (read)	t_{AA}	$1.5 \times T_C - 7.5$	—	67.5	—	42.5	ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	ns

Table 2-13 DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2] (Continued)

No.	Characteristics[3]	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$2.75 \times T_C - 4.0$	133.5	—	87.7	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$1.5 \times T_C \pm 2$	73.0	77.0	48.0	52.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$1.25 \times T_C \pm 2$	60.5	64.5	39.7	43.7	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$2.25 \times T_C - 4.0$	108.5	—	71.0	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.25 \times T_C - 4.0$	8.5	—	4.3	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$2 \times T_C - 4.0$	96.0	—	62.7	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$1.5 \times T_C - 3.8$	71.2	—	46.2	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$ assertion	t_{RCH}	$0.75 \times T_C - 3.7$	33.8	—	21.3	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$ assertion	t_{RRH}	$0.25 \times T_C - 3.7$	8.8	—	4.6	—	ns

Table 2-13 DRAM Out-of-Page and Refresh Timings, Four Wait States[1, 2] (Continued)

No.	Characteristics[3]	Symbol	Expression	20 MHz[4]		30 MHz[4]		Unit
				Min	Max	Min	Max	
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$1.5 \times T_C - 4.2$	70.8	—	45.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$3 \times T_C - 4.2$	145.8	—	95.8	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$4.5 \times T_C - 4.5$	220.5	—	145.5	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$4.75 \times T_C - 4.3$	233.2	—	154.0	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$4.25 \times T_C - 4.3$	208.2	—	137.4	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$2.25 \times T_C - 4.0$	108.5	—	71.0	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$1.75 \times T_C - 4.0$	83.5	—	54.3	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$3.25 \times T_C - 4.0$	158.5	—	104.3	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$3 \times T_C - 4.3$	145.7	—	95.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$0.5 \times T_C - 4.0$	21.0	—	12.7	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$1.25 \times T_C - 4.0$	58.5	—	37.7	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$4.5 \times T_C - 4.0$	221.0	—	146.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	$4 \times T_C - 7.5$	—	192.5	—	125.8	ns
193	$\overline{RD}$ deassertion to data not valid[3]	t_{GZ}		0.0	—	0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	37.2	—	24.7	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	12.5	—	8.3	ns

Notes:
1. The number of wait states for out of page access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
4. Reduced DSP clock speed allows use of DRAM out-of-page access with four Wait states (see **Figure 2-17**).

Table 2-14 DRAM Out-of-Page and Refresh Timings, Eight Wait States[1, 2]

No.	Characteristics[4]	Symbol	Expression[3]	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
157	Random read or write cycle time	t_{RC}	$9 \times T_C$	136.4	—	112.5	—	90.0	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	**66 MHz:** $4.75 \times T_C - 7.5$	—	64.5	—	—	—	—	ns
			80 MHz: $4.75 \times T_C - 6.5$	—	—	—	52.9	—	—	ns
			100 MHz: $4.75 \times T_C - 5.7$	—	—	—	—	—	41.8	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	**66 MHz:** $2.25 \times T_C - 7.5$	—	26.6	—	—	—	—	ns
			80 MHz: $2.25 \times T_C - 6.5$	—	—	—	21.6	—	—	ns
			100 MHz: $2.25 \times T_C - 5.7$	—	—	—	—	—	16.8	ns
160	Column address valid to data valid (read)	t_{AA}	**66 MHz:** $3 \times T_C - 7.5$	—	40.0	—	—	—	—	ns
			80 MHz: $3 \times T_C - 6.5$	—	—	—	31.0	—	—	ns
			100 MHz: $3 \times T_C - 5.7$	—	—	—	—	—	24.3	ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$3.25 \times T_C - 4.0$	45.2	—	36.6	—	28.5	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$5.75 \times T_C - 4.0$	83.1	—	67.9	—	53.5	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$3.25 \times T_C - 4.0$	45.2	—	36.6	—	28.5	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$4.75 \times T_C - 4.0$	68.0	—	55.4	—	43.5	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$2.25 \times T_C - 4.0$	30.1	—	24.1	—	18.5	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$2.5 \times T_C \pm 2$	35.9	39.9	29.3	33.3	23.0	27.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$1.75 \times T_C \pm 2$	24.5	28.5	19.9	23.9	15.5	19.5	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$4.25 \times T_C - 4.0$	59.8	—	49.1	—	38.5	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$2.75 \times T_C - 4.0$	37.7	—	30.4	—	23.5	—	ns

Table 2-14 DRAM Out-of-Page and Refresh Timings, Eight Wait States[1, 2] (Continued)

No.	Characteristics[4]	Symbol	Expression[3]	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$3.25 \times T_C - 4.0$	45.2	—	36.6	—	28.5	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$1.75 \times T_C - 4.0$	22.5	—	17.9	—	13.5	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	7.4	—	5.4	—	3.5	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$3.25 \times T_C - 4.0$	45.2	—	36.6	—	28.5	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$5.75 \times T_C - 4.0$	83.1	—	67.9	—	53.5	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$4 \times T_C - 4.0$	56.6	—	46.0	—	36.0	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$2 \times T_C - 3.8$	26.5	—	21.2	—	16.2	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RCH}	$1.25 \times T_C - 3.7$	15.2	—	11.9	—	8.8	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RRH}	**66 MHz:** $0.25 \times T_C - 3.7$	0.1	—	—	—	—	—	ns
			80 MHz: $0.25 \times T_C - 3.0$	—	—	0.1	—	—	—	ns
			100 MHz: $0.25 \times T_C - 2.4$	—	—	—	—	0.1	—	ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$3 \times T_C - 4.2$	41.3	—	33.3	—	25.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$5.5 \times T_C - 4.2$	79.1	—	64.6	—	50.8	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$8.5 \times T_C - 4.5$	124.3	—	101.8	—	80.5	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$8.75 \times T_C - 4.3$	128.3	—	105.1	—	83.2	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$7.75 \times T_C - 4.3$	113.1	—	92.6	—	73.2	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$4.75 \times T_C - 4.0$	68.0	—	55.4	—	43.5	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$3.25 \times T_C - 4.0$	45.2	—	36.6	—	28.5	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$5.75 \times T_C - 4.0$	83.1	—	67.9	—	53.5	—	ns

Table 2-14 DRAM Out-of-Page and Refresh Timings, Eight Wait States[1, 2] (Continued)

No.	Characteristics[4]	Symbol	Expression[3]	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$5.5 \times T_C - 4.3$	79.0	—	64.5	—	50.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	18.7	—	14.8	—	11.0	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$1.75 \times T_C - 4.0$	22.5	—	17.9	—	13.5	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$8.5 \times T_C - 4.0$	124.8	—	102.3	—	81.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	**66 MHz:** $7.5 \times T_C - 7.5$	—	106.1	—	—	—	—	ns
			80 MHz: $7.5 \times T_C - 6.5$	—	—	—	87.3	—	—	ns
			100 MHz: $7.5 \times T_C - 5.7$	—	—	—	—	—	69.3	ns
193	$\overline{RD}$ deassertion to data not valid[4]	t_{GZ}	0.0	0.0	—	0.0	—	0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	11.1	—	9.1	—	7.2	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.8	—	3.1	—	2.5	ns

Notes:
1. The number of wait states for out-of-page access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56303.
4. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
5. Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

Table 2-15 DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2]

No.	Characteristics[4]	Symbol	Expression[3]	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
157	Random read or write cycle time	t_{RC}	$12 \times T_C$	181.8	—	150.0	—	120.0	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	**66 MHz:** $6.25 \times T_C - 7.5$	—	87.2	—	—	—	—	ns
			80 MHz: $6.25 \times T_C - 6.5$	—	—	—	71.6	—	—	ns
			100 MHz: $6.25 \times T_C - 5.7$	—	—	—	—	—	56.8	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	**66 MHz:** $3.75 \times T_C - 7.5$	—	49.3	—	—	—	—	ns
			80 MHz: $3.75 \times T_C - 6.5$	—	—	—	40.4	—	—	ns
			100 MHz: $3.75 \times T_C - 5.7$	—	—	—	—	—	31.8	ns
160	Column address valid to data valid (read)	t_{AA}	**66 MHz:** $4.5 \times T_C - 7.5$	—	60.7	—	—	—	—	ns
			80 MHz: $4.5 \times T_C - 6.5$	—	—	—	49.8	—	—	ns
			100 MHz: $4.5 \times T_C - 5.7$	—	—	—	—	—	39.3	ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}		0.0	—	0.0	—	0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$4.25 \times T_C - 4.0$	60.4	—	49.1	—	38.5	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$7.75 \times T_C - 4.0$	113.4	—	92.9	—	73.5	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$5.25 \times T_C - 4.0$	75.5	—	61.6	—	48.5	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$6.25 \times T_C - 4.0$	90.7	—	74.1	—	58.5	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$3.75 \times T_C - 4.0$	52.8	—	42.9	—	33.5	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$2.5 \times T_C \pm 2$	35.9	39.9	29.3	33.3	23.0	27.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$1.75 \times T_C \pm 2$	24.5	28.5	19.9	23.9	15.5	19.5	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$5.75 \times T_C - 4.0$	83.1	—	67.9	—	53.5	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$4.25 \times T_C - 4.0$	60.4	—	49.1	—	38.5	—	ns

Table 2-15 DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2] (Continued)

No.	Characteristics[4]	Symbol	Expression[3]	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$4.25 \times T_C - 4.0$	60.4	—	49.1	—	38.5	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$1.75 \times T_C - 4.0$	22.5	—	17.9	—	13.5	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	7.4	—	5.4	—	3.5	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$5.25 \times T_C - 4.0$	75.5	—	61.6	—	48.5	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$7.75 \times T_C - 4.0$	113.4	—	92.9	—	73.5	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$6 \times T_C - 4.0$	86.9	—	71.0	—	56.0	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$3.0 \times T_C - 3.8$	41.7	—	33.7	—	26.2	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RCH}	$1.75 \times T_C - 3.7$	22.8	—	18.2	—	13.8	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RRH}	**66 MHz:** $0.25 \times T_C - 3.7$	0.1	—	—	—	—	—	ns
			80 MHz: $0.25 \times T_C - 3.0$	—	—	0.1	—	—	—	ns
			100 MHz: $0.25 \times T_C - 2.4$	—	—	—	—	0.1	—	ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$5 \times T_C - 4.2$	71.6	—	58.3	—	45.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$7.5 \times T_C - 4.2$	109.4	—	89.6	—	70.8	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$11.5 \times T_C - 4.5$	169.7	—	139.3	—	110.5	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$11.75 \times T_C - 4.3$	173.7	—	142.7	—	113.2	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	$10.25 \times T_C - 4.3$	151.0	—	130.1	—	103.2	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$5.75 \times T_C - 4.0$	83.1	—	67.9	—	53.5	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$5.25 \times T_C - 4.0$	75.5	—	61.6	—	48.5	—	ns
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$7.75 \times T_C - 4.0$	113.4	—	92.9	—	73.5	—	ns

Table 2-15 DRAM Out-of-Page and Refresh Timings, Eleven Wait States[1, 2] (Continued)

No.	Characteristics[4]	Symbol	Expression[3]	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$6.5 \times T_C - 4.3$	94.2	—	77.0	—	60.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	18.7	—	14.8	—	11.0	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$2.75 \times T_C - 4.0$	37.7	—	30.4	—	23.5	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$11.5 \times T_C - 4.0$	170.2	—	139.8	—	111.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	**66 MHz**: $10 \times T_C - 7.5$ **80 MHz**: $10 \times T_C - 6.5$ **100 MHz**: $10 \times T_C - 5.7$	— — —	144.0 — —	— — —	— 118.5 —	— — —	— — 94.3	ns ns ns
193	$\overline{RD}$ deassertion to data not valid[4]	t_{GZ}		0.0	—	0.0	—	0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	11.1	—	9.1	—	7.2	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.8	—	3.1	—	2.5	ns

Notes:
1. The number of wait states for out-of-page access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. The asynchronous delays specified in the expressions are valid for DSP56303.
4. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
5. Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

Table 2-16 DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2]

No.	Characteristics[3]	Symbol	Expression	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
157	Random read or write cycle time	t_{RC}	$16 \times T_C$	242.4	—	200.0	—	160.0	—	ns
158	$\overline{RAS}$ assertion to data valid (read)	t_{RAC}	**66 MHz:** $8.25 \times T_C - 7.5$	—	117.5	—	—	—	—	ns
			80 MHz: $8.25 \times T_C - 6.5$	—	—	—	96.6	—	—	ns
			100 MHz: $8.25 \times T_C - 5.7$	—	—	—	—	—	76.8	ns
159	$\overline{CAS}$ assertion to data valid (read)	t_{CAC}	**66 MHz:** $4.75 \times T_C - 7.5$	—	64.5	—	—	—	—	ns
			80 MHz: $4.75 \times T_C - 6.5$	—	—	—	52.9	—	—	ns
			100 MHz: $4.75 \times T_C - 5.7$	—	—	—	—	—	41.8	ns
160	Column address valid to data valid (read)	t_{AA}	**66 MHz:** $5.5 \times T_C - 7.5$	—	75.8	—	—	—	—	ns
			80 MHz: $5.5 \times T_C - 6.5$	—	—	—	62.3	—	—	ns
			100 MHz: $5.5 \times T_C - 5.7$	—	—	—	—	—	49.3	ns
161	$\overline{CAS}$ deassertion to data not valid (read hold time)	t_{OFF}	0.0	0.0	—	0.0	—	0.0	—	ns
162	$\overline{RAS}$ deassertion to $\overline{RAS}$ assertion	t_{RP}	$6.25 \times T_C - 4.0$	90.7	—	74.1	—	58.5	—	ns
163	$\overline{RAS}$ assertion pulse width	t_{RAS}	$9.75 \times T_C - 4.0$	143.7	—	117.9	—	93.5	—	ns
164	$\overline{CAS}$ assertion to $\overline{RAS}$ deassertion	t_{RSH}	$6.25 \times T_C - 4.0$	90.7	—	74.1	—	58.5	—	ns
165	$\overline{RAS}$ assertion to $\overline{CAS}$ deassertion	t_{CSH}	$8.25 \times T_C - 4.0$	121.0	—	99.1	—	78.5	—	ns
166	$\overline{CAS}$ assertion pulse width	t_{CAS}	$4.75 \times T_C - 4.0$	68.0	—	55.4	—	43.5	—	ns
167	$\overline{RAS}$ assertion to $\overline{CAS}$ assertion	t_{RCD}	$3.5 \times T_C \pm 2$	51.0	55.0	41.8	45.8	33.0	37.0	ns
168	$\overline{RAS}$ assertion to column address valid	t_{RAD}	$2.75 \times T_C \pm 2$	39.7	43.7	32.4	36.4	25.5	29.5	ns
169	$\overline{CAS}$ deassertion to $\overline{RAS}$ assertion	t_{CRP}	$7.75 \times T_C - 4.0$	113.4	—	92.9	—	73.5	—	ns
170	$\overline{CAS}$ deassertion pulse width	t_{CP}	$6.25 \times T_C - 4.0$	90.7	—	74.1	—	58.5	—	ns

Table 2-16 DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2] (Continued)

No.	Characteristics[3]	Symbol	Expression	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
171	Row address valid to $\overline{RAS}$ assertion	t_{ASR}	$6.25 \times T_C - 4.0$	90.7	—	74.1	—	58.5	—	ns
172	$\overline{RAS}$ assertion to row address not valid	t_{RAH}	$2.75 \times T_C - 4.0$	37.7	—	30.4	—	23.5	—	ns
173	Column address valid to $\overline{CAS}$ assertion	t_{ASC}	$0.75 \times T_C - 4.0$	7.4	—	5.4	—	3.5	—	ns
174	$\overline{CAS}$ assertion to column address not valid	t_{CAH}	$6.25 \times T_C - 4.0$	90.7	—	74.1	—	58.5	—	ns
175	$\overline{RAS}$ assertion to column address not valid	t_{AR}	$9.75 \times T_C - 4.0$	143.7	—	117.9	—	93.5	—	ns
176	Column address valid to $\overline{RAS}$ deassertion	t_{RAL}	$7 \times T_C - 4.0$	102.1	—	83.5	—	66.0	—	ns
177	$\overline{WR}$ deassertion to $\overline{CAS}$ assertion	t_{RCS}	$5 \times T_C - 3.8$	72.0	—	58.7	—	46.2	—	ns
178	$\overline{CAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RCH}	$1.75 \times T_C - 3.7$	22.8	—	18.2	—	13.8	—	ns
179	$\overline{RAS}$ deassertion to $\overline{WR}$[5] assertion	t_{RRH}	**66 MHz:** $0.25 \times T_C - 3.7$	0.1	—	—	—	—	—	ns
			80 MHz: $0.25 \times T_C - 3.0$	—	—	0.1	—	—	—	ns
			100 MHz: $0.25 \times T_C - 2.4$	—	—	—	—	0.1	—	ns
180	$\overline{CAS}$ assertion to $\overline{WR}$ deassertion	t_{WCH}	$6 \times T_C - 4.2$	86.7	—	70.8	—	55.8	—	ns
181	$\overline{RAS}$ assertion to $\overline{WR}$ deassertion	t_{WCR}	$9.5 \times T_C - 4.2$	139.7	—	114.6	—	90.8	—	ns
182	$\overline{WR}$ assertion pulse width	t_{WP}	$15.5 \times T_C - 4.5$	230.3	—	189.3	—	150.5	—	ns
183	$\overline{WR}$ assertion to $\overline{RAS}$ deassertion	t_{RWL}	$15.75 \times T_C - 4.3$	234.3	—	192.6	—	153.2	—	ns
184	$\overline{WR}$ assertion to $\overline{CAS}$ deassertion	t_{CWL}	**66–80 MHz:** $14.25 \times T_C - 4.3$	211.6	—	180.1	—	—	—	ns
			100 MHz: $14.75 \times T_C - 4.3$	—	—	—	—	143.2	—	ns
185	Data valid to $\overline{CAS}$ assertion (write)	t_{DS}	$8.75 \times T_C - 4.0$	128.6	—	105.4	—	83.5	—	ns
186	$\overline{CAS}$ assertion to data not valid (write)	t_{DH}	$6.25 \times T_C - 4.0$	90.7	—	74.1	—	58.5	—	ns

Table 2-16 DRAM Out-of-Page and Refresh Timings, Fifteen Wait States[1, 2] (Continued)

No.	Characteristics[3]	Symbol	Expression	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
187	$\overline{RAS}$ assertion to data not valid (write)	t_{DHR}	$9.75 \times T_C - 4.0$	143.7	—	117.9	—	93.5	—	ns
188	$\overline{WR}$ assertion to $\overline{CAS}$ assertion	t_{WCS}	$9.5 \times T_C - 4.3$	139.6	—	114.5	—	90.7	—	ns
189	$\overline{CAS}$ assertion to $\overline{RAS}$ assertion (refresh)	t_{CSR}	$1.5 \times T_C - 4.0$	18.7	—	14.8	—	11.0	—	ns
190	$\overline{RAS}$ deassertion to $\overline{CAS}$ assertion (refresh)	t_{RPC}	$4.75 \times T_C - 4.0$	68.0	—	55.4	—	43.5	—	ns
191	$\overline{RD}$ assertion to $\overline{RAS}$ deassertion	t_{ROH}	$15.5 \times T_C - 4.0$	230.8	—	189.8	—	151.0	—	ns
192	$\overline{RD}$ assertion to data valid	t_{GA}	**66 MHz:** $14 \times T_C - 7.5$ **80 MHz:** $14 \times T_C - 6.5$ **100 MHz:** $14 \times T_C - 5.7$	— — —	204.6 — —	— — —	— 168.5 —	— — —	— — 134.3	ns ns ns
193	$\overline{RD}$ deassertion to data not valid[3]	t_{GZ}		0.0	—	0.0	—	0.0	—	ns
194	$\overline{WR}$ assertion to data active		$0.75 \times T_C - 0.3$	11.1	—	9.1	—	7.2	—	ns
195	$\overline{WR}$ deassertion to data high impedance		$0.25 \times T_C$	—	3.8	—	3.1	—	2.5	ns

Notes:
1. The number of wait states for out-of-page access is specified in the DCR.
2. The refresh period is specified in the DCR.
3. $\overline{RD}$ deassertion will always occur after $\overline{CAS}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}.
4. Either t_{RCH} or t_{RRH} must be satisfied for read cycles.

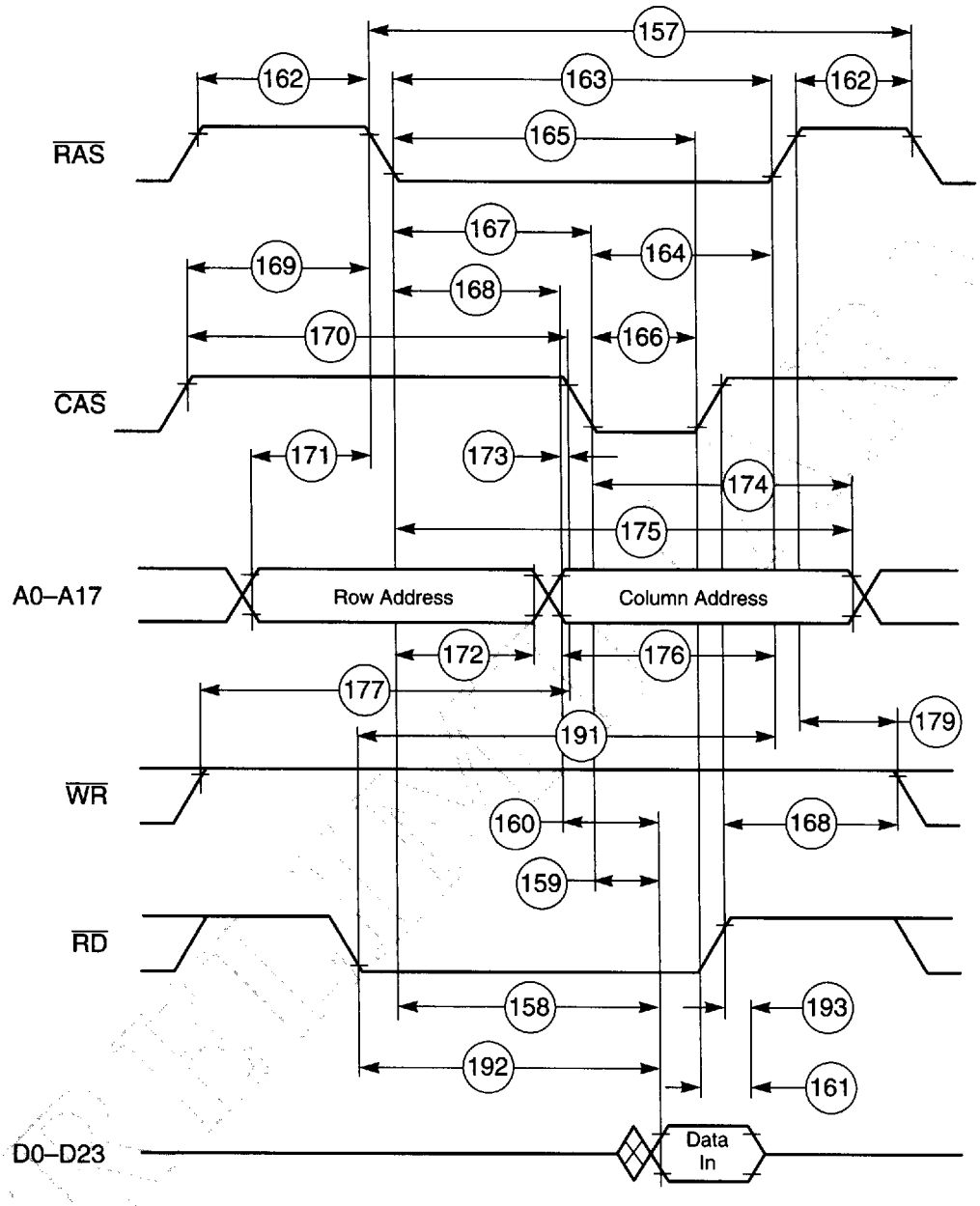


Figure 2-18 DRAM Out-of-Page Read Access

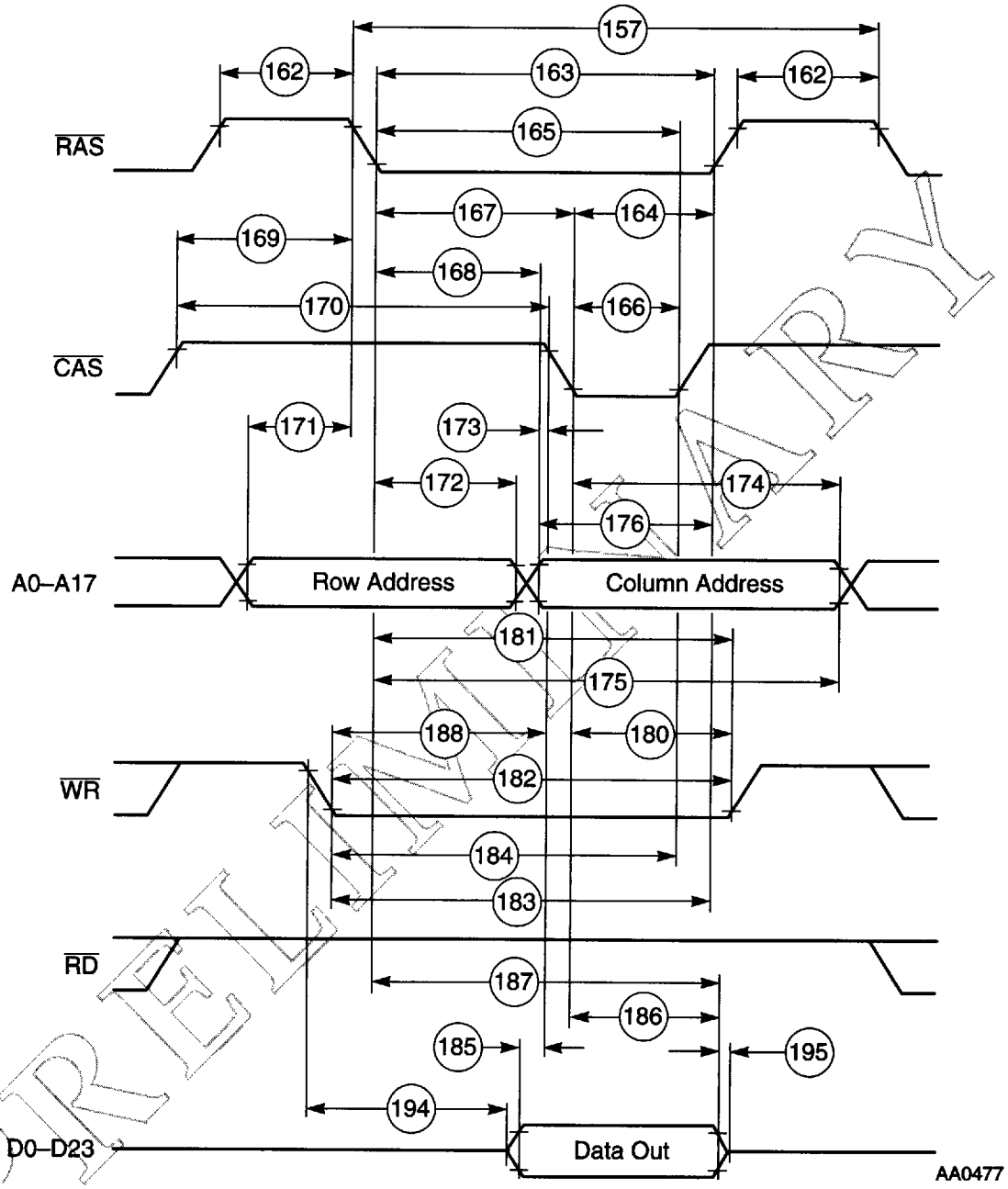


Figure 2-19 DRAM Out-of-Page Write Access

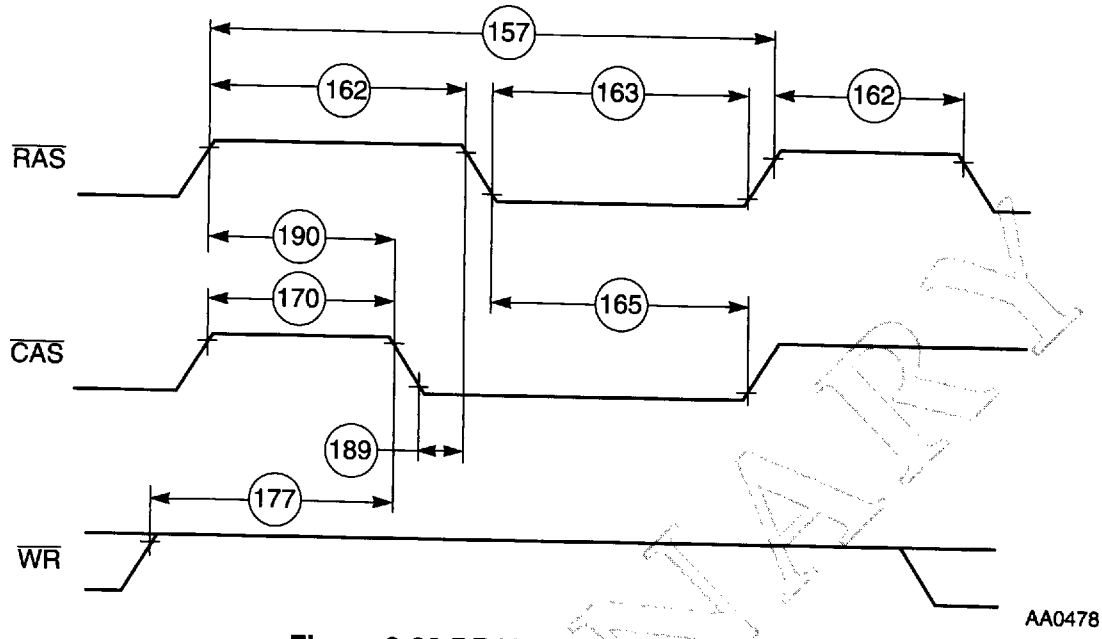


Figure 2-20 DRAM Refresh Access

Synchronous Timings (SRAM)

Table 2-17 External Bus Synchronous Timings (SRAM Access)[4]

No.	Characteristics	Expression[1, 2]	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
198	CLKOUT high to address, and AA valid[5]	**66 MHz:** $0.25 \times T_C + 5.0$	—	8.8	—	—	—	—	ns
		80 MHz: $0.25 \times T_C + 4.5$	—	—	—	7.6	—	—	ns
		100 MHz: $0.25 \times T_C + 4.0$	—	—	—	—	—	6.5	ns
199	CLKOUT high to address, and AA invalid[5]	$0.25 \times T_C$	3.8	—	3.1	—	2.5	—	ns
200	$\overline{TA}$ valid to CLKOUT high (setup time)		6.0	—	5.0	—	4.0	—	ns
201	CLKOUT high to $\overline{TA}$ invalid (hold time)		0.0	—	0.0	—	0.0	—	ns
202	CLKOUT high to data out active	$0.25 \times T_C$	3.8	—	3.1	—	2.5	—	ns
203	CLKOUT high to data out valid	**66 MHz:** $0.25 \times T_C + 5.0$	4.8	8.8	—	—	—	—	ns
		80 MHz: $0.25 \times T_C + 4.5$	—	—	4.1	7.6	—	—	ns
		100 MHz: $0.25 \times T_C + 4.0$	—	—	—	—	3.3	6.5	ns
204	CLKOUT high to data out invalid	$0.25 \times T_C$	3.8	—	3.1	—	2.5	—	ns
205	CLKOUT high to data out high impedance	**66 MHz:** $0.25 \times T_C + 1.0$	—	4.8	—	—	—	—	ns
		80 MHz: $0.25 \times T_C + 0.5$	—	—	—	3.6	—	—	ns
		100 MHz: $0.25 \times T_C$	—	—	—	—	—	2.5	ns
206	Data in valid to CLKOUT high (setup)		6.0	—	5.0	—	4.0	—	ns
207	CLKOUT high to data in invalid (hold)		0.0	—	0.0	—	0.0	—	ns
208	CLKOUT high to $\overline{RD}$ assertion	**66 MHz:** $0.75 \times T_C + 5.0$	12.4	16.4	—	—	—	—	ns
		80 MHz: $0.75 \times T_C + 4.5$	—	—	10.4	13.9	—	—	ns
		100 MHz: $0.75 \times T_C + 4.0$	—	—	—	—	8.2	11.5	ns
209	CLKOUT high to $\overline{RD}$ deassertion		0.0	5.0	0.0	4.5	0.0	4.0	ns

Table 2-17 External Bus Synchronous Timings (SRAM Access)[4] (Continued)

No.	Characteristics	Expression[1, 2]	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
210	CLKOUT high to $\overline{WR}$ assertion[3]	**66 MHz:** $0.5 \times T_C + 5.3$ [WS = 1 or WS ≥ 4]	8.9	12.9	—	—	—	—	ns
		80 MHz: $0.5 \times T_C + 4.8$ [WS = 1 or WS ≥ 4]	—	—	7.6	11.1	—	—	ns
		100 MHz: $0.5 \times T_C + 4.3$ [WS = 1 or WS ≥ 4]	—	—	—	—	6.3	9.3	ns
		All frequencies: [2 ≤ WS ≤ 3]	1.3	5.3	1.3	4.8	1.3	4.3	ns
211	CLKOUT high to $\overline{WR}$ deassertion		0.0	4.8	0.0	4.3	0.0	3.8	ns

Notes:
1. WS is the number of wait states specified in the BCR.
2. The asynchronous delays specified in the expressions are valid for DSP56303.
3. If WS > 1, $\overline{WR}$ assertion refers to the next rising edge of CLKOUT.
4. External bus synchronous timings should be used only for reference to the clock and *not* for relative timings.
5. T198 and T199 are valid for Address Trace mode if the ATE bit in the OMR is set. Use the status of $\overline{BR}$ (See T212) to determine whether the access referenced by A0–A23 is internal or external, when this mode is enabled

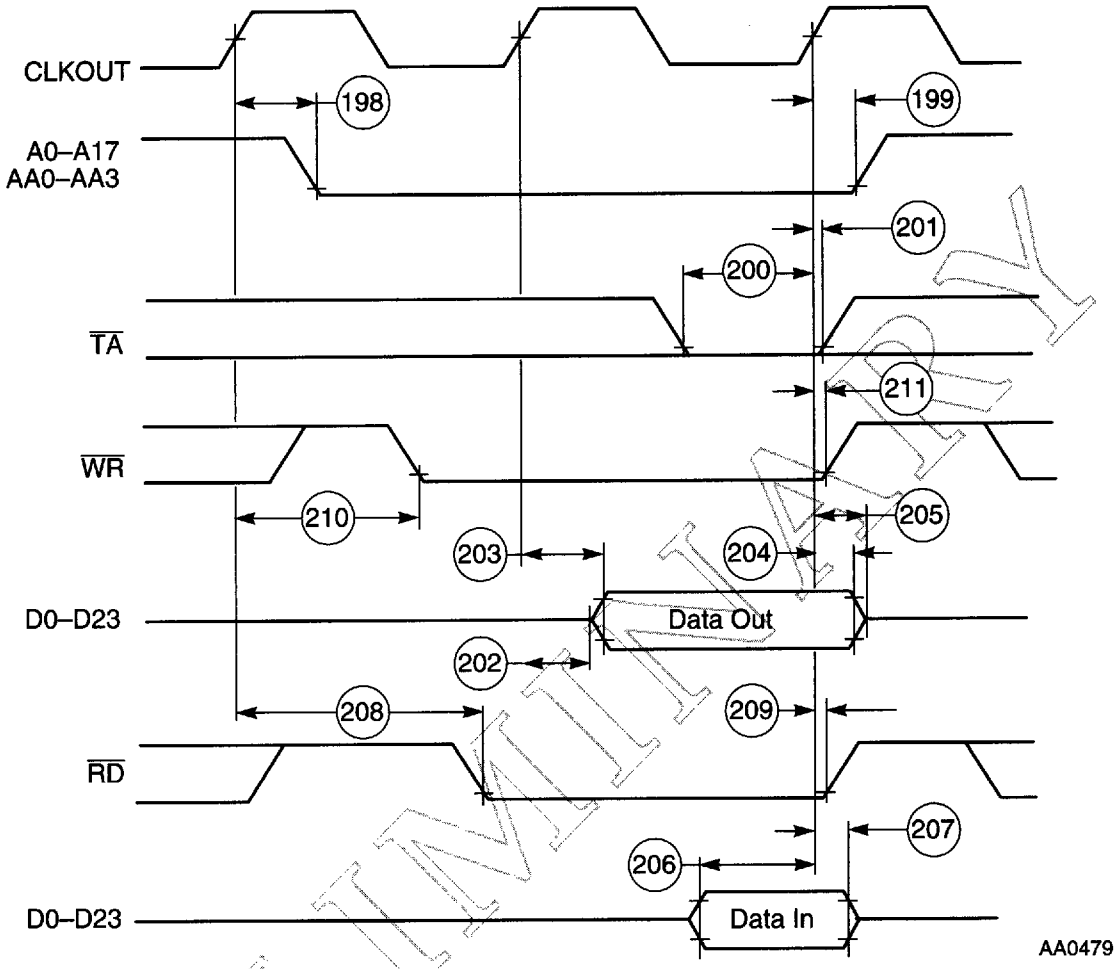


Figure 2-21 Synchronous Bus Timings SRAM 1 WS (BCR Controlled)

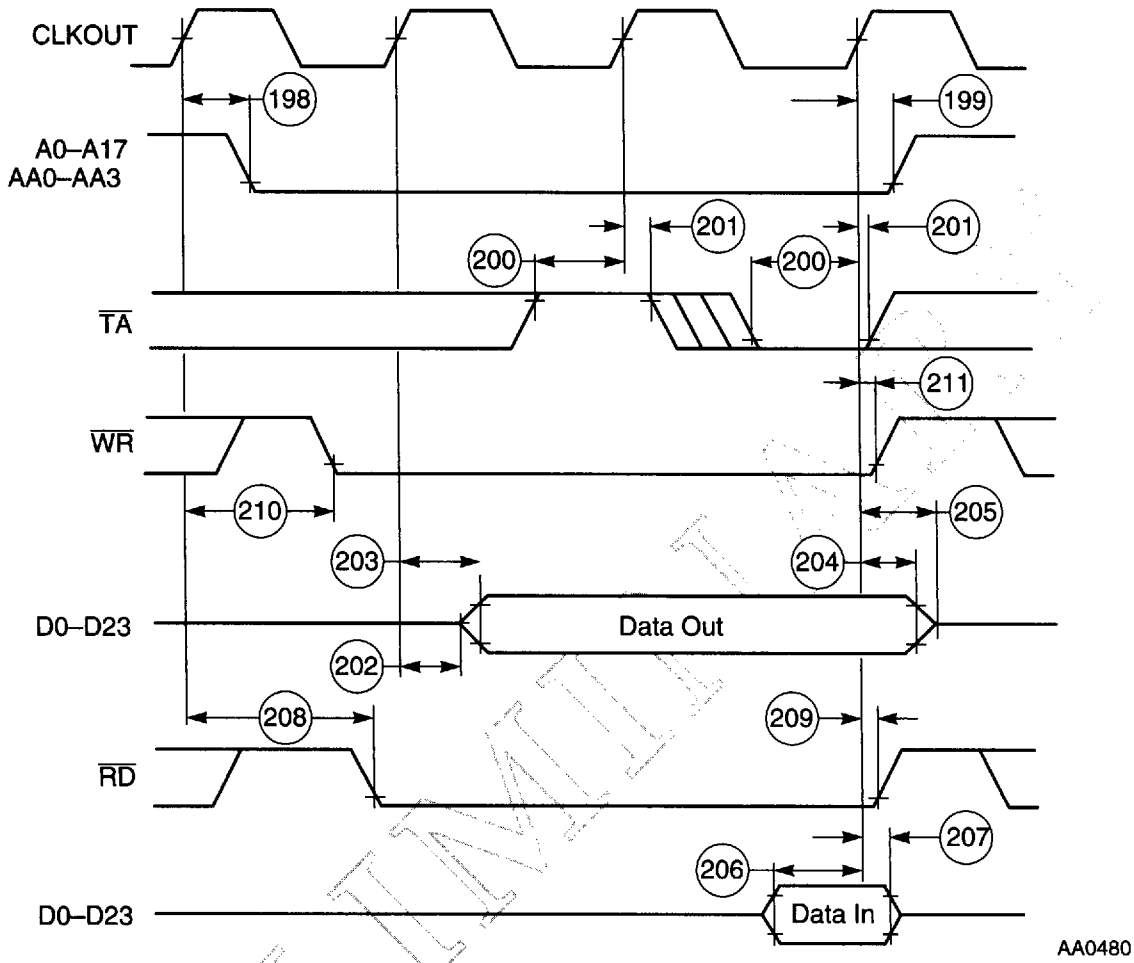


Figure 2-22 Synchronous Bus Timings SRAM 2 WS ($\overline{TA}$ Controlled)

Arbitration Timings

Table 2-18 Arbitration Bus Timings[1]

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
212	CLKOUT high to $\overline{BR}$ assertion/ deassertion[2]		1.0	5.0	1.0	4.5	1.0	4.0	ns
213	$\overline{BG}$ asserted/deasserted to CLKOUT high (setup)		6.0	—	5.0	—	4.0	—	ns
214	CLKOUT high to $\overline{BG}$ deasserted/ asserted (hold)		0.0	—	0.0	—	0.0	—	ns
215	$\overline{BB}$ deassertion to CLKOUT high (input setup)		6.0	—	5.0	—	4.0	—	ns
216	CLKOUT high to $\overline{BB}$ assertion (input hold)		0.0	—	0.0	—	0.0	—	ns
217	CLKOUT high to $\overline{BB}$ assertion (output)		1.0	5.0	1.0	4.5	1.0	4.0	ns
218	CLKOUT high to $\overline{BB}$ deassertion (output)		1.0	5.0	1.0	4.5	1.0	4.0	ns
219	$\overline{BB}$ high to $\overline{BB}$ high impedance (output)		—	6.8	—	5.6	—	4.5	ns
220	CLKOUT high to address and controls active	$0.25 \times T_C$	3.8	—	3.1	—	2.5	—	ns
221	CLKOUT high to address and controls high impedance	**66 MHz:** $0.25 \times T_C + 1.0$	—	4.8	—	—	—	—	ns
		80 MHz: $0.25 \times T_C + 0.5$	—	—	—	3.6	—	—	ns
		100 MHz: $0.25 \times T_C$	—	—	—	—	—	2.5	ns
222	CLKOUT high to AA active	$0.25 \times T_C$	3.8	—	3.1	—	2.5	—	ns
223	CLKOUT high to AA deassertion	**66 MHz:** $0.25 \times T_C + 5.0$	4.8	8.8	—	—	—	—	ns
		80 MHz: $0.25 \times T_C + 4.5$	—	—	4.1	7.6	—	—	ns
		100 MHz: $0.25 \times T_C + 4.0$	—	—	—	—	3.2	6.5	ns
224	CLKOUT high to AA high impedance	**66 MHz:** $0.75 \times T_C + 1.0$	—	12.4	—	—	—	—	ns
		80 MHz: $0.75 \times T_C + 0.5$	—	—	—	9.9	—	—	ns
		100 MHz: $0.75 \times T_C$	—	—	—	—	—	7.5	ns

Notes: 1. The asynchronous delays specified in the expressions are valid for DSP56303.
2. T212 is valid for Address Trace mode when the ATE bit in the OMR is set. $\overline{BR}$ is deasserted for internal accesses and asserted for external accesses.

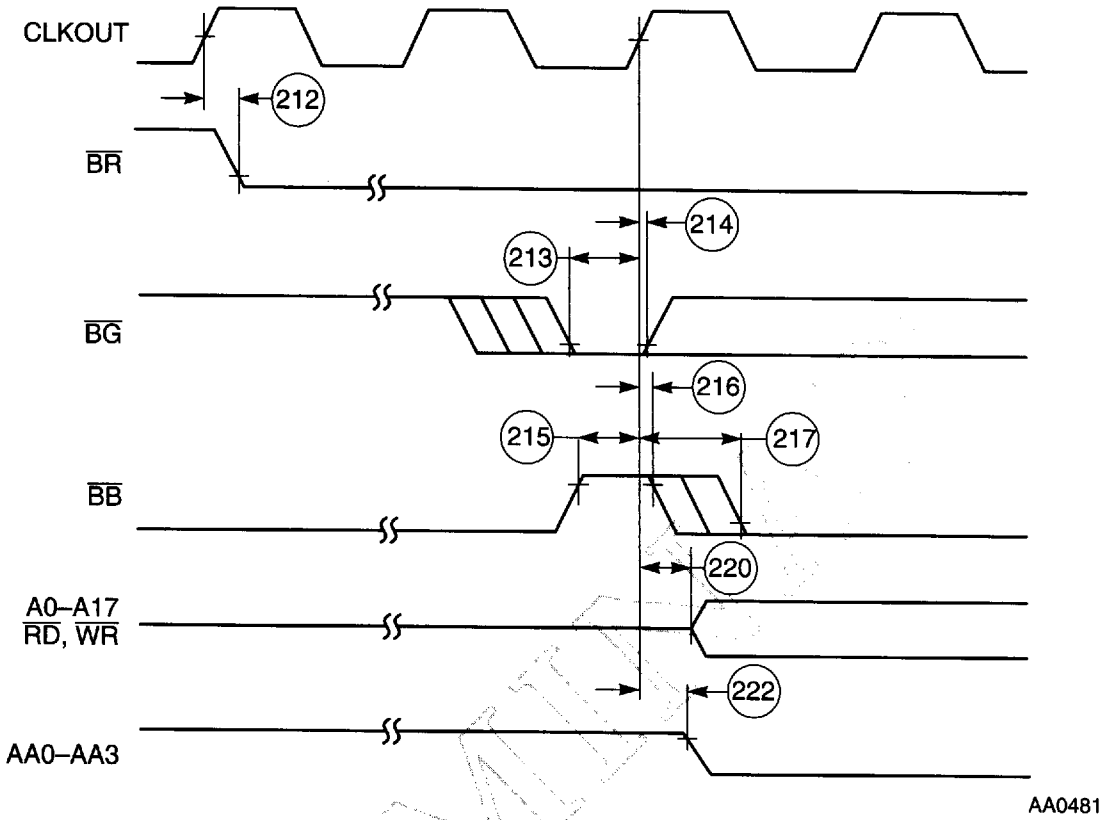


Figure 2-23 Bus Acquisition Timings

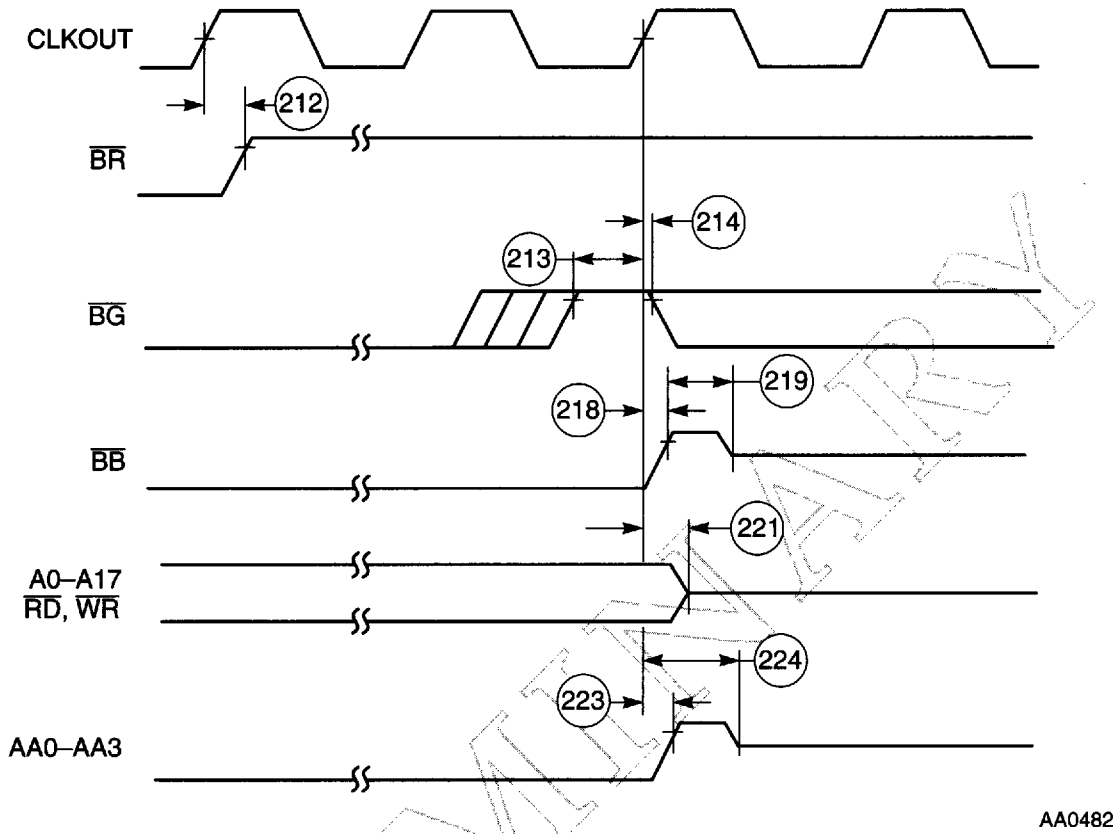


Figure 2-24 Bus Release Timings Case 1 (BRT Bit in OMR Cleared)

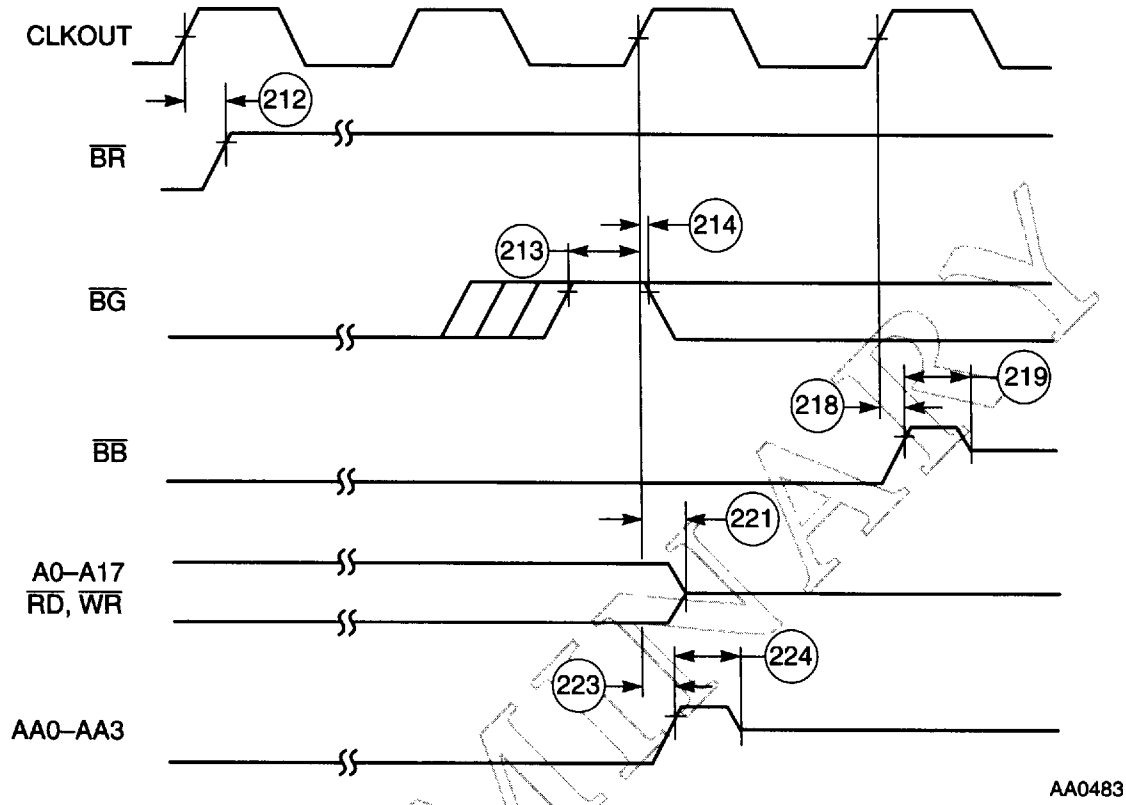


Figure 2-25 Bus Release Timings Case 2 (BRT Bit in OMR Set)

HOST INTERFACE TIMING

Table 2-19 Host Interface Timing[1, 2]

No.	Characteristic[10]	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
317	Read data strobe assertion width[5] $\overline{HACK}$ assertion width	**66 MHz:** $T_C + 15.0$ **80 MHz:** $T_C + 12.4$ **100 MHz:** $T_C + 9.0$	30.2 — —	— — —	— 24.9 —	— — —	— — 19.9	— — —	ns ns ns
318	Read data strobe deassertion width[5] $\overline{HACK}$ deassertion width		15.0	—	12.4	—	9.9	—	ns
319	Read data strobe deassertion width[5] after "Last Data Register" reads[8,11], or between two consecutive CVR, ICR, or ISR reads[3] $\overline{HACK}$ deassertion width after "Last Data Register" reads[8,11]	**66 MHz:** $2.5 \times T_C + 10.0$ **80 MHz:** $2.5 \times T_C + 8.3$ **100 MHz:** $2.5 \times T_C + 6.6$	47.9 — —	— — —	— 39.5 —	— — —	— — 33.6	— — —	ns ns ns
320	Write data strobe assertion width[6]		20.0	—	16.5	—	13.2	—	ns
321	Write data strobe deassertion width[6]	**66 MHz:** $2.5 \times T_C + 10.0$ **80 MHz:** $2.5 \times T_C + 8.3$ **100 MHz:** $2.5 \times T_C + 6.6$	47.9 — —	— — —	— 39.5 —	— — —	— — 33.6	— — —	ns ns ns
322	$\overline{HAS}$ assertion width		15.0	—	12.4	—	9.9	—	ns
323	$\overline{HAS}$ deassertion to data strobe assertion[4]		0.0	—	0.0	—	0.0	—	ns
324	Host data input setup time before write data strobe deassertion[6]		15.0	—	12.4	—	9.9	—	ns
325	Host data input hold time after write data strobe deassertion[6]		5.0	—	4.1	—	3.3	—	ns
326	Read data strobe assertion to output data active from high impedance[5] $\overline{HACK}$ assertion to output data active from high impedance		5.0	—	4.1	—	3.3	—	ns
327	Read data strobe assertion to output data valid[5] $\overline{HACK}$ assertion to output data valid		—	30.0	—	26.68	—	23.54	ns

Table 2-19 Host Interface Timing[1, 2] (Continued)

No.	Characteristic[10]	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
328	Read data strobe deassertion to output data high impedance[5] $\overline{HACK}$ deassertion to output data high impedance		—	15.0	—	12.4	—	9.9	ns
329	Output data hold time after read data strobe deassertion[5] Output data hold time after $\overline{HACK}$ deassertion		5.0	—	4.1	—	4.1	—	ns
330	$\overline{HCS}$ assertion to read data strobe deassertion[5]	**66 MHz:** $T_C + 15.0$ **80 MHz:** $T_C + 12.4$ **100 MHz:** $T_C + 9.9$	30.2 — —	— — —	— 24.9 —	— — —	— — 19.9	— — —	ns ns ns
331	$\overline{HCS}$ assertion to write data strobe deassertion[6]		15.0	—	12.4	—	9.9	—	ns
332	$\overline{HCS}$ assertion to output data valid		—	25.0	—	20.6	—	16.5	ns
333	$\overline{HCS}$ hold time after data strobe deassertion[4]		0.0	—	0.0	—	0.0	—	ns
334	Address (AD7–AD0) setup time before $\overline{HAS}$ deassertion (HMUX=1)		7.0	—	5.8	—	4.7	—	ns
335	Address (AD7–AD0) hold time after $\overline{HAS}$ deassertion (HMUX=1)		5.0	—	4.1	—	3.3	—	ns
336	A10–A8 (HMUX=1), A2–A0 (HMUX=0), HR/$\overline{W}$ setup time before data strobe assertion[4] • Read • Write		 0 7.0	 — —	 0 5.8	 — —	 0 4.7	 — —	 ns ns
337	A10–A8 (HMUX=1), A2–A0 (HMUX=0), HR/$\overline{W}$ hold time after data strobe deassertion[4]		5.0	—	4.1	—	3.3	—	ns
338	Delay from read data strobe deassertion to host request assertion for "Last Data Register" read[5, 7, 8]	**66 MHz:** $2 \times T_C + 25.0$ **80 MHz:** $2 \times T_C + 20.6$ **100 MHz:** $2 \times T_C + 20.6$	55.3 — —	— — —	— 45.6 —	— — —	— — 36.5	— — —	ns ns ns

Table 2-19 Host Interface Timing[1, 2] (Continued)

No.	Characteristic[10]	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
339	Delay from write data strobe deassertion to host request assertion for "Last Data Register" write[6, 7, 8]	**66 MHz:** $1.5 \times T_C + 25.0$	47.7	—	—	—	—	—	ns
		80 MHz: $1.5 \times T_C + 20.6$	—	—	39.4	—	—	—	ns
		100 MHz: $1.5 \times T_C + 16.5$	—	—	—	—	31.5	—	ns
340	Delay from data strobe assertion to host request deassertion for "Last Data Register" read or write (HROD=0)[4, 7, 8]		—	25.0	—	22.55	—	20.24	ns
341	Delay from data strobe assertion to host request deassertion for "Last Data Register" read or write (HROD=1, open drain host request)[4, 7, 8, 9]		—	300.0	—	300.0	—	300.0	ns

Notes:
1. See **Host Port Usage Considerations** on page 1-11.
2. In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.
3. This timing is applicable only if two consecutive reads from one of these registers are executed.
4. The data strobe is Host Read (HRD) or Host Write (HWR) in the Dual Data Strobe mode and Host Data Strobe (HDS) in the Single Data Strobe mode.
5. The read data strobe is HRD in the Dual Data Strobe mode and HDS in the Single Data Strobe mode.
6. The write data strobe is HWR in the Dual Data Strobe mode and HDS in the Single Data Strobe mode.
7. The host request is HREQ in the Single Host Request mode and HRRQ and HTRQ in the Double Host Request mode.
8. The "Last Data Register" is the register at address $7, which is the last location to be read or written in data transfers. This is RXL/TXL in the Little Endian mode (HBE = 0), or RXH/TXH in the Big Endian mode (HBE = 1).
9. In this calculation, the host request signal is pulled up by a 4.7 kΩ resistor in the Open-drain mode.
10. V_{CC} = 3.3 V ± 0.3 V; T_J = −40°C to +100 °C, C_L = 50 pF + 2 TTL loads
11. This timing is applicable only if a read from the "Last Data Register" is followed by a read from the RXL, RXM, or RXH registers without first polling RXDF or HREQ bits, or waiting for the assertion of the HREQ signal.

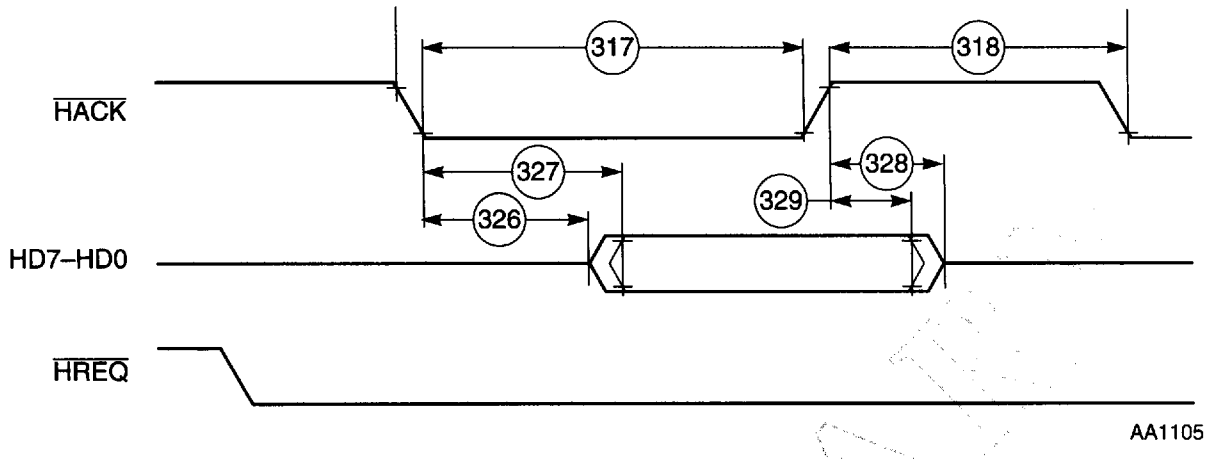


Figure 2-26 Host Interrupt Vector Register (IVR) Read Timing Diagram

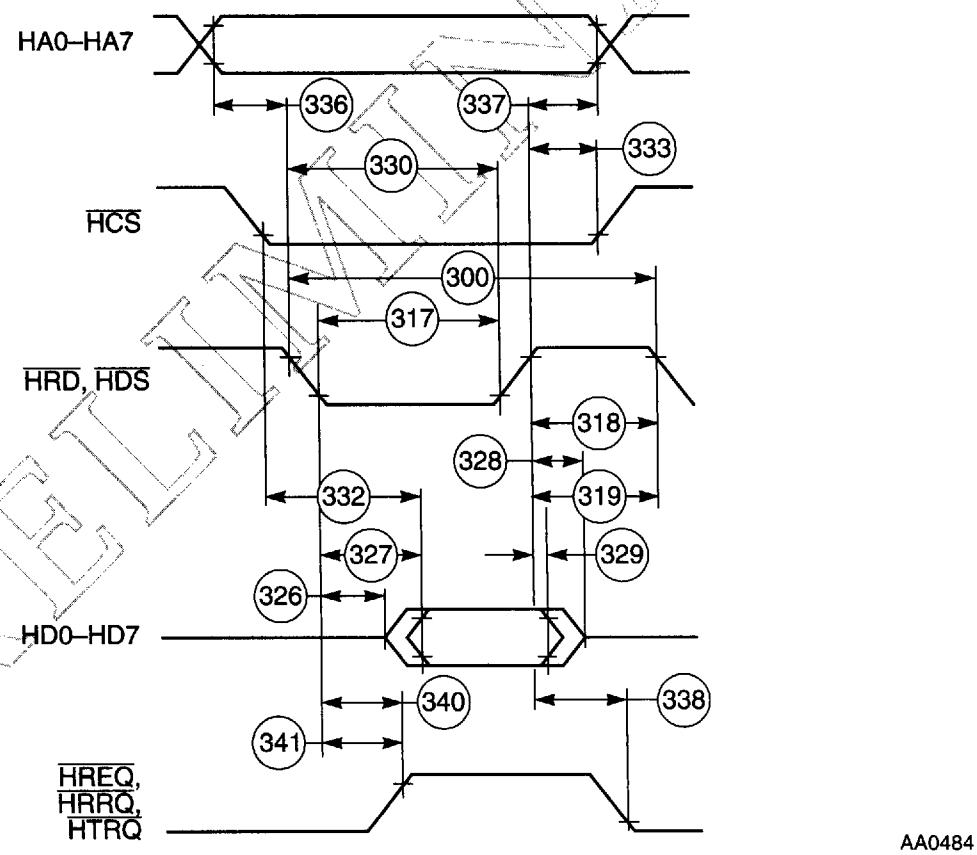


Figure 2-27 Read Timing Diagram, Non-Multiplexed Bus

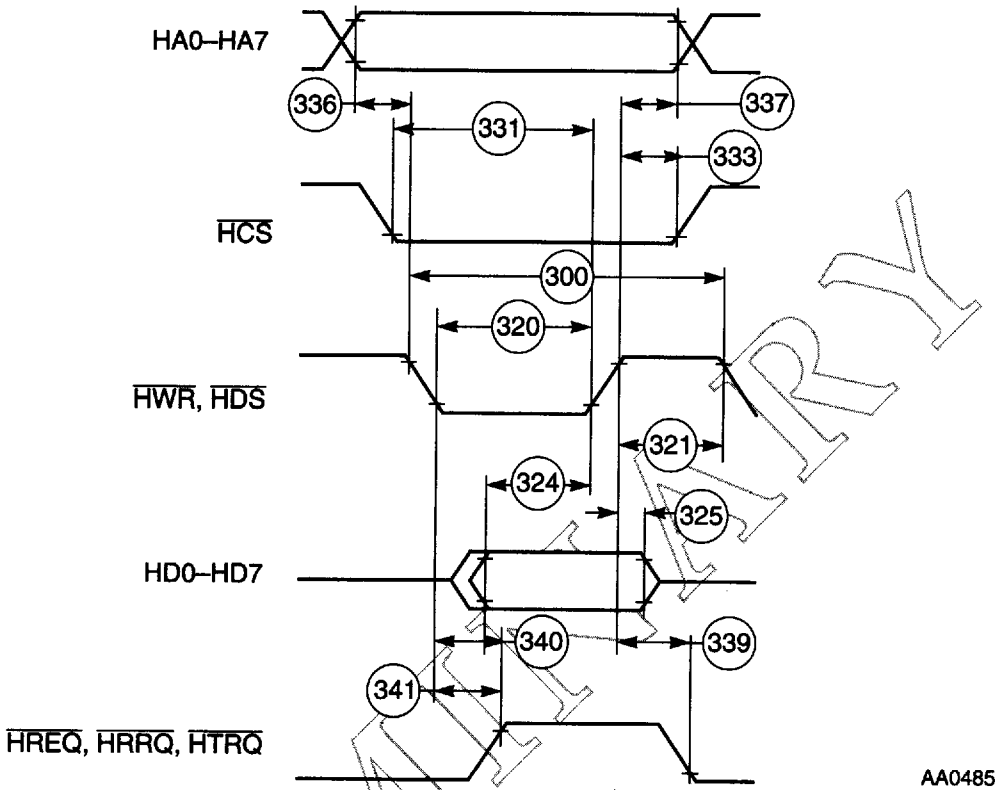


Figure 2-28 Write Timing Diagram, Non-Multiplexed Bus

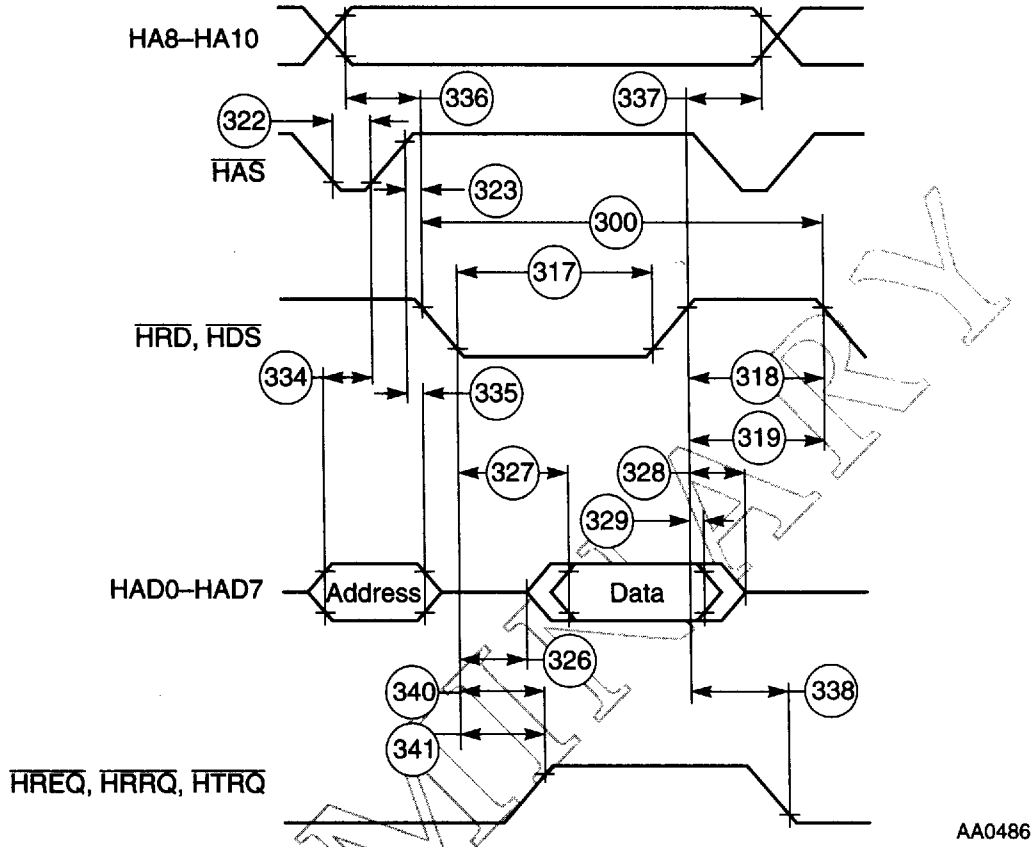


Figure 2-29 Read Timing Diagram, Multiplexed Bus

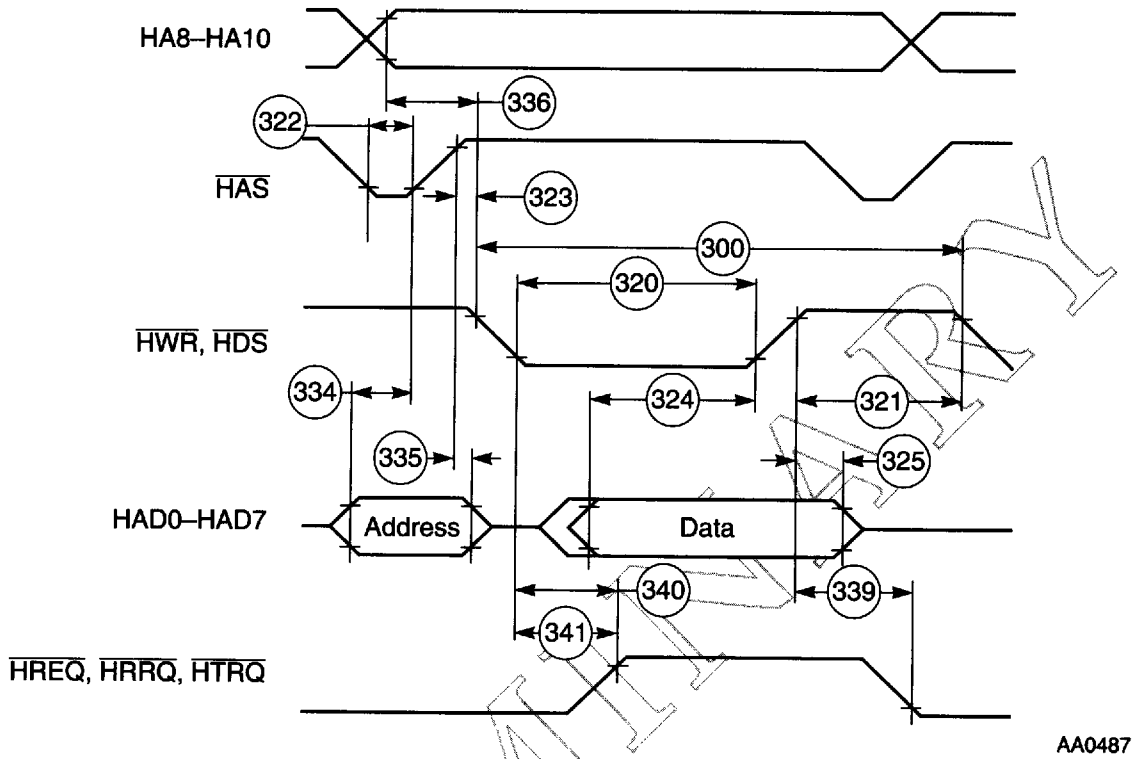


Figure 2-30 Write Timing Diagram, Multiplexed Bus

SCI TIMING

Table 2-20 SCI Timing

No.	Characteristics[1]	Symbol	Expression	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
400	Synchronous clock cycle	t_{SCC}[2]	$8 \times T_C$	121.0	—	100.0	—	80.0	—	ns
401	Clock low period		$t_{SCC}/2 - 10.0$	50.5	—	40.0	—	30.0	—	ns
402	Clock high period		$t_{SCC}/2 - 10.0$	50.5	—	40.0	—	30.0	—	ns
403	Output data setup to clock falling edge (internal clock)		$t_{SCC}/4 + 0.5 \times T_C - 17.0$	20.5	—	14.3	—	8.0	—	ns
404	Output data hold after clock rising edge (internal clock)		$t_{SCC}/4 - 0.5 \times T_C$	22.5	—	18.8	—	15.0	—	ns
405	Input data setup time before clock rising edge (internal clock)		$t_{SCC}/4 + 0.5 \times T_C + 25.0$	63.0	—	56.3	—	50.0	—	ns
406	Input data not valid before clock rising edge (internal clock)		$t_{SCC}/4 + 0.5 \times T_C - 5.5$	—	32.0	—	25.8	—	19.5	ns
407	Clock falling edge to output data valid (external clock)			—	32.0	—	32.0	—	32.0	ns
408	Output data hold after clock rising edge (external clock)		$T_C + 8.0$	23.0	—	20.5	—	18.0	—	ns
409	Input data setup time before clock rising edge (external clock)			0.0	—	0.0	—	0.0	—	ns
410	Input data hold time after clock rising edge (external clock)			9.0	—	9.0	—	9.0	—	ns
411	Asynchronous clock cycle	t_{ACC}[3]	$64 \times T_C$	969.7	—	800.0	—	640.0	—	ns
412	Clock low period		$t_{ACC}/2 - 10.0$	474.8	—	390.0	—	310.0	—	ns
413	Clock high period		$t_{ACC}/2 - 10.0$	474.8	—	390.0	—	310.0	—	ns

Table 2-20 SCI Timing (Continued)

No.	Characteristics[1]	Symbol	Expression	66 MHz		80 MHz		100 MHz		Unit
				Min	Max	Min	Max	Min	Max	
414	Output data setup to clock rising edge (internal clock)		$t_{ACC}/2 - 30.0$	458.8	—	370.0	—	290.0	—	ns
415	Output data hold after clock rising edge (internal clock)		$t_{ACC}/2 - 30.0$	458.8	—	370.0	—	290.0	—	ns

Notes:
1. $V_{CC} = 3.3\ V \pm 0.3\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF + 2$ TTL Loads
2. t_{SCC} = synchronous clock cycle time (For internal clock, t_{SCC} is determined by the SCI clock control register and T_C.)
3. t_{ACC} = asynchronous clock cycle time; value given for 1X Clock mode (For internal clock, t_{ACC} is determined by the SCI clock control register and T_C.)

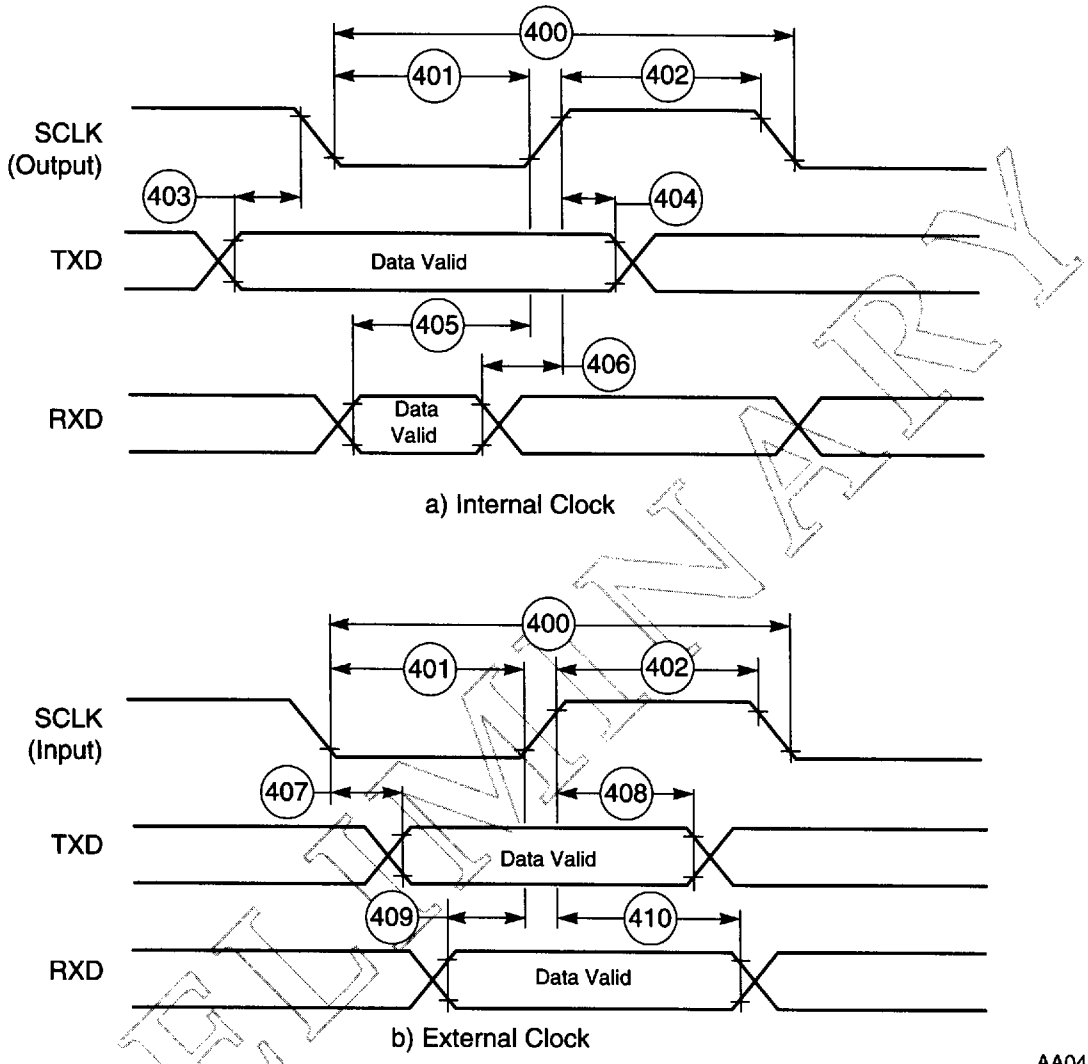


Figure 2-31 SCI Synchronous Mode Timing

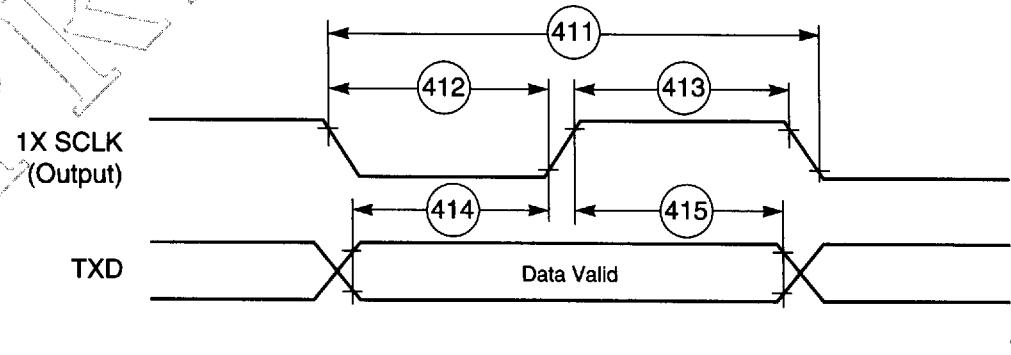


Figure 2-32 SCI Asynchronous Mode Timing

ESSI0/ESSI1 TIMING

Table 2-21 ESSI Timings

No.	Characteristics[4, 6, 7]	Symbol	Expression	66 MHz		80 MHz		100 MHz		Condition[5]	Unit
				Min	Max	Min	Max	Min	Max		
430	Clock cycle[1]	t_{SSICC}	$4 \times T_C$ $3 \times T_C$	60.6 45.5	— —	50.0 37.5	— —	40.0 30.0	— —	i ck x ck	ns
431	Clock high period • For internal clock • For external clock		 $2 \times T_C - 10.0$ $1.5 \times T_C$	 20.3 22.7	 — —	 15.0 18.8	 — —	 10.0 15.0	 — —		 ns ns
432	Clock low period • For internal clock • For external clock		 $2 \times T_C - 10.0$ $1.5 \times T_C$	 20.3 22.7	 — —	 15.0 18.8	 — —	 10.0 15.0	 — —		 ns ns
433	RXC rising edge to FSR out (bl) high			— —	37.0 22.0	— —	37.0 22.0	— —	37.0 22.0	x ck i ck a	ns
434	RXC rising edge to FSR out (bl) low			— —	37.0 22.0	— —	37.0 22.0	— —	37.0 22.0	x ck i ck a	ns
435	RXC rising edge to FSR out (wr) high[2]			— —	39.0 24.0	— —	39.0 24.0	— —	39.0 24.0	x ck i ck a	ns
436	RXC rising edge to FSR out (wr) low[2]			— —	39.0 24.0	— —	39.0 24.0	— —	39.0 24.0	x ck i ck a	ns
437	RXC rising edge to FSR out (wl) high			— —	36.0 21.0	— —	36.0 21.0	— —	36.0 21.0	x ck i ck a	ns
438	RXC rising edge to FSR out (wl) low			— —	37.0 22.0	— —	37.0 22.0	— —	37.0 22.0	x ck i ck a	ns
439	Data in setup time before RXC (SCK in Synchronous mode) falling edge			0.0 19.0	— —	0.0 19.0	— —	0.0 19.0	— —	x ck i ck	ns
440	Data in hold time after RXC falling edge			5.0 3.0	— —	5.0 3.0	— —	5.0 3.0	— —	x ck i ck	ns
441	FSR input (bl, wr) high before RXC falling edge[2]			23.0 1.0	— —	23.0 1.0	— —	23.0 1.0	— —	x ck i ck a	ns
442	FSR input (wl) high before RXC falling edge			23.0 1.0	— —	23.0 1.0	— —	23.0 1.0	— —	x ck i ck a	ns
443	FSR input hold time after RXC falling edge			3.0 0.0	— —	3.0 0.0	— —	3.0 0.0	— —	x ck i ck a	ns
444	Flags input setup before RXC falling edge			0.0 19.0	— —	0.0 19.0	— —	0.0 19.0	— —	x ck i ck s	ns

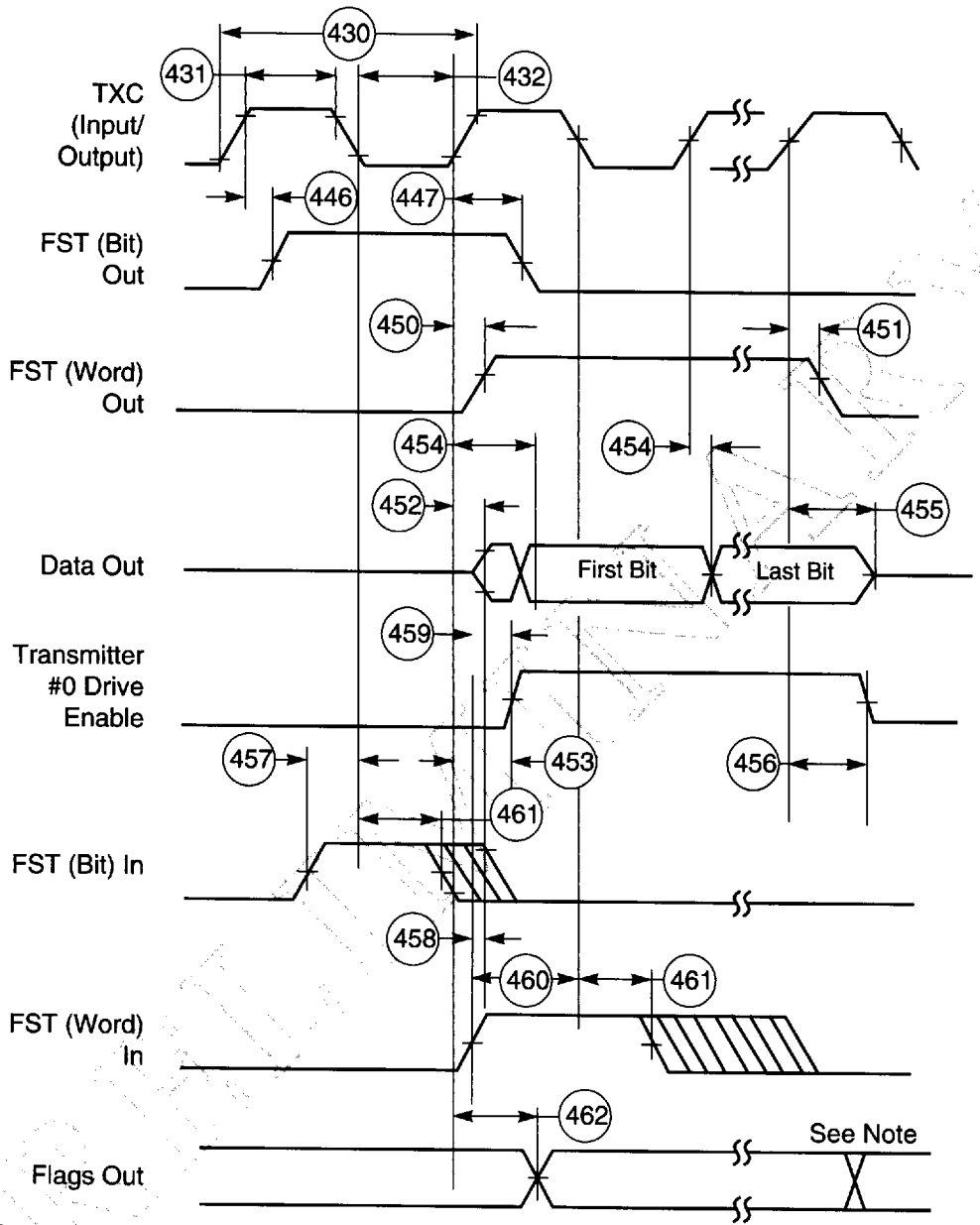
Table 2-21 ESSI Timings (Continued)

No.	Characteristics[4, 6, 7]	Symbol	Expression	66 MHz		80 MHz		100 MHz		Condition[5]	Unit
				Min	Max	Min	Max	Min	Max		
445	Flags input hold time after RXC falling edge			6.0 0.0	— —	6.0 0.0	— —	6.0 0.0	— —	x ck i ck s	ns
446	TXC rising edge to FST out (bl) high			— —	29.0 15.0	— —	29.0 15.0	— —	29.0 15.0	x ck i ck	ns
447	TXC rising edge to FST out (bl) low			— —	31.0 17.0	— —	31.0 17.0	— —	31.0 17.0	x ck i ck	ns
448	TXC rising edge to FST out (wr) high[2]			— —	31.0 17.0	— —	31.0 17.0	— —	31.0 17.0	x ck i ck	ns
449	TXC rising edge to FST out (wr) low[2]			— —	33.0 19.0	— —	33.0 19.0	— —	33.0 19.0	x ck i ck	ns
450	TXC rising edge to FST out (wl) high			— —	30.0 16.0	— —	30.0 16.0	— —	30.0 16.0	x ck i ck	ns
451	TXC rising edge to FST out (wl) low			— —	31.0 17.0	— —	31.0 17.0	— —	31.0 17.0	x ck i ck	ns
452	TXC rising edge to data out enable from high impedance			— —	31.0 17.0	— —	31.0 17.0	— —	31.0 17.0	x ck i ck	ns
453	TXC rising edge to Transmitter #0 drive enable assertion			— —	34.0 20.0	— —	34.0 20.0	— —	34.0 20.0	x ck i ck	ns
454	TXC rising edge to data out valid		$35 + 0.5 \times T_C$ 21.0	— —	42.6 21.0	— —	41.3 21.0	— —	40.0 21.0	x ck i ck	ns
455	TXC rising edge to data out high impedance[3]			— —	31.0 16.0	— —	31.0 16.0	— —	31.0 16.0	x ck i ck	ns
456	TXC rising edge to Transmitter #0 drive enable deassertion[3]			— —	34.0 20.0	— —	34.0 20.0	— —	34.0 20.0	x ck i ck	ns
457	FST input (bl, wr) setup time before TXC falling edge[2]			2.0 21.0	— —	2.0 21.0	— —	2.0 21.0	— —	x ck i ck	ns
458	FST input (wl) to data out enable from high impedance			—	27.0	—	27.0	—	27.0	—	ns
459	FST input (wl) to Transmitter #0 drive enable assertion			—	31.0	—	31.0	—	31.0	—	ns

Table 2-21 ESSI Timings (Continued)

No.	Characteristics[4, 6, 7]	Symbol	Expression	66 MHz		80 MHz		100 MHz		Condition[5]	Unit
				Min	Max	Min	Max	Min	Max		
460	FST input (wl) setup time before TXC falling edge			2.0 21.0	— —	2.0 21.0	— —	2.0 21.0	— —	x ck i ck	ns
461	FST input hold time after TXC falling edge			4.0 0.0	— —	4.0 0.0	— —	4.0 0.0	— —	x ck i ck	ns
462	Flag output valid after TXC rising edge			— —	32.0 18.0	— —	32.0 18.0	— —	32.0 18.0	x ck i ck	ns

Notes:
1. For the internal clock, the external clock cycle is defined by Icyc and the ESSI control register.
2. The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but spreads from one serial clock before first bit clock (same as Bit Length Frame Sync signal), until the one before last bit clock of the first word in frame.
3. Periodically sampled and not 100% tested
4. V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100 °C, C_L = 50 pF + 2 TTL Loads
5. TXC (SCK Pin) = Transmit Clock
   RXC (SC0 or SCK Pin) = Receive Clock
   FST (SC2 Pin) = Transmit Frame Sync
   FSR (SC1 or SC2 Pin) Receive Frame Sync
6. i ck = Internal Clock
   x ck = External Clock
   i ck a = Internal Clock, Asynchronous Mode
   (Asynchronous implies that TXC and RXC are two different clocks)
   i ck s = Internal Clock, Synchronous Mode
   (Synchronous implies that TXC and RXC are the same clock)
7. bl = bit length
   wl = word length
   wr = word length relative



Note: In Network mode, output flag transitions can occur at the start of each time slot within the frame. In Normal mode, the output flag state is asserted for the entire frame period.

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Figure 2-33 ESSI Transmitter Timing

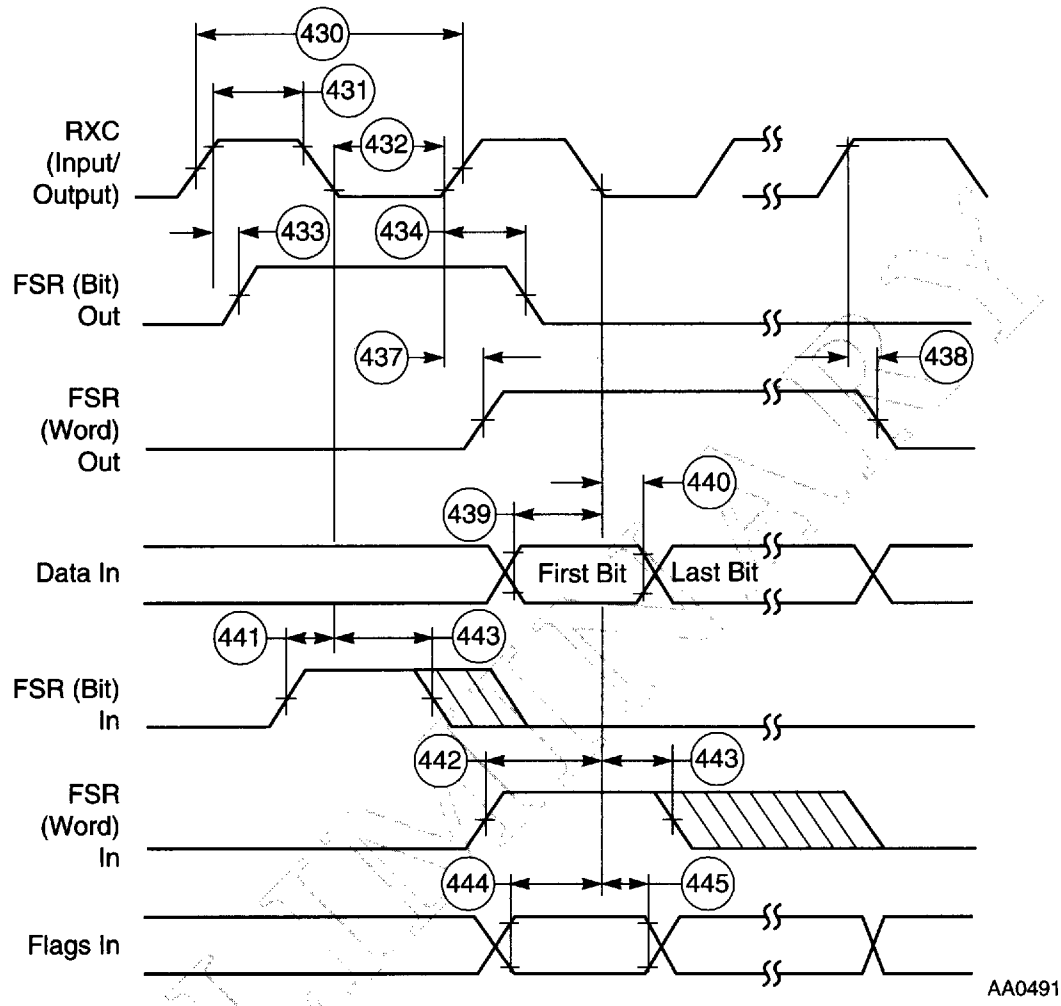


Figure 2-34 ESSI Receiver Timing

TIMER TIMING

Table 2-22 Timer Timing

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
480	TIO Low	$2 \times T_C + 2.0$	32.5	—	27.0	—	22.0	—	ns
481	TIO High	$2 \times T_C + 2.0$	32.5	—	27.0	—	22.0	—	ns
482	Timer setup time from TIO (Input) assertion to CLKOUT rising edge		9.0	15.15	9.0	12.5	9.0	10.0	ns
483	Synchronous timer delay time from CLKOUT rising edge to the external memory access address out valid caused by first interrupt instruction execution	$10.25 \times T_C + 1.0$	156.0	—	129.1	—	103.5	—	ns
484	CLKOUT rising edge to TIO (Output) assertion • Minimum • Maximum	 $0.5 \times T_C + 3.5$ $0.5 \times T_C + 19.8$	 11.1 —	 — 28.1	 9.8 —	 — 26.1	 8.5 —	 — 24.8	 ns ns
485	CLKOUT rising edge to TIO (Output) deassertion • Minimum • Maximum	 $0.5 \times T_C + 3.5$ **66–80 MHz:** $0.5 \times T_C + 19.8$ **100 MHz:** $0.5 \times T_C + 19.0$	 11.1 — —	 — 28.1 —	 9.8 — —	 — 26.1 —	 8.5 — —	 — — 24.8	 ns ns ns

Note: $V_{CC} = 3.3\ V \pm 0.3\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF + 2$ TTL Loads

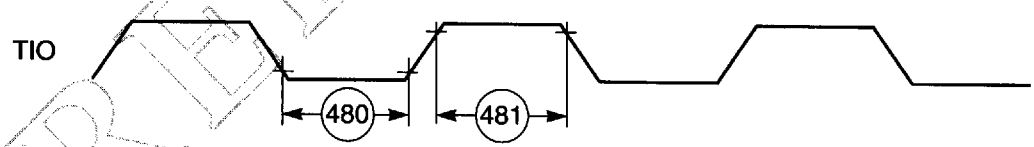


Figure 2-35 TIO Timer Event Input Restrictions

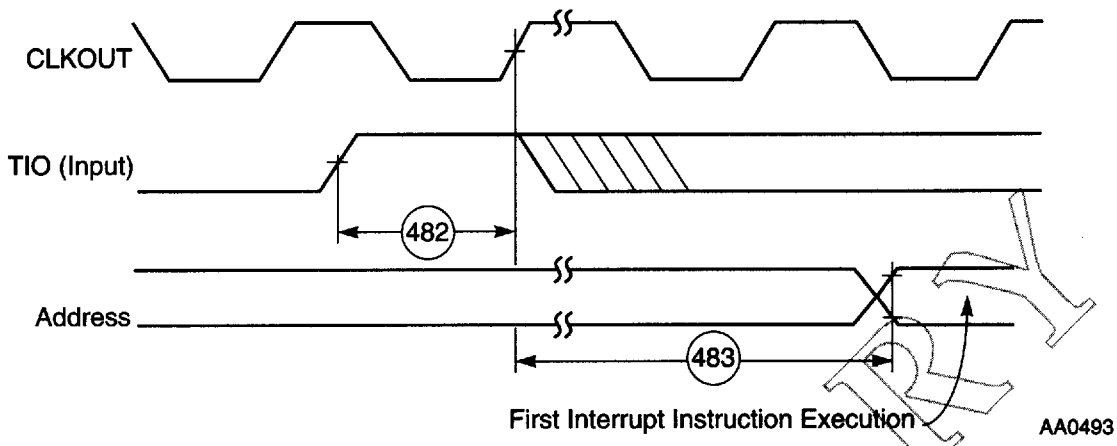


Figure 2-36 Timer Interrupt Generation

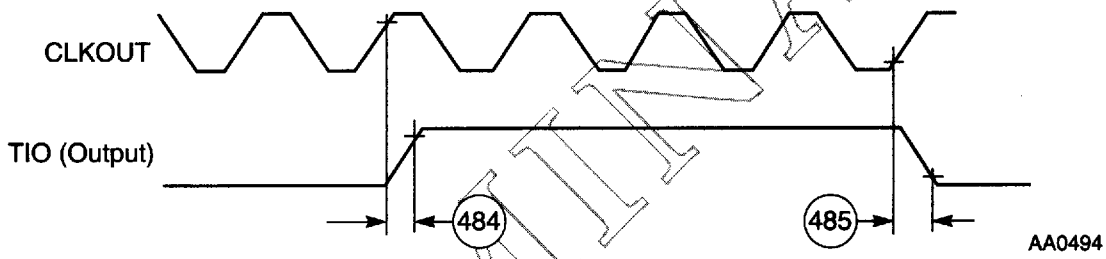


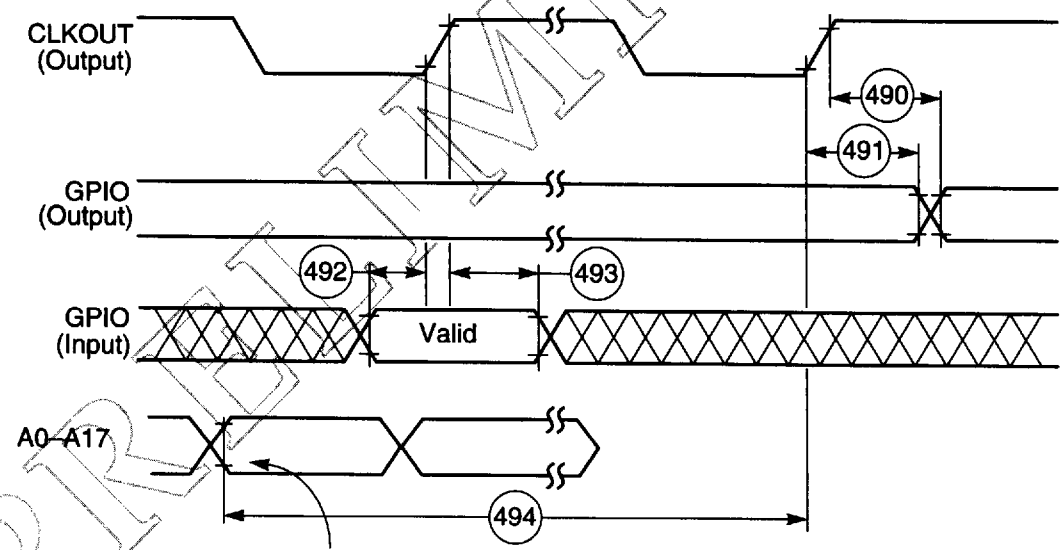
Figure 2-37 External Pulse Generation

GPIO TIMING

Table 2-23 GPIO Timing

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
490	CLKOUT edge to GPIO out valid (GPIO out delay time)		—	31.0	—	31.0	—	31.0	ns
491	CLKOUT edge to GPIO out not valid (GPIO out hold time)		3.0	—	3.0	—	3.0	—	ns
492	GPIO In valid to CLKOUT edge (GPIO in set-up time)		12.0	—	12.0	—	12.0	—	ns
493	CLKOUT edge to GPIO in not valid (GPIO in hold time)		0.0	—	0.0	—	0.0	—	ns
494	Fetch to CLKOUT edge before GPIO change	$6.75 \times T_C$	102.3	—	84.4	—	67.5	—	ns

Note: V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100 °C, C_L = 50 pF + 2 TTL Loads



Fetch the instruction MOVE X0,X:(R0); X0 contains the new value of GPIO and R0 contains the address of GPIO data register.

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Figure 2-38 GPIO Timing

JTAG TIMING

Table 2-24 JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
500	TCK frequency of operation ($1/(T_C \times 3)$; maximum 22 MHz)	0.0	22.0	MHz
501	TCK cycle time in Crystal mode	45.0	—	ns
502	TCK clock pulse width measured at 1.5 V	20.0	—	ns
503	TCK rise and fall times	0.0	3.0	ns
504	Boundary scan input data setup time	5.0	—	ns
505	Boundary scan input data hold time	24.0	—	ns
506	TCK low to output data valid	0.0	40.0	ns
507	TCK low to output high impedance	0.0	40.0	ns
508	TMS, TDI data setup time	5.0	—	ns
509	TMS, TDI data hold time	25.0	—	ns
510	TCK low to TDO data valid	0.0	44.0	ns
511	TCK low to TDO high impedance	0.0	44.0	ns
512	$\overline{\text{TRST}}$ assert time	100.0	—	ns
513	$\overline{\text{TRST}}$ setup time to TCK low	40.0	—	ns

Notes: 1. V_{CC} = 3.3 V ± 0.3 V; T_J = –40°C to +100 °C, C_L = 50 pF + 2 TTL Loads
2. All timings apply to OnCE module data transfers because it uses the JTAG port as an interface.

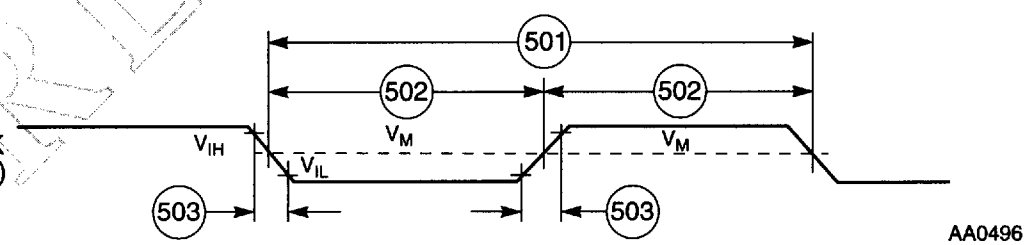

Figure 2-39 Test Clock Input Timing Diagram

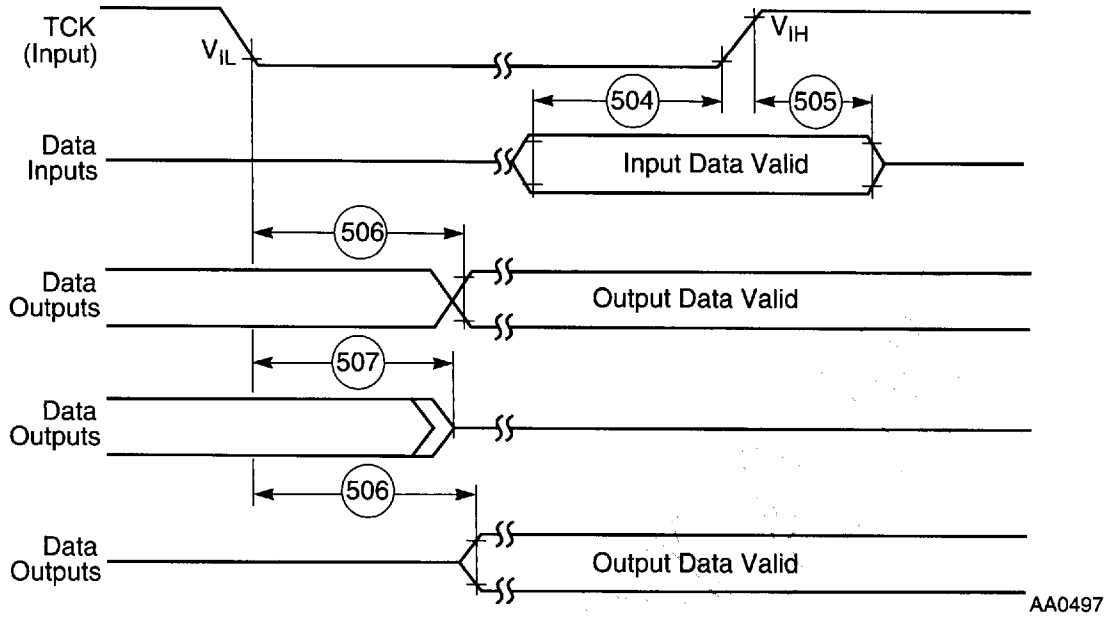

Figure 2-40 Boundary Scan (JTAG) Timing Diagram

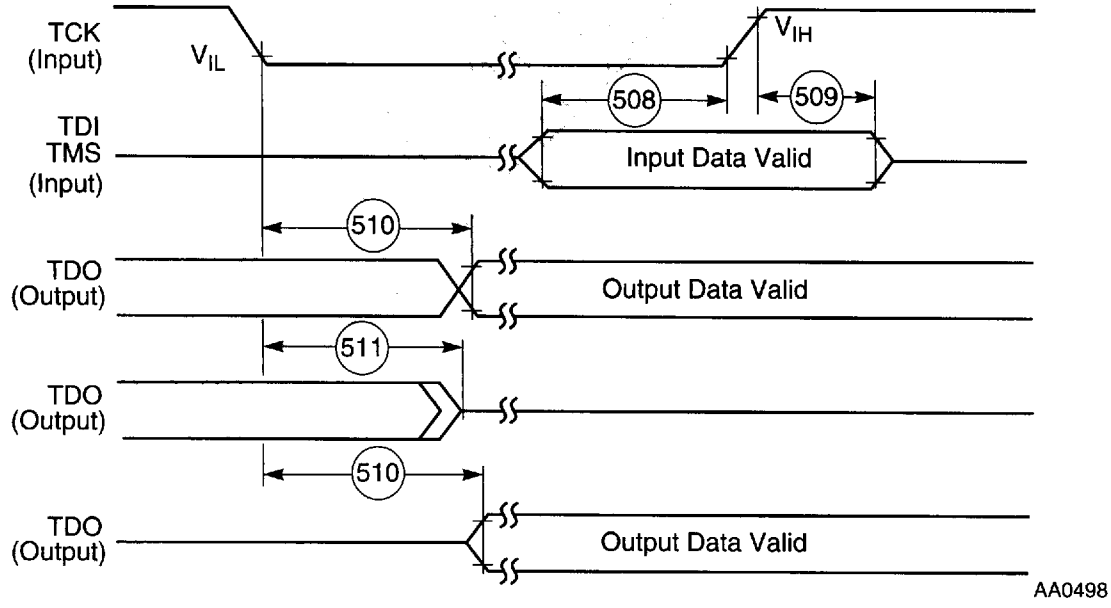

Figure 2-41 Test Access Port Timing Diagram

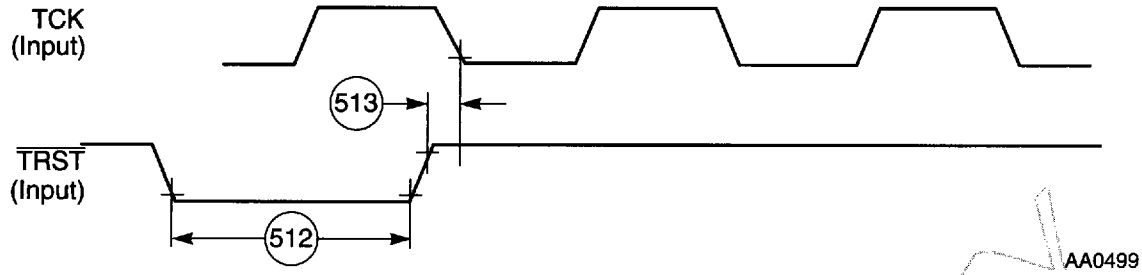

Figure 2-42 $\overline{\text{TRST}}$ Timing Diagram

OnCE MODULE TIMING

Table 2-25 OnCE Module Timing

No.	Characteristics	Expression	66 MHz		80 MHz		100 MHz		Unit
			Min	Max	Min	Max	Min	Max	
500	TCK frequency of operation	$1/(T_C \times 3)$, max 22.0 MHz	0.0	22.0	0.0	22.0	0.0	22.0	MHz
514	$\overline{\text{DE}}$ assertion time in order to enter Debug mode	$1.5 \times T_C + 10.0$	32.7	—	28.8	—	25.0	—	ns
515	Response time when DSP56303 is executing NOP instructions from internal memory	$5.5 \times T_C + 30.0$	—	113.3	—	98.8	—	85.0	ns
516	Debug acknowledge assertion time	$3 \times T_C + 10.0$	55.5	—	47.5	—	40.0	—	ns

Note: $V_{CC} = 3.3\ V \pm 0.3\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF + 2$ TTL Loads

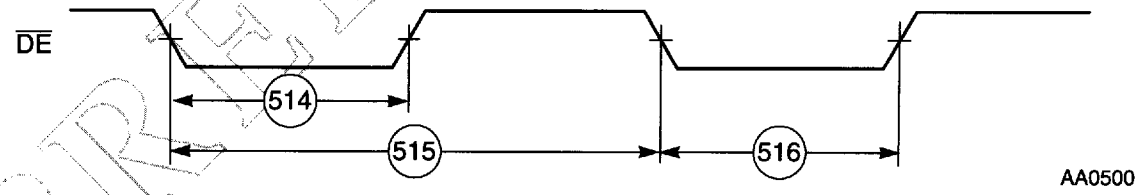

Figure 2-43 OnCE—Debug Request