Features

- High-performance Complex Programmable Logic Devices (CPLDs)
  - 7.5 ns pin-to-pin speeds on all fast inputs
  - Up to 125 MHz maximum clock frequency
- 100% PCI compliant
- 18 outputs with 24 mA drive
- I/O operation at 3.3 V or 5 V
- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V
- 100% interconnect matrix
  - Maximizes resource utilization
  - Wire-AND capability via SMARTswitch
- High-speed arithmetic carry network
  - 1 ns ripple-carry delay per bit
  - 56 MHz 18-bit accumulators
- Multiple independent clocks
- Up to 120 inputs programmable as direct, latched, or registered
- Power management options
- Multiple security bits for design protection
- 108 macrocells with programmable I/O architecture
- Advanced Dual-Block architecture
  - 2 Fast Function Blocks
  - 10 High-Density Function Blocks
- 0.8 µ CMOS EPROM technology
- Available in 84-pin PLCC/CLCC, 144-pin PGA, 100-pin and 160-pin PQFP, and 225-pin BGA packages

General Description

The XC73108 is a high performance CPLD providing general purpose logic integration. It consists of two PAL-like 24V9 Fast Function Blocks and ten High Density Function Blocks interconnected by the 100%-populated Universal Interconnect Matrix (UIM™).

Power Management

The XC73108 features a power-management scheme that permits non-speed-critical paths of a design to be operated at reduced power. Overall power dissipation is often reduced significantly, since, in most systems only a few paths are speed critical.

Macrocells can individually be specified for high performance or low power operation by adding attributes to the logic schematic, or declaration statements to the behavioral description. To minimize power dissipation, unused Function Blocks are turned off and unused macrocells in used Function Blocks are configured for low power operation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC}\ (mA) = MC_{HP}\ (2.4) + MC_{LP}\ (2.1) + MC\ (0.015\ mA/MHz)\ f$$

Where:

MC_{HP} = Macrocells in high-performance mode
MC_{LP} = Macrocells in low-power mode
MC = Total number of macrocells used
f = Clock frequency (MHz)

Figure 1 shows a typical power calculation for the XC73108 device, programmed as six 16-bit counters and operating at the indicated clock frequency.

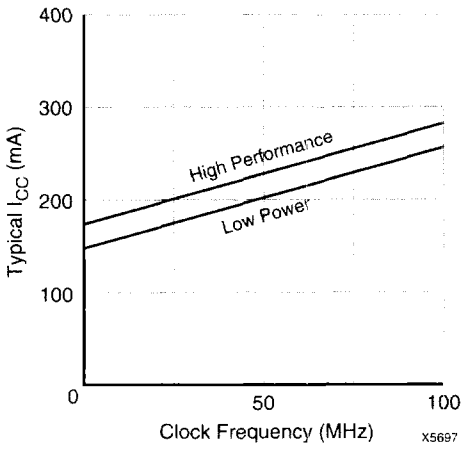


Figure 1: Typical I_{CC} vs. Frequency for XC73108

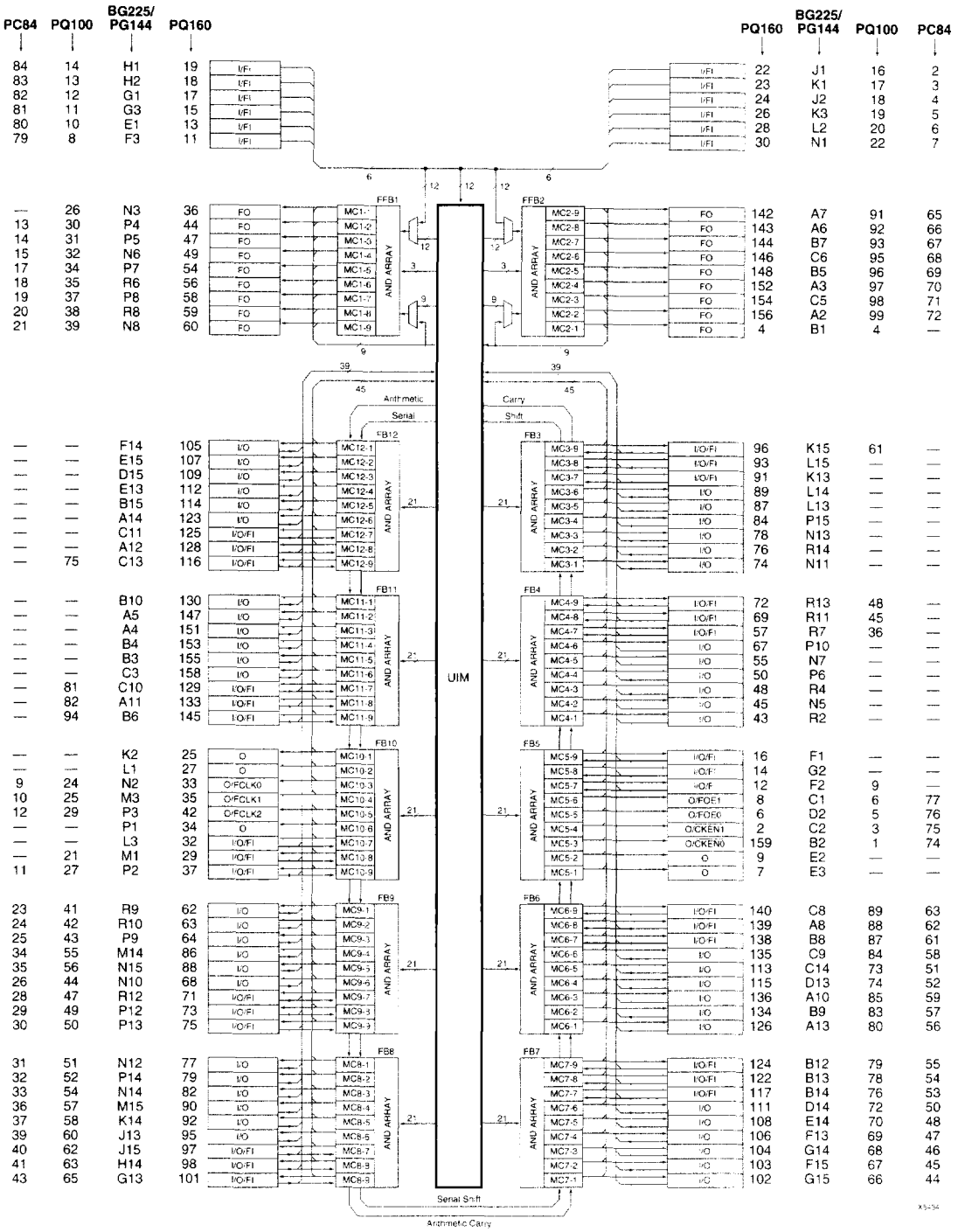


Figure 2: XC73108 Architecture

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CCINT} V_{CCIO}	Supply voltage relative to GND Commercial T_A = 0°C to 70°C	4.75	5.25	V
	Supply voltage relative to GND Industrial T_A = –40°C to 85°C	4.5	5.5	V
	Supply voltage relative to GND Military T_A = –55°C to T_C + 125°C	4.5	5.5	V
V_{CCIO}	I/O supply voltage relative to GND	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{IH}	High-level input voltage	2.0	V_{CC} +0.5	V
V_O	Output voltage	0	V_{CCIO}	V
T_{IN}	Input signal transition time		50	ns

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	5 V TTL High-level output voltage	I_{OH} = -4.0 mA V_{CC} = Min	2.4		V
	3.3 V High-level output voltage	I_{OH} = -3.2 mA V_{CC} = Min	2.4		V
V_{OL}	5 V TTL Low-level output voltage	I_{OL} = 24 mA (FO) I_{OL} = 12 mA (I/O) V_{CC} = Min		0.5	V
	3.3 V Low-level output voltage	I_{OL} = 10 mA V_{CC} = Min		0.4	V
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	µA
I_{OZ}	Output high-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CCIO}		±10.0	µA
C_{IN}	Input capacitance for Input and I/O pins	V_{IN} = GND f = 1.0 MHz		8.0	pF
C_{IN}	Input capacitance for global control pins (FCLK0, FCLK1, FCLK2, FOE0, FOE1)	V_{IN} = GND f = 1.0 MHz		12.0	pF
C_{OUT}[1]	Output capacitance	V_{IN} = GND f = 1.0 MHz		20.0	pF
I_{CC}[2]	Supply current (low power mode)	V_{IN} = V_{CC} or GND V_{CCINT} = V_{CCIO} = 5V f = 1.0 MHz @ 25°C	227 Typ		mA

Notes: 1. Sample tested.
2. Measured with device programmed as six 16-bit counters.

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{RESET}	Configuration completion time		80	160	µs

Fast Function Block (FFB) External AC Characteristics[3]

Symbol	Parameter	XC73108-7 (Com only)		XC73108-10 (Com only)		XC73108-12 (Com/Ind only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{CF}	Max count frequency [1, 2, 4]	125.0		100.0		80.0		66.7		50.0		MHz
t_{SUF}	Fast input setup time before FCLK ↑ [1]	4.0		5.0		6.0		7.0		10.0		ns
t_{HF}	Fast input hold time after FCLK ↑	0		0		0		0		0		ns
t_{COF}	FCLK ↑ to output valid		5.5		8.0		9.0		12.0		15.0	ns
t_{PDFO}	Fast input to output valid [1, 2]		7.5		10.0		12.0		15.0		20.0	ns
t_{PDFU}	I/O to output valid [1, 2]		13.5		19.0		22.0		27.0		35.0	ns
t_{CWF}	Fast clock pulse width (High or Low)	4.0		5.0		5.5		6.0		6.0		ns

Notes: 1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of $t_{FLOGILP} - t_{FLOGI}$ or $t_{LOGILP} - t_{LOGI}$.
2. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.
3. All appropriate AC specifications tested using Figure 3 as the test load circuit.
4. Export Control Max. flip-flop toggle rate.

High-Density Function Block (FB) External AC Characteristics

Symbol	Parameter	XC73108-7 (Com only)		XC73108-10 (Com only)		XC73108-12 (Com/Ind only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_C	Max count frequency [1, 2]	83.3		62.5		55.6		45.5		35.7		MHz
t_{SU}	I/O setup time before FCLK ↑ [1, 2]	12.0		16.0		18.0		22.0		28.0		ns
t_H	I/O hold time after FCLK ↑	0		0		0		0		0		ns
t_{CO}	FCLK ↑ to output valid		7.0		10.0		12.0		15.0		20.0	ns
t_{PSU}	I/O setup time before p-term clock ↑ [2]	4.0		6.0		7.0		9.0		12.0		ns
t_{PH}	I/O hold time after p-term clock ↑	0		0		0		0		0		ns
t_{PCO}	P-term clock ↑ to output valid		15.0		20.0		23.0		28.0		36.0	ns
t_{PD}	I/O to output valid [1, 2]		18.0		25.0		30.0		36.0		45.0	ns
t_{CW}	Fast clock pulse width	4.0		5.0		5.5		6.0		6.0		ns
t_{PCW}	P-term clock pulse width	5.0		6.0		7.5		8.5		12.0		ns

Notes: 1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of $t_{FLOGILP} - t_{FLOGI}$ or $t_{LOGILP} - t_{LOGI}$.
2. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

Fast Function Block (FFB) Internal AC Characteristics

Symbol	Parameter	XC73108-7 (Com only)		XC73108-10 (Com only)		XC73108-12 (Com/Ind only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{FLOGI}	FFB logic array delay [1]		1.5		1.5		2.0		2.0		3.0	ns
$t_{FLOGILP}$	Low-power FFB logic array delay [1]		3.5		5.5		7.0		8.0		11.0	ns
t_{FSUI}	FFB register setup time	1.5		2.5		3.0		4.0		6.0		ns
t_{FHI}	FFB register hold time	2.5		2.5		3.0		3.0		4.0		ns
t_{FCOI}	FFB register clock-to-output delay		1.0		1.0		1.0		1.0		1.0	ns
t_{FPDI}	FFB register pass through delay		0.5		0.5		1.0		1.0		2.0	ns
t_{FAOI}	FFB register async. set delay		2.0		2.5		3.0		4.0		6.0	ns
t_{PTXI}	FFB p-term assignment delay		0.8		1.0		1.2		1.5		2.0	ns
t_{FFD}	FFB feedback delay		4.0		5.0		6.5		8.0		10.0	ns

Note: 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

High-Density Function Block (FB) Internal AC Characteristics

Symbol	Parameter	XC73108-7 (Com only)		XC73108-10 (Com only)		XC73108-12 (Com/Ind only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{LOGI}	FB logic array delay [1]		3.5		3.5		4.0		5.0		6.0	ns
t_{LOGILP}	Low power FB logic delay [1]		7.0		7.5		9.0		11.0		14.0	ns
t_{SUI}	FB register setup time	1.5		2.5		3.0		4.0		6.0		ns
t_{HI}	FB register hold time	3.5		3.5		4.0		5.0		6.0		ns
t_{COI}	FB register clock-to-output delay		1.0		1.0		1.0		1.0		1.0	ns
t_{PDI}	FB register pass through delay		1.5		2.5		4.0		4.0		4.0	ns
t_{AOI}	FB register async. set/reset delay		2.5		3.0		4.0		5.0		7.0	ns
t_{RA}	Set/reset recovery time before FCLK ↑	15.0		19.0		21.0		25.0		31.0		ns
t_{HA}	Set/reset hold time after FCLK ↑	0		0		0		0		0		ns
t_{PRA}	Set/reset recovery time before p-term clock ↑	7.5		10.0		12.0		15.0		20.0		ns
t_{PHA}	Set/reset hold time after p-term clock ↑	5.0		6.0		8.0		9.0		12.0		ns
t_{PCI}	FB p-term clock delay		1.0		0		0		0		0	ns
t_{OEI}	FB p-term output enable delay		3.0		4.0		5.0		7.0		9.0	ns
t_{CARY8}	ALU carry delay within 1 FB [2]		5.0		6.0		8.0		12.0		15.0	ns
t_{CARYFB}	Carry lookahead delay per additional Functional Block [2]		1.0		1.5		2.0		3.0		4.0	ns

Notes: 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.
2. Arithmetic carry delays are measured as the increase in required set-up time to adjacent macrocell(s) for adder with registered outputs.

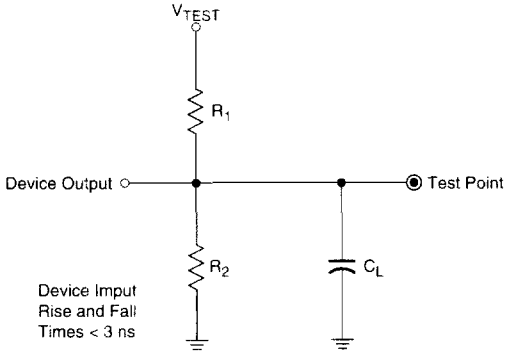
I/O Block External AC Characteristics

Symbol	Parameter	XC73108-7 (Com only)		XC73108-10 (Com only)		XC73108-12 (Com/Ind only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{IN}	Max pipeline frequency (input register to FFB or FB register) [1]	83.3		62.5		55.6		45.5		35.7		MHz
t_{SUIN}	Input register/latch setup time before FCLK ↑	4.0		5.0		6.0		7.0		10.0		ns
t_{HIN}	Input register/latch hold time after FCLK ↑	0		0		0		0		0		ns
t_{COIN}	FCLK ↑ to input register/latch output		2.5		3.5		4.0		5.0		6.0	ns
t_{CESUIN}	Clock enable setup time before FCLK ↑	5.0		7.0		8.0		10.0		12.0		ns
t_{CEHIN}	Clock enable hold time after FCLK ↑	0		0		0		0		0		ns
t_{CWHIN}	FCLK pulse width high time	4.0		5.0		5.5		6.0		6.0		ns
t_{CWLIN}	FCLK pulse width low time	4.0		5.0		5.5		6.0		6.0		ns

Note: 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

Internal AC Characteristics

Symbol	Parameter	XC73108-7 (Com only)		XC73108-10 (Com only)		XC73108-12 (Com/Ind only)		XC73108-15		XC73108-20		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay		2.5		3.5		4.0		5.0		6.0	ns
t_{FOUT}	FFB output buffer and pad delay		3.0		4.5		5.0		7.0		9.0	ns
t_{OUT}	FB output buffer and pad delay		4.5		6.5		8.0		10.0		14.0	ns
t_{UIM}	Universal Interconnect Matrix delay		6.0		9.0		10.0		12.0		15.0	ns
t_{FOE}	FOE input to output valid		7.5		10.0		12.0		15.0		20.0	ns
t_{FOD}	FOE input to output disable		7.5		10.0		12.0		15.0		20.0	ns
t_{FCLKI}	Fast clock buffer delay		1.5		2.5		3.0		4.0		5.0	ns



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
FO	5.0 V	5.0 V	160 Ω	120 Ω	35 pF
	3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X3491

Figure 3: AC Load Circuit

XC73108 Pinouts

PQ160	PG144 BG225	PQ100	PC84	Input	XC73108	Output
1	D3	–	–		V_{CCIO}	
2	C2	3	75	O/CKEN1		MC5-4
3	–	–	–		N/C	
4	B1	4	–	FO		MC2-1
5	–	–	–		N/C	
6	D2	5	76	O/FOE0		MC5-5
7	E3	–	–	O		MC5-1
8	C1	6	77	O/FOE1		MC5-6
9	E2	–	–	O		MC5-2
10	D1	7	78		V_{CCINT}/V_{PP}	
11	F3	8	79	I/FI		
12	F2	9	–	I/O/FI		MC5-7
13	E1	10	80	I/FI		
14	G2	–	–	I/O/FI		MC5-8
15	G3	11	81	I/FI		
16	F1	–	–	I/O/FI		MC5-9
17	G1	12	82	I/FI		
18	H2	13	83	I/FI		
19	H1	14	84	I/FI		
20	H3	–	–		**GND**	
21	J3	15	1		MR	
22	J1	16	2	I/FI		
23	K1	17	3	I/FI		
24	J2	18	4	I/FI		
25	K2	–	–	O		MC10-1
26	K3	19	5	I/FI		
27	L1	–	-	O		MC10-2
28	L2	20	6	I/FI		
29	M1	21	–	I/O/FI		MC10-8
30	N1	22	7	I/FI		
31	M2	23	8		**GND**	
32	L3	–	–	I/O/FI		MC10-7
33	N2	24	9	O/FCLK0		MC10-3
34	P1	–	–	O		MC10-6
35	M3	25	10	O/FCLK1		MC10-4
36	N3	26	–	FO		MC1-1
37	P2	27	11	I/O/FI		MC10-9
38	–	–	–		N/C	
39	–	–	–		N/C	
40	R1	–	–		**GND**	

PQ160	PG144 BG225	PQ100	PC84	Input	XC73108	Output
41	N4	28	–		V_{CCIO}	
42	P3	29	12	O/FCLK2		MC10-5
43	R2	–	–	I/O		MC4-1
44	P4	30	13	FO		MC1-2
45	N5	–	–	I/O		MC4-2
46	R3	–	–		V_{CCINT}	
47	P5	31	14	FO		MC1-3
48	R4	–	–	I/O		MC4-3
49	N6	32	15	FO		MC1-4
50	P6	–	–	I/O		MC4-4
51	R5	33	16		**GND**	
52	–	–	–		N/C	
53	–	–	–		N/C	
54	P7	34	17	FO		MC1-5
55	N7	–	–	I/O		MC4-5
56	R6	35	18	FO		MC1-6
57	R7	36	–	I/O/FI		MC4-7
58	P8	37	19	FO		MC1-7
59	R8	38	20	FO		MC1-8
60	N8	39	21	FO		MC1-9
61	N9	40	22		V_{CCIO}	
62	R9	41	23	I/O		MC9-1
63	R10	42	24	I/O		MC9-2
64	P9	43	25	I/O		MC9-3
65	–	–	–		N/C	
66	–	–	–		N/C	
67	P10	–	–	I/O		MC4-6
68	N10	44	26	I/O		MC9-6
69	R11	45	–	I/O/FI		MC4-8
70	P11	46	27		**GND**	
71	R12	47	28	I/O/FI		MC9-7
72	R13	48	–	I/O/FI		MC4-9
73	P12	49	29	I/O/FI		MC9-8
74	N11		–	I/O		MC3-1
75	P13	50	30	I/O/FI		MC9-9
76	R14	–	–	I/O		MC3-2
77	N12	51	31	I/O		MC8-1
78	N13	–	–	I/O		MC3-3
79	P14	52	32	I/O		MC8-2
80	R15	–	–		**GND**	

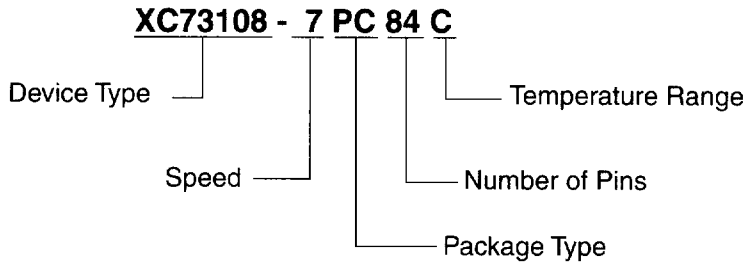
Note: With the XC73108 in the 225-pin ball grid array package, only 144 of the solder balls are connected, the remaining solder balls should be left unconnected.

XC73108 Pinouts (continued)

PQ160	PG144 BG225	PQ100	PC84	Input	XC73108	Output
81	M13	53	–		V_{CCIO}	
82	N14	54	33	I/O		MC8-3
83	–	–	–		N/C	
84	P15	–	–	I/O		MC3-4
85	–	–	–		N/C	
86	M14	55	34	I/O		MC9-4
87	L13	–	–	I/O		MC3-5
88	N15	56	35	I/O		MC9-5
89	L14	–	–	I/O		MC3-6
90	M15	57	36	I/O		MC8-4
91	K13	–	–	I/O/FI		MC3-7
92	K14	58	37	I/O		MC8-5
93	L15	–	–	I/O/FI		MC3-8
94	J14	59	38		V_{CCINT}	
95	J13	60	39	I/O		MC8-6
96	K15	61	–	I/O/FI		MC3-9
97	J15	62	40	I/O/FI		MC8-7
98	H14	63	41	I/O/FI		MC8-8
99	H15	–	–		**GND**	
100	H13	64	42		**GND**	
101	G13	65	43	I/O/FI		MC8-9
102	G15	66	44	I/O		MC7-1
103	F15	67	45	I/O		MC7-2
104	G14	68	46	I/O		MC7-3
105	F14	–	–	I/O		MC12-1
106	F13	69	47	I/O		MC7-4
107	E15	–	–	I/O		MC12-2
108	E14	70	48	I/O		MC7-5
109	D15	–	–	I/O		MC12-3
110	C15	71	49		**GND**	
111	D14	72	50	I/O		MC7-6
112	E13	–	–	I/O		MC12-4
113	C14	73	51	I/O		MC6-5
114	B15	–	–	I/O		MC12-5
115	D13	74	52	I/O		MC6-4
116	C13	75	–	I/O/FI		MC12-9
117	B14	76	53	I/O/FI		MC7-7
118	–	–	–		N/C	
119	–	–	–		N/C	
120	A15	77	–		**GND**	

PQ160	PG144 BG225	PQ100	PC84	Input	XC73108	Output
121	C12	–	–		V_{CCIO}	
122	B13	78	54	I/O/FI		MC7-8
123	A14	–	–	I/O		MC12-6
124	B12	79	55	I/O/FI		MC7-9
125	C11	–	–	I/O/FI		MC12-7
126	A13	80	56	I/O		MC6-1
127	B11	–	–		**GND**	
128	A12	–	–	I/O/FI		MC12-8
129	C10	81	–	I/O/FI		MC11-7
130	B10	–	–	I/O		MC11-1
131	–	–	–		N/C	
132	–	–	–		N/C	
133	A11	82	–	I/O/FI		MC11-8
134	B9	83	57	I/O		MC6-2
135	C9	84	58	I/O		MC6-6
136	A10	85	59	I/O		MC6-3
137	A9	86	60		**GND**	
138	B8	87	61	I/O/FI		MC6-7
139	A8	88	62	I/O/FI		MC6-8
140	C8	89	63	I/O/FI		MC6-9
141	C7	90	64		V_{CCIO}	
142	A7	91	65	FO		MC2-9
143	A6	92	66	FO		MC2-8
144	B7	93	67	FO		MC2-7
145	B6	94	–	I/O/FI		MC11-9
146	C6	95	68	FO		MC2-6
147	A5	–	–	I/O		MC11-2
148	B5	96	69	FO		MC2-5
149	–	–	–		N/C	
150	–	–	–		N/C	
151	A4	–	–	I/O		MC11-3
152	A3	97	70	FO		MC2-4
153	B4	–	–	I/O		MC11-4
154	C5	98	71	FO		MC2-3
155	B3	–	–	I/O		MC11-5
156	A2	99	72	FO		MC2-2
157	C4	100	73		V_{CCINT}	
158	C3	–	–	I/O		MC11-6
159	B2	1	74	O/CKEN0		MC5-3
160	A1	2	–		**GND**	

Ordering Information



Speed Options

-20	20 ns pin-to-pin delay
-15	15 ns pin-to-pin delay
-12	12 ns pin-to-pin delay
-10	10 ns pin-to-pin delay (commercial and industrial only)
-7	7.5 ns pin-to-pin delay (commercial only)

Packaging Options

PC84	84-Pin Plastic Leaded Chip Carrier
WC84	84-Pin Windowed Ceramic Leaded Chip Carrier
PQ100	100-Pin Plastic Quad Flat Pack
PG144	144-Pin Windowed Pin-Grid-Array
PQ160	160-Pin Plastic Quad Flat Pack
BG225	225-Pin Plastic Ball-Grid-Array

Temperature Options

C	Commercial	0°C to 70°C
I	Industrial	-40°C to 85°C
M	Military	-55°C (Ambient) to 125°C (Case)

Component Availability

Pins		84		100	144	160	225
Type		Plastic PLCC	Ceramic CLCC	Plastic PQFP	Ceramic PGA	Plastic PQFP	Plastic BGA
Code		PC84	WC84	PQ100	PG144	PQ160	BG225
XC73108	-20	CI	CI	CI	CIM	CI	CI
	-15	CI	CI	CI	CIM	CI	CI
	-12	CI	CI	CI	CI	CI	CI
	-10	C	C	C	C	C	C
	-7	C	C	C	C	C	C

C = Commercial = 0° to +70°C I = Industrial = –40° to 85°C M = Military = –55°C(A) to 125°C (C)