XC7336
36 Macrocell CMOS EPLD

Advance Product Information

Features

- Ultra high-performance EPLD
  - 7.5 ns pin-to-pin delay
  - 125 MHz maximum clock frequency
- Incorporates four Fast Function Blocks
- 100% interconnect matrix
- 36 Macrocells with programmable I/O architecture
- 18 outputs with 24 mA drive
- 3.3 V or 5 V I/O operation
- Meets JEDEC Standard (8-1A) for 3.3 V ±0.3 V
- Power management options
- Multiple security bits for design protection
- 44-pin leaded chip carrier package

General Description

The XC7336 is a member of the Xilinx XC7300 EPLD family. It consists of four Fast Function Blocks interconnected by a central Universal Interconnect Matrix (UIM).

The four Function Blocks in the XC7336 (Figure 1) are PAL-like structures, complete with programmable product term arrays and programmable multilevel Macrocells. Each Function Block receives 24 inputs, contains nine Macrocells configurable for registered or combinatorial logic and produces nine outputs which feedback to the UIM. For complete description of device functionality, see the XC7300 EPLD Family data sheet.

The Universal Interconnect Matrix connects the Function Blocks to each other and to all input pins, providing 100% connectivity between the Function Blocks. This allows logic functions to be mapped into the Function Blocks and interconnected without routing restrictions.

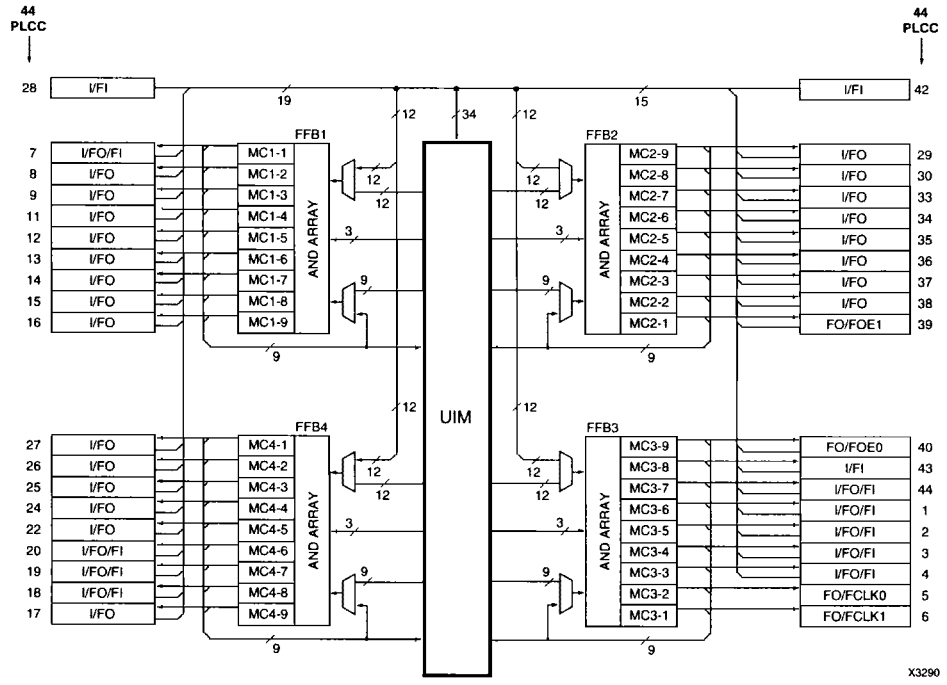

Figure 1. XC7336 Functional Block Diagram

Notice: The information contained in this data sheet pertains to products in the initial production phases of development. These specifications are subject to change without notice. Verify with your local Xilinx sales office that you have the latest data sheet before finalizing a design.

For a detailed description of the device architecture, see the XC7300 CMOS EPLD Family data sheet, page 4-2.

For a detailed description of the device timing, see pages 4-9 and 4-10.

For component availability and package physical dimensions, see Section 5.