7 Series FPGAs Overview

DS180 (v1.16.1) December 17, 2014 **Product Specification**

General Description

Xilinx® 7 series FPGAs comprise three new FPGA families that address the complete range of system requirements, ranging from low cost, small form factor, cost-sensitive, high-volume applications to ultra high-end connectivity bandwidth, logic capacity, and signal processing capability for the most demanding high-performance applications. The 7 series FPGAs include:

- Artix®-7 Family: Optimized for lowest cost and power with small form-factor packaging for the highest volume applications.
- Kintex®-7 Family: Optimized for best price-performance with a 2X improvement compared to previous generation, enabling a new class of FPGAs.
- Virtex®-7 Family: Optimized for highest system performance and capacity with a 2X improvement in system performance. Highest capability devices enabled by stacked silicon interconnect (SSI) technology.

Built on a state-of-the-art, high-performance, low-power (HPL), 28 nm, high-k metal gate (HKMG) process technology, 7 series FPGAs enable an unparalleled increase in system performance with 2.9 Tb/s of I/O bandwidth, 2 million logic cell capacity, and 5.3 TMAC/s DSP, while consuming 50% less power than previous generation devices to offer a fully programmable alternative to ASSPs and ASICs.

Summary of 7 Series FPGA Features

- Advanced high-performance FPGA logic based on real 6-input look-up table (LUT) technology configurable as distributed memory.
- 36 Kb dual-port block RAM with built-in FIFO logic for on-chip data buffering.
- High-performance SelectIO™ technology with support for DDR3 interfaces up to 1,866 Mb/s.
- High-speed serial connectivity with built-in multi-gigabit transceivers from 600 Mb/s to maximum rates of 6.6 Gb/s up to 28.05 Gb/s, offering a special low-power mode, optimized for chip-to-chip interfaces.
- A user configurable analog interface (XADC), incorporating dual 12-bit 1MSPS analog-to-digital converters with on-chip thermal and supply sensors.
- DSP slices with 25 x 18 multiplier, 48-bit accumulator, and pre-adder for high-performance filtering, including optimized symmetric coefficient filtering.
- Powerful clock management tiles (CMT), combining phase-locked loop (PLL) and mixed-mode clock manager (MMCM) blocks for high precision and low jitter.
- Integrated block for PCI Express® (PCIe), for up to x8 Gen3 Endpoint and Root Port designs.
- Wide variety of configuration options, including support for commodity memories, 256-bit AES encryption with HMAC/SHA-256 authentication, and built-in SEU detection and correction.
- Low-cost, wire-bond, lidless flip-chip, and high signal integrity flip-chip packaging offering easy migration between family members in the same package. All packages available in Pb-free and selected packages in Pb option.
- Designed for high performance and lowest power with 28 nm, HKMG, HPL process, 1.0V core voltage process technology and 0.9V core voltage option for even lower power.

Table 1: **7 Series Families Comparison**

Maximum Capability	Artix-7 Family	Kintex-7 Family	Virtex-7 Family
Logic Cells	215K	478K	1,955K
Block RAM(1)	13 Mb	34 Mb	68 Mb
DSP Slices	740	1,920	3,600
Peak DSP Performance(2)	929 GMAC/s	2,845 GMAC/s	5,335 GMAC/s
Transceivers	16	32	96
Peak Transceiver Speed	6.6 Gb/s	12.5 Gb/s	28.05 Gb/s
Peak Serial Bandwidth (Full Duplex)	211 Gb/s	800 Gb/s	2,784 Gb/s
PCIe Interface	x4 Gen2	x8 Gen2	x8 Gen3
Memory Interface	1,066 Mb/s	1,866 Mb/s	1,866 Mb/s
I/O Pins	500	500	1,200
I/O Voltage	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V
Package Options	Low-Cost, Wire-Bond, Lidless Flip-Chip	Low-Cost, Lidless Flip-Chip and High-Performance Flip-Chip	Highest Performance Flip-Chip

Notes:

1. Additional memory available in the form of distributed RAM.
2. Peak DSP performance numbers are based on symmetrical filter implementation.

Artix-7 FPGA Feature Summary

Table 2: **Artix-7 FPGA Feature Summary by Device**

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP48E1 Slices[2]	Block RAM Blocks[3]			CMTs[4]	PCIe[5]	GTPs	XADC Blocks	Total I/O Banks[6]	Max User I/O[7]
		Slices[1]	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)						
XC7A15T	16,640	2,600	200	45	50	25	900	5	1	4	1	5	250
XC7A35T	33,280	5,200	400	90	100	50	1,800	5	1	4	1	5	250
XC7A50T	52,160	8,150	600	120	150	75	2,700	5	1	4	1	5	250
XC7A75T	75,520	11,800	892	180	210	105	3,780	6	1	8	1	6	300
XC7A100T	101,440	15,850	1,188	240	270	135	4,860	6	1	8	1	6	300
XC7A200T	215,360	33,650	2,888	740	730	365	13,140	10	1	16	1	10	500

Notes:
1. Each 7 series FPGA slice contains four LUTs and eight flip-flops; only some slices can use their LUTs as distributed RAM or SRLs.
2. Each DSP slice contains a pre-adder, a 25 x 18 multiplier, an adder, and an accumulator.
3. Block RAMs are fundamentally 36 Kb in size; each block can also be used as two independent 18 Kb blocks.
4. Each CMT contains one MMCM and one PLL.
5. Artix-7 FPGA Interface Blocks for PCI Express support up to x4 Gen 2.
6. Does not include configuration Bank 0.
7. This number does not include GTP transceivers.

Table 3: **Artix-7 FPGA Device-Package Combinations and Maximum I/Os**

Package[1]	CPG236		CSG324		CSG325		FTG256		SBG484		FGG484[2]		FBG484[2]		FGG676[3]		FBG676[3]		FFG1156	
Size (mm)	10 x 10		15 x 15		15 x 15		17 x 17		19 x 19		23 x 23		23 x 23		27 x 27		27 x 27		35 x 35	
Ball Pitch (mm)	0.5		0.8		0.8		1.0		0.8		1.0		1.0		1.0		1.0		1.0	
Device	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]	GTP	I/O HR[4]
XC7A15T	2	106	0	210	4	150	0	170			4	250								
XC7A35T	2	106	0	210	4	150	0	170			4	250								
XC7A50T	2	106	0	210	4	150	0	170			4	250								
XC7A75T			0	210			0	170			4	285			8	300				
XC7A100T			0	210			0	170			4	285			8	300				
XC7A200T									4	285			4	285			8	400	16	500

Notes:
1. All packages listed are Pb-free. Some packages are available in Pb option.
2. Devices in FGG484 and FBG484 are footprint compatible.
3. Devices in FGG676 and FBG676 are footprint compatible.
4. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.

Kintex-7 FPGA Feature Summary

Table 4: **Kintex-7 FPGA Feature Summary by Device**

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP Slices[2]	Block RAM Blocks[3]			CMTs[4]	PCIe[5]	GTXs	XADC Blocks	Total I/O Banks[6]	Max User I/O[7]
		Slices[1]	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)						
XC7K70T	65,600	10,250	838	240	270	135	4,860	6	1	8	1	6	300
XC7K160T	162,240	25,350	2,188	600	650	325	11,700	8	1	8	1	8	400
XC7K325T	326,080	50,950	4,000	840	890	445	16,020	10	1	16	1	10	500
XC7K355T	356,160	55,650	5,088	1,440	1,430	715	25,740	6	1	24	1	6	300
XC7K410T	406,720	63,550	5,663	1,540	1,590	795	28,620	10	1	16	1	10	500
XC7K420T	416,960	65,150	5,938	1,680	1,670	835	30,060	8	1	32	1	8	400
XC7K480T	477,760	74,650	6,788	1,920	1,910	955	34,380	8	1	32	1	8	400

Notes:
1. Each 7 series FPGA slice contains four LUTs and eight flip-flops; only some slices can use their LUTs as distributed RAM or SRLs.
2. Each DSP slice contains a pre-adder, a 25 x 18 multiplier, an adder, and an accumulator.
3. Block RAMs are fundamentally 36 Kb in size; each block can also be used as two independent 18 Kb blocks.
4. Each CMT contains one MMCM and one PLL.
5. Kintex-7 FPGA Interface Blocks for PCI Express support up to x8 Gen 2.
6. Does not include configuration Bank 0.
7. This number does not include GTX transceivers.

Table 5: **Kintex-7 FPGA Device-Package Combinations and Maximum I/Os**

Package[1]	FBG484			FBG676[2]			FFG676[2]			FBG900[3]			FFG900[3]			FFG901			FFG1156		
Size (mm)	23 x 23			27 x 27			27 x 27			31 x 31			31 x 31			31 x 31			35 x 35		
Ball Pitch (mm)	1.0			1.0			1.0			1.0			1.0			1.0			1.0		
Device	GTX	I/O		GTX	I/O		GTX	I/O		GTX	I/O		GTX	I/O		GTX	I/O		GTX	I/O	
		HR[4]	HP[5]		HR[4]	HP[5]		HR[4]	HP[5]		HR[4]	HP[5]		HR[4]	HP[5]		HR[4]	HP[5]		HR[4]	HP[5]
XC7K70T	4	185	100	8	200	100															
XC7K160T	4	185	100	8	250	150	8	250	150												
XC7K325T				8	250	150	8	250	150	16	350	150	16	350	150						
XC7K355T																24	300	0			
XC7K410T				8	250	150	8	250	150	16	350	150	16	350	150						
XC7K420T																28	380	0	32	400	0
XC7K480T																28	380	0	32	400	0

Notes:
1. All packages listed are Pb-free. Some packages are available in Pb option.
2. Devices in FBG676 and FFG676 are footprint compatible.
3. Devices in FBG900 and FFG900 are footprint compatible.
4. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.
5. HP = High-performance I/O with support for I/O voltage from 1.2V to 1.8V.

Virtex-7 FPGA Feature Summary

Table 6: **Virtex-7 FPGA Feature Summary**

Device[1]	Logic Cells	Configurable Logic Blocks (CLBs)		DSP Slices[3]	Block RAM Blocks[4]			CMTs[5]	PCIe[6]	GTX	GTH	GTZ	XADC Blocks	Total I/O Banks[7]	Max User I/O[8]	SLRs[9]
		Slices[2]	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)									
XC7V585T	582,720	91,050	6,938	1,260	1,590	795	28,620	18	3	36	0	0	1	17	850	N/A
XC7V2000T	1,954,560	305,400	21,550	2,160	2,584	1,292	46,512	24	4	36	0	0	1	24	1,200	4
XC7VX330T	326,400	51,000	4,388	1,120	1,500	750	27,000	14	2	0	28	0	1	14	700	N/A
XC7VX415T	412,160	64,400	6,525	2,160	1,760	880	31,680	12	2	0	48	0	1	12	600	N/A
XC7VX485T	485,760	75,900	8,175	2,800	2,060	1,030	37,080	14	4	56	0	0	1	14	700	N/A
XC7VX550T	554,240	86,600	8,725	2,880	2,360	1,180	42,480	20	2	0	80	0	1	16	600	N/A
XC7VX690T	693,120	108,300	10,888	3,600	2,940	1,470	52,920	20	3	0	80	0	1	20	1,000	N/A
XC7VX980T	979,200	153,000	13,838	3,600	3,000	1,500	54,000	18	3	0	72	0	1	18	900	N/A
XC7VX1140T	1,139,200	178,000	17,700	3,360	3,760	1,880	67,680	24	4	0	96	0	1	22	1,100	4
XC7VH580T	580,480	90,700	8,850	1,680	1,880	940	33,840	12	2	0	48	8	1	12	600	2
XC7VH870T	876,160	136,900	13,275	2,520	2,820	1,410	50,760	18	3	0	72	16	1	6	300	3

Notes:
1. EasyPath™-7 FPGAs are also available to provide a fast, simple, and risk-free solution for cost reducing Virtex-7 T and Virtex-7 XT FPGA designs
2. Each 7 series FPGA slice contains four LUTs and eight flip-flops; only some slices can use their LUTs as distributed RAM or SRLs.
3. Each DSP slice contains a pre-adder, a 25 x 18 multiplier, an adder, and an accumulator.
4. Block RAMs are fundamentally 36 Kb in size; each block can also be used as two independent 18 Kb blocks.
5. Each CMT contains one MMCM and one PLL.
6. Virtex-7 T FPGA Interface Blocks for PCI Express support up to x8 Gen 2. Virtex-7 XT and Virtex-7 HT Interface Blocks for PCI Express support up to x8 Gen 3, with the exception of the XC7VX485T device, which supports x8 Gen 2.
7. Does not include configuration Bank 0.
8. This number does not include GTX, GTH, or GTZ transceivers.
9. Super logic regions (SLRs) are the constituent parts of FPGAs that use SSI technology. Virtex-7 HT devices use SSI technology to connect SLRs with 28.05 Gb/s transceivers.

Table 7: **Virtex-7 FPGA Device-Package Combinations and Maximum I/Os**

Package[1]	FFG1157				FFG1761[2]				FHG1761[2]				FLG1925		
Size (mm)	35 x 35				42.5 x 42.5				45 x 45				45 x 45		
Ball Pitch	1.0				1.0				1.0				1.0		
Device	GTX	GTH	I/O		GTX	GTH	I/O		GTX	GTH	I/O		GTX	I/O	
			HR[3]	HP[4]			HR[3]	HP[4]			HR[3]	HP[4]		HR[3]	HP[4]
XC7V585T	20	0	0	600	36	0	100	750							
XC7V2000T									36	0	0	850	16	0	1,200
XC7VX330T	0	20	0	600	0	28	50	650							
XC7VX415T	0	20	0	600											
XC7VX485T	20	0	0	600	28	0	0	700							
XC7VX550T															
XC7VX690T	0	20	0	600	0	36	0	850							
XC7VX980T															
XC7VX1140T															

Notes:
1. All packages listed are Pb-free. Some packages are available in Pb option.
2. Devices in FFG1761 and FHG1761 are footprint compatible.
3. HR = High-range I/O with support for I/O voltage from 1.2V to 3.3V.
4. HP = High-performance I/O with support for I/O voltage from 1.2V to 1.8V.

Table 8: **Virtex-7 FPGA Device-Package Combinations and Maximum I/Os - Continued**

Package[1]	FFG1158			FFG1926[2]			FLG1926[2]			FFG1927			FFG1928[3]			FLG1928[3]			FFG1930[4]			FLG1930[4]		
Size (mm)	35 x 35			45 x 45			45 x 45			45 x 45			45 x 45			45 x 45			45 x 45			45 x 45		
Ball Pitch	1.0			1.0			1.0			1.0			1.0			1.0			1.0			1.0		
Device	GTX	GTH	I/O	GTX	GTH	I/O	GTX	GTH	I/O	GTX	GTH	I/O	GTX	GTH	I/O	GTX	GTH	I/O	GTX	GTH	I/O	GTX	GTH	I/O
			HP[5]			HP[5]			HP[5]			HP[5]			HP[5]			HP[5]			HP[5]			HP[5]
XC7V585T																								
XC7V2000T																								
XC7VX330T																								
XC7VX415T	0	48	350							0	48	600												
XC7VX485T	48	0	350							56	0	600							24	0	700			
XC7VX550T	0	48	350							0	80	600												
XC7VX690T	0	48	350	0	64	720				0	80	600							0	24	1,000			
XC7VX980T				0	64	720							0	72	480				0	24	900			
XC7VX1140T							0	64	720							0	96	480				0	24	1,100

Notes:
1. All packages listed are Pb-free. Some packages are available in Pb option.
2. Devices in FFG1926 and FLG1926 are footprint compatible.
3. Devices in FFG1928 and FLG1928 are footprint compatible.
4. Devices in FFG1930 and FLG1930 are footprint compatible.
5. HP = High-performance I/O with support for I/O voltage from 1.2V to 1.8V.

Table 9: **Virtex-7 HT FPGA Device-Package Combinations and Maximum I/Os**

Package[1]	FLG1155			HCG1155			FLG1931			FLG1932		
Size (mm)	35 x 35			35 x 35			45 x 45			45 x 45		
Ball Pitch	1.0			1.0			1.0			1.0		
Device	GTH	GTZ	I/O	GTH	GTZ	I/O	GTH	GTZ	I/O	GTH	GTZ	I/O
			HP[2]			HP[2]			HP[2]			HP[2]
XC7VH580T	24	8	400	24	8	400	48	8	600			
XC7VH870T										72	16	300

Notes:
1. All packages listed are Pb-free. Some packages are available in Pb option.
2. HP = High-performance I/O with support for I/O voltage from 1.2V to 1.8V.

Stacked Silicon Interconnect (SSI) Technology

There are many challenges associated with creating high capacity FPGAs that Xilinx addresses with the SSI technology. SSI technology enables multiple super logic regions (SLRs) to be combined on a passive interposer layer, using proven manufacturing and assembly techniques from industry leaders, to create a single FPGA with more than ten thousand inter-SLR connections, providing ultra-high bandwidth connectivity with low latency and low power consumption. There are two types of SLRs used in Virtex-7 FPGAs: a logic intensive SLR used in the Virtex-7 T devices and a DSP/block RAM/transceiver-rich SLR used in the Virtex-7 XT and HT devices. SSI technology enables the production of higher capability FPGAs than traditional manufacturing methods, enabling the highest capacity and highest performance FPGAs ever created to reach production more quickly and with less risk than would otherwise be possible. Thousands of super long line (SLL) routing resources and ultra-high performance clock lines that cross between the SLRs ensure that designs span seamlessly across these high-density programmable logic devices.

CLBs, Slices, and LUTs

Some key features of the CLB architecture include:

- Real 6-input look-up tables (LUTs)
- Memory capability within the LUT
- Register and shift register functionality

The LUTs in 7 series FPGAs can be configured as either one 6-input LUT (64-bit ROMs) with one output, or as two 5-input LUTs (32-bit ROMs) with separate outputs but common addresses or logic inputs. Each LUT output can optionally be registered in a flip-flop. Four such LUTs and their eight flip-flops as well as multiplexers and arithmetic carry logic form a slice, and two slices form a configurable logic block (CLB). Four of the eight flip-flops per slice (one per LUT) can optionally be configured as latches.

Between 25–50% of all slices can also use their LUTs as distributed 64-bit RAM or as 32-bit shift registers (SRL32) or as two SRL16s. Modern synthesis tools take advantage of these highly efficient logic, arithmetic, and memory features.

Clock Management

Some of the key highlights of the clock management architecture include:

- High-speed buffers and routing for low-skew clock distribution
- Frequency synthesis and phase shifting
- Low-jitter clock generation and jitter filtering

Each 7 series FPGA has up to 24 clock management tiles (CMTs), each consisting of one mixed-mode clock manager (MMCM) and one phase-locked loop (PLL).

Mixed-Mode Clock Manager and Phase-Locked Loop

The MMCM and PLL share many characteristics. Both can serve as a frequency synthesizer for a wide range of frequencies and as a jitter filter for incoming clocks. At the center of both components is a voltage-controlled oscillator (VCO), which speeds up and slows down depending on the input voltage it receives from the phase frequency detector (PFD).

There are three sets of programmable frequency dividers: D, M, and O. The pre-divider D (programmable by configuration and afterwards via DRP) reduces the input frequency and feeds one input of the traditional PLL phase/frequency comparator. The feedback divider M (programmable by configuration and afterwards via DRP) acts as a multiplier because it divides the VCO output frequency before feeding the other input of the phase comparator. D and M must be chosen appropriately to keep the VCO within its specified frequency range. The VCO has eight equally-spaced output phases (0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°). Each can be selected to drive one of the output dividers (six for the PLL, O0 to O5, and seven for the MMCM, O0 to O6), each programmable by configuration to divide by any integer from 1 to 128.

The MMCM and PLL have three input-jitter filter options: low bandwidth, high bandwidth, or optimized mode. Low-bandwidth mode has the best jitter attenuation but not the smallest phase offset. High-bandwidth mode has the best phase offset, but not the best jitter attenuation. Optimized mode allows the tools to find the best setting.

MMCM Additional Programmable Features

The MMCM can have a fractional counter in either the feedback path (acting as a multiplier) or in one output path. Fractional counters allow non-integer increments of $^1/_8$ and can thus increase frequency synthesis capabilities by a factor of 8.

The MMCM can also provide fixed or dynamic phase shift in small increments that depend on the VCO frequency. At 1600 MHz, the phase-shift timing increment is 11.2 ps.

Clock Distribution

Each 7 series FPGA provides six different types of clock lines (BUFG, BUFR, BUFIO, BUFH, BUFMR, and the high-performance clock) to address the different clocking requirements of high fanout, short propagation delay, and extremely low skew.

Global Clock Lines

In each 7 series FPGA, 32 global clock lines have the highest fanout and can reach every flip-flop clock, clock enable, and set/reset, as well as many logic inputs. There are 12 global clock lines within any clock region driven by the horizontal clock buffers (BUFH). Each BUFH can be independently enabled/disabled, allowing for clocks to be turned off within a region, thereby offering fine-grain control over which clock regions consume power. Global clock lines can be driven by global clock buffers, which can also perform glitchless clock multiplexing and clock enable functions. Global clocks are often driven from the CMT, which can completely eliminate the basic clock distribution delay.

Regional Clocks

Regional clocks can drive all clock destinations in their region. A region is defined as an area that is 50 I/O and 50 CLB high and half the chip wide. 7 series FPGAs have between six and twenty-four regions. There are four regional clock tracks in every region. Each regional clock buffer can be driven from any of four clock-capable input pins, and its frequency can optionally be divided by any integer from 1 to 8.

I/O Clocks

I/O clocks are especially fast and serve only I/O logic and serializer/deserializer (SerDes) circuits, as described in the I/O Logic section. The 7 series devices have a direct connection from the MMCM to the I/O for low-jitter, high-performance interfaces.

Block RAM

Some of the key features of the block RAM include:

- Dual-port 36 Kb block RAM with port widths of up to 72
- Programmable FIFO logic
- Built-in optional error correction circuitry

Every 7 series FPGA has between 25 and 1,880 dual-port block RAMs, each storing 36 Kb. Each block RAM has two completely independent ports that share nothing but the stored data.

Synchronous Operation

Each memory access, read or write, is controlled by the clock. All inputs, data, address, clock enables, and write enables are registered. Nothing happens without a clock. The input address is always clocked, retaining data until the next operation. An optional output data pipeline register allows higher clock rates at the cost of an extra cycle of latency.

During a write operation, the data output can reflect either the previously stored data, the newly written data, or can remain unchanged.

Programmable Data Width

Each port can be configured as 32K × 1, 16K × 2, 8K × 4, 4K × 9 (or 8), 2K × 18 (or 16), 1K × 36 (or 32), or 512 × 72 (or 64). The two ports can have different aspect ratios without any constraints.

Each block RAM can be divided into two completely independent 18 Kb block RAMs that can each be configured to any aspect ratio from 16K × 1 to 512 × 36. Everything described previously for the full 36 Kb block RAM also applies to each of the smaller 18 Kb block RAMs.

Only in simple dual-port (SDP) mode can data widths of greater than 18 bits (18 Kb RAM) or 36 bits (36 Kb RAM) be accessed. In this mode, one port is dedicated to read operation, the other to write operation. In SDP mode, one side (read or write) can be variable, while the other is fixed to 32/36 or 64/72.

Both sides of the dual-port 36 Kb RAM can be of variable width.

Two adjacent 36 Kb block RAMs can be configured as one cascaded 64K × 1 dual-port RAM without any additional logic.

Error Detection and Correction

Each 64-bit-wide block RAM can generate, store, and utilize eight additional Hamming code bits and perform single-bit error correction and double-bit error detection (ECC) during the read process. The ECC logic can also be used when writing to or reading from external 64- to 72-bit-wide memories.

FIFO Controller

The built-in FIFO controller for single-clock (synchronous) or dual-clock (asynchronous or multirate) operation increments the internal addresses and provides four handshaking flags: full, empty, almost full, and almost empty. The almost full and almost empty flags are freely programmable. Similar to the block RAM, the FIFO width and depth are programmable, but the write and read ports always have identical width.

First word fall-through mode presents the first-written word on the data output even before the first read operation. After the first word has been read, there is no difference between this mode and the standard mode.

Digital Signal Processing — DSP Slice

Some highlights of the DSP functionality include:

- 25 × 18 two's complement multiplier/accumulator high-resolution (48 bit) signal processor
- Power saving pre-adder to optimize symmetrical filter applications
- Advanced features: optional pipelining, optional ALU, and dedicated buses for cascading

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP slices. All 7 series FPGAs have many dedicated, full custom, low-power DSP slices, combining high speed with small size while retaining system design flexibility.

Each DSP slice fundamentally consists of a dedicated 25 × 18 bit two's complement multiplier and a 48-bit accumulator, both capable of operating up to 741 MHz. The multiplier can be dynamically bypassed, and two 48-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP slice count by up to 50%. The DSP also includes a 48-bit-wide Pattern Detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 96-bit-wide logic functions when used in conjunction with the logic unit.

The DSP slice provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

Input/Output

Some highlights of the input/output functionality include:

- High-performance SelectIO technology with support for 1,866 Mb/s DDR3
- High-frequency decoupling capacitors within the package for enhanced signal integrity
- Digitally Controlled Impedance that can be 3-stated for lowest power, high-speed I/O operation

The number of I/O pins varies depending on device and package size. Each I/O is configurable and can comply with a large number of I/O standards. With the exception of the supply pins and a few dedicated configuration pins, all other package pins have the same I/O capabilities, constrained only by certain banking rules. The I/O in 7 series FPGAs are classed as high range (HR) or high performance (HP). The HR I/Os offer the widest range of voltage support, from 1.2V to 3.3V. The HP I/Os are optimized for highest performance operation, from 1.2V to 1.8V.

HR and HP I/O pins in 7 series FPGAs are organized in banks, with 50 pins per bank. Each bank has one common V_{CCO} output supply, which also powers certain input buffers. Some single-ended input buffers require an internally generated or an externally applied reference voltage (V_{REF}). There are two V_{REF} pins per bank (except configuration bank 0). A single bank can have only one V_{REF} voltage value.

Xilinx 7 series FPGAs use a variety of package types to suit the needs of the user, including small form factor wire-bond packages for lowest cost; conventional, high performance flip-chip packages; and lidless flip-chip packages that balance smaller form factor with high performance. In the flip-chip packages, the silicon device is attached to the package substrate using a high-performance flip-chip process. Controlled ESR discrete decoupling capacitors are mounted on the package substrate to optimize signal integrity under simultaneous switching of outputs (SSO) conditions.

I/O Electrical Characteristics

Single-ended outputs use a conventional CMOS push/pull output structure driving High towards V_{CCO} or Low towards ground, and can be put into a high-Z state. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up or a weak pull-down resistor.

Most signal pin pairs can be configured as differential input pairs or output pairs. Differential input pin pairs can optionally be terminated with a 100Ω internal resistor. All 7 series devices support differential standards beyond LVDS: HT, RSDS, BLVDS, differential SSTL, and differential HSTL.

Each of the I/Os supports memory I/O standards, such as single-ended and differential HSTL as well as single-ended SSTL and differential SSTL. The SSTL I/O standard can support data rates of up to 1,866 Mb/s for DDR3 interfacing applications.

3-State Digitally Controlled Impedance and Low Power I/O Features

The 3-state Digitally Controlled Impedance (T_DCI) can control the output drive impedance (series termination) or can provide parallel termination of an input signal to V_{CCO} or split (Thevenin) termination to $V_{CCO}/2$. This allows users to eliminate off-chip termination for signals using T_DCI. In addition to board space savings, the termination automatically turns off when in output mode or when 3-stated, saving considerable power compared to off-chip termination. The I/Os also have low power modes for IBUF and IDELAY to provide further power savings, especially when used to implement memory interfaces.

I/O Logic

Input and Output Delay

All inputs and outputs can be configured as either combinatorial or registered. Double data rate (DDR) is supported by all inputs and outputs. Any input and some outputs can be individually delayed by up to 32 increments of 78 ps, 52 ps, or 39 ps each. Such delays are implemented as IDELAY and ODELAY. The number of delay steps can be set by configuration and can also be incremented or decremented while in use.

ISERDES and OSERDES

Many applications combine high-speed, bit-serial I/O with slower parallel operation inside the device. This requires a serializer and deserializer (SerDes) inside the I/O structure. Each I/O pin possesses an 8-bit IOSERDES (ISERDES and OSERDES) capable of performing serial-to-parallel or parallel-to-serial conversions with programmable widths of 2, 3, 4, 5, 6, 7, or 8 bits. By cascading two IOSERDES from two adjacent pins (default from differential I/O), wider width conversions of 10 and 14 bits can also be supported. The ISERDES has a special oversampling mode capable of asynchronous data recovery for applications like a 1.25 Gb/s LVDS I/O-based SGMII interface.

Low-Power Gigabit Transceivers

Some highlights of the Low-Power Gigabit Transceivers include:

- High-performance transceivers capable of up to 6.6 Gb/s (GTP), 12.5 Gb/s (GTX), 13.1 Gb/s (GTH), or 28.05 Gb/s (GTZ) line rates depending on the family, enabling the first single device for 400G implementations.
- Low-power mode optimized for chip-to-chip interfaces.
- Advanced Transmit pre and post emphasis, receiver linear equalization (CTLE), and decision feedback equalization (DFE) for long reach or backplane applications. Auto-adaption at receiver equalization and on-chip Eye Scan for easy serial link tuning.

Ultra-fast serial data transmission to optical modules, between ICs on the same PCB, over the backplane, or over longer distances is becoming increasingly popular and important to enable customer line cards to scale to 100 Gb/s and onwards to 400 Gb/s. It requires specialized dedicated on-chip circuitry and differential I/O capable of coping with the signal integrity issues at these high data rates.

The transceiver count in the 7 series FPGAs ranges from up to 16 transceiver circuits in the Artix-7 family, up to 32 transceiver circuits in the Kintex-7 family, and up to 96 transceiver circuits in the Virtex-7 family. Each serial transceiver is a combined transmitter and receiver. The various 7 series serial transceivers use either a combination of ring oscillators and LC tank or, in the case of the GTZ, a single LC tank architecture to allow the ideal blend of flexibility and performance while enabling IP portability across the family members. The different 7 series family members offer different top-end data rates. The GTP operates up to 6.6 Gb/s, the GTX operates up to 12.5 Gb/s, the GTH operates up to 13.1 Gb/s, and the GTZ operates up to 28.05 Gb/s. Lower data rates can be achieved using FPGA logic-based oversampling. The serial transmitter and receiver are independent circuits that use an advanced PLL architecture to multiply the reference frequency input by certain programmable numbers up to 100 to become the bit-serial data clock. Each transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

Transmitter

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 16, 20, 32, 40, 64, or 80. Additionally, the GTZ transmitter supports up to 160 bit data widths. This allows the designer to trade-off datapath width for timing margin in high-performance designs. These transmitter outputs drive the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data is fed through an optional FIFO and has additional hardware support for the 8B/10B, 64B/66B, or 64B/67B encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

Receiver

The receiver is fundamentally a serial-to-parallel converter, changing the incoming bit-serial differential signal into a parallel stream of words, each 16, 20, 32, 40, 64, or 80 bits. Additionally, the GTZ receiver supports up to 160 bit data widths. This allows the FPGA designer to trade-off internal datapath width versus logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable linear and decision feedback equalizers (to compensate for PC board and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. There is no need for a separate clock line. The data pattern uses non-return-to-zero (NRZ) encoding and optionally guarantees sufficient data transitions by using the selected encoding scheme. Parallel data is then transferred into the FPGA logic using

the RXUSRCLK clock. For short channels, the transceivers offers a special low power mode (LPM) to reduce power consumption by approximately 30%.

Out-of-Band Signaling

The transceivers provide out-of-band (OOB) signaling, often used to send low-speed signals from the transmitter to the receiver while high-speed serial data transmission is not active. This is typically done when the link is in a powered-down state or has not yet been initialized. This benefits PCI Express and SATA/SAS applications.

Integrated Interface Blocks for PCI Express Designs

Highlights of the integrated blocks for PCI Express include:

- Compliant to the PCI Express Base Specification 2.1 or 3.0 (depending of family) with Endpoint and Root Port capability
- Supports Gen1 (2.5 Gb/s), Gen2 (5 Gb/s), and Gen3 (8 Gb/s) depending on device family
- Advanced configuration options, Advanced Error Reporting (AER), and End-to-End CRC (ECRC) Advanced Error Reporting and ECRC features
- Multiple-function and single root I/O virtualization (SR-IOV) support enabled through soft-logic wrappers or embedded in the integrated block depending on family

All 7 series devices include at least one integrated block for PCI Express technology that can be configured as an Endpoint or Root Port, compliant to the PCI Express Base Specification Revision 2.1 or 3.0. The Root Port can be used to build the basis for a compatible Root Complex, to allow custom FPGA-to-FPGA communication via the PCI Express protocol, and to attach ASSP Endpoint devices, such as Ethernet Controllers or Fibre Channel HBAs, to the FPGA.

This block is highly configurable to system design requirements and can operate 1, 2, 4, or 8 lanes at the 2.5 Gb/s, 5.0 Gb/s, and 8.0 Gb/s data rates. For high-performance applications, advanced buffering techniques of the block offer a flexible maximum payload size of up to 1,024 bytes. The integrated block interfaces to the integrated high-speed transceivers for serial connectivity and to block RAMs for data buffering. Combined, these elements implement the Physical Layer, Data Link Layer, and Transaction Layer of the PCI Express protocol.

Xilinx provides a light-weight, configurable, easy-to-use LogiCORE™ IP wrapper that ties the various building blocks (the integrated block for PCI Express, the transceivers, block RAM, and clocking resources) into an Endpoint or Root Port solution. The system designer has control over many configurable parameters: lane width, maximum payload size, FPGA logic interface speeds, reference clock frequency, and base address register decoding and filtering.

Xilinx offers two wrappers for the integrated block: AXI4-Stream and AXI4 (memory mapped). Note that legacy TRN/Local Link is not available in 7 series devices for the integrated block for PCI Express. AXI4-Stream is designed for existing customers of the integrated block and enables easy migration to AXI4-Stream from TRN. AXI4 (memory mapped) is designed for Xilinx Platform Studio/EDK design flow and MicroBlaze™ processor based designs.

More information and documentation on solutions for PCI Express designs can be found at: http://www.xilinx.com/technology/protocols/pciexpress.htm.

Configuration

There are many advanced configuration features, including:

- High-speed SPI and BPI (parallel NOR) configuration
- Built-in MultiBoot and safe-update capability
- 256-bit AES encryption with HMAC/SHA-256 authentication
- Built-in SEU detection and correction
- Partial reconfiguration

Xilinx 7 series FPGAs store their customized configuration in SRAM-type internal latches. The number of configuration bits is between 17 Mb and 450 Mb, depending on device size and user-design implementation options. The configuration storage is volatile and must be reloaded whenever the FPGA is powered up. This storage can also be reloaded at any time

by pulling the PROGRAM_B pin Low. Several methods and data formats for loading configuration are available, determined by the three mode pins.

The SPI interface (x1, x2, and x4 modes) and the BPI interface (parallel-NOR x8 and x16) are two common methods used for configuring the FPGA. Users can directly connect an SPI or BPI flash to the FPGA, and the FPGA's internal configuration logic reads the bitstream out of the flash and configures itself. The FPGA automatically detects the bus width on the fly, eliminating the need for any external controls or switches. Bus widths supported are x1, x2, and x4 for SPI, and x8 and x16 for BPI. The larger bus widths increase configuration speed and reduce the amount of time it takes for the FPGA to start up after power-on. Note that BPI is not supported in the CPG236 package used by the XC7A15T, XC7A35T, and XC7A50T.

In master mode, the FPGA can drive the configuration clock from an internally generated clock, or for higher speed configuration, the FPGA can use an external configuration clock source. This allows high-speed configuration with the ease of use characteristic of master mode. Slave modes up to 32 bits wide are also supported by the FPGA that are especially useful for processor-driven configuration.

The FPGA has the ability to reconfigure itself with a different image using SPI or BPI flash, eliminating the need for an external controller. The FPGA can reload its original design in case there are any errors in the data transmission, ensuring an operational FPGA at the end of the process. This is especially useful for updates to a design after the end product has been shipped. Customers can ship their products with an early version of the design, thus getting their products to market faster. This feature allows customers to keep their end users current with the most up-to-date designs while the product is already in the field.

The dynamic reconfiguration port (DRP) gives the system designer easy access to the configuration and status registers of the MMCM, PLL, XADC, transceivers, and integrated block for PCI Express. The DRP behaves like a set of memory-mapped registers, accessing and modifying block-specific configuration bits as well as status and control registers.

Encryption, Readback, and Partial Reconfiguration

In all 7 series FPGAs devices, the FPGA bitstream, which contains sensitive customer IP, can be protected with 256-bit AES encryption and HMAC/SHA-256 authentication to prevent unauthorized copying of the design. The FPGA performs decryption on the fly during configuration using an internally stored 256-bit key. This key can reside in battery-backed RAM or in nonvolatile eFUSE bits.

Most configuration data can be read back without affecting the system's operation. Typically, configuration is an all-or-nothing operation, but Xilinx 7 series FPGAs support partial reconfiguration. This is an extremely powerful and flexible feature that allows the user to change portions of the FPGA while other portions remain static. Users can time-slice these portions to fit more IP into smaller devices, saving cost and power. Where applicable in certain designs, partial reconfiguration can greatly improve the versatility of the FPGA.

XADC (Analog-to-Digital Converter)

Highlights of the XADC architecture include:

- Dual 12-bit 1 MSPS analog-to-digital converters (ADCs)
- Up to 17 flexible and user-configurable analog inputs
- On-chip or external reference option
- On-chip temperature (±4°C max error) and power supply (±1% max error) sensors
- Continuous JTAG access to ADC measurements

All Xilinx 7 series FPGAs integrate a new flexible analog interface called XADC. When combined with the programmable logic capability of the 7 series FPGAs, the XADC can address a broad range of data acquisition and monitoring requirements. For more information, go to: http://www.xilinx.com/ams.

The XADC contains two 12-bit 1 MSPS ADCs with separate track and hold amplifiers, an on-chip analog multiplexer (up to 17 external analog input channels supported), and on-chip thermal and supply sensors. The two ADCs can be configured to simultaneously sample two external-input analog channels. The track and hold amplifiers support a range of analog input signal types, including unipolar, bipolar, and differential. The analog inputs can support signal bandwidths of at least 500 KHz at sample rates of 1MSPS. It is possible to support higher analog bandwidths using external analog multiplexer

mode with the dedicated analog input (see UG480, 7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide).

The XADC optionally uses an on-chip reference circuit (±1%), thereby eliminating the need for any external active components for basic on-chip monitoring of temperature and power supply rails. To achieve the full 12-bit performance of the ADCs, an external 1.25V reference IC is recommended.

If the XADC is not instantiated in a design, then by default it digitizes the output of all on-chip sensors. The most recent measurement results (together with maximum and minimum readings) are stored in dedicated registers for access at any time via the JTAG interface. User-defined alarm thresholds can automatically indicate over-temperature events and unacceptable power supply variation. A user-specified limit (for example, 100°C) can be used to initiate an automatic powerdown.

EasyPath-7 FPGAs

EasyPath-7 FPGAs provide a fast, simple, and risk-free solution for cost reducing Kintex-7, Virtex-7 T, and Virtex-7 XT FPGA designs. EasyPath-7 FPGAs support the same packages, speed grades, and match all Kintex-7 or Virtex-7 FPGA data sheet specifications (in function and timing). With no re-engineering or re-qualification, EasyPath-7 FPGAs deliver the lowest total product cost compared to any other FPGA cost-reduction solution.

7 Series FPGA Documentation

For more information about 7 series FPGAs, go to:

http://www.xilinx.com/support/index.html/content/xilinx/en/supportNav/silicon_devices/fpga/num-7-series.html

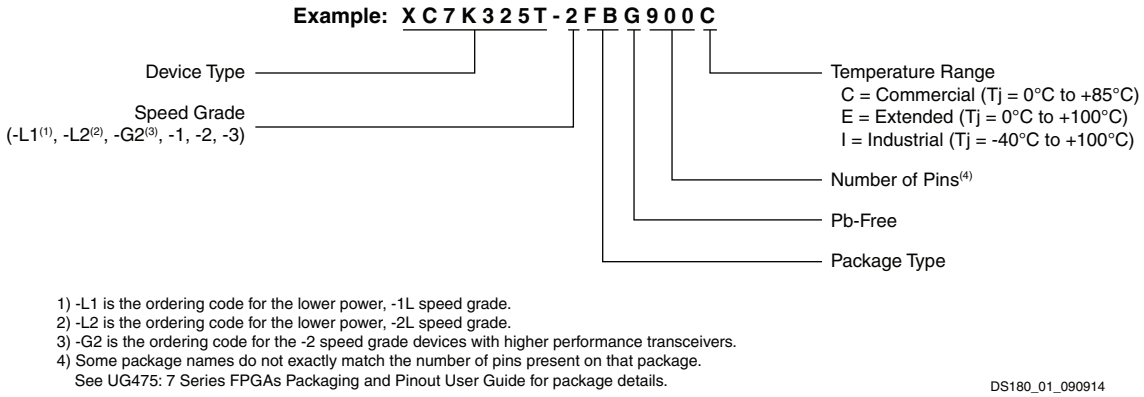
7 Series FPGA Ordering Information

Table 10 shows the speed and temperature grades available in the different device families. Some devices might not be available in every speed and temperature grade.

Table 10: **7 Series Speed Grade and Temperature Ranges**

Device Family	Devices	Speed Grade, Temperature Range, and Operating Voltage		
		Commercial (C) 0°C to +85°C	Extended (E) 0°C to +100°C	Industrial (I) –40°C to +100°C
Artix-7	All		-3E (1.0V)	
		-2C (1.0V)		-2I (1.0V)
			-2LE (1.0V or 0.9V)	
		-1C (1.0V)		-1I (1.0V)
				-1LI (0.95V)
Kintex-7	XC7K70T		-3E (1.0V)	
		-2C (1.0V)		-2I (1.0V)
			-2LE (1.0V or 0.9V)	
		-1C (1.0V)		-1I (1.0V)
	XC7K160T XC7K325T XC7K355T XC7K410T XC7K420T XC7K480T		-3E (1.0V)	
		-2C (1.0V)		-2I (1.0V)
			-2LE (1.0V or 0.9V)	-2LI (0.95V)
		-1C (1.0V)		-1I (1.0V)
Virtex-7 T	XC7V585T		-3E (1.0V)	
		-2C (1.0V)		-2I (1.0V)
			-2LE (1.0V)	
		-1C (1.0V)		-1I (1.0V)
	XC7V2000T	-2C (1.0V)		
			-2GE (1.0V)	
			-2LE (1.0V)	
		-1C (1.0V)		-1I (1.0V)
Virtex-7 XT	XC7VX330T XC7VX415T XC7VX485T XC7VX550T XC7VX690T		-3E (1.0V)	
		-2C (1.0V)		-2I (1.0V)
			-2LE (1.0V)	
		-1C (1.0V)		-1I (1.0V)
	XC7VX980T	-2C (1.0V)		
			-2LE (1.0V)	
		-1C (1.0V)		-1I (1.0V)
	XC7VX1140T	-2C (1.0V)		
			-2GE (1.0V)	
			-2LE (1.0V)	
		-1C (1.0V)		-1I (1.0V)
Virtex-7 HT	All	-2C (1.0V)		
			-2GE (1.0V)	
			-2LE (1.0V)	
		-1C (1.0V)		

The Artix-7, Kintex-7, and Virtex-7 FPGA ordering information, shown in Figure 1, applies to all packages including Pb-Free. Refer to the Package Marking section of UG475, *7 Series FPGAs Packaging and Pinout* for a more detailed explanation of the device markings.



1) -L1 is the ordering code for the lower power, -1L speed grade.
2) -L2 is the ordering code for the lower power, -2L speed grade.
3) -G2 is the ordering code for the -2 speed grade devices with higher performance transceivers.
4) Some package names do not exactly match the number of pins present on that package.
See UG475: 7 Series FPGAs Packaging and Pinout User Guide for package details.

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Figure 1: **Ordering Information**

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/21/10	1.0	Initial Xilinx release.
07/30/10	1.1	Added SHA-256 to authentication information. Updated Table 3, Table 5, Virtex-7 FPGA Device-Package Combinations and Maximum I/Os table (Virtex-7 T devices), and Table 7 with ball pitch information and voltage bank information. Updated DSP and Logic Slice information in Table 6. Updated Low-Power Gigabit Transceivers.
09/24/10	1.2	In General Description, updated 4.7 TMACS DSP to 5.0 TMACS DSP. In Table 1, added Note 1; updated Peak DSP Performance for Kintex-7 and Virtex-7 families. In Table 2, updated CMT information for XC7A175T and XC7A355T. In Table 4, replaced XC7K120T with XC7K160T and replaced XC7K230T with XC7K325T—and updated corresponding information. Also added XC7K355T, XC7K420T, and XC7K480T. In Table 5,replaced XC7K230T with XC7K325T. In Table 6, updated XC7V450T Logic Cell, CLB, block RAM, and PCI information; updated XC7VX415T and XC7VX690T PCI information; updated XC7V1500T, and XC7V2000T block RAM information; and replaced XC7VX605T with XC7VX575T, replaced XC7VX895T with XC7VX850T, and replaced XC7VX910T with XC7VX865T—and updated corresponding information. Updated Digital Signal Processing — DSP Slice with operating speed of 640 MHz. Removed specific transceiver type from Out-of-Band Signaling. In Virtex-7 FPGA Device-Package Combinations and Maximum I/Os table (Virtex-7 T devices), replaced XC7VX605T with XC7VX575T and added table notes 2 and 3. In Table 7, removed the FFG784 package for the XC7VX485T device; replaced XC7VX605T with XC7VX575T; replaced XC7VX895T with XC7VX850T; and replaced XC7VX910T with XC7VX865T.
10/20/10	1.3	In Table 5, replaced XC7K120T with XC7K160T. Updated Digital Signal Processing — DSP Slice.
11/17/10	1.4	Updated maximum I/O bandwidth to 3.1 Tb/s in General Description. Updated Peak Transceiver Speed for Virtex-7 FPGAs in Summary of 7 Series FPGA Features and in Table 1. Updated Peak DSP Performance values in Table 1 and Digital Signal Processing — DSP Slice. In Table 5, updated XC7K70T I/O information. In Table 6, added XC7VH290T, XC7VH580T, and XC7VH870T devices and updated total I/O banks information for the XC7V585T, XC7V855T, XC7V1500T, and XC7VX865T devices. In Table 7, updated XC7VX415T, XC7VX485T, XC7VX690T, XC7VX850T, and XC7VX865T device information. Added Table 9. Updated Low-Power Gigabit Transceivers information, including the addition of the GTZ transceivers.
02/22/11	1.5	Updated Summary of 7 Series FPGA Features and the Low-Power Gigabit Transceivers highlights and section. In Table 1, updated Kintex-7 FPGA, Artix-7 FPGA information. In Table 2, updated XC7A175T. Also, updated XC7A355T. Added three Artix-7 FPGA packages to Table 3: SBG325, SBG484, and FBG485, changed package from FGG784 to FBG784, and updated package information for XC7A175T and XC7A355T devices. In Table 4, updated XC7K160T and added three devices: XC7K355T, XC7K420T, and XC7K480T. In Table 5, updated XC7K70T package information and added three devices: XC7K355T, XC7K420T, and XC7K480T. In Table 6, added note 1 (EasyPath FPGAs) and updated note 7 to include GTZ transceivers. In Virtex-7 FPGA Device-Package Combinations and Maximum I/Os table (Virtex-7 T devices), added two Virtex-7 FPGA packages: FHG1157 and FHG1761, and updated XC7V1500T (no FFG1157) and XC7V2000T (no FFG1761) package information and removed the associated notes. Added CLBs, Slices, and LUTs. Updated Input/Output. Added EasyPath-7 FPGAs.
03/28/11	1.6	Updated General Description, Summary of 7 Series FPGA Features, Table 1, Table 2, Table 3, Table 4, Table 5, Table 6, Table 7 (combined Virtex-7 T and XT devices in one table), and Table 9. Updated the Low-Power Gigabit Transceivers highlights and section. Updated Block RAM, Integrated Interface Blocks for PCI Express Designs, Configuration, Encryption, Readback, and Partial Reconfiguration, XADC (Analog-to-Digital Converter), 7 Series FPGA Ordering Information, and EasyPath-7 FPGAs.
07/06/11	1.7	Updated General Description, Summary of 7 Series FPGA Features, Table 1, Table 2, Table 4, Table 6, Table 7 and Table 9. Added Table 8. Added Stacked Silicon Interconnect (SSI) Technology. Updated Transmitter, Configuration, and XADC (Analog-to-Digital Converter). Updated Figure 1.
09/13/11	1.8	Updated General Description, Table 1, Table 2, Table 3, Table 6, CLBs, Slices, and LUTs, Configuration, and 7 Series FPGA Ordering Information.

Date	Version	Description of Revisions
01/15/12	1.9	Updated General Description, Table 1, Table 2, Table 3, Table 4, Table 5, Table 6, Table 8, Table 9, Block RAM, Digital Signal Processing — DSP Slice, Low-Power Gigabit Transceivers, Integrated Interface Blocks for PCI Express Designs, Configuration, EasyPath-7 FPGAs, and 7 Series FPGA Ordering Information.
03/02/12	1.10	Updated General Description, Table 3, and Table 10.
05/02/12	1.11	Updated Table 5, Table 7, Table 8, Low-Power Gigabit Transceivers, and 7 Series FPGA Ordering Information. Added 7 Series FPGA Documentation.
10/15/12	1.12	Updated overview with Artix-7 SL and SLT devices. Updated Table 1, Table 2, Table 3, Table 6, Table 7, Table 8, Table 9, and Table 10. Added Table 3. Updated Regional Clocks, Block RAM, Integrated Interface Blocks for PCI Express Designs, Configuration, and 7 Series FPGA Ordering Information.
11/30/12	1.13	Updated notes in Table 2 and Table 10. Updated XADC (Analog-to-Digital Converter).
07/29/13	1.14	Removed SL and SLT devices. Updated General Description, Table 2, Table 3, notes in Table 4 and Table 6, Regional Clocks, Input/Output, Low-Power Gigabit Transceivers, Integrated Interface Blocks for PCI Express Designs, Configuration, and 7 Series FPGA Ordering Information. Removed previous Table 3.
02/18/14	1.15	Changed document classification to Product Specification from Preliminary Product Specification. Updated HR I/O information for XC7A35T and XC7A50T in Table 3. Updated XC7VH870T I/O information in Table 6. Updated Table 9.
10/08/14	1.16	Added XC7A15T to Table 2 and Table 3. Removed HCG1931 and HCG1932 from Table 9. Updated Input/Output Delay; Block RAM; Configuration; I/O Clocks; and Updated Table 10 and Figure 1.
12/17/14	1.16.1	Typographical edit.

Notice of Disclaimer

Automotive Applications Disclaimer

Kintex-7 FPGAs Data Sheet: DC and AC Switching Characteristics

DS182 (v2.13) February 23, 2015 **Product Specification**

Introduction

Kintex®-7 FPGAs are available in -3, -2, -1, and -2L speed grades, with -3 having the highest performance. The -2L devices are screened for lower maximum static power and can operate at lower core voltages for lower dynamic power. The -2L industrial (I) temperature devices operate only at V_{CCINT} = 0.95V. The -2L extended (E) temperature devices can operate at either V_{CCINT} = 0.9V or 1.0V. The -2LE devices when operated at V_{CCINT} = 1.0V, and the -2LI devices when operated at V_{CCINT} = 0.95V, have the same speed specifications as the -2 speed grade, except where noted. When the -2LE devices are operated at V_{CCINT} = 0.9V, the speed specifications, static power, and dynamic power are reduced.

Kintex-7 FPGA DC and AC characteristics are specified in commercial, extended, industrial, and military temperature ranges. Except for the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade military device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices are available in each temperature range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

Available device and package combinations can be found in:

- *7 Series FPGAs Overview* (DS180)
- *Defense-Grade 7 Series FPGAs Overview* (DS185)

This Kintex-7 FPGA data sheet, part of an overall set of documentation on the 7 series FPGAs, is available on the Xilinx website at www.xilinx.com/7.

DC Characteristics

Table 1: **Absolute Maximum Ratings** (1)

Symbol	Description	Min	Max	Units
FPGA Logic				
V_{CCINT}	Internal supply voltage	–0.5	1.1	V
V_{CCAUX}	Auxiliary supply voltage	–0.5	2.0	V
V_{CCBRAM}	Supply voltage for the block RAM memories	–0.5	1.1	V
V_{CCO}	Output drivers supply voltage for HR I/O banks	–0.5	3.6	V
	Output drivers supply voltage for HP I/O banks	–0.5	2.0	V
V_{CCAUX_IO}	Auxiliary supply voltage	–0.5	2.06	V
V_{REF}	Input reference voltage	–0.5	2.0	V
V_{IN} (2)(3)(4)	I/O input voltage for HR I/O banks	–0.40	V_{CCO} + 0.55	V
	I/O input voltage for HP I/O banks	–0.55	V_{CCO} + 0.55	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33 (5)	–0.40	2.625	V
V_{CCBATT}	Key memory battery backup supply	–0.5	2.0	V
GTX Transceiver				
$V_{MGTAVCC}$	Analog supply voltage for the GTX transmitter and receiver circuits	–0.5	1.1	V
$V_{MGTAVTT}$	Analog supply voltage for the GTX transmitter and receiver termination circuits	–0.5	1.32	V
$V_{MGTVCCAUX}$	Auxiliary analog Quad PLL (QPLL) voltage supply for the GTX transceivers	–0.5	1.935	V

Table 1: **Absolute Maximum Ratings (1) *(Cont'd)***

Symbol	Description	Min	Max	Units
$V_{MGTREFCLK}$	GTX transceiver reference clock absolute input voltage	–0.5	1.32	V
$V_{MGTAVTTRCAL}$	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	–0.5	1.32	V
V_{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	–0.5	1.26	V
$I_{DCIN-FLOAT}$	DC input current for receiver input pins DC coupled RX termination = floating	–	14	mA
$I_{DCIN-MGTAVTT}$	DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$	–	12	mA
$I_{DCIN-GND}$	DC input current for receiver input pins DC coupled RX termination = GND	–	6.5	mA
$I_{DCOUT-FLOAT}$	DC output current for transmitter pins DC coupled RX termination = floating	–	14	mA
$I_{DCOUT-MGTAVTT}$	DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$	–	12	mA
XADC				
V_{CCADC}	XADC supply relative to GNDADC	–0.5	2.0	V
V_{REFP}	XADC reference input relative to GNDADC	–0.5	2.0	V
Temperature				
T_{STG}	Storage temperature (ambient)	–65	150	°C
T_{SOL}	Maximum soldering temperature for Pb/Sn component bodies (6)	–	+220	°C
	Maximum soldering temperature for Pb-free component bodies (6)	–	+260	°C
T_j	Maximum junction temperature(6)	–	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. The lower absolute voltage specification always applies.
3. For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide* (UG471).
4. The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4 and Table 5.
5. See Table 10 for TMDS_33 specifications.
6. For soldering guidelines and thermal considerations, see the *7 Series FPGA Packaging and Pinout Specification* (UG475).

Table 2: **Recommended Operating Conditions (1)(2)**

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V_{CCINT}(3)	For -3, -2, -2LE (1.0V), -1, -1M devices: internal supply voltage	0.97	1.00	1.03	V
	For -2LE (0.9V) devices: internal supply voltage	0.87	0.90	0.93	V
	For -2LI (0.95V) devices: internal supply voltage	0.93	0.95	0.97	V
V_{CCBRAM}(3)	For -3, -2, -2LE (1.0V), -1, -1M devices: block RAM supply voltage	0.97	1.00	1.03	V
	For -2LE (0.9V) devices: block RAM supply voltage	0.87	0.90	1.03	V
	For -2LI (0.95V) devices: block RAM supply voltage	0.93	0.95	0.97	V
V_{CCAUX}	Auxiliary supply voltage	1.71	1.80	1.89	V
V_{CCO}(4)(5)	Supply voltage for HR I/O banks	1.14	–	3.465	V
	Supply voltage for HP I/O banks	1.14	–	1.89	V
V_{CCAUX_IO}(6)	Auxiliary supply voltage when set to 1.8V	1.71	1.80	1.89	V
	Auxiliary supply voltage when set to 2.0V	1.94	2.00	2.06	V
V_{IN}(7)	I/O input voltage	–0.20	–	V_{CCO} + 0.2	V
	I/O input voltage (when V_{CCO} = 3.3V) for V_{REF} and differential I/O standards except TMDS_33(8)	–0.20	–	2.625	V

Table 2: **Recommended Operating Conditions (1)(2) *(Cont'd)***

Symbol	Description	Min	Typ	Max	Units
I_{IN}(9)	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
V_{CCBATT}(10)	Battery voltage	1.0	–	1.89	V
GTX Transceiver					
$V_{MGTAVCC}$(11)	Analog supply voltage for the GTX transceiver QPLL frequency range ≤ 10.3125 GHz(12)(13)	0.97	1.0	1.08	V
	Analog supply voltage for the GTX transceiver QPLL frequency range > 10.3125 GHz	1.02	1.05	1.08	V
$V_{MGTAVTT}$(11)	Analog supply voltage for the GTX transmitter and receiver termination circuits	1.17	1.2	1.23	V
$V_{MGTVCCAUX}$(11)	Auxiliary analog QPLL voltage supply for the transceivers	1.75	1.80	1.85	V
$V_{MGTAVTTRCAL}$(11)	Analog supply voltage for the resistor calibration circuit of the GTX transceiver column	1.17	1.2	1.23	V
XADC					
V_{CCADC}	XADC supply relative to GNDADC	1.71	1.80	1.89	V
V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
Temperature					
T_j	Junction temperature operating range for commercial (C) temperature devices	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices	–40	–	100	°C
	Junction temperature operating range for military (M) temperature devices	–55	–	125	°C

Notes:

1. All voltages are relative to ground.
2. For the design of the power distribution system, consult the *7 Series FPGAs PCB Design and Pin Planning Guide* (UG483).
3. V_{CCINT} and V_{CCBRAM} should be connected to the same supply.
4. Configuration data is retained even if V_{CCO} drops to 0V.
5. Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V at ±5%.
6. For more information, refer to the V_{CCAUX_IO} section of *7 Series FPGAs SelectIO Resources User Guide* (UG471).
7. The lower absolute voltage specification always applies.
8. See Table 10 for TMDS_33 specifications.
9. A total of 200 mA per bank should not be exceeded.
10. V_{CCBATT} is required only when using bitstream encryption. If battery is not used, connect V_{CCBATT} to either ground or V_{CCAUX}.
11. Each voltage listed requires the filter circuit described in the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476).
12. For data rates ≤ 10.3125 Gb/s, $V_{MGTAVCC}$ should be 1.0V ±3% for lower power consumption.
13. For lower power consumption, $V_{MGTAVCC}$ should be 1.0V ±3% over the entire CPLL frequency range.

Table 3: **DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ(1)	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data might be lost)	0.75	–	–	V
V_{DRI}	Data retention V_{CCAUX} voltage (below which configuration data might be lost)	1.5	–	–	V
I_{REF}	V_{REF} leakage current per pin	–	–	15	µA
I_L	Input or output leakage current per pin (sample-tested)	–	–	15	µA
C_{IN}(2)	Die input capacitance at the pad	–	–	8	pF

Table 3: **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

Symbol	Description	Min	Typ[1]	Max	Units
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V	90	–	330	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 2.5V	68	–	250	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.8V	34	–	220	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.5V	23	–	150	µA
	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 1.2V	12	–	120	µA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.3V	68	–	330	µA
	Pad pull-down (when selected) @ V_{IN} = 1.8V	45	–	180	µA
I_{CCADC}	Analog supply current, analog circuits in powered up state	–	–	25	mA
I_{BATT}[3]	Battery supply current	–	–	150	nA
R_{IN_TERM}[4]	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_40)	28	40	55	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_50)	35	50	65	Ω
	Thevenin equivalent resistance of programmable input termination to V_{CCO}/2 (UNTUNED_SPLIT_60)	44	60	83	Ω
n	Temperature diode ideality factor	–	1.010	–	–
r	Temperature diode series resistance	–	2	–	Ω

Notes:

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a V_{CCO}/2 level.

Table 4: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HR I/O Banks[1][2]**

AC Voltage Overshoot	% of UI at –55°C to 125°C	AC Voltage Undershoot	% of UI at –55°C to 125°C
V_{CCO} + 0.55	100	–0.40	100
		–0.45	61.7
		–0.50	25.8
		–0.55	11.0
V_{CCO} + 0.60	46.6	–0.60	4.77
V_{CCO} + 0.65	21.2	–0.65	2.10
V_{CCO} + 0.70	9.75	–0.70	0.94
V_{CCO} + 0.75	4.55	–0.75	0.43
V_{CCO} + 0.80	2.15	–0.80	0.20
V_{CCO} + 0.85	1.02	–0.85	0.09
V_{CCO} + 0.90	0.49	–0.90	0.04
V_{CCO} + 0.95	0.24	–0.95	0.02

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above V_{CCO} + 0.20V or below GND – 0.20V, must not exceed the values in this table.

Table 5: **V_{IN} Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks(1)(2)**

AC Voltage Overshoot	% of UI at –55°C to 125°C	AC Voltage Undershoot	% of UI at –55°C to 125°C
V_{CCO} + 0.55	100	–0.55	100
V_{CCO} + 0.60	50.0(3)	–0.60	50.0(3)
V_{CCO} + 0.65	50.0(3)	–0.65	50.0(3)
V_{CCO} + 0.70	47.0	–0.70	50.0(3)
V_{CCO} + 0.75	21.2	–0.75	50.0(3)
V_{CCO} + 0.80	9.71	–0.80	50.0(3)
V_{CCO} + 0.85	4.51	–0.85	28.4
V_{CCO} + 0.90	2.12	–0.90	12.7
V_{CCO} + 0.95	1.01	–0.95	5.79

Notes:

1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above V_{CCO} + 0.20V or below GND – 0.20V, must not exceed the values in this table.
3. For UI lasting less than 20 µs.

Table 6: **Typical Quiescent Supply Current**

Symbol	Description	Device	Speed Grade						Units
			1.0V				0.95V	0.9V	
			-3	-2/-2LE	-1	-1M	-2LI	-2LE	
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC7K70T	241	241	241	N/A	N/A	187	mA
		XC7K160T	474	474	474	N/A	271	368	mA
		XC7K325T	810	810	810	N/A	463	629	mA
		XC7K355T	993	993	993	N/A	568	771	mA
		XC7K410T	1080	1080	1080	N/A	618	838	mA
		XC7K420T	1313	1313	1313	N/A	751	1019	mA
		XC7K480T	1313	1313	1313	N/A	751	1019	mA
		XQ7K325T	N/A	810	810	810	N/A	629	mA
		XQ7K410T	N/A	1080	1080	1080	N/A	838	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC7K70T	1	1	1	N/A	N/A	1	mA
		XC7K160T	1	1	1	N/A	1	1	mA
		XC7K325T	1	1	1	N/A	1	1	mA
		XC7K355T	1	1	1	N/A	1	1	mA
		XC7K410T	1	1	1	N/A	1	1	mA
		XC7K420T	1	1	1	N/A	1	1	mA
		XC7K480T	1	1	1	N/A	1	1	mA
		XQ7K325T	N/A	1	1	1	N/A	1	mA
		XQ7K410T	N/A	1	1	1	N/A	1	mA

Table 6: **Typical Quiescent Supply Current *(Cont'd)***

Symbol	Description	Device	Speed Grade						Units
			1.0V				0.95V	0.9V	
			-3	-2/-2LE	-1	-1M	-2LI	-2LE	
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC7K70T	21	21	21	N/A	N/A	21	mA
		XC7K160T	40	40	40	N/A	36	40	mA
		XC7K325T	68	68	68	N/A	61	68	mA
		XC7K355T	75	75	75	N/A	67	75	mA
		XC7K410T	85	85	85	N/A	76	85	mA
		XC7K420T	99	99	99	N/A	89	99	mA
		XC7K480T	99	99	99	N/A	89	99	mA
		XQ7K325T	N/A	68	68	68	N/A	68	mA
		XQ7K410T	N/A	85	85	85	N/A	85	mA
I_{CCAUX_IOQ}	Quiescent V_{CCAUX_IO} supply current	XC7K70T	N/A	N/A	N/A	N/A	N/A	N/A	mA
		XC7K160T	2	2	2	N/A	1	2	mA
		XC7K325T	2	2	2	N/A	1	2	mA
		XC7K355T	N/A	N/A	N/A	N/A	N/A	N/A	mA
		XC7K410T	2	2	2	N/A	1	2	mA
		XC7K420T	N/A	N/A	N/A	N/A	N/A	N/A	mA
		XC7K480T	N/A	N/A	N/A	N/A	N/A	N/A	mA
		XQ7K325T	N/A	2	2	2	N/A	2	mA
		XQ7K410T	N/A	2	2	2	N/A	2	mA
$I_{CCBRAMQ}$	Quiescent V_{CCBRAM} supply current	XC7K70T	6	6	6	N/A	N/A	6	mA
		XC7K160T	14	14	14	N/A	8	14	mA
		XC7K325T	19	19	19	N/A	10	19	mA
		XC7K355T	31	31	31	N/A	17	31	mA
		XC7K410T	34	34	34	N/A	19	34	mA
		XC7K420T	41	41	41	N/A	23	41	mA
		XC7K480T	41	41	41	N/A	23	41	mA
		XQ7K325T	N/A	19	19	19	N/A	19	mA
		XQ7K410T	N/A	34	34	34	N/A	34	mA

Notes:

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T_j) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate static power consumption for conditions other than those specified.

Power-On/Off Power Supply Sequencing

The recommended power-on sequence is V_{CCINT}, V_{CCBRAM}, V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM} have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If V_{CCAUX}, V_{CCAUX_IO}, and V_{CCO} have the same recommended voltage levels then they can be powered by the same supply and ramped simultaneously.

For V_{CCO} voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between V_{CCO} and V_{CCAUX} must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTX transceivers is V_{CCINT}, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, V_{CCINT}, $V_{MGTAVTT}$. There is no recommended sequencing for $V_{MGTVCCAUX}$. Both $V_{MGTAVCC}$ and V_{CCINT} can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before V_{CCINT} and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during V_{CCINT} ramp up. The duration of the current draw can be up to 0.3 x T_{VCCINT} (ramp time from GND to 90% of V_{CCINT}). The reverse is true for power-down.

There is no recommended sequence for supplies not shown.

Table 7 shows the minimum current, in addition to I_{CCQ}, that are required by Kintex-7 devices for proper power-on and configuration. If the current minimums shown in Table 6 and Table 7 are met, the device powers on after all five supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after V_{CCINT} is applied.

Once initialized and configured, use the Xilinx Power Estimator (XPE) spreadsheet tool (download at www.xilinx.com/power) to estimate current drain on these supplies.

Table 7: **Power-On Current for Kintex-7 Devices**

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	I_{CCOMIN}	I_{CCAUX_IOMIN}	$I_{CCBRAMMIN}$	Units
XC7K70T	I_{CCINTQ} + 450	I_{CCAUXQ} + 40	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 40	mA
XC7K160T	I_{CCINTQ} + 550	I_{CCAUXQ} + 50	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 40	mA
XC7K325T	I_{CCINTQ} + 600	I_{CCAUXQ} + 80	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 40	mA
XC7K355T	I_{CCINTQ} + 1450	I_{CCAUXQ} + 109	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 81	mA
XC7K410T	I_{CCINTQ} + 1500	I_{CCAUXQ} + 125	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 90	mA
XC7K420T	I_{CCINTQ} + 2200	I_{CCAUXQ} + 180	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 108	mA
XC7K480T	I_{CCINTQ} + 2200	I_{CCAUXQ} + 180	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 108	mA
XQ7K325T	I_{CCINTQ} + 600	I_{CCAUXQ} + 80	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 40	mA
XQ7K410T	I_{CCINTQ} + 1500	I_{CCAUXQ} + 125	I_{CCOQ} + 40 mA per bank	$I_{CCOAUXIOQ}$ + 40 mA per bank	$I_{CCBRAMQ}$ + 90	mA

Table 8: **Power Supply Ramp Time**

Symbol	Description	Conditions	Min	Max	Units
T_{VCCINT}	Ramp time from GND to 90% of V_{CCINT}		0.2	50	ms
T_{VCCO}	Ramp time from GND to 90% of V_{CCO}		0.2	50	ms
T_{VCCAUX}	Ramp time from GND to 90% of V_{CCAUX}		0.2	50	ms
T_{VCCAUX_IO}	Ramp time from GND to 90% of V_{CCAUX_IO}		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of V_{CCBRAM}		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625$V	$T_J = 125°C$[1]	–	300	ms
		$T_J = 100°C$[1]	–	500	
		$T_J = 85°C$[1]	–	800	
$T_{MGTAVCC}$	Ramp time from GND to 90% of $V_{MGTAVCC}$		0.2	50	ms
$T_{MGTAVTT}$	Ramp time from GND to 90% of $V_{MGTAVTT}$		0.2	50	ms

Table 8: **Power Supply Ramp Time *(Cont'd)***

Symbol	Description	Conditions	Min	Max	Units
$T_{MGTVCCAUX}$	Ramp time from GND to 90% of $V_{MGTVCCAUX}$		0.2	50	ms

Notes:

1. Based on 240,000 power cycles with nominal V_{CCO} of 3.3V or 36,500 power cycles with a worst case V_{CCO} of 3.465V.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 9: **SelectIO DC Input and Output Levels** (1)(2)

I/O Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8	–8
HSTL_I_12	–0.300	V_{REF} – 0.080	V_{REF} + 0.080	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	6.3	–6.3
HSTL_I_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	8	–8
HSTL_II	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16	–16
HSTL_II_18	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	16	–16
HSUL_12	–0.300	V_{REF} – 0.130	V_{REF} + 0.130	V_{CCO} + 0.300	20% V_{CCO}	80% V_{CCO}	0.1	–0.1
LVCMOS12	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 3	Note 3
LVCMOS15, LVDCI_15	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	25% V_{CCO}	75% V_{CCO}	Note 4	Note 4
LVCMOS18, LVDCI_18	–0.300	35% V_{CCO}	65% V_{CCO}	V_{CCO} + 0.300	0.450	V_{CCO} – 0.450	Note 5	Note 5
LVCMOS25	–0.300	0.700	1.700	V_{CCO} + 0.300	0.400	V_{CCO} – 0.400	Note 6	Note 6
LVCMOS33	–0.300	0.800	2.000	3.450	0.400	V_{CCO} – 0.400	Note 6	Note 6
LVTTL	–0.300	0.800	2.000	3.450	0.400	2.400	Note 7	Note 7
MOBILE_DDR	–0.300	20% V_{CCO}	80% V_{CCO}	V_{CCO} + 0.300	10% V_{CCO}	90% V_{CCO}	0.1	–0.1
PCI33_3	–0.400	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.500	10% V_{CCO}	90% V_{CCO}	1.5	–0.5
SSTL12	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	14.25	–14.25
SSTL135	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	13.0	–13.0
SSTL135_R	–0.300	V_{REF} – 0.090	V_{REF} + 0.090	V_{CCO} + 0.300	V_{CCO}/2 – 0.150	V_{CCO}/2 + 0.150	8.9	–8.9
SSTL15	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	13.0	–13.0
SSTL15_R	–0.300	V_{REF} – 0.100	V_{REF} + 0.100	V_{CCO} + 0.300	V_{CCO}/2 – 0.175	V_{CCO}/2 + 0.175	8.9	–8.9
SSTL18_I	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.470	V_{CCO}/2 + 0.470	8	–8
SSTL18_II	–0.300	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCO} + 0.300	V_{CCO}/2 – 0.600	V_{CCO}/2 + 0.600	13.4	–13.4

Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in HR I/O banks.
3. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks and 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, 12, or 16 mA in HP I/O banks and 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. Supported drive strengths of 4, 8, 12, or 16 mA
7. Supported drive strengths of 4, 8, 12, 16, or 24 mA
8. For detailed interface specific DC voltage levels, see the *7 Series FPGAs SelectIO Resources User Guide* (UG471).

Table 10: **Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]			V_{OCM}[3]			V_{OD}[4]		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	–	–	–	1.250	–	Note 5		
MINI_LVDS_25	0.300	1.200	V_{CCAUX}	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	V_{CCAUX}	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	V_{CCO}–0.405	V_{CCO}–0.300	V_{CCO}–0.190	0.400	0.600	0.800

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OCM} is the output common mode voltage.
4. V_{OD} is the output differential voltage (Q – $\overline{Q}$).
5. V_{OD} for BLVDS will vary significantly depending on topology and loading.
6. LVDS_25 is specified in Table 12.
7. LVDS is specified in Table 13.

Table 11: **Complementary Differential SelectIO DC Input and Output Levels**

I/O Standard	V_{ICM}[1]			V_{ID}[2]		V_{OL}[3]	V_{OH}[4]	I_{OL}	I_{OH}
	V, Min	V, Typ	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	V_{CCO}–0.400	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% V_{CCO}	80% V_{CCO}	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	–	10% V_{CCO}	90% V_{CCO}	0.100	–0.100
DIFF_SSTL12	0.300	0.600	0.850	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	14.25	–14.25
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	(V_{CCO}/2) – 0.150	(V_{CCO}/2) + 0.150	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	(V_{CCO}/2) – 0.175	(V_{CCO}/2) + 0.175	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.470	(V_{CCO}/2) + 0.470	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	(V_{CCO}/2) – 0.600	(V_{CCO}/2) + 0.600	13.4	–13.4

Notes:

1. V_{ICM} is the input common mode voltage.
2. V_{ID} is the input differential voltage (Q – $\overline{Q}$).
3. V_{OL} is the single-ended low-output voltage.
4. V_{OH} is the single-ended high-output voltage.

LVDS DC Specifications (LVDS_25)

The LVDS_25 standard is available in the HR I/O banks. See the *7 Series FPGAs SelectIO Resources User Guide* (UG471) for more information.

Table 12: **LVDS_25 DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		2.375	2.500	2.625	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.700	–	–	V
V_{ODIFF}	Differential Output Voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
V_{ICM}	Input Common-Mode Voltage		0.300	1.200	1.500	V

Notes:

1. Differential inputs for LVDS_25 can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Refer to the *7 Series FPGAs SelectIO Resources User Guide* (UG471) for more information.

LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See the *7 Series FPGAs SelectIO Resources User Guide* (UG471) for more information.

Table 13: **LVDS DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply Voltage		1.710	1.800	1.890	V
V_{OH}	Output High Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	–	–	1.675	V
V_{OL}	Output Low Voltage for Q and $\overline{Q}$	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.825	–	–	V
V_{ODIFF}	Differential Output Voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100 Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V_{OCM}	Output Common-Mode Voltage	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V_{IDIFF}	Differential Input Voltage: (Q – $\overline{Q}$), Q = High ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25V	100	350	600	mV
V_{ICM}	Input Common-Mode Voltage	Differential input voltage = ±350 mV	0.300	1.200	1.425	V

Notes:

1. Differential inputs for LVDS can be placed in banks with V_{CCO} levels that are different from the required level for outputs. Refer to the *7 Series FPGAs SelectIO Resources User Guide* (UG471) for more information.

AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite 2014.4 and ISE® software 14.7 as outlined in Table 14.

Table 14: **Kintex-7 FPGA Speed Specification Version By Device**

Version In:		Typical V_{CCINT}	Device
ISE 14.7	Vivado 2014.4	(Table 2)	
1.10	1.12	1.0V	XC7K70T, XC7K160T, XC7K325T, XC7K355T, XC7K410T, XC7K420T, XC7K480T
N/A	1.12	0.95V	XC7K160T, XC7K325T, XC7K355T, XC7K410T, XC7K420T, XC7K480T
1.09	1.09	0.9V	XC7K70T, XC7K160T, XC7K325T, XC7K355T, XC7K410T, XC7K420T, XC7K480T
1.05	1.08	1.0V	XQ7K325T, XQ7K410T
1.05	1.07	0.9V	XQ7K325T, XQ7K410T

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Kintex-7 FPGAs.

Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 15 correlates the current status of each Kintex-7 device on a per speed grade basis.

Table 15: **Kintex-7 Device Speed Grade Designations**

Device	Speed Grade Designations		
	Advance	Preliminary	Production
XC7K70T			-3, -2, -2LE(1.0V), -1, and -2LE (0.9V)
XC7K160T			-3, -2, -2LE(1.0V), -2LI (0.95V), -1, and -2LE (0.9V)
XC7K325T			-3, -2, -2LE(1.0V), -2LI (0.95V), -1, and -2LE (0.9V)
XC7K355T			-3, -2, -2LE(1.0V), -2LI (0.95V), -1, and -2LE (0.9V)
XC7K410T			-3, -2, -2LE(1.0V), -2LI (0.95V), -1, and -2LE (0.9V)
XC7K420T			-3, -2, -2LE(1.0V), -2LI (0.95V), -1, and -2LE (0.9V)
XC7K480T			-3, -2, -2LE(1.0V), -2LI (0.95V), -1, and -2LE (0.9V)
XQ7K325T			-2I, -2LE(1.0V), -1I, -2LE(0.9V), and -1M
XQ7K410T			-2I, -2LE(1.0V), -1I, -2LE(0.9V), and -1M

Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 16 lists the production released Kintex-7 device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 16: **Kintex-7 Device Production Software and Speed Specification Release**

Device	Speed Grade Designations					
	1.0V				0.95V	0.9V
	-3	-2/-2LE	-1	-1M	-2LI	-2LE
XC7K70T	Vivado tools 2012.4 v1.08 or ISE tools 14.2 v1.06			N/A	N/A	Vivado tools 2012.4 v1.07 or ISE tools 14.3 v1.06
XC7K160T	Vivado tools 2012.4 v1.08 or ISE tools 14.2 v1.06			N/A	Vivado tools 2014.4 v1.12	Vivado tools 2012.4 v1.07 or ISE tools 14.3 v1.06
XC7K325T	Vivado tools 2012.4 v1.08 or ISE tools 14.2 v1.06			N/A	Vivado tools 2014.4 v1.12	Vivado tools 2012.4 v1.07 or ISE tools 14.3 v1.06
XC7K355T	Vivado tools 2012.4 v1.08 or ISE tools 14.2 v1.06			N/A	Vivado tools 2014.4 v1.12	Vivado tools 2012.4 v1.07 or ISE tools 14.3 v1.06
XC7K410T	Vivado tools 2012.4 v1.08 or ISE tools 14.2 v1.06			N/A	Vivado tools 2014.4 v1.12	Vivado tools 2012.4 v1.07 or ISE tools 14.3 v1.06
XC7K420T	Vivado tools 2012.4 v1.08 or ISE tools 14.2 v1.06			N/A	Vivado tools 2014.4 v1.12	Vivado tools 2012.4 v1.07 or ISE tools 14.3 v1.06
XC7K480T	Vivado tools 2012.4 v1.08 or ISE tools 14.2 v1.06			N/A	Vivado tools 2014.4 v1.12	Vivado tools 2012.4 v1.07 or ISE tools 14.3 v1.06
XQ7K325T	N/A	Vivado tools 2013.1 v1.04 or ISE tools 14.5 v1.04			N/A	Vivado tools 2013.1 v1.04 or ISE tools 14.5 v1.04
XQ7K410T	N/A	Vivado tools 2013.1 v1.04 or ISE tools 14.5 v1.04			N/A	Vivado tools 2013.1 v1.04 or ISE tools 14.5 v1.04

Selecting the Correct Speed Grade and Voltage in the Vivado Tools

It is important to select the correct device speed grade and voltage in the Vivado tools for the device that you are selecting.

To select the 1.0V speed specifications in the Vivado tools, select the **Kintex-7** or **Defense Grade Kintex-7Q** sub-family, and then select the part name that is the device name followed by the package name followed by the speed grade. For example, select the **xc7k325tffg900-3** part name for the XC7K325T device in the FFG900 package and -3 (1.0V) speed grade or select the **xc7k325tffg900-2L** part name for the XC7K325T device in the FFG900 package and -2LE (1.0V) speed grade.

To select the -2LI (0.95V) speed specifications in the Vivado tools, select the **Kintex-7** sub-family and then select the part name that is the device name followed by an *i* followed by the package name followed by the speed grade. For example, select the **xc7k325tiffg900-2L** part name for the XC7K325T device in the FFG900 package and -2LI (0.95V) speed grade. The -2LI (0.95V) speed specifications are not supported in the ISE tools.

To select the -2LE (0.9V) speed specifications in the Vivado tools, select the **Kintex-7 Low Voltage** or **Defense Grade Kintex-7Q Low Voltage** sub-family, and then select the part name that is the device name followed by an *l* followed by the package name followed by the speed grade. For example, select the **xc7k325tlffg900-2L** part name for the XC7K325T device in the FFG900 package and -2LE (0.9V) speed grade.

A similar part naming convention applies to the speed specifications selection in the ISE tools for supported devices. See Table 16 for the subset of 7 series FPGAs supported in the ISE tools.

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Kintex-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 11. In each table, the I/O bank type is either High Performance (HP) or High Range (HR).

Table 17: **Networking Applications Interface Performances**

Description	I/O Bank Type	Speed Grade					Units
		1.0V			0.95V	0.9V	
		-3	-2/-2LE	-1	-2LI	-2LE	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	HR	710	710	625	710	625	Mb/s
	HP	710	710	625	710	625	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	HR	1250	1250	950	1250	950	Mb/s
	HP	1600	1400	1250	1400	1250	Mb/s
SDR LVDS receiver (SFI-4.1)(1)	HR	710	710	625	710	625	Mb/s
	HP	710	710	625	710	625	Mb/s
DDR LVDS receiver (SPI-4.2)(1)	HR	1250	1250	950	1250	950	Mb/s
	HP	1600	1400	1250	1400	1250	Mb/s

Notes:

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 18: **Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator (FFG and RF Packages)(1)(2)**

Memory Standard	I/O Bank Type	V_{CCAUX_IO}	Speed Grade						Units
			1.0V				0.95V	0.9V	
			-3	-2/-2LE	-1	-1M	-2LI	-2LE	
4:1 Memory Controllers									
DDR3	HP	2.0V	1866(3)	1866(3)	1600	1066	1600	1333	Mb/s
	HP	1.8V	1600	1333	1066	800	1333	1066	Mb/s
	HR	N/A	1066	1066	800	800	1066	800	Mb/s
DDR3L	HP	2.0V	1600	1600	1333	1066	1600	1066	Mb/s
	HP	1.8V	1333	1066	800	800	1066	800	Mb/s
	HR	N/A	800	800	667	N/A	800	667	Mb/s
DDR2	HP	2.0V	800	800	800	667	800	800	Mb/s
	HP	1.8V	800	800	800	667	800	800	Mb/s
	HR	N/A	800	800	800	533	800	800	Mb/s
RLDRAM III	HP	2.0V	800	667	667	550	667	533	MHz
	HP	1.8V	550	500	450	400	500	450	MHz
	HR	N/A	N/A						
2:1 Memory Controllers									
DDR3	HP	2.0V	1066	1066	800	667	1066	800	Mb/s
	HP	1.8V	1066	1066	800	667	1066	800	Mb/s
	HR	N/A	1066	1066	800	667	1066	800	Mb/s
DDR3L	HP	2.0V	1066	1066	800	667	1066	800	Mb/s
	HP	1.8V	1066	1066	800	667	1066	800	Mb/s
	HR	N/A	800	800	667	N/A	800	667	Mb/s
DDR2	HP	2.0V	800	800	800	667	800	800	Mb/s
	HP	1.8V				667			
	HR	N/A				533			
QDR II+(4)	HP	2.0V	550	500	450	300	500	450	MHz
	HP	1.8V							
	HR	N/A	500	450	400	300	450	400	MHz
RLDRAM II	HP	2.0V	533	500	450	400	500	450	MHz
	HP	1.8V							
	HR	N/A							
LPDDR2	HP	2.0V	667	667	667	533	667	667	Mb/s
	HP	1.8V	667	667	667	533	667	667	Mb/s
	HR	N/A	667	667	667	533	667	667	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see the *7 Series FPGAs Memory Interface Solutions User Guide* (UG586).
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).
3. For designs that require > 1800 Mb/s, contact Xilinx Technical Support and open a WebCase.
4. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

Table 19: **Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator (FBG Packages)(1)(2)**

Memory Standard	I/O Bank Type	V_{CCAUX_IO}(3)	Speed Grade						Units
			1.0V				0.95V	0.9V	
			-3	-2/-2LE	-1	-1M	-2LI	-2LE	
4:1 Memory Controllers									
DDR3	HP	N/A	1333	1066	800	800	1066	800	Mb/s
	HR	N/A	1066	800	800	800	800	800	Mb/s
DDR3L	HP	N/A	1066	800	667	667	800	667	Mb/s
	HR	N/A	800	800	667	N/A	800	667	Mb/s
DDR2	HP	N/A	800	800	800	667	800	800	Mb/s
	HR	N/A	800	667	667	533	667	667	Mb/s
RLDRAM III	HP	N/A	550	500	450	350	500	450	MHz
	HR	N/A	N/A						
2:1 Memory Controllers									
DDR3	HP	N/A	1066	1066	800	667	1066	800	Mb/s
	HR	N/A	1066	800	800	667	800	800	Mb/s
DDR3L	HP	N/A	1066	800	667	667	800	667	Mb/s
	HR	N/A	800	800	667	N/A	800	667	Mb/s
DDR2	HP	N/A	800	800	800	667	800	800	Mb/s
	HR	N/A	800	667	667	533	667	667	Mb/s
QDR II+(4)	HP	N/A	550	500	450	300	500	450	MHz
	HR	N/A	450	400	350	300	400	350	MHz
RLDRAM II	HP	N/A	533	500	450	400	500	450	MHz
	HR	N/A							
LPDDR2	HP	N/A	667	667	667	400	667	667	Mb/s
	HR	N/A	667	667	533	400	667	533	Mb/s

Notes:

1. V_{REF} tracking is required. For more information, see the *7 Series FPGAs Memory Interface Solutions User Guide* (UG586).
2. When using the internal V_{REF}, the maximum data rate is 800 Mb/s (400 MHz).
3. FBG packages do not have separate V_{CCAUX_IO} supply pins to adjust the pre-driver voltage of the HP I/O banks.
4. The maximum QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations. Burst length 2 (BL = 2) implementations are limited to 333 MHz for all speed grades and I/O bank types.

IOB Pad Input/Output/3-State

Table 20 (high-range IOB (HR)) and Table 21 (high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than T_{IOTP} when the DCITERMDISABLE pin is used. In HR I/O banks, the IN_TERM termination turn-on time is always faster than T_{IOTP} when the INTERMDISABLE pin is used.

Table 20: **IOB High Range (HR) Switching Characteristics**

I/O Standard	T_{IOPI}						T_{IOOP}						T_{IOTP}						Units
	Speed Grade						Speed Grade						Speed Grade						
	1.0V				0.95V	0.9V	1.0V				0.95V	0.9V	1.0V				0.95V	0.9V	
	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	
LVTTL_S4	1.31	1.42	1.64	1.64	1.42	1.51	3.77	3.90	4.00	4.00	3.90	4.13	3.52	3.67	3.86	3.86	3.67	3.85	ns
LVTTL_S8	1.31	1.42	1.64	1.64	1.42	1.51	3.50	3.64	3.73	3.73	3.64	3.86	3.26	3.40	3.60	3.60	3.40	3.58	ns
LVTTL_S12	1.31	1.42	1.64	1.64	1.42	1.51	3.49	3.62	3.72	3.72	3.62	3.84	3.24	3.39	3.58	3.58	3.39	3.56	ns
LVTTL_S16	1.31	1.42	1.64	1.64	1.42	1.51	3.03	3.17	3.26	3.26	3.17	3.39	2.79	2.93	3.13	3.13	2.93	3.11	ns
LVTTL_S24	1.31	1.42	1.64	1.64	1.42	1.51	3.25	3.39	3.48	3.48	3.39	3.61	3.01	3.15	3.35	3.35	3.15	3.33	ns
LVTTL_F4	1.31	1.42	1.64	1.64	1.42	1.51	3.22	3.36	3.45	3.45	3.36	3.58	2.98	3.12	3.32	3.32	3.12	3.30	ns
LVTTL_F8	1.31	1.42	1.64	1.64	1.42	1.51	2.71	2.84	2.93	2.93	2.84	3.06	2.46	2.61	2.80	2.80	2.61	2.78	ns
LVTTL_F12	1.31	1.42	1.64	1.64	1.42	1.51	2.69	2.82	2.92	2.92	2.82	3.05	2.44	2.59	2.79	2.79	2.59	2.77	ns
LVTTL_F16	1.31	1.42	1.64	1.64	1.42	1.51	2.57	2.85	3.15	3.15	2.85	2.88	2.33	2.61	3.02	3.02	2.61	2.60	ns
LVTTL_F24	1.31	1.42	1.64	1.64	1.42	1.51	2.41	2.64	2.89	3.04	2.64	2.94	2.16	2.41	2.76	2.91	2.41	2.66	ns
LVDS_25	0.64	0.68	0.80	0.87	0.68	0.83	1.36	1.47	1.55	1.55	1.47	1.58	1.11	1.24	1.41	1.41	1.24	1.30	ns
MINI_LVDS_25	0.68	0.70	0.79	0.87	0.70	0.83	1.36	1.47	1.55	1.55	1.47	1.59	1.11	1.24	1.41	1.41	1.24	1.31	ns
BLVDS_25	0.65	0.69	0.80	0.85	0.69	0.83	1.83	2.02	2.20	2.57	2.02	2.16	1.59	1.79	2.07	2.44	1.79	1.88	ns
RSDS_25 (point to point)	0.63	0.68	0.79	0.87	0.68	0.83	1.36	1.48	1.55	1.55	1.48	1.59	1.11	1.24	1.41	1.41	1.24	1.31	ns
PPDS_25	0.65	0.69	0.80	0.87	0.69	0.83	1.36	1.49	1.58	1.58	1.49	1.59	1.11	1.25	1.45	1.45	1.25	1.31	ns
TMDS_33	0.72	0.76	0.86	0.90	0.76	0.83	1.43	1.54	1.60	1.60	1.54	1.70	1.18	1.31	1.47	1.47	1.31	1.42	ns
PCI33_3	1.28	1.41	1.65	1.65	1.41	1.50	2.71	3.08	3.52	3.52	3.08	3.42	2.46	2.84	3.39	3.39	2.84	3.14	ns
HSUL_12_S	0.63	0.64	0.71	0.85	0.64	0.79	1.77	1.90	2.00	2.00	1.90	2.13	1.52	1.67	1.86	1.86	1.67	1.85	ns
HSUL_12_F	0.63	0.64	0.71	0.85	0.64	0.79	1.26	1.40	1.50	1.50	1.40	1.61	1.01	1.16	1.37	1.37	1.16	1.33	ns
DIFF_HSUL_ 12_S	0.58	0.61	0.70	0.84	0.61	0.81	1.55	1.68	1.78	1.78	1.68	1.92	1.30	1.45	1.65	1.65	1.45	1.64	ns
DIFF_HSUL_ 12_F	0.58	0.61	0.70	0.84	0.61	0.81	1.16	1.28	1.35	1.35	1.28	1.50	0.92	1.04	1.21	1.21	1.04	1.22	ns
MOBILE_DDR_S	0.64	0.66	0.74	0.74	0.66	0.89	2.58	2.91	3.31	3.31	2.91	1.95	2.33	2.68	3.17	3.17	2.68	1.67	ns
MOBILE_DDR_F	0.64	0.66	0.74	0.74	0.66	0.89	1.91	2.13	2.36	2.36	2.13	1.69	1.66	1.89	2.23	2.23	1.89	1.41	ns
DIFF_MOBILE_ DDR_S	0.63	0.66	0.75	0.75	0.66	0.79	2.51	2.84	3.24	3.24	2.84	1.95	2.26	2.61	3.10	3.10	2.61	1.67	ns
DIFF_MOBILE_ DDR_F	0.63	0.66	0.75	0.75	0.66	0.79	1.89	2.11	2.34	2.34	2.11	1.72	1.64	1.88	2.21	2.21	1.88	1.44	ns

Table 20: **IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}						T_{IOOP}						T_{IOTP}						Units
	Speed Grade						Speed Grade						Speed Grade						
	1.0V				0.95V	0.9V	1.0V				0.95V	0.9V	1.0V				0.95V	0.9V	
	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	
HSTL_I_S	0.61	0.64	0.73	0.84	0.64	0.79	1.55	1.69	1.80	1.80	1.69	1.91	1.30	1.46	1.67	1.67	1.46	1.63	ns
HSTL_II_S	0.61	0.64	0.73	0.84	0.64	0.78	1.21	1.34	1.43	1.61	1.34	1.70	0.96	1.11	1.30	1.47	1.11	1.42	ns
HSTL_I_18_S	0.64	0.67	0.76	0.85	0.67	0.79	1.28	1.39	1.45	1.45	1.39	1.58	1.04	1.16	1.31	1.32	1.16	1.30	ns
HSTL_II_18_S	0.64	0.67	0.76	0.85	0.67	0.79	1.18	1.31	1.40	1.57	1.31	1.69	0.93	1.08	1.27	1.44	1.08	1.41	ns
DIFF_HSTL_I_S	0.63	0.67	0.77	0.84	0.67	0.78	1.42	1.54	1.61	1.78	1.54	1.84	1.17	1.31	1.48	1.65	1.31	1.56	ns
DIFF_HSTL_II_S	0.63	0.67	0.77	0.84	0.67	0.79	1.15	1.24	1.27	1.61	1.24	1.78	0.91	1.01	1.14	1.47	1.01	1.50	ns
DIFF_HSTL_I_ 18_S	0.65	0.69	0.78	0.84	0.69	0.79	1.27	1.38	1.43	1.45	1.38	1.67	1.03	1.14	1.30	1.32	1.14	1.39	ns
DIFF_HSTL_II_ 18_S	0.65	0.69	0.78	0.85	0.69	0.81	1.14	1.23	1.26	1.57	1.23	1.72	0.90	1.00	1.13	1.44	1.00	1.44	ns
HSTL_I_F	0.61	0.64	0.73	0.84	0.64	0.79	1.10	1.19	1.23	1.31	1.19	1.41	0.85	0.96	1.10	1.18	0.96	1.13	ns
HSTL_II_F	0.61	0.64	0.73	0.84	0.64	0.78	1.05	1.18	1.28	1.31	1.18	1.42	0.80	0.95	1.15	1.18	0.95	1.14	ns
HSTL_I_18_F	0.64	0.67	0.76	0.85	0.67	0.79	1.05	1.18	1.28	1.36	1.18	1.44	0.80	0.95	1.15	1.22	0.95	1.16	ns
HSTL_II_18_F	0.64	0.67	0.76	0.85	0.67	0.79	1.03	1.14	1.23	1.32	1.14	1.42	0.78	0.90	1.10	1.19	0.90	1.14	ns
DIFF_HSTL_I_F	0.63	0.67	0.77	0.84	0.67	0.78	1.09	1.18	1.22	1.31	1.18	1.48	0.84	0.95	1.09	1.18	0.95	1.20	ns
DIFF_HSTL_II_F	0.63	0.67	0.77	0.84	0.67	0.79	1.02	1.11	1.14	1.31	1.11	1.48	0.77	0.88	1.01	1.18	0.88	1.20	ns
DIFF_HSTL_I_ 18_F	0.65	0.69	0.78	0.84	0.69	0.79	1.08	1.17	1.21	1.36	1.17	1.48	0.83	0.94	1.07	1.22	0.94	1.20	ns
DIFF_HSTL_II_ 18_F	0.65	0.69	0.78	0.85	0.69	0.81	1.01	1.10	1.13	1.32	1.10	1.48	0.76	0.87	1.00	1.19	0.87	1.20	ns
LVCMOS33_S4	1.31	1.40	1.60	1.60	1.40	1.54	3.77	3.90	4.00	4.00	3.90	4.13	3.52	3.67	3.86	3.86	3.67	3.85	ns
LVCMOS33_S8	1.31	1.40	1.60	1.60	1.40	1.54	3.49	3.62	3.72	3.72	3.62	3.84	3.24	3.39	3.58	3.58	3.39	3.56	ns
LVCMOS33_S12	1.31	1.40	1.60	1.60	1.40	1.54	3.05	3.18	3.28	3.28	3.18	3.41	2.80	2.95	3.15	3.15	2.95	3.13	ns
LVCMOS33_S16	1.31	1.40	1.60	1.60	1.40	1.54	3.06	3.43	3.88	3.88	3.43	3.72	2.81	3.20	3.75	3.75	3.20	3.44	ns
LVCMOS33_F4	1.31	1.40	1.60	1.60	1.40	1.54	3.22	3.36	3.45	3.45	3.36	3.58	2.98	3.12	3.32	3.32	3.12	3.30	ns
LVCMOS33_F8	1.31	1.40	1.60	1.60	1.40	1.54	2.71	2.84	2.93	2.93	2.84	3.06	2.46	2.61	2.80	2.80	2.61	2.78	ns
LVCMOS33_F12	1.31	1.40	1.60	1.60	1.40	1.54	2.57	2.85	3.15	3.15	2.85	2.88	2.33	2.61	3.02	3.02	2.61	2.60	ns
LVCMOS33_F16	1.31	1.40	1.60	1.60	1.40	1.54	2.44	2.69	2.96	2.96	2.69	2.88	2.19	2.45	2.82	2.82	2.45	2.60	ns
LVCMOS25_S4	1.08	1.16	1.32	1.35	1.16	1.36	3.08	3.22	3.31	3.31	3.22	3.44	2.84	2.98	3.18	3.18	2.98	3.16	ns
LVCMOS25_S8	1.08	1.16	1.32	1.35	1.16	1.36	2.85	2.98	3.07	3.08	2.98	3.20	2.60	2.75	2.94	2.94	2.75	2.92	ns
LVCMOS25_S12	1.08	1.16	1.32	1.35	1.16	1.36	2.44	2.57	2.67	2.67	2.57	2.80	2.19	2.34	2.54	2.54	2.34	2.52	ns
LVCMOS25_S16	1.08	1.16	1.32	1.35	1.16	1.36	2.79	2.92	3.01	3.01	2.92	3.14	2.54	2.68	2.88	2.88	2.68	2.86	ns
LVCMOS25_F4	1.08	1.16	1.32	1.35	1.16	1.36	2.71	2.84	2.93	2.93	2.84	3.06	2.46	2.61	2.80	2.80	2.61	2.78	ns
LVCMOS25_F8	1.08	1.16	1.32	1.35	1.16	1.36	2.14	2.28	2.37	2.37	2.28	2.50	1.90	2.04	2.24	2.24	2.04	2.22	ns
LVCMOS25_F12	1.08	1.16	1.32	1.35	1.16	1.36	2.15	2.29	2.52	2.52	2.29	2.48	1.91	2.05	2.38	2.38	2.05	2.20	ns
LVCMOS25_F16	1.08	1.16	1.32	1.35	1.16	1.36	1.92	2.17	2.45	2.45	2.17	2.33	1.67	1.94	2.32	2.32	1.94	2.05	ns
LVCMOS18_S4	0.64	0.66	0.74	0.95	0.66	0.87	1.55	1.68	1.78	1.78	1.68	1.91	1.30	1.45	1.65	1.65	1.45	1.63	ns
LVCMOS18_S8	0.64	0.66	0.74	0.95	0.66	0.87	2.14	2.28	2.37	2.37	2.28	2.50	1.90	2.04	2.24	2.24	2.04	2.22	ns
LVCMOS18_S12	0.64	0.66	0.74	0.95	0.66	0.87	2.14	2.28	2.37	2.37	2.28	2.50	1.90	2.04	2.24	2.24	2.04	2.22	ns
LVCMOS18_S16	0.64	0.66	0.74	0.95	0.66	0.87	1.49	1.62	1.72	1.72	1.62	1.84	1.24	1.39	1.58	1.58	1.39	1.56	ns

Table 20: **IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}						T_{IOOP}						T_{IOTP}						Units
	Speed Grade						Speed Grade						Speed Grade						
	1.0V				0.95V	0.9V	1.0V				0.95V	0.9V	1.0V				0.95V	0.9V	
	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	
LVCMOS18_S24	0.64	0.66	0.74	0.95	0.66	0.87	1.74	1.92	2.08	2.22	1.92	1.92	1.50	1.69	1.95	2.08	1.69	1.64	ns
LVCMOS18_F4	0.64	0.66	0.74	0.95	0.66	0.87	1.38	1.51	1.61	1.64	1.51	1.77	1.13	1.28	1.47	1.50	1.28	1.49	ns
LVCMOS18_F8	0.64	0.66	0.74	0.95	0.66	0.87	1.64	1.78	1.87	1.87	1.78	2.00	1.40	1.54	1.74	1.74	1.54	1.72	ns
LVCMOS18_F12	0.64	0.66	0.74	0.95	0.66	0.87	1.64	1.78	1.87	1.87	1.78	2.00	1.40	1.54	1.74	1.74	1.54	1.72	ns
LVCMOS18_F16	0.64	0.66	0.74	0.95	0.66	0.87	1.52	1.68	1.81	1.81	1.68	1.72	1.28	1.45	1.68	1.68	1.45	1.44	ns
LVCMOS18_F24	0.64	0.66	0.74	0.95	0.66	0.87	1.34	1.46	1.55	2.09	1.46	1.66	1.09	1.23	1.42	1.96	1.23	1.38	ns
LVCMOS15_S4	0.66	0.69	0.81	0.93	0.69	0.90	1.86	2.00	2.09	2.09	2.00	2.22	1.62	1.76	1.96	1.96	1.76	1.94	ns
LVCMOS15_S8	0.66	0.69	0.81	0.93	0.69	0.90	2.05	2.18	2.28	2.28	2.18	2.41	1.80	1.95	2.14	2.15	1.95	2.13	ns
LVCMOS15_S12	0.66	0.69	0.81	0.93	0.69	0.90	1.83	2.03	2.23	2.23	2.03	1.91	1.59	1.80	2.10	2.10	1.80	1.63	ns
LVCMOS15_S16	0.66	0.69	0.81	0.93	0.69	0.90	1.76	1.95	2.13	2.13	1.95	1.91	1.52	1.72	1.99	1.99	1.72	1.63	ns
LVCMOS15_F4	0.66	0.69	0.81	0.93	0.69	0.90	1.63	1.76	1.86	1.86	1.76	1.98	1.38	1.53	1.72	1.72	1.53	1.70	ns
LVCMOS15_F8	0.66	0.69	0.81	0.93	0.69	0.90	1.79	1.99	2.18	2.18	1.99	1.92	1.55	1.76	2.05	2.05	1.76	1.64	ns
LVCMOS15_F12	0.66	0.69	0.81	0.93	0.69	0.90	1.40	1.54	1.65	1.65	1.54	1.67	1.15	1.31	1.52	1.52	1.31	1.39	ns
LVCMOS15_F16	0.66	0.69	0.81	0.93	0.69	0.90	1.37	1.51	1.61	1.89	1.51	1.66	1.13	1.27	1.48	1.75	1.27	1.38	ns
LVCMOS12_S4	0.88	0.91	1.00	1.17	0.91	1.01	2.53	2.67	2.76	2.76	2.67	2.89	2.29	2.43	2.63	2.63	2.43	2.61	ns
LVCMOS12_S8	0.88	0.91	1.00	1.17	0.91	1.01	2.05	2.18	2.28	2.28	2.18	2.41	1.80	1.95	2.14	2.15	1.95	2.13	ns
LVCMOS12_S12	0.88	0.91	1.00	1.17	0.91	1.01	1.75	1.89	1.98	1.98	1.89	2.11	1.51	1.65	1.85	1.85	1.65	1.83	ns
LVCMOS12_F4	0.88	0.91	1.00	1.17	0.91	1.01	1.94	2.07	2.17	2.17	2.07	2.30	1.69	1.84	2.04	2.04	1.84	2.02	ns
LVCMOS12_F8	0.88	0.91	1.00	1.17	0.91	1.01	1.50	1.64	1.73	1.73	1.64	1.86	1.26	1.40	1.60	1.60	1.40	1.58	ns
LVCMOS12_F12	0.88	0.91	1.00	1.17	0.91	1.01	1.54	1.71	1.87	1.87	1.71	1.69	1.29	1.48	1.74	1.74	1.48	1.41	ns
SSTL135_S	0.61	0.64	0.73	0.85	0.64	0.79	1.27	1.40	1.50	1.53	1.40	1.64	1.02	1.17	1.36	1.40	1.17	1.36	ns
SSTL15_S	0.61	0.64	0.73	0.73	0.64	0.73	1.24	1.37	1.47	1.53	1.37	1.59	0.99	1.14	1.33	1.40	1.14	1.31	ns
SSTL18_I_S	0.64	0.67	0.76	0.84	0.67	0.79	1.59	1.74	1.85	1.85	1.74	1.95	1.34	1.50	1.72	1.72	1.50	1.67	ns
SSTL18_II_S	0.64	0.67	0.76	0.85	0.67	0.78	1.27	1.40	1.50	1.50	1.40	1.63	1.02	1.17	1.36	1.36	1.17	1.35	ns
DIFF_SSTL135_S	0.59	0.61	0.73	0.85	0.61	0.79	1.27	1.40	1.50	1.53	1.40	1.64	1.02	1.17	1.36	1.40	1.17	1.36	ns
DIFF_SSTL15_S	0.63	0.67	0.77	0.85	0.67	0.79	1.24	1.37	1.47	1.53	1.37	1.59	0.99	1.14	1.33	1.40	1.14	1.31	ns
DIFF_SSTL18_I_S	0.65	0.69	0.78	0.85	0.69	0.79	1.50	1.63	1.72	1.82	1.63	1.95	1.26	1.40	1.59	1.69	1.40	1.67	ns
DIFF_SSTL18_II_S	0.65	0.69	0.78	0.85	0.69	0.79	1.13	1.22	1.25	1.50	1.22	1.66	0.88	0.99	1.12	1.36	0.99	1.38	ns

Table 20: **IOB High Range (HR) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}						T_{IOOP}						T_{IOTP}						Units
	Speed Grade						Speed Grade						Speed Grade						
	1.0V				0.95V	0.9V	1.0V				0.95V	0.9V	1.0V				0.95V	0.9V	
	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	
SSTL135_F	0.61	0.64	0.73	0.85	0.64	0.79	1.04	1.17	1.26	1.31	1.17	1.42	0.79	0.93	1.13	1.18	0.93	1.14	ns
SSTL15_F	0.61	0.64	0.73	0.73	0.64	0.73	1.04	1.17	1.26	1.26	1.17	1.39	0.79	0.93	1.13	1.13	0.93	1.11	ns
SSTL18_I_F	0.64	0.67	0.76	0.84	0.67	0.79	1.12	1.22	1.26	1.34	1.22	1.44	0.88	0.99	1.13	1.21	0.99	1.16	ns
SSTL18_II_F	0.64	0.67	0.76	0.85	0.67	0.78	1.05	1.18	1.28	1.32	1.18	1.42	0.80	0.95	1.15	1.19	0.95	1.14	ns
DIFF_SSTL135_F	0.59	0.61	0.73	0.85	0.61	0.79	1.04	1.17	1.26	1.31	1.17	1.42	0.79	0.93	1.13	1.18	0.93	1.14	ns
DIFF_SSTL15_F	0.63	0.67	0.77	0.85	0.67	0.79	1.04	1.17	1.26	1.26	1.17	1.39	0.79	0.93	1.13	1.13	0.93	1.11	ns
DIFF_SSTL18_I_F	0.65	0.69	0.78	0.85	0.69	0.79	1.10	1.19	1.23	1.34	1.19	1.52	0.85	0.96	1.10	1.21	0.96	1.24	ns
DIFF_SSTL18_II_F	0.65	0.69	0.78	0.85	0.69	0.79	1.02	1.10	1.14	1.32	1.10	1.50	0.77	0.87	1.00	1.19	0.87	1.22	ns

Table 21: **IOB High Performance (HP) Switching Characteristics**

I/O Standard	T_{IOPI}						T_{IOOP}						T_{IOTP}						Units
	Speed Grade						Speed Grade						Speed Grade						
	1.0V				0.95V	0.9V	1.0V				0.95V	0.9V	1.0V				0.95V	0.9V	
	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	
LVDS	0.75	0.79	0.92	0.96	0.79	0.89	1.05	1.17	1.24	1.26	1.17	1.43	0.88	1.01	1.08	1.10	1.01	1.32	ns
HSUL_12_S	0.69	0.72	0.82	0.98	0.72	0.95	1.65	1.84	2.05	2.05	1.84	1.80	1.48	1.68	1.89	1.89	1.68	1.70	ns
HSUL_12_F	0.69	0.72	0.82	0.98	0.72	0.95	1.39	1.54	1.68	1.68	1.54	1.49	1.22	1.38	1.52	1.52	1.38	1.39	ns
DIFF_HSUL_12_S	0.69	0.72	0.82	0.98	0.72	0.92	1.65	1.84	2.05	2.05	1.84	1.47	1.48	1.68	1.89	1.89	1.68	1.37	ns
DIFF_HSUL_12_F	0.69	0.72	0.82	0.98	0.72	0.92	1.39	1.54	1.68	1.68	1.54	1.35	1.22	1.38	1.52	1.52	1.38	1.24	ns
DIFF_HSUL_12_DCI_S	0.69	0.72	0.82	0.82	0.72	0.92	1.78	1.91	2.05	2.05	1.91	1.46	1.61	1.76	1.89	1.89	1.76	1.35	ns
DIFF_HSUL_12_DCI_F	0.69	0.72	0.82	0.82	0.72	0.92	1.56	1.67	1.76	1.76	1.67	1.35	1.39	1.51	1.60	1.60	1.51	1.24	ns
HSTL_I_S	0.68	0.72	0.82	0.90	0.72	0.84	1.15	1.28	1.38	1.38	1.28	1.46	0.98	1.12	1.22	1.22	1.12	1.35	ns
HSTL_II_S	0.68	0.72	0.82	0.90	0.72	0.84	1.05	1.17	1.26	1.27	1.17	1.44	0.88	1.01	1.10	1.11	1.01	1.34	ns
HSTL_I_18_S	0.70	0.72	0.82	0.95	0.72	0.86	1.12	1.24	1.34	1.34	1.24	1.41	0.95	1.08	1.18	1.18	1.08	1.31	ns
HSTL_II_18_S	0.70	0.72	0.82	0.90	0.72	0.86	1.06	1.18	1.26	1.27	1.18	1.44	0.89	1.02	1.10	1.11	1.02	1.34	ns
HSTL_I_12_S	0.68	0.72	0.82	0.96	0.72	0.94	1.14	1.27	1.37	1.37	1.27	1.43	0.97	1.11	1.21	1.21	1.11	1.32	ns
HSTL_I_DCI_S	0.68	0.72	0.82	0.90	0.72	0.78	1.11	1.23	1.33	1.33	1.23	1.36	0.94	1.07	1.17	1.17	1.07	1.26	ns
HSTL_II_DCI_S	0.68	0.72	0.82	0.85	0.72	0.78	1.05	1.17	1.26	1.26	1.17	1.33	0.88	1.01	1.10	1.10	1.01	1.23	ns
HSTL_II_T_DCI_S	0.70	0.72	0.82	0.82	0.72	0.76	1.15	1.28	1.38	1.38	1.28	1.40	0.98	1.12	1.22	1.22	1.12	1.29	ns
HSTL_I_DCI_18_S	0.70	0.72	0.82	0.90	0.72	0.76	1.11	1.23	1.33	1.33	1.23	1.36	0.94	1.07	1.17	1.17	1.07	1.26	ns
HSTL_II_DCI_18_S	0.70	0.72	0.82	0.82	0.72	0.76	1.05	1.16	1.24	1.24	1.16	1.32	0.88	1.00	1.08	1.08	1.00	1.21	ns
HSTL_II_T_DCI_18_S	0.70	0.72	0.82	0.84	0.72	0.76	1.11	1.23	1.33	1.34	1.23	1.36	0.94	1.07	1.17	1.18	1.07	1.26	ns
DIFF_HSTL_I_S	0.75	0.79	0.92	1.02	0.79	0.89	1.15	1.28	1.38	1.38	1.28	1.47	0.98	1.12	1.22	1.22	1.12	1.37	ns
DIFF_HSTL_II_S	0.75	0.79	0.92	1.02	0.79	0.89	1.05	1.17	1.26	1.32	1.17	1.47	0.88	1.01	1.10	1.16	1.01	1.37	ns
DIFF_HSTL_I_DCI_S	0.75	0.79	0.92	0.92	0.79	0.76	1.15	1.28	1.38	1.38	1.28	1.47	0.98	1.12	1.22	1.22	1.12	1.37	ns
DIFF_HSTL_II_DCI_S	0.75	0.79	0.92	0.92	0.79	0.76	1.05	1.17	1.26	1.26	1.17	1.40	0.88	1.01	1.10	1.10	1.01	1.29	ns
DIFF_HSTL_I_18_S	0.75	0.79	0.92	0.98	0.79	0.89	1.12	1.24	1.34	1.34	1.24	1.46	0.95	1.08	1.18	1.18	1.08	1.35	ns
DIFF_HSTL_II_18_S	0.75	0.79	0.92	0.99	0.79	0.89	1.06	1.18	1.26	1.32	1.18	1.47	0.89	1.02	1.10	1.16	1.02	1.37	ns
DIFF_HSTL_I_DCI_18_S	0.75	0.79	0.92	0.92	0.79	0.75	1.11	1.23	1.33	1.33	1.23	1.46	0.94	1.07	1.17	1.17	1.07	1.35	ns
DIFF_HSTL_II_DCI_18_S	0.75	0.79	0.92	0.93	0.79	0.75	1.05	1.16	1.24	1.26	1.16	1.41	0.88	1.00	1.08	1.10	1.00	1.31	ns
DIFF_HSTL_II_T_DCI_18_S	0.75	0.79	0.92	0.92	0.79	0.76	1.11	1.23	1.33	1.33	1.23	1.46	0.94	1.07	1.17	1.17	1.07	1.35	ns
HSTL_I_F	0.68	0.72	0.82	0.90	0.72	0.84	1.02	1.14	1.22	1.22	1.14	1.26	0.85	0.98	1.06	1.06	0.98	1.15	ns
HSTL_II_F	0.68	0.72	0.82	0.90	0.72	0.84	0.97	1.08	1.15	1.15	1.08	1.29	0.80	0.92	0.99	0.99	0.92	1.18	ns
HSTL_I_18_F	0.70	0.72	0.82	0.95	0.72	0.86	1.04	1.16	1.24	1.24	1.16	1.32	0.87	1.00	1.08	1.08	1.00	1.21	ns

Table 21: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}						T_{IOOP}						T_{IOTP}						Units
	Speed Grade						Speed Grade						Speed Grade						
	1.0V				0.95V	0.9V	1.0V				0.95V	0.9V	1.0V				0.95V	0.9V	
	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	
HSTL_II_18_F	0.70	0.72	0.82	0.90	0.72	0.86	0.98	1.09	1.16	1.20	1.09	1.35	0.81	0.94	1.00	1.03	0.94	1.24	ns
HSTL_I_12_F	0.68	0.72	0.82	0.96	0.72	0.94	1.02	1.13	1.21	1.21	1.13	1.26	0.85	0.97	1.05	1.05	0.97	1.15	ns
HSTL_I_DCI_F	0.68	0.72	0.82	0.90	0.72	0.78	1.04	1.16	1.24	1.24	1.16	1.30	0.87	1.00	1.08	1.08	1.00	1.20	ns
HSTL_II_DCI_F	0.68	0.72	0.82	0.85	0.72	0.78	0.97	1.08	1.15	1.15	1.08	1.22	0.80	0.92	0.99	0.99	0.92	1.12	ns
HSTL_II_T_DCI_F	0.70	0.72	0.82	0.82	0.72	0.76	1.02	1.14	1.22	1.22	1.14	1.26	0.85	0.98	1.06	1.06	0.98	1.15	ns
HSTL_I_DCI_ 18_F	0.70	0.72	0.82	0.90	0.72	0.76	1.04	1.16	1.24	1.24	1.16	1.30	0.87	1.00	1.08	1.08	1.00	1.20	ns
HSTL_II_DCI_ 18_F	0.70	0.72	0.82	0.82	0.72	0.76	0.98	1.09	1.16	1.16	1.09	1.27	0.81	0.93	1.00	1.00	0.93	1.17	ns
HSTL_II _T_DCI_18_F	0.70	0.72	0.82	0.84	0.72	0.76	1.04	1.16	1.24	1.24	1.16	1.30	0.87	1.00	1.08	1.08	1.00	1.20	ns
DIFF_HSTL_I_F	0.75	0.79	0.92	1.02	0.79	0.89	1.02	1.14	1.22	1.22	1.14	1.35	0.85	0.98	1.06	1.06	0.98	1.24	ns
DIFF_HSTL_II_F	0.75	0.79	0.92	1.02	0.79	0.89	0.97	1.08	1.15	1.20	1.08	1.35	0.80	0.92	0.99	1.03	0.92	1.24	ns
DIFF_HSTL_I_ DCI_F	0.75	0.79	0.92	0.92	0.79	0.76	1.02	1.14	1.22	1.22	1.14	1.35	0.85	0.98	1.06	1.06	0.98	1.24	ns
DIFF_HSTL_II_ DCI_F	0.75	0.79	0.92	0.92	0.79	0.76	0.97	1.08	1.15	1.15	1.08	1.30	0.80	0.92	0.99	0.99	0.92	1.20	ns
DIFF_HSTL_I_ 18_F	0.75	0.79	0.92	0.98	0.79	0.89	1.04	1.16	1.24	1.24	1.16	1.38	0.87	1.00	1.08	1.08	1.00	1.28	ns
DIFF_HSTL_II_ 18_F	0.75	0.79	0.92	0.99	0.79	0.89	0.98	1.09	1.16	1.24	1.09	1.40	0.81	0.94	1.00	1.08	0.94	1.29	ns
DIFF_HSTL_I_ DCI_18_F	0.75	0.79	0.92	0.92	0.79	0.75	1.04	1.16	1.24	1.24	1.16	1.38	0.87	1.00	1.08	1.08	1.00	1.28	ns
DIFF_HSTL_II_ DCI_18_F	0.75	0.79	0.92	0.93	0.79	0.75	0.98	1.09	1.16	1.18	1.09	1.33	0.81	0.93	1.00	1.02	0.93	1.23	ns
DIFF_HSTL_II _T_DCI_18_F	0.75	0.79	0.92	0.92	0.79	0.76	1.04	1.16	1.24	1.24	1.16	1.38	0.87	1.00	1.08	1.08	1.00	1.28	ns
LVCMOS18_S2	0.47	0.50	0.60	0.90	0.50	0.87	3.95	4.28	4.85	4.85	4.28	3.40	3.78	4.13	4.69	4.69	4.13	3.29	ns
LVCMOS18_S4	0.47	0.50	0.60	0.90	0.50	0.87	2.67	2.98	3.43	3.43	2.98	2.69	2.50	2.82	3.27	3.27	2.82	2.59	ns
LVCMOS18_S6	0.47	0.50	0.60	0.90	0.50	0.87	2.14	2.38	2.72	2.72	2.38	2.18	1.97	2.22	2.56	2.56	2.22	2.07	ns
LVCMOS18_S8	0.47	0.50	0.60	0.90	0.50	0.87	1.98	2.21	2.52	2.52	2.21	2.02	1.81	2.05	2.36	2.36	2.05	1.92	ns
LVCMOS18_S12	0.47	0.50	0.60	0.90	0.50	0.87	1.70	1.91	2.17	2.17	1.91	1.85	1.53	1.75	2.01	2.01	1.75	1.74	ns
LVCMOS18_S16	0.47	0.50	0.60	0.90	0.50	0.87	1.57	1.75	1.97	1.97	1.75	1.76	1.40	1.59	1.81	1.81	1.59	1.65	ns
LVCMOS18_F2	0.47	0.50	0.60	0.90	0.50	0.87	3.50	3.87	4.48	4.48	3.87	2.85	3.33	3.71	4.32	4.32	3.71	2.74	ns
LVCMOS18_F4	0.47	0.50	0.60	0.90	0.50	0.87	2.23	2.50	2.87	2.87	2.50	2.26	2.06	2.34	2.71	2.71	2.34	2.15	ns
LVCMOS18_F6	0.47	0.50	0.60	0.90	0.50	0.87	1.80	2.00	2.26	2.26	2.00	1.52	1.63	1.84	2.09	2.09	1.84	1.42	ns
LVCMOS18_F8	0.47	0.50	0.60	0.90	0.50	0.87	1.46	1.72	2.04	2.04	1.72	1.51	1.29	1.56	1.88	1.88	1.56	1.40	ns
LVCMOS18_F12	0.47	0.50	0.60	0.90	0.50	0.87	1.26	1.40	1.53	1.53	1.40	1.46	1.09	1.24	1.37	1.37	1.24	1.35	ns
LVCMOS18_F16	0.47	0.50	0.60	0.90	0.50	0.87	1.19	1.33	1.44	1.66	1.33	1.46	1.02	1.17	1.28	1.50	1.17	1.35	ns
LVCMOS15_S2	0.59	0.62	0.73	0.88	0.62	0.86	3.55	3.89	4.45	4.45	3.89	3.11	3.38	3.73	4.29	4.29	3.73	3.01	ns
LVCMOS15_S4	0.59	0.62	0.73	0.88	0.62	0.86	2.45	2.70	3.06	3.06	2.70	2.46	2.28	2.54	2.90	2.90	2.54	2.35	ns
LVCMOS15_S6	0.59	0.62	0.73	0.88	0.62	0.86	2.24	2.51	2.88	2.88	2.51	2.33	2.07	2.35	2.72	2.72	2.35	2.23	ns

Table 21: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}						T_{IOOP}						T_{IOTP}						Units
	Speed Grade						Speed Grade						Speed Grade						
	1.0V				0.95V	0.9V	1.0V				0.95V	0.9V	1.0V				0.95V	0.9V	
	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	
LVCMOS15_S8	0.59	0.62	0.73	0.88	0.62	0.86	1.91	2.16	2.49	2.49	2.16	2.05	1.74	2.00	2.32	2.32	2.00	1.95	ns
LVCMOS15_S12	0.59	0.62	0.73	0.88	0.62	0.86	1.77	1.98	2.23	2.23	1.98	1.97	1.60	1.82	2.07	2.07	1.82	1.87	ns
LVCMOS15_S16	0.59	0.62	0.73	0.88	0.62	0.86	1.62	1.81	2.02	2.02	1.81	1.85	1.45	1.65	1.86	1.86	1.65	1.74	ns
LVCMOS15_F2	0.59	0.62	0.73	0.88	0.62	0.86	3.38	3.69	4.18	4.18	3.69	2.74	3.21	3.53	4.02	4.02	3.53	2.64	ns
LVCMOS15_F4	0.59	0.62	0.73	0.88	0.62	0.86	2.04	2.21	2.44	2.44	2.21	1.72	1.87	2.06	2.27	2.27	2.06	1.62	ns
LVCMOS15_F6	0.59	0.62	0.73	0.88	0.62	0.86	1.47	1.74	2.09	2.09	1.74	1.49	1.30	1.58	1.93	1.93	1.58	1.39	ns
LVCMOS15_F8	0.59	0.62	0.73	0.88	0.62	0.86	1.31	1.46	1.61	1.61	1.46	1.47	1.14	1.30	1.45	1.45	1.30	1.37	ns
LVCMOS15_F12	0.59	0.62	0.73	0.88	0.62	0.86	1.21	1.34	1.45	1.45	1.34	1.44	1.04	1.18	1.29	1.29	1.18	1.34	ns
LVCMOS15_F16	0.59	0.62	0.73	0.88	0.62	0.86	1.18	1.31	1.41	1.68	1.31	1.41	1.01	1.15	1.25	1.52	1.15	1.31	ns
LVCMOS12_S2	0.64	0.67	0.78	1.04	0.67	0.95	3.38	3.80	4.48	4.48	3.80	3.27	3.21	3.64	4.31	4.31	3.64	3.17	ns
LVCMOS12_S4	0.64	0.67	0.78	1.04	0.67	0.95	2.62	2.94	3.43	3.43	2.94	2.76	2.45	2.78	3.27	3.27	2.78	2.65	ns
LVCMOS12_S6	0.64	0.67	0.78	1.04	0.67	0.95	2.05	2.33	2.72	2.72	2.33	2.24	1.88	2.17	2.56	2.56	2.17	2.14	ns
LVCMOS12_S8	0.64	0.67	0.78	1.04	0.67	0.95	1.94	2.18	2.51	2.51	2.18	2.16	1.77	2.02	2.34	2.34	2.02	2.06	ns
LVCMOS12_F2	0.64	0.67	0.78	1.04	0.67	0.95	2.84	3.15	3.62	3.62	3.15	2.47	2.67	2.99	3.46	3.46	2.99	2.37	ns
LVCMOS12_F4	0.64	0.67	0.78	1.04	0.67	0.95	1.97	2.18	2.44	2.44	2.18	1.69	1.80	2.02	2.28	2.28	2.02	1.59	ns
LVCMOS12_F6	0.64	0.67	0.78	1.04	0.67	0.95	1.33	1.51	1.70	1.70	1.51	1.43	1.16	1.35	1.54	1.54	1.35	1.32	ns
LVCMOS12_F8	0.64	0.67	0.78	1.04	0.67	0.95	1.27	1.42	1.55	1.55	1.42	1.41	1.10	1.26	1.39	1.39	1.26	1.31	ns
LVDCI_18	0.47	0.50	0.60	0.87	0.50	0.86	1.99	2.15	2.35	2.35	2.15	2.44	1.82	1.99	2.19	2.19	1.99	2.34	ns
LVDCI_15	0.59	0.62	0.73	0.92	0.62	0.87	1.98	2.23	2.58	2.58	2.23	2.40	1.81	2.07	2.41	2.41	2.07	2.29	ns
LVDCI_DV2_18	0.47	0.50	0.60	0.88	0.50	0.87	1.99	2.15	2.34	2.34	2.15	1.86	1.82	1.99	2.18	2.18	1.99	1.76	ns
LVDCI_DV2_15	0.59	0.62	0.73	0.88	0.62	0.87	1.98	2.23	2.58	2.58	2.23	1.83	1.81	2.07	2.41	2.41	2.07	1.73	ns
HSLVDCI_18	0.68	0.72	0.82	0.90	0.72	0.86	1.99	2.15	2.35	2.35	2.15	2.43	1.82	1.99	2.19	2.19	1.99	2.32	ns
HSLVDCI_15	0.68	0.72	0.82	0.93	0.72	0.84	1.98	2.23	2.58	2.58	2.23	2.27	1.81	2.07	2.41	2.41	2.07	2.17	ns
SSTL18_I_S	0.68	0.72	0.82	0.95	0.72	0.86	1.02	1.15	1.24	1.24	1.15	1.41	0.85	0.99	1.08	1.08	0.99	1.31	ns
SSTL18_II_S	0.68	0.72	0.82	1.01	0.72	0.87	1.17	1.29	1.37	1.38	1.29	1.55	1.00	1.13	1.21	1.22	1.13	1.45	ns
SSTL18_I_DCI_S	0.68	0.72	0.82	0.87	0.72	0.76	0.92	1.06	1.17	1.18	1.06	1.32	0.75	0.90	1.01	1.02	0.90	1.21	ns
SSTL18_II_DCI_S	0.68	0.72	0.82	0.82	0.72	0.78	0.88	0.98	1.08	1.12	0.98	1.26	0.71	0.83	0.92	0.96	0.83	1.15	ns
SSTL18_II_T_ DCI_S	0.68	0.72	0.82	0.98	0.72	0.78	0.92	1.06	1.17	1.18	1.06	1.32	0.75	0.90	1.01	1.02	0.90	1.21	ns
SSTL15_S	0.68	0.72	0.82	0.82	0.72	0.81	0.94	1.06	1.15	1.16	1.06	1.32	0.77	0.91	0.99	1.00	0.91	1.21	ns
SSTL15_DCI_S	0.68	0.72	0.82	0.90	0.72	0.78	0.94	1.06	1.15	1.16	1.06	1.30	0.77	0.90	0.99	1.00	0.90	1.20	ns
SSTL15_T_DCI_S	0.68	0.72	0.82	0.87	0.72	0.80	0.94	1.06	1.15	1.15	1.06	1.30	0.77	0.90	0.99	0.99	0.90	1.20	ns
SSTL135_S	0.69	0.72	0.82	0.93	0.72	0.89	0.97	1.10	1.19	1.20	1.10	1.35	0.80	0.94	1.03	1.03	0.94	1.24	ns
SSTL135_DCI_S	0.69	0.72	0.82	0.85	0.72	0.84	0.97	1.09	1.19	1.20	1.09	1.33	0.80	0.93	1.03	1.03	0.93	1.23	ns
SSTL135_T_ DCI_S	0.69	0.72	0.82	0.93	0.72	0.84	0.97	1.09	1.19	1.20	1.09	1.33	0.80	0.93	1.03	1.03	0.93	1.23	ns
SSTL12_S	0.69	0.72	0.82	1.02	0.72	0.95	0.96	1.09	1.18	1.18	1.09	1.33	0.79	0.93	1.02	1.02	0.93	1.23	ns
SSTL12_DCI_S	0.69	0.72	0.82	0.90	0.72	0.91	1.03	1.17	1.27	1.27	1.17	1.33	0.86	1.01	1.11	1.11	1.01	1.23	ns
SSTL12_T_DCI_S	0.69	0.72	0.82	0.88	0.72	0.91	1.03	1.17	1.27	1.27	1.17	1.33	0.86	1.01	1.11	1.11	1.01	1.23	ns

Table 21: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}						T_{IOOP}						T_{IOTP}						Units
	Speed Grade						Speed Grade						Speed Grade						
	1.0V				0.95V	0.9V	1.0V				0.95V	0.9V	1.0V				0.95V	0.9V	
	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	
DIFF_SSTL18_I_S	0.75	0.79	0.92	0.99	0.79	0.89	1.02	1.15	1.24	1.29	1.15	1.43	0.85	0.99	1.08	1.13	0.99	1.32	ns
DIFF_SSTL18_II_S	0.75	0.79	0.92	0.93	0.79	0.89	1.17	1.29	1.37	1.40	1.29	1.55	1.00	1.13	1.21	1.24	1.13	1.45	ns
DIFF_SSTL18_I_DCI_S	0.75	0.79	0.92	0.92	0.79	0.76	0.92	1.06	1.17	1.24	1.06	1.40	0.75	0.90	1.01	1.08	0.90	1.29	ns
DIFF_SSTL18_II_DCI_S	0.75	0.79	0.92	0.96	0.79	0.75	0.88	0.98	1.08	1.18	0.98	1.33	0.71	0.83	0.92	1.02	0.83	1.23	ns
DIFF_SSTL18_II_T_DCI_S	0.75	0.79	0.92	0.92	0.79	0.76	0.92	1.06	1.17	1.24	1.06	1.40	0.75	0.90	1.01	1.08	0.90	1.29	ns
DIFF_SSTL15_S	0.68	0.72	0.82	0.99	0.72	0.89	0.94	1.06	1.15	1.16	1.06	1.32	0.77	0.91	0.99	1.00	0.91	1.21	ns
DIFF_SSTL15_DCI_S	0.68	0.72	0.82	0.96	0.72	0.75	0.94	1.06	1.15	1.16	1.06	1.30	0.77	0.90	0.99	1.00	0.90	1.20	ns
DIFF_SSTL15_T_DCI_S	0.68	0.72	0.82	0.88	0.72	0.76	0.94	1.06	1.15	1.23	1.06	1.38	0.77	0.90	0.99	1.07	0.90	1.28	ns
DIFF_SSTL135_S	0.69	0.72	0.82	1.09	0.72	0.91	0.97	1.10	1.19	1.20	1.10	1.35	0.80	0.94	1.03	1.03	0.94	1.24	ns
DIFF_SSTL135_DCI_S	0.69	0.72	0.82	0.90	0.72	0.76	0.97	1.09	1.19	1.20	1.09	1.33	0.80	0.93	1.03	1.03	0.93	1.23	ns
DIFF_SSTL135_T_DCI_S	0.69	0.72	0.82	0.84	0.72	0.76	0.97	1.09	1.19	1.27	1.09	1.43	0.80	0.93	1.03	1.11	0.93	1.32	ns
DIFF_SSTL12_S	0.69	0.72	0.82	0.96	0.72	0.91	0.96	1.09	1.18	1.18	1.09	1.33	0.79	0.93	1.02	1.02	0.93	1.23	ns
DIFF_SSTL12_DCI_S	0.69	0.72	0.82	0.87	0.72	0.78	1.03	1.17	1.27	1.27	1.17	1.33	0.86	1.01	1.11	1.11	1.01	1.23	ns
DIFF_SSTL12_T_DCI_S	0.69	0.72	0.82	0.96	0.72	0.80	1.03	1.17	1.27	1.27	1.17	1.41	0.86	1.01	1.11	1.11	1.01	1.31	ns
SSTL18_I_F	0.68	0.72	0.82	0.95	0.72	0.86	0.94	1.06	1.15	1.15	1.06	1.32	0.77	0.91	0.99	0.99	0.91	1.21	ns
SSTL18_II_F	0.68	0.72	0.82	1.01	0.72	0.87	0.97	1.09	1.16	1.21	1.09	1.36	0.80	0.93	1.00	1.05	0.93	1.26	ns
SSTL18_I_DCI_F	0.68	0.72	0.82	0.87	0.72	0.76	0.89	1.02	1.10	1.15	1.02	1.30	0.72	0.86	0.94	0.99	0.86	1.20	ns
SSTL18_II_DCI_F	0.68	0.72	0.82	0.82	0.72	0.78	0.89	1.02	1.10	1.10	1.02	1.24	0.72	0.86	0.94	0.94	0.86	1.14	ns
SSTL18_II_T_DCI_F	0.68	0.72	0.82	0.98	0.72	0.78	0.89	1.02	1.10	1.15	1.02	1.27	0.72	0.86	0.94	0.99	0.86	1.17	ns
SSTL15_F	0.68	0.72	0.82	0.82	0.72	0.81	0.89	1.01	1.09	1.09	1.01	1.24	0.72	0.85	0.93	0.93	0.85	1.14	ns
SSTL15_DCI_F	0.68	0.72	0.82	0.90	0.72	0.78	0.89	1.01	1.09	1.12	1.01	1.27	0.72	0.85	0.93	0.96	0.85	1.17	ns
SSTL15_T_DCI_F	0.68	0.72	0.82	0.87	0.72	0.80	0.89	1.01	1.09	1.12	1.01	1.27	0.72	0.85	0.93	0.96	0.85	1.17	ns
SSTL135_F	0.69	0.72	0.82	0.93	0.72	0.89	0.88	1.00	1.08	1.12	1.00	1.27	0.71	0.85	0.92	0.96	0.85	1.17	ns
SSTL135_DCI_F	0.69	0.72	0.82	0.85	0.72	0.84	0.89	1.00	1.08	1.12	1.00	1.27	0.72	0.85	0.92	0.96	0.85	1.17	ns
SSTL135_T_DCI_F	0.69	0.72	0.82	0.93	0.72	0.84	0.89	1.00	1.08	1.12	1.00	1.27	0.72	0.85	0.92	0.96	0.85	1.17	ns
SSTL12_F	0.69	0.72	0.82	1.02	0.72	0.95	0.88	1.00	1.08	1.12	1.00	1.26	0.71	0.84	0.92	0.96	0.84	1.15	ns
SSTL12_DCI_F	0.69	0.72	0.82	0.90	0.72	0.91	0.91	1.03	1.11	1.11	1.03	1.24	0.74	0.88	0.95	0.95	0.88	1.14	ns
SSTL12_T_DCI_F	0.69	0.72	0.82	0.88	0.72	0.91	0.91	1.03	1.11	1.12	1.03	1.26	0.74	0.88	0.95	0.96	0.88	1.15	ns
DIFF_SSTL18_I_F	0.75	0.79	0.92	0.99	0.79	0.89	0.94	1.06	1.15	1.23	1.06	1.38	0.77	0.91	0.99	1.07	0.91	1.28	ns
DIFF_SSTL18_II_F	0.75	0.79	0.92	0.93	0.79	0.89	0.97	1.09	1.16	1.24	1.09	1.40	0.80	0.93	1.00	1.08	0.93	1.29	ns

Table 21: **IOB High Performance (HP) Switching Characteristics *(Cont'd)***

I/O Standard	T_{IOPI}						T_{IOOP}						T_{IOTP}						Units
	Speed Grade						Speed Grade						Speed Grade						
	1.0V				0.95V	0.9V	1.0V				0.95V	0.9V	1.0V				0.95V	0.9V	
	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	-3	-2/ -2LE	-1	-1M	-2LI	-2LE	
DIFF_SSTL18_I_DCI_F	0.75	0.79	0.92	0.92	0.79	0.76	0.89	1.02	1.10	1.23	1.02	1.36	0.72	0.86	0.94	1.07	0.86	1.26	ns
DIFF_SSTL18_II_DCI_F	0.75	0.79	0.92	0.96	0.79	0.75	0.89	1.02	1.10	1.16	1.02	1.32	0.72	0.86	0.94	1.00	0.86	1.21	ns
DIFF_SSTL18_II_T_DCI_F	0.75	0.79	0.92	0.92	0.79	0.76	0.89	1.02	1.10	1.24	1.02	1.38	0.72	0.86	0.94	1.08	0.86	1.28	ns
DIFF_SSTL15_F	0.68	0.72	0.82	0.99	0.72	0.89	0.89	1.01	1.09	1.09	1.01	1.24	0.72	0.85	0.93	0.93	0.85	1.14	ns
DIFF_SSTL15_DCI_F	0.68	0.72	0.82	0.96	0.72	0.75	0.89	1.01	1.09	1.12	1.01	1.27	0.72	0.85	0.93	0.96	0.85	1.17	ns
DIFF_SSTL15_T_DCI_F	0.68	0.72	0.82	0.88	0.72	0.76	0.89	1.01	1.09	1.20	1.01	1.35	0.72	0.85	0.93	1.03	0.85	1.24	ns
DIFF_SSTL135_F	0.69	0.72	0.82	1.09	0.72	0.91	0.88	1.00	1.08	1.12	1.00	1.27	0.71	0.85	0.92	0.96	0.85	1.17	ns
DIFF_SSTL135_DCI_F	0.69	0.72	0.82	0.90	0.72	0.76	0.89	1.00	1.08	1.12	1.00	1.27	0.72	0.85	0.92	0.96	0.85	1.17	ns
DIFF_SSTL135_T_DCI_F	0.69	0.72	0.82	0.84	0.72	0.76	0.89	1.00	1.08	1.20	1.00	1.35	0.72	0.85	0.92	1.03	0.85	1.24	ns
DIFF_SSTL12_F	0.69	0.72	0.82	0.96	0.72	0.91	0.88	1.00	1.08	1.12	1.00	1.26	0.71	0.84	0.92	0.96	0.84	1.15	ns
DIFF_SSTL12_DCI_F	0.69	0.72	0.82	0.87	0.72	0.78	0.91	1.03	1.11	1.11	1.03	1.24	0.74	0.88	0.95	0.95	0.88	1.14	ns
DIFF_SSTL12_T_DCI_F	0.69	0.72	0.82	0.96	0.72	0.80	0.91	1.03	1.11	1.18	1.03	1.33	0.74	0.88	0.95	1.02	0.88	1.23	ns

Table 22 specifies the values of T_{IOTPHZ} and $T_{IOIBUFDISABLE}$. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than T_{IOTPHZ} when the DCITERMDISABLE pin is used. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than T_{IOTPHZ} when the INTERMDISABLE pin is used.

Table 22: **IOB 3-state Output Switching Characteristics**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
T_{IOTPHZ}	T input to pad high-impedance	0.76	0.86	0.99	0.99	0.86	0.62	ns
$T_{IOIBUFDISABLE\_HR}$	IBUF turn-on time from IBUFDISABLE to O output for HR I/O banks	1.72	1.89	2.14	2.14	1.89	2.17	ns
$T_{IOIBUFDISABLE\_HP}$	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	1.31	1.46	1.76	1.76	1.46	1.86	ns

I/O Standard Adjustment Measurement Methodology

Input Delay Measurements

Table 23 shows the test setup parameters used for measuring input delay.

Table 23: **Input Delay Measurement Methodology**

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(6)	V_{REF} (1)(3)(5)
LVCMOS, 1.2V	LVCMOS12	0.1	1.1	0.6	–
LVCMOS, 1.5V	LVCMOS15	0.1	1.4	0.75	–
LVCMOS, 1.8V	LVCMOS18	0.1	1.7	0.9	–
LVCMOS, 2.5V	LVCMOS25	0.1	2.4	1.25	–
LVCMOS, 3.3V	LVCMOS33	0.1	3.2	1.75	–
LVTTL, 3.3V	LVTTL	0.1	3.2	1.75	–
MOBILE_DDR, 1.8V	MOBILE_DDR	0.1	1.7	0.9	–
PCI33, 3.3V	PCI33_3	0.1	3.2	1.32	–
HSTL (High-Speed Transceiver Logic), Class I, 1.2V	HSTL_I_12	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.60
HSTL, Class I & II, 1.5V	HSTL_I, HSTL_II	V_{REF} – 0.65	V_{REF} + 0.65	V_{REF}	0.75
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	V_{REF} – 0.8	V_{REF} + 0.8	V_{REF}	0.90
HSUL (High-Speed Unterminated Logic), 1.2V	HSUL_12	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.60
SSTL (Stub Terminated Transceiver Logic), 1.2V	SSTL12	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.60
SSTL, 1.35V	SSTL135, SSTL135_R	V_{REF} – 0.575	V_{REF} + 0.575	V_{REF}	0.675
SSTL, 1.5V	SSTL15, SSTL15_R	V_{REF} – 0.65	V_{REF} + 0.65	V_{REF}	0.75
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	V_{REF} – 0.8	V_{REF} + 0.8	V_{REF}	0.90
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	0.9 – 0.125	0.9 + 0.125	0(6)	–
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	0.6 – 0.125	0.6 + 0.125	0(6)	–
DIFF_HSTL, Class I & II,1.5V	DIFF_HSTL_I, DIFF_HSTL_II	0.75 – 0.125	0.75 + 0.125	0(6)	–
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	0.9 – 0.125	0.9 + 0.125	0(6)	–
DIFF_HSUL, 1.2V	DIFF_HSUL_12	0.6 – 0.125	0.6 + 0.125	0(6)	–
DIFF_SSTL, 1.2V	DIFF_SSTL12	0.6 – 0.125	0.6 + 0.125	0(6)	–
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	0.675 – 0.125	0.675 + 0.125	0(6)	–
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	0.75 – 0.125	0.75 + 0.125	0(6)	–
DIFF_SSTL18_I/DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	0.9 – 0.125	0.9 + 0.125	0(6)	–
LVDS (Low-Voltage Differential Signaling), 1.8V	LVDS	0.9 – 0.125	0.9 + 0.125	0(6)	–
LVDS_25, 2.5V	LVDS_25	1.2 – 0.125	1.2 + 0.125	0(6)	–
BLVDS_25, 2.5V	BLVDS_25	1.25 – 0.125	1.25 + 0.125	0(6)	–
MINI_LVDS_25, 2.5V	MINI_LVDS_25	1.25 – 0.125	1.25 + 0.125	0(6)	–
PPDS_25	PPDS_25	1.25 – 0.125	1.25 + 0.125	0(6)	–
RSDS_25	RSDS_25	1.25 – 0.125	1.25 + 0.125	0(6)	–

Table 23: **Input Delay Measurement Methodology *(Cont'd)***

Description	I/O Standard Attribute	V_L (1)(2)	V_H (1)(2)	V_{MEAS} (1)(4)(6)	V_{REF} (1)(3)(5)
TMDS_33	TMDS_33	3 – 0.125	3 + 0.125	0(6)	–

Notes:

1. The input delay measurement methodology parameters for LVDCI are the same for LVCMOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between $V_L$and V_H.
3. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 1.
6. The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 1 and Figure 2.

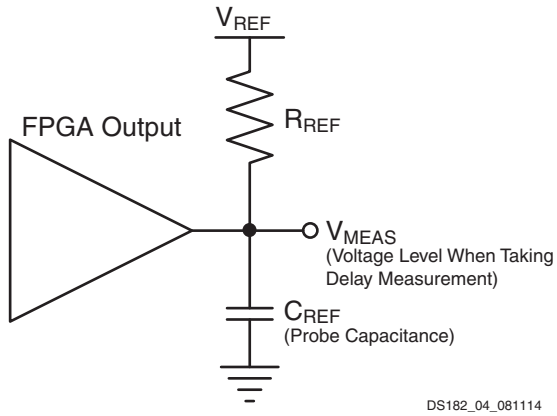


Figure 1: **Single-Ended Test Setup**

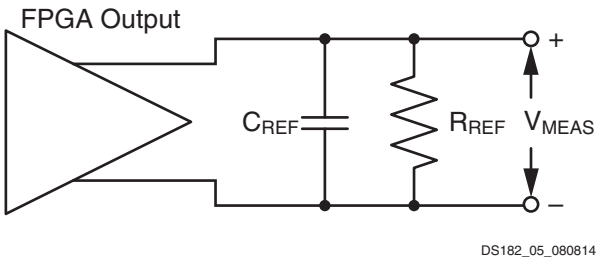


Figure 2: **Differential Test Setup**

Parameters V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 24.
2. Record the time to V_{MEAS}.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS}.

5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 24: **Output Delay Measurement Methodology**

Description	I/O Standard Attribute	R_{REF} (Ω)	C_{REF}[1] (pF)	V_{MEAS} (V)	V_{REF} (V)
LVCMOS, 1.2V	LVCMOS12	1M	0	0.6	0
LVCMOS/LVDCI/HSLVDCI, 1.5V	LVCMOS15, LVDCI_15, HSLVDCI_15	1M	0	0.75	0
LVCMOS/LVDCI/HSLVDCI, 1.8V	LVCMOS18, LVDCI_15, HSLVDCI_18	1M	0	0.9	0
LVCMOS, 2.5V	LVCMOS25	1M	0	1.25	0
LVCMOS, 3.3V	LVCMOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
PCI33, 3.3V	PCI33_3	25	10	1.65	0
HSTL (High-Speed Transceiver Logic), Class I, 1.2V	HSTL_I_12	50	0	V_{REF}	0.6
HSTL, Class I, 1.5V	HSTL_I	50	0	V_{REF}	0.75
HSTL, Class II, 1.5V	HSTL_II	25	0	V_{REF}	0.75
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V_{REF}	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V_{REF}	0.9
HSUL (High-Speed Unterminated Logic), 1.2V	HSUL_12	50	0	V_{REF}	0.6
SSTL12, 1.2V	SSTL12	50	0	V_{REF}	0.6
SSTL135/SSTL135_R, 1.35V	SSTL135, SSTL135_R	50	0	V_{REF}	0.675
SSTL15/SSTL15_R, 1.5V	SSTL15, SSTL15_R	50	0	V_{REF}	0.75
SSTL (Stub Series Terminated Logic), Class I & Class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V_{REF}	0.9
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	50	0	V_{REF}	0.9
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	50	0	V_{REF}	0.6
DIFF_HSTL, Class I & II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	50	0	V_{REF}	0.75
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	50	0	V_{REF}	0.9
DIFF_HSUL_12, 1.2V	DIFF_HSUL_12	50	0	V_{REF}	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V_{REF}	0.6
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	50	0	V_{REF}	0.675
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	50	0	V_{REF}	0.75
DIFF_SSTL18, Class I & II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V_{REF}	0.9
LVDS (Low-Voltage Differential Signaling), 1.8V	LVDS	100	0	0[2]	0
LVDS, 2.5V	LVDS_25	100	0	0[2]	0
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0[2]	0
Mini LVDS, 2.5V	MINI_LVDS_25	100	0	0[2]	0
PPDS_25	PPDS_25	100	0	0[2]	0
RSDS_25	RSDS_25	100	0	0[2]	0
TMDS_33	TMDS_33	50	0	0[2]	3.3

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

Input/Output Logic Switching Characteristics

Table 25: **ILOGIC Switching Characteristics**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
Setup/Hold								
T_{ICE1CK}/ T_{ICKCE1}	CE1 pin Setup/Hold with respect to CLK	0.42/0.00	0.48/0.00	0.67/0.00	0.67/0.00	0.48/0.00	0.56/–0.16	ns
T_{ISRCK}/T_{ICKSR}	SR pin Setup/Hold with respect to CLK	0.53/0.01	0.61/0.01	0.99/0.01	0.99/0.01	0.61/0.01	0.88/–0.30	ns
$T_{IDOCKE2}$/ $T_{IOCKDE2}$	D pin Setup/Hold with respect to CLK without Delay (HP I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	0.01/0.34	0.01/0.29	0.01/0.41	ns
$T_{IDOCKDE2}$/ $T_{IOCKDDE2}$	DDLY pin Setup/Hold with respect to CLK (using IDELAY) (HP I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	0.02/0.34	0.02/0.29	0.01/0.41	ns
$T_{IDOCKE3}$/ $T_{IOCKDE3}$	D pin Setup/Hold with respect to CLK without Delay (HR I/O banks only)	0.01/0.27	0.01/0.29	0.01/0.34	0.01/0.34	0.01/0.29	0.01/0.41	ns
$T_{IDOCKDE3}$/ $T_{IOCKDDE3}$	DDLY pin Setup/Hold with respect to CLK (using IDELAY) (HR I/O banks only)	0.01/0.27	0.02/0.29	0.02/0.34	0.02/0.34	0.02/0.29	0.01/0.41	ns
Combinatorial								
T_{IDIE2}	D pin to O pin propagation delay, no Delay (HP I/O banks only)	0.09	0.10	0.12	0.12	0.10	0.14	ns
T_{IDIDE2}	DDLY pin to O pin propagation delay (using IDELAY) (HP I/O banks only)	0.10	0.11	0.13	0.13	0.11	0.15	ns
T_{IDIE3}	D pin to O pin propagation delay, no Delay (HR I/O banks only)	0.09	0.10	0.12	0.12	0.10	0.14	ns
T_{IDIDE3}	DDLY pin to O pin propagation delay (using IDELAY) (HR I/O banks only)	0.10	0.11	0.13	0.13	0.11	0.15	ns
Sequential Delays								
T_{IDLOE2}	D pin to Q1 pin using flip-flop as a latch without Delay (HP I/O banks only)	0.36	0.39	0.45	0.45	0.39	0.54	ns
$T_{IDLODE2}$	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HP I/O banks only)	0.36	0.39	0.45	0.45	0.39	0.55	ns
T_{IDLOE3}	D pin to Q1 pin using flip-flop as a latch without Delay (HR I/O banks only)	0.36	0.39	0.45	0.45	0.39	0.54	ns
$T_{IDLODE3}$	DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) (HR I/O banks only)	0.36	0.39	0.45	0.45	0.39	0.55	ns
T_{ICKQ}	CLK to Q outputs	0.47	0.50	0.58	0.58	0.50	0.71	ns
$T_{RQ\_ILOGICE2}$	SR pin to OQ/TQ out (HP I/O banks only)	0.84	0.94	1.16	1.16	0.94	1.32	ns
$T_{GSRQ\_ILOGICE2}$	Global Set/Reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	10.51	7.60	11.39	ns
$T_{RQ\_ILOGICE3}$	SR pin to OQ/TQ out (HR I/O banks only)	0.84	0.94	1.16	1.16	0.94	1.32	ns
$T_{GSRQ\_ILOGICE3}$	Global Set/Reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	10.51	7.60	11.39	ns

Table 25: **ILOGIC Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
Set/Reset								
$T_{RPW\_ILOGICE2}$	Minimum Pulse Width, SR inputs (HP I/O banks only)	0.54	0.63	0.63	0.63	0.63	0.68	ns, Min
$T_{RPW\_ILOGICE3}$	Minimum Pulse Width, SR inputs (HR I/O banks only)	0.54	0.63	0.63	0.63	0.63	0.68	ns, Min

Table 26: **OLOGIC Switching Characteristics**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
Setup/Hold								
T_{ODCK}/T_{OCKD}	D1/D2 pins Setup/Hold with respect to CLK	0.45/–0.13	0.50/–0.13	0.58/–0.13	0.58/–0.13	0.50/–0.13	0.79/–0.18	ns
T_{OOCECK}/T_{OCKOCE}	OCE pin Setup/Hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	0.45/0.03	0.29/0.03	0.35/–0.10	ns
T_{OSRCK}/T_{OCKSR}	SR pin Setup/Hold with respect to CLK	0.32/0.18	0.38/0.18	0.70/0.18	0.70/0.18	0.38/0.18	0.62/–0.04	ns
T_{OTCK}/T_{OCKT}	T1/T2 pins Setup/Hold with respect to CLK	0.49/–0.16	0.56/–0.16	0.68/–0.16	0.68/–0.13	0.56/–0.16	0.67/–0.18	ns
T_{OTCECK}/T_{OCKTCE}	TCE pin Setup/Hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	0.45/0.06	0.30/0.01	0.31/–0.10	ns
Combinatorial								
T_{ODQ}	D1 to OQ out or T1 to TQ out	0.73	0.81	0.97	0.97	0.81	1.18	ns
Sequential Delays								
T_{OCKQ}	CLK to OQ/TQ out	0.41	0.43	0.49	0.49	0.43	0.63	ns
$T_{RQ\_OLOGICE2}$	SR pin to OQ/TQ out (HP I/O banks only)	0.63	0.70	0.83	0.83	0.70	1.12	ns
$T_{GSRQ\_OLOGICE2}$	Global Set/Reset to Q outputs (HP I/O banks only)	7.60	7.60	10.51	10.51	7.60	11.39	ns
$T_{RQ\_OLOGICE3}$	SR pin to OQ/TQ out (HR I/O banks only)	0.63	0.70	0.83	0.83	0.70	1.12	ns
$T_{GSRQ\_OLOGICE3}$	Global Set/Reset to Q outputs (HR I/O banks only)	7.60	7.60	10.51	10.51	7.60	11.39	ns
Set/Reset								
$T_{RPW\_OLOGICE2}$	Minimum Pulse Width, SR inputs (HP I/O banks only)	0.54	0.54	0.63	0.63	0.54	0.68	ns, Min
$T_{RPW\_OLOGICE3}$	Minimum Pulse Width, SR inputs (HR I/O banks only)	0.54	0.54	0.63	0.63	0.54	0.68	ns, Min

Input Serializer/Deserializer Switching Characteristics

Table 27: **ISERDES Switching Characteristics**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
Setup/Hold for Control Lines								
$T_{ISCCK\_BITSLIP}$/ $T_{ISCKC\_BITSLIP}$	BITSLIP pin Setup/Hold with respect to CLKDIV	0.01/0.12	0.02/0.13	0.02/0.15	0.02/0.15	0.02/0.13	0.02/0.21	ns
T_{ISCCK_CE}/ T_{ISCKC_CE}(2)	CE pin Setup/Hold with respect to CLK (for CE1)	0.39/–0.02	0.44/–0.02	0.63/–0.02	0.63/–0.02	0.44/–0.02	0.51/–0.22	ns
T_{ISCCK_CE2}/ T_{ISCKC_CE2}(2)	CE pin Setup/Hold with respect to CLKDIV (for CE2)	–0.12/0.29	–0.12/0.31	–0.12/0.35	–0.12/0.35	–0.12/0.31	–0.17/0.40	ns
Setup/Hold for Data Lines								
T_{ISDCK_D}/ T_{ISCKD_D}	D pin Setup/Hold with respect to CLK	–0.02/0.11	–0.02/0.12	–0.02/0.15	–0.02/0.15	–0.02/0.12	–0.04/0.19	ns
T_{ISDCK_DDLY}/ T_{ISCKD_DDLY}	DDLY pin Setup/Hold with respect to CLK (using IDELAY)(1)	–0.02/0.11	–0.02/0.12	–0.02/0.15	–0.02/0.15	–0.02/0.12	–0.03/0.19	ns
$T_{ISDCK\_D\_DDR}$/ $T_{ISCKD\_D\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode	–0.02/0.11	–0.02/0.12	–0.02/0.15	–0.02/0.15	–0.02/0.12	–0.04/0.19	ns
$T_{ISDCK\_DDLY\_DDR}$/ $T_{ISCKD\_DDLY\_DDR}$	D pin Setup/Hold with respect to CLK at DDR mode (using IDELAY)(1)	0.11/0.11	0.12/0.12	0.15/0.15	0.15/0.15	0.12/0.12	0.19/0.19	ns
Sequential Delays								
T_{ISCKO_Q}	CLKDIV to out at Q pin	0.46	0.47	0.58	0.58	0.47	0.67	ns
Propagation Delays								
T_{ISDO_DO}	D input to DO output pin	0.09	0.10	0.12	0.12	0.10	0.14	ns

Notes:

1. Recorded at 0 tap value.
2. T_{ISCCK_CE2} and T_{ISCKC_CE2} are reported as T_{ISCCK_CE}/T_{ISCKC_CE} in the timing report.

Output Serializer/Deserializer Switching Characteristics

Table 28: **OSERDES Switching Characteristics**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
Setup/Hold								
T_{OSDCK_D}/ T_{OSCKD_D}	D input Setup/Hold with respect to CLKDIV	0.37/0.02	0.40/0.02	0.55/0.02	0.55/0.02	0.40/0.02	0.44/–0.24	ns
T_{OSDCK_T}/ T_{OSCKD_T}(1)	T input Setup/Hold with respect to CLK	0.49/–0.15	0.56/–0.15	0.68/–0.15	0.68/–0.15	0.56/–0.15	0.67/–0.25	ns
T_{OSDCK_T2}/ T_{OSCKD_T2}(1)	T input Setup/Hold with respect to CLKDIV	0.27/–0.15	0.30/–0.15	0.34/–0.15	0.34/–0.15	0.30/–0.15	0.46/–0.25	ns
T_{OSCCK_OCE}/ T_{OSCKC_OCE}	OCE input Setup/Hold with respect to CLK	0.28/0.03	0.29/0.03	0.45/0.03	0.45/0.03	0.29/0.03	0.35/–0.15	ns
T_{OSCCK_S}	SR (Reset) input Setup with respect to CLKDIV	0.41	0.46	0.75	0.75	0.46	0.70	ns
T_{OSCCK_TCE}/ T_{OSCKC_TCE}	TCE input Setup/Hold with respect to CLK	0.28/0.01	0.30/0.01	0.45/0.01	0.45/0.01	0.30/0.01	0.31/–0.15	ns
Sequential Delays								
T_{OSCKO_OQ}	Clock to out from CLK to OQ	0.35	0.37	0.42	0.42	0.37	0.54	ns
T_{OSCKO_TQ}	Clock to out from CLK to TQ	0.41	0.43	0.49	0.49	0.43	0.63	ns
Combinatorial								
T_{OSDO_TTQ}	T input to TQ Out	0.73	0.81	0.97	0.97	0.81	1.18	ns

Notes:

1. T_{OSDCK_T2} and T_{OSCKD_T2} are reported as T_{OSDCK_T}/T_{OSCKD_T} in the timing report.

Input/Output Delay Switching Characteristics

Table 29: **Input/Output Delay Switching Characteristics**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
IDELAYCTRL								
T_{DLYCCO_RDY}	Reset to Ready for IDELAYCTRL	3.22	3.22	3.22	3.22	3.22	3.22	µs
$F_{IDELAYCTRL\_REF}$	Attribute REFCLK frequency = 200.00(1)	200.00	200.00	200.00	200.00	200.00	200.00	MHz
	Attribute REFCLK frequency = 300.00(1)	300.00	300.00	N/A	N/A	300.00	N/A	MHz
	Attribute REFCLK frequency = 400.00(1)	400.00	400.00	N/A	N/A	400.00	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	±10	±10	±10	MHz
$T_{IDELAYCTRL\_RPW}$	Minimum Reset pulse width	52.00	52.00	52.00	52.00	52.00	52.00	ns
IDELAY/ODELAY								
$T_{IDELAYRESOLUTION}$	IDELAY/ODELAY chain delay resolution	$1/(32 \times 2 \times F_{REF})$						ps
$T_{IDELAYPAT\_JIT}$ and $T_{ODELAYPAT\_JIT}$	Pattern dependent period jitter in delay chain for clock pattern.(2)	0	0	0	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(3)	±5	±5	±5	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(4)	±9	±9	±9	±9	±9	±9	ps per tap
$T_{IDELAY\_CLK\_MAX}$/ $T_{ODELAY\_CLK\_MAX}$	Maximum frequency of CLK input to IDELAY/ODELAY	800.00	800.00	710.00	710.00	800.00	710.00	MHz
T_{IDCCK_CE} / T_{IDCKC_CE}	CE pin Setup/Hold with respect to C for IDELAY	0.11/0.10	0.14/0.12	0.18/0.14	0.18/0.14	0.14/0.12	0.14/0.16	ns
T_{ODCCK_CE} / T_{ODCKC_CE}	CE pin Setup/Hold with respect to C for ODELAY	0.14/0.03	0.16/0.04	0.19/0.05	0.19/0.05	0.16/0.04	0.28/0.06	ns
T_{IDCCK_INC}/ T_{IDCKC_INC}	INC pin Setup/Hold with respect to C for IDELAY	0.10/0.14	0.12/0.16	0.14/0.20	0.14/0.20	0.12/0.16	0.10/0.23	ns
T_{ODCCK_INC}/ T_{ODCKC_INC}	INC pin Setup/Hold with respect to C for ODELAY	0.10/0.07	0.12/0.08	0.13/0.09	0.13/0.09	0.12/0.08	0.19/0.16	ns
T_{IDCCK_RST}/ T_{IDCKC_RST}	RST pin Setup/Hold with respect to C for IDELAY	0.13/0.08	0.14/0.10	0.16/0.12	0.16/0.12	0.14/0.10	0.22/0.19	ns
T_{ODCCK_RST}/ T_{ODCKC_RST}	RST pin Setup/Hold with respect to C for ODELAY	0.16/0.04	0.19/0.06	0.24/0.08	0.24/0.08	0.19/0.06	0.32/0.11	ns
$T_{IDDO\_IDATAIN}$	Propagation delay through IDELAY	Note 5	Note 5	Note 5	Note 5	Note 5	Note 5	ps
$T_{ODDO\_ODATAIN}$	Propagation delay through ODELAY	Note 5	Note 5	Note 5	Note 5	Note 5	Note 5	ps

Notes:

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps, and at 400 MHz = 39 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY/ODELAY tap setting. See the timing report for actual values.

Table 30: **IO_FIFO Switching Characteristics**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
IO_FIFO Clock to Out Delays								
T_{OFFCKO_DO}	RDCLK to Q outputs	0.51	0.56	0.63	0.63	0.56	0.81	ns
T_{CKO_FLAGS}	Clock to IO_FIFO Flags	0.59	0.62	0.81	0.81	0.62	0.77	ns
Setup/Hold								
T_{CCK_D}/ T_{CKC_D}	D inputs to WRCLK	0.43/–0.01	0.47/–0.01	0.53/–0.01	0.53/0.09	0.47/–0.01	0.76/–0.05	ns
T_{IFFCCK_WREN} / T_{IFFCKC_WREN}	WREN to WRCLK	0.39/–0.01	0.43/–0.01	0.50/–0.01	0.50/–0.01	0.43/–0.01	0.70/–0.05	ns
T_{OFFCCK_RDEN}/ T_{OFFCKC_RDEN}	RDEN to RDCLK	0.49/0.01	0.53/0.02	0.61/0.02	0.61/0.02	0.53/0.02	0.79/–0.02	ns
Minimum Pulse Width								
$T_{PWH\_IO\_FIFO}$	RESET, RDCLK, WRCLK	0.81	0.92	1.08	1.08	0.92	1.29	ns
$T_{PWL\_IO\_FIFO}$	RESET, RDCLK, WRCLK	0.81	0.92	1.08	1.08	0.92	1.29	ns
Maximum Frequency								
F_{MAX}	RDCLK and WRCLK	533.05	470.37	400.00	400.00	470.37	333.33	MHz

CLB Switching Characteristics

Table 31: **CLB Switching Characteristics**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
Combinatorial Delays								
T_{ILO}	An – Dn LUT address to A	0.05	0.05	0.06	0.06	0.05	0.07	ns, Max
T_{ILO_2}	An – Dn LUT address to AMUX/CMUX	0.15	0.16	0.19	0.19	0.16	0.22	ns, Max
T_{ILO_3}	An – Dn LUT address to BMUX_A	0.24	0.25	0.30	0.30	0.25	0.37	ns, Max
T_{ITO}	An – Dn inputs to A – D Q outputs	0.58	0.61	0.74	0.74	0.61	0.91	ns, Max
T_{AXA}	AX inputs to AMUX output	0.38	0.40	0.49	0.49	0.40	0.62	ns, Max
T_{AXB}	AX inputs to BMUX output	0.40	0.42	0.52	0.52	0.42	0.66	ns, Max
T_{AXC}	AX inputs to CMUX output	0.39	0.41	0.50	0.50	0.41	0.62	ns, Max
T_{AXD}	AX inputs to DMUX output	0.43	0.44	0.52	0.52	0.44	0.67	ns, Max
T_{BXB}	BX inputs to BMUX output	0.31	0.33	0.40	0.40	0.33	0.51	ns, Max
T_{BXD}	BX inputs to DMUX output	0.38	0.39	0.47	0.47	0.39	0.62	ns, Max
T_{CXC}	CX inputs to CMUX output	0.27	0.28	0.34	0.34	0.28	0.43	ns, Max
T_{CXD}	CX inputs to DMUX output	0.33	0.34	0.41	0.41	0.34	0.54	ns, Max
T_{DXD}	DX inputs to DMUX output	0.32	0.33	0.40	0.40	0.33	0.52	ns, Max
Sequential Delays								
T_{CKO}	Clock to AQ – DQ outputs	0.26	0.27	0.32	0.32	0.27	0.40	ns, Max
T_{SHCKO}	Clock to AMUX – DMUX outputs	0.32	0.32	0.39	0.39	0.32	0.46	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK								
T_{AS}/T_{AH}	A_N – D_N input to CLK on A – D flip-flops	0.01/0.12	0.02/0.13	0.03/0.18	0.03/0.24	0.02/0.13	0.02/0.18	ns, Min
T_{DICK}/T_{CKDI}	A_X – D_X input to CLK on A – D flip-flops	0.04/0.14	0.04/0.14	0.05/0.20	0.05/0.26	0.04/0.14	0.05/0.21	ns, Min
	A_X – D_X input through MUXs and/or carry logic to CLK on A – D flip-flops	0.36/0.10	0.37/0.11	0.46/0.16	0.46/0.22	0.37/0.11	0.56/0.15	ns, Min
$T_{CECK\_CLB}/T_{CKCE\_CLB}$	CE input to CLK on A – D flip-flops	0.19/0.05	0.20/0.05	0.25/0.05	0.25/0.11	0.20/0.05	0.24/0.04	ns, Min
T_{SRCK}/T_{CKSR}	SR input to CLK on A – D flip-flops	0.30/0.05	0.31/0.07	0.37/0.09	0.37/0.22	0.31/0.07	0.48/0.05	ns, Min
Set/Reset								
T_{SRMIN}	SR input minimum pulse width	0.52	0.78	1.04	1.04	0.78	0.95	ns, Min
T_{RQ}	Delay from SR input to AQ – DQ flip-flops	0.38	0.38	0.46	0.46	0.38	0.59	ns, Max
T_{CEO}	Delay from CE input to AQ – DQ flip-flops	0.34	0.35	0.43	0.43	0.35	0.54	ns, Max
F_{TOG}	Toggle frequency (for export control)	1818	1818	1818	1818	1818	1286	MHz

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 32: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
Sequential Delays								
T_{SHCKO}	Clock to A – B outputs	0.68	0.70	0.85	0.85	0.70	1.08	ns, Max
T_{SHCKO_1}	Clock to AMUX – BMUX outputs	0.91	0.95	1.15	1.15	0.95	1.44	ns, Max
Setup and Hold Times Before/After Clock CLK								
T_{DS_LRAM}/ T_{DH_LRAM}	A – D inputs to CLK	0.45/0.23	0.45/0.24	0.54/0.27	0.54/0.28	0.45/0.24	0.69/0.33	ns, Min
T_{AS_LRAM}/ T_{AH_LRAM}	Address An inputs to clock	0.13/0.50	0.14/0.50	0.17/0.58	0.17/0.61	0.14/0.50	0.21/0.63	ns, Min
	Address An inputs through MUXs and/or carry logic to clock	0.40/0.16	0.42/0.17	0.52/0.23	0.52/0.29	0.42/0.17	0.63/0.23	ns, Min
T_{WS_LRAM}/ T_{WH_LRAM}	WE input to clock	0.29/0.09	0.30/0.09	0.36/0.09	0.36/0.11	0.30/0.09	0.46/0.10	ns, Min
T_{CECK_LRAM}/ T_{CKCE_LRAM}	CE input to CLK	0.29/0.09	0.30/0.09	0.37/0.09	0.37/0.11	0.30/0.09	0.47/0.10	ns, Min
Clock CLK								
T_{MPW}	Minimum pulse width	0.68	0.77	0.91	0.91	0.77	1.11	ns, Min
T_{MCP}	Minimum clock period	1.35	1.54	1.82	1.82	1.54	2.22	ns, Min

Notes:

1. T_{SHCKO} also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 33: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
Sequential Delays								
T_{REG}	Clock to A – D outputs	0.96	0.98	1.20	1.20	0.98	1.35	ns, Max
T_{REG_MUX}	Clock to AMUX – DMUX output	1.19	1.23	1.50	1.50	1.23	1.72	ns, Max
T_{REG_M31}	Clock to DMUX output via M31 output	0.89	0.91	1.10	1.10	0.91	1.25	ns, Max
Setup and Hold Times Before/After Clock CLK								
T_{WS_SHFREG}/ T_{WH_SHFREG}	WE input	0.26/0.09	0.27/0.09	0.33/0.09	0.33/0.11	0.27/0.09	0.41/0.10	ns, Min
T_{CECK_SHFREG}/ T_{CKCE_SHFREG}	CE input to CLK	0.27/0.09	0.28/0.09	0.33/0.09	0.33/0.11	0.28/0.09	0.42/0.10	ns, Min
T_{DS_SHFREG}/ T_{DH_SHFREG}	A – D inputs to CLK	0.28/0.26	0.28/0.26	0.33/0.30	0.33/0.36	0.28/0.26	0.41/0.36	ns, Min
Clock CLK								
T_{MPW_SHFREG}	Minimum pulse width	0.55	0.65	0.78	0.78	0.65	0.91	ns, Min

Block RAM and FIFO Switching Characteristics

Table 34: **Block RAM and FIFO Switching Characteristics**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
Block RAM and FIFO Clock-to-Out Delays								
T_{RCKO_DO} and $T_{RCKO\_DO\_REG}$[1]	Clock CLK to DOUT output (without output register)[2][3]	1.57	1.80	2.08	2.08	1.80	2.44	ns, Max
	Clock CLK to DOUT output (with output register)[4][5]	0.54	0.63	0.75	0.75	0.63	0.86	ns, Max
$T_{RCKO\_DO\_ECC}$ and $T_{RCKO\_DO\_ECC\_REG}$	Clock CLK to DOUT output with ECC (without output register)[2][3]	2.35	2.58	3.26	3.26	2.58	4.49	ns, Max
	Clock CLK to DOUT output with ECC (with output register)[4][5]	0.62	0.69	0.80	0.80	0.69	0.94	ns, Max
$T_{RCKO\_DO\_CASCOUT}$ and $T_{RCKO\_DO\_CASCOUT\_REG}$	Clock CLK to DOUT output with Cascade (without output register)[2]	2.21	2.45	2.80	2.80	2.45	3.19	ns, Max
	Clock CLK to DOUT output with Cascade (with output register)[4]	0.98	1.08	1.24	1.24	1.08	1.32	ns, Max
T_{RCKO_FLAGS}	Clock CLK to FIFO flags outputs[6]	0.65	0.74	0.89	0.89	0.74	0.97	ns, Max
$T_{RCKO\_POINTERS}$	Clock CLK to FIFO pointers outputs[7]	0.79	0.87	0.98	0.98	0.87	1.10	ns, Max
$T_{RCKO\_PARITY\_ECC}$	Clock CLK to ECCPARITY in ECC encode only mode	0.66	0.72	0.80	0.80	0.72	0.93	ns, Max
$T_{RCKO\_SDBIT\_ECC}$ and $T_{RCKO\_SDBIT\_ECC\_REG}$	Clock CLK to BITERR (without output register)	2.17	2.38	3.01	3.01	2.38	4.15	ns, Max
	Clock CLK to BITERR (with output register)	0.57	0.65	0.76	0.76	0.65	0.89	ns, Max
$T_{RCKO\_RDADDR\_ECC}$ and $T_{RCKO\_RDADDR\_ECC\_REG}$	Clock CLK to RDADDR output with ECC (without output register)	0.64	0.74	0.90	0.90	0.74	0.98	ns, Max
	Clock CLK to RDADDR output with ECC (with output register)	0.71	0.79	0.92	0.92	0.79	1.10	ns, Max
Setup and Hold Times Before/After Clock CLK								
T_{RCCK_ADDRA}/ T_{RCKC_ADDRA}	ADDR inputs[8]	0.38/ 0.27	0.42/ 0.28	0.48/ 0.31	0.48/ 0.38	0.42/ 0.28	0.65/ 0.38	ns, Min
$T_{RDCK\_DI\_WF\_NC}$/ $T_{RCKD\_DI\_WF\_NC}$	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode[9]	0.49/ 0.51	0.55/ 0.53	0.63/ 0.57	0.63/ 0.57	0.55/ 0.53	0.78/ 0.64	ns, Min
$T_{RDCK\_DI\_RF}$/ $T_{RCKD\_DI\_RF}$	Data input setup/hold time when block RAM is configured in READ_FIRST mode[9]	0.17/ 0.25	0.19/ 0.29	0.21/ 0.35	0.21/ 0.35	0.19/ 0.29	0.25/ 0.32	ns, Min
$T_{RDCK\_DI\_ECC}$/ $T_{RCKD\_DI\_ECC}$	DIN inputs with block RAM ECC in standard mode[9]	0.42/ 0.37	0.47/ 0.39	0.53/ 0.43	0.53/ 0.58	0.47/ 0.39	0.66/ 0.46	ns, Min
$T_{RDCK\_DI\_ECCW}$/ $T_{RCKD\_DI\_ECCW}$	DIN inputs with block RAM ECC encode only[9]	0.79/ 0.37	0.87/ 0.39	0.99/ 0.43	0.99/ 0.58	0.87/ 0.39	1.17/ 0.41	ns, Min
$T_{RDCK\_DI\_ECC\_FIFO}$/ $T_{RCKD\_DI\_ECC\_FIFO}$	DIN inputs with FIFO ECC in standard mode[9]	0.89/ 0.47	0.98/ 0.50	1.12/ 0.54	1.12/ 0.69	0.98/ 0.50	1.32/ 0.65	ns, Min

Table 34: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
$T_{RCCK\_INJECTBITERR}$/ $T_{RCKC\_INJECTBITERR}$	Inject single/double bit error in ECC mode	0.49/ 0.30	0.55/ 0.31	0.63/ 0.34	0.63/ 0.43	0.55/ 0.31	0.78/ 0.41	ns, Min
T_{RCCK_EN}/T_{RCKC_EN}	Block RAM Enable (EN) input	0.30/ 0.17	0.33/ 0.18	0.38/ 0.20	0.38/ 0.32	0.33/ 0.18	0.48/ 0.22	ns, Min
T_{RCCK_REGCE}/ T_{RCKC_REGCE}	CE input of output register	0.21/ 0.13	0.25/ 0.13	0.31/ 0.14	0.31/ 0.19	0.25/ 0.13	0.34/ 0.16	ns, Min
T_{RCCK_RSTREG}/ T_{RCKC_RSTREG}	Synchronous RSTREG input	0.25/ 0.06	0.27/ 0.06	0.29/ 0.06	0.29/ 0.14	0.27/ 0.06	0.35/ 0.06	ns, Min
T_{RCCK_RSTRAM}/ T_{RCKC_RSTRAM}	Synchronous RSTRAM input	0.27/ 0.35	0.29/ 0.37	0.31/ 0.39	0.31/ 0.39	0.29/ 0.37	0.34/ 0.40	ns, Min
T_{RCCK_WEA}/ T_{RCKC_WEA}	Write Enable (WE) input (Block RAM only)	0.38/ 0.15	0.41/ 0.16	0.46/ 0.17	0.46/ 0.29	0.41/ 0.16	0.54/ 0.19	ns, Min
T_{RCCK_WREN}/ T_{RCKC_WREN}	WREN FIFO inputs	0.39/ 0.25	0.39/ 0.30	0.40/ 0.37	0.40/ 0.49	0.39/ 0.30	0.65/ 0.37	ns, Min
T_{RCCK_RDEN}/ T_{RCKC_RDEN}	RDEN FIFO inputs	0.36/ 0.26	0.36/ 0.30	0.37/ 0.37	0.37/ 0.49	0.36/ 0.30	0.60/ 0.38	ns, Min
Reset Delays								
T_{RCO_FLAGS}	Reset RST to FIFO flags/pointers(10)	0.76	0.83	0.93	0.93	0.83	1.06	ns, Max
T_{RREC_RST}/ T_{RREM_RST}	FIFO reset recovery and removal timing(11)	1.59/ –0.68	1.76/ –0.68	2.01/ –0.68	2.01/ –0.68	1.76/ –0.68	2.07/ –0.60	ns, Max
Maximum Frequency								
$F_{MAX\_BRAM\_WF\_NC}$	Block RAM (Write first and No change modes) When not in SDP RF mode	601.32	543.77	458.09	458.09	543.77	372.44	MHz
$F_{MAX\_BRAM\_RF\_PERFORMANCE}$	Block RAM (Read first, Performance mode) When in SDP RF mode but no address overlap between port A and port B	601.32	543.77	458.09	458.09	543.77	372.44	MHz
$F_{MAX\_BRAM\_RF\_DELAYED\_WRITE}$	Block RAM (Read first, Delayed_write mode) When in SDP RF mode and there is possibility of overlap between port A and port B addresses	528.26	477.33	400.80	400.80	477.33	317.36	MHz
$F_{MAX\_CAS\_WF\_NC}$	Block RAM Cascade (Write first, No change mode) When cascade but not in RF mode	551.27	493.83	408.00	408.00	493.83	322.48	MHz
$F_{MAX\_CAS\_RF\_PERFORMANCE}$	Block RAM Cascade (Read first, Performance mode) When in cascade with RF mode and no possibility of address overlap/one port is disabled	551.27	493.83	408.00	408.00	493.83	322.48	MHz

Table 34: **Block RAM and FIFO Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
$F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$	When in cascade RF mode and there is a possibility of address overlap between port A and port B	478.24	427.35	350.88	350.88	427.35	267.38	MHz
F_{MAX_FIFO}	FIFO in all modes without ECC	601.32	543.77	458.09	458.09	543.77	372.44	MHz
F_{MAX_ECC}	Block RAM and FIFO in ECC configuration	484.26	430.85	351.12	351.12	430.85	254.13	MHz

Notes:

1. The timing report shows all of these parameters as T_{RCKO_DO}.
2. T_{RCKO_DOR} includes T_{RCKO_DOW}, T_{RCKO_DOPR}, and T_{RCKO_DOPW} as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. T_{RCKO_DO} includes T_{RCKO_DOP} as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. T_{RCKO_FLAGS} includes the following parameters: T_{RCKO_AEMPTY}, T_{RCKO_AFULL}, T_{RCKO_EMPTY}, T_{RCKO_FULL}, T_{RCKO_RDERR}, T_{RCKO_WRERR}.
7. $T_{RCKO\_POINTERS}$ includes both $T_{RCKO\_RDCOUNT}$ and $T_{RCKO\_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. T_{RCO_FLAGS} includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

DSP48E1 Switching Characteristics

Table 35: **DSP48E1 Switching Characteristics**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
Setup and Hold Times of Data/Control Pins to the Input Register Clock								
$T_{DSPDCK\_A\_AREG}$/ $T_{DSPCKD\_A\_AREG}$	A input to A register CLK	0.24/ 0.12	0.27/ 0.14	0.31/ 0.16	0.33/ 0.18	0.27/ 0.14	0.38/ 0.12	ns
$T_{DSPDCK\_B\_BREG}$/ $T_{DSPCKD\_B\_BREG}$	B input to B register CLK	0.28/ 0.13	0.32/ 0.14	0.39/ 0.15	0.41/ 0.18	0.32/ 0.14	0.51/ 0.16	ns
$T_{DSPDCK\_C\_CREG}$/ $T_{DSPCKD\_C\_CREG}$	C input to C register CLK	0.15/ 0.15	0.17/ 0.17	0.20/ 0.20	0.20/ 0.22	0.17/ 0.17	0.31/ 0.21	ns
$T_{DSPDCK\_D\_DREG}$/ $T_{DSPCKD\_D\_DREG}$	D input to D register CLK	0.21/ 0.19	0.27/ 0.22	0.35/ 0.26	0.35/ 0.27	0.27/ 0.22	0.46/ 0.20	ns
$T_{DSPDCK\_ACIN\_AREG}$/ $T_{DSPCKD\_ACIN\_AREG}$	ACIN input to A register CLK	0.21/ 0.12	0.24/ 0.14	0.27/ 0.16	0.30/ 0.16	0.24/ 0.14	0.31/ 0.12	ns
$T_{DSPDCK\_BCIN\_BREG}$/ $T_{DSPCKD\_BCIN\_BREG}$	BCIN input to B register CLK	0.22/ 0.13	0.25/ 0.14	0.30/ 0.15	0.32/ 0.15	0.25/ 0.14	0.34/ 0.16	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock								
$T_{DSPDCK\_\{A, B\}\_MREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\_MREG\_MULT}$	{A, B} input to M register CLK using multiplier	2.04/ –0.01	2.34/ –0.01	2.79/ –0.01	2.79/ –0.01	2.34/ –0.01	3.66/ –0.06	ns
$T_{DSPDCK\_\{A, D\}\_ADREG}$/ $T_{DSPCKD\_\{A, D\}\_ADREG}$	{A, D} input to AD register CLK	1.09/ –0.02	1.25/ –0.02	1.49/ –0.02	1.49/ –0.02	1.25/ –0.02	1.94/ –0.23	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock								
$T_{DSPDCK\_\{A, B\}\_PREG\_MULT}$/ $T_{DSPCKD\_\{A, B\}\ \_PREG\_MULT}$	{A, B,} input to P register CLK using multiplier	3.41/ –0.24	3.90/ –0.24	4.64/ –0.24	4.64/ –0.24	3.90/ –0.24	5.89/ –0.41	ns
$T_{DSPDCK\_D\_PREG\_MULT}$/ $T_{DSPCKD\_D\_PREG\_MULT}$	D input to P register CLK using multiplier	3.33/ –0.62	3.81/ –0.62	4.53/ –0.62	4.53/ –0.62	3.81/ –0.62	5.70/ –1.42	ns
$T_{DSPDCK\_\{A, B\}\ \_PREG}$/ $T_{DSPCKD\_\{A, B\}\ \_PREG}$	A or B input to P register CLK not using multiplier	1.47/ –0.24	1.68/ –0.24	2.00/ –0.24	2.00/ –0.24	1.68/ –0.24	2.37/ –0.41	ns
$T_{DSPDCK\_C\_PREG}$/ $T_{DSPCKD\_C\_PREG}$	C input to P register CLK not using multiplier	1.30/ –0.22	1.49/ –0.22	1.78/ –0.22	1.78/ –0.22	1.49/ –0.22	2.11/ –0.36	ns
$T_{DSPDCK\_PCIN\_PREG}$/ $T_{DSPCKD\_PCIN\_PREG}$	PCIN input to P register CLK	1.12/ –0.13	1.28/ –0.13	1.52/ –0.13	1.52/ –0.13	1.28/ –0.13	1.81/ –0.21	ns
Setup and Hold Times of the CE Pins								
$T_{DSPDCK\_\{CEA;CEB\}\_\{AREG;BREG\}}$/ $T_{DSPCKD\_\{CEA;CEB\}\_\{AREG;BREG\}}$	{CEA; CEB} input to {A; B} register CLK	0.30/ 0.05	0.36/ 0.06	0.44/ 0.09	0.44/ 0.09	0.36/ 0.06	0.55/ 0.09	ns
$T_{DSPDCK\_CEC\_CREG}$/ $T_{DSPCKD\_CEC\_CREG}$	CEC input to C register CLK	0.24/ 0.08	0.29/ 0.09	0.36/ 0.11	0.36/ 0.11	0.29/ 0.09	0.43/ 0.11	ns
$T_{DSPDCK\_CED\_DREG}$/ $T_{DSPCKD\_CED\_DREG}$	CED input to D register CLK	0.31/ –0.02	0.36/ –0.02	0.44/ –0.02	0.44/ 0.02	0.36/ –0.02	0.58/ 0.12	ns
$T_{DSPDCK\_CEM\_MREG}$/ $T_{DSPCKD\_CEM\_MREG}$	CEM input to M register CLK	0.26/ 0.15	0.29/ 0.17	0.33/ 0.20	0.33/ 0.20	0.29/ 0.17	0.39/ 0.25	ns
$T_{DSPDCK\_CEP\_PREG}$/ $T_{DSPCKD\_CEP\_PREG}$	CEP input to P register CLK	0.31/ 0.01	0.36/ 0.01	0.45/ 0.01	0.45/ 0.01	0.36/ 0.01	0.54/ 0.00	ns

Table 35: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
Setup and Hold Times of the RST Pins								
$T_{DSPDCK\_\{RSTA;\ RSTB\}\_\{AREG;\ BREG\}}$/ $T_{DSPCKD\_\{RSTA;\ RSTB\}\_\{AREG;\ BREG\}}$	{RSTA, RSTB} input to {A, B} register CLK	0.34/ 0.10	0.39/ 0.11	0.47/ 0.13	0.47/ 0.14	0.39/ 0.11	0.53/ 0.34	ns
$T_{DSPDCK\_RSTC\_CREG}$/ $T_{DSPCKD\_RSTC\_CREG}$	RSTC input to C register CLK	0.06/ 0.22	0.07/ 0.24	0.08/ 0.26	0.08/ 0.26	0.07/ 0.24	0.08/ 0.31	ns
$T_{DSPDCK\_RSTD\_DREG}$/ $T_{DSPCKD\_RSTD\_DREG}$	RSTD input to D register CLK	0.37/ 0.06	0.42/ 0.06	0.50/ 0.07	0.50/ 0.07	0.42/ 0.06	0.57/ 0.07	ns
$T_{DSPDCK\_RSTM\_MREG}$/ $T_{DSPCKD\_RSTM\_MREG}$	RSTM input to M register CLK	0.18/ 0.18	0.20/ 0.21	0.23/ 0.24	0.23/ 0.24	0.20/ 0.21	0.24/ 0.29	ns
$T_{DSPDCK\_RSTP\_PREG}$/ $T_{DSPCKD\_RSTP\_PREG}$	RSTP input to P register CLK	0.24/ 0.01	0.26/ 0.01	0.30/ 0.01	0.30/ 0.11	0.26/ 0.01	0.37/ 0.00	ns
Combinatorial Delays from Input Pins to Output Pins								
$T_{DSPDO\_A\_CARRYOUT\_MULT}$	A input to CARRYOUT output using multiplier	3.21	3.69	4.39	4.39	3.69	5.60	ns
$T_{DSPDO\_D\_P\_MULT}$	D input to P output using multiplier	3.15	3.61	4.30	4.30	3.61	5.44	ns
$T_{DSPDO\_A\_P}$	A input to P output not using multiplier	1.30	1.48	1.76	1.76	1.48	2.10	ns
$T_{DSPDO\_C\_P}$	C input to P output	1.13	1.30	1.55	1.55	1.30	1.84	ns
Combinatorial Delays from Input Pins to Cascading Output Pins								
$T_{DSPDO\_\{A;\ B\}\_\{ACOUT;\ BCOUT\}}$	{A, B} input to {ACOUT, BCOUT} output	0.47	0.53	0.63	0.63	0.53	0.75	ns
$T_{DSPDO\_\{A,\ B\}\_CARRYCASCOUT\_MULT}$	{A, B} input to CARRYCASCOUT output using multiplier	3.44	3.94	4.69	4.69	3.94	5.96	ns
$T_{DSPDO\_D\_CARRYCASCOUT\_MULT}$	D input to CARRYCASCOUT output using multiplier	3.36	3.85	4.58	4.58	3.85	5.77	ns
$T_{DSPDO\_\{A,\ B\}\_CARRYCASCOUT}$	{A, B} input to CARRYCASCOUT output not using multiplier	1.50	1.72	2.04	2.04	1.72	2.44	ns
$T_{DSPDO\_C\_CARRYCASCOUT}$	C input to CARRYCASCOUT output	1.34	1.53	1.83	1.83	1.53	2.18	ns
Combinatorial Delays from Cascading Input Pins to All Output Pins								
$T_{DSPDO\_ACIN\_P\_MULT}$	ACIN input to P output using multiplier	3.09	3.55	4.24	4.24	3.55	5.42	ns
$T_{DSPDO\_ACIN\_P}$	ACIN input to P output not using multiplier	1.16	1.33	1.59	1.59	1.33	2.07	ns
$T_{DSPDO\_ACIN\_ACOUT}$	ACIN input to ACOUT output	0.32	0.37	0.45	0.45	0.37	0.53	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT\_MULT}$	ACIN input to CARRYCASCOUT output using multiplier	3.30	3.79	4.52	4.52	3.79	5.76	ns
$T_{DSPDO\_ACIN\_CARRYCASCOUT}$	ACIN input to CARRYCASCOUT output not using multiplier	1.37	1.57	1.87	1.87	1.57	2.40	ns
$T_{DSPDO\_PCIN\_P}$	PCIN input to P output	0.94	1.08	1.29	1.29	1.08	1.54	ns
$T_{DSPDO\_PCIN\_CARRYCASCOUT}$	PCIN input to CARRYCASCOUT output	1.15	1.32	1.57	1.57	1.32	1.88	ns

Table 35: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
Clock to Outs from Output Register Clock to Output Pins								
$T_{DSPCKO\_P\_PREG}$	CLK PREG to P output	0.33	0.35	0.39	0.39	0.35	0.45	ns
$T_{DSPCKO\_CARRYCASCOUT\_PREG}$	CLK PREG to CARRYCASCOUT output	0.44	0.50	0.59	0.59	0.50	0.71	ns
Clock to Outs from Pipeline Register Clock to Output Pins								
$T_{DSPCKO\_P\_MREG}$	CLK MREG to P output	1.42	1.64	1.96	1.96	1.64	2.31	ns
$T_{DSPCKO\_CARRYCASCOUT\_MREG}$	CLK MREG to CARRYCASCOUT output	1.63	1.87	2.24	2.24	1.87	2.65	ns
$T_{DSPCKO\_P\_ADREG\_MULT}$	CLK ADREG to P output using multiplier	2.30	2.63	3.13	3.13	2.63	3.90	ns
$T_{DSPCKO\_CARRYCASCOUT\_ADREG\_MULT}$	CLK ADREG to CARRYCASCOUT output using multiplier	2.51	2.87	3.41	3.41	2.87	4.23	ns
Clock to Outs from Input Register Clock to Output Pins								
$T_{DSPCKO\_P\_AREG\_MULT}$	CLK AREG to P output using multiplier	3.34	3.83	4.55	4.55	3.83	5.80	ns
$T_{DSPCKO\_P\_BREG}$	CLK BREG to P output not using multiplier	1.39	1.59	1.88	1.88	1.59	2.24	ns
$T_{DSPCKO\_P\_CREG}$	CLK CREG to P output not using multiplier	1.43	1.64	1.95	1.95	1.64	2.32	ns
$T_{DSPCKO\_P\_DREG\_MULT}$	CLK DREG to P output using multiplier	3.32	3.80	4.51	4.51	3.80	5.74	ns
Clock to Outs from Input Register Clock to Cascading Output Pins								
$T_{DSPCKO\_\{ACOUT; BCOUT\}\_\{AREG; BREG\}}$	CLK (ACOUT, BCOUT) to {A,B} register output	0.55	0.62	0.74	0.74	0.62	0.87	ns
$T_{DSPCKO\_CARRYCASCOUT\_\{AREG, BREG\}\_MULT}$	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier	3.55	4.06	4.84	4.84	4.06	6.13	ns
$T_{DSPCKO\_CARRYCASCOUT\_BREG}$	CLK BREG to CARRYCASCOUT output not using multiplier	1.60	1.82	2.16	2.16	1.82	2.58	ns
$T_{DSPCKO\_CARRYCASCOUT\_DREG\_MULT}$	CLK DREG to CARRYCASCOUT output using multiplier	3.52	4.03	4.79	4.79	4.03	6.07	ns
$T_{DSPCKO\_CARRYCASCOUT\_CREG}$	CLK CREG to CARRYCASCOUT output	1.64	1.88	2.23	2.23	1.88	2.65	ns
Maximum Frequency								
F_{MAX}	With all registers used	741.84	650.20	547.95	547.95	650.20	429.37	MHz
F_{MAX_PATDET}	With pattern detector	627.35	549.75	463.61	463.61	549.75	365.90	MHz
$F_{MAX\_MULT\_NOMREG}$	Two register multiply without MREG	412.20	360.75	303.77	303.77	360.75	248.32	MHz
$F_{MAX\_MULT\_NOMREG\_PATDET}$	Two register multiply without MREG with pattern detect	374.25	327.65	276.01	276.01	327.65	225.73	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG}$	Without ADREG	468.82	408.66	342.70	342.70	408.66	263.44	MHz
$F_{MAX\_PREADD\_MULT\_NOADREG\_PATDET}$	Without ADREG with pattern detect	468.82	408.66	342.70	342.70	408.66	263.44	MHz

Table 35: **DSP48E1 Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
$F_{MAX\_NOPIPELINEREG}$	Without pipeline registers (MREG, ADREG)	306.84	267.81	225.02	225.02	267.81	177.15	MHz
$F_{MAX\_NOPIPELINEREG\_PATDET}$	Without pipeline registers (MREG, ADREG) with pattern detect	285.23	249.13	209.38	209.38	249.13	165.32	MHz

Clock Buffers and Networks

Table 36: **Global Clock Switching Characteristics (Including BUFGCTRL)**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
T_{BCCCK_CE}/ T_{BCCKC_CE}(1)	CE pins Setup/Hold	0.12/0.30	0.14/0.38	0.26/0.38	0.26/0.92	0.14/0.38	0.23/0.40	ns
T_{BCCCK_S}/ T_{BCCKC_S}(1)	S pins Setup/Hold	0.12/0.30	0.14/0.38	0.26/0.38	0.26/0.92	0.14/0.38	0.23/0.40	ns
T_{BCCKO_O}(2)	BUFGCTRL delay from I0/I1 to O	0.08	0.10	0.12	0.12	0.10	0.10	ns
Maximum Frequency								
F_{MAX_BUFG}	Global clock tree (BUFG)	741.00	710.00	625.00	625.00	710.00	560.00	MHz

Notes:

1. T_{BCCCK_CE} and T_{BCCKC_CE} must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T_{BGCKO_O} (BUFG delay from I0 to O) values are the same as T_{BCCKO_O} values.

Table 37: **Input/Output Clock Switching Characteristics (BUFIO)**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
T_{BIOCKO_O}	Clock to out delay from I to O	1.04	1.14	1.32	1.32	1.14	1.48	ns
Maximum Frequency								
F_{MAX_BUFIO}	I/O clock tree (BUFIO)	800.00	800.00	710.00	710.00	800.00	710.00	MHz

Table 38: **Regional Clock Buffer Switching Characteristics (BUFR)**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
T_{BRCKO_O}	Clock to out delay from I to O	0.60	0.65	0.77	0.77	0.65	1.06	ns
$T_{BRCKO\_O\_BYP}$	Clock to out delay from I to O with Divide Bypass attribute set	0.30	0.32	0.38	0.38	0.32	0.57	ns
T_{BRDO_O}	Propagation delay from CLR to O	0.71	0.75	0.96	0.96	0.75	0.93	ns

Table 38: **Regional Clock Buffer Switching Characteristics (BUFR) *(Cont'd)***

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
Maximum Frequency								
F_{MAX_BUFR}[1]	Regional clock tree (BUFR)	600.00	540.00	450.00	450.00	540.00	450.00	MHz

Notes:

1. The maximum input frequency to the BUFR and BUFMR is the BUFIO F_{MAX} frequency.

Table 39: **Horizontal Clock Buffer Switching Characteristics (BUFH)**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
T_{BHCKO_O}	BUFH delay from I to O	0.10	0.11	0.13	0.13	0.11	0.12	ns
T_{BHCCK_CE}/ T_{BHCKC_CE}	CE pin Setup and Hold	0.20/0.16	0.23/0.20	0.38/0.21	0.38/0.79	0.23/0.20	0.28/0.09	ns
Maximum Frequency								
F_{MAX_BUFH}	Horizontal clock buffer (BUFH)	741.00	710.00	625.00	625.00	710.00	560.00	MHz

Table 40: **Duty Cycle Distortion and Clock-Tree Skew**

Symbol	Description	Device	Speed Grade						Units
			1.0V				0.95V	0.9V	
			-3	-2/-2LE	-1	-1M	-2LI	-2LE	
T_{DCD_CLK}	Global Clock Tree Duty Cycle Distortion[1]	All	0.20	0.20	0.20	0.20	All	0.25	ns
T_{CKSKEW}	Global Clock Tree Skew[2]	XC7K70T	0.29	0.40	0.40	N/A	N/A	0.47	ns
		XC7K160T	0.42	0.53	0.57	N/A	0.53	0.59	ns
		XC7K325T	0.59	0.74	0.79	N/A	0.74	0.91	ns
		XC7K355T	0.45	0.57	0.59	N/A	0.57	0.69	ns
		XC7K410T	0.60	0.74	0.79	N/A	0.74	0.91	ns
		XC7K420T	0.60	0.74	0.79	N/A	0.74	0.91	ns
		XC7K480T	0.60	0.74	0.79	N/A	0.74	0.91	ns
		XQ7K325T	N/A	0.74	0.79	0.79	N/A	0.91	ns
		XQ7K410T	N/A	0.74	0.79	0.79	N/A	0.91	ns
T_{DCD_BUFIO}	I/O clock tree duty cycle distortion	All	0.12	0.12	0.12	0.12	0.12	0.12	ns
$T_{BUFIOSKEW}$	I/O clock tree skew across one clock region	All	0.02	0.02	0.02	0.02	0.02	0.03	ns
T_{DCD_BUFR}	Regional clock tree duty cycle distortion	All	0.15	0.15	0.15	0.15	0.15	0.15	ns

Notes:

1. These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate clock skew specific to your application.

MMCM Switching Characteristics

Table 41: **MMCM Specification**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
MMCM_F_{INMAX}	Maximum Input Clock Frequency	1066.00	933.00	800.00	800.00	933.00	800.00	MHz
MMCM_F_{INMIN}	Minimum Input Clock Frequency	10.00	10.00	10.00	10.00	10.00	10.00	MHz
MMCM_$F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max						
MMCM_F_{INDUTY}	Allowable Input Duty Cycle: 10–49 MHz	25.00	25.00	25.00	25.00	25.00	25.00	%
	Allowable Input Duty Cycle: 50–199 MHz	30.00	30.00	30.00	30.00	30.00	30.00	%
	Allowable Input Duty Cycle: 200–399 MHz	35.00	35.00	35.00	35.00	35.00	35.00	%
	Allowable Input Duty Cycle: 400–499 MHz	40.00	40.00	40.00	40.00	40.00	40.00	%
	Allowable Input Duty Cycle: >500 MHz	45.00	45.00	45.00	45.00	45.00	45.00	%
MMCM_F_{MIN_PSCLK}	Minimum Dynamic Phase Shift Clock Frequency	0.01	0.01	0.01	0.01	0.01	0.01	MHz
MMCM_F_{MAX_PSCLK}	Maximum Dynamic Phase Shift Clock Frequency	550.00	500.00	450.00	450.00	500.00	450.00	MHz
MMCM_F_{VCOMIN}	Minimum MMCM VCO Frequency	600.00	600.00	600.00	600.00	600.00	600.00	MHz
MMCM_F_{VCOMAX}	Maximum MMCM VCO Frequency	1600.00	1440.00	1200.00	1200.00	1440.00	1200.00	MHz
MMCM_$F_{BANDWIDTH}$	Low MMCM Bandwidth at Typical(1)	1.00	1.00	1.00	1.00	1.00	1.00	MHz
	High MMCM Bandwidth at Typical(1)	4.00	4.00	4.00	4.00	4.00	4.00	MHz
MMCM_$T_{STATPHAOFFSET}$	Static Phase Offset of the MMCM Outputs(2)	0.12	0.12	0.12	0.12	0.12	0.12	ns
MMCM_$T_{OUTJITTER}$	MMCM Output Jitter	Note 3						
MMCM_$T_{OUTDUTY}$	MMCM Output Clock Duty Cycle Precision(4)	0.20	0.20	0.20	0.20	0.20	0.25	ns
MMCM_$T_{LOCKMAX}$	MMCM Maximum Lock Time	100.00	100.00	100.00	100.00	100.00	100.00	µs
MMCM_F_{OUTMAX}	MMCM Maximum Output Frequency	1066.00	933.00	800.00	800.00	933.00	800.00	MHz
MMCM_F_{OUTMIN}	MMCM Minimum Output Frequency(5)(6)	4.69	4.69	4.69	4.69	4.69	4.69	MHz
MMCM_$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max						
MMCM_$RST_{MINPULSE}$	Minimum Reset Pulse Width	5.00	5.00	5.00	5.00	5.00	5.00	ns
MMCM_F_{PFDMAX}	Maximum Frequency at the Phase Frequency Detector	550.00	500.00	450.00	450.00	500.00	450.00	MHz
MMCM_F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	10.00	10.00	10.00	10.00	10.00	10.00	MHz

Table 41: **MMCM Specification *(Cont'd)***

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
MMCM_$T_{FBDELAY}$	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle						
MMCM Switching Characteristics Setup and Hold								
$T_{MMCMDCK\_PSEN}$/ $T_{MMCMCKD\_PSEN}$	Setup and Hold of Phase Shift Enable	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	ns
$T_{MMCMDCK\_PSINCDEC}$/ $T_{MMCMCKD\_PSINCDEC}$	Setup and Hold of Phase Shift Increment/Decrement	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	1.04/0.00	ns
$T_{MMCMCKO\_PSDONE}$	Phase Shift Clock-to-Out of PSDONE	0.59	0.68	0.81	0.81	0.68	0.78	ns
Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK								
$T_{MMCMDCK\_DADDR}$/ $T_{MMCMCKD\_DADDR}$	DADDR Setup/Hold	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	1.40/0.15	1.43/0.00	ns, Min
$T_{MMCMDCK\_DI}$/ $T_{MMCMCKD\_DI}$	DI Setup/Hold	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	1.40/0.15	1.43/0.00	ns, Min
$T_{MMCMDCK\_DEN}$/ $T_{MMCMCKD\_DEN}$	DEN Setup/Hold	1.76/0.00	1.97/0.00	2.29/0.00	2.29/0.00	1.97/0.00	2.40/0.00	ns, Min
$T_{MMCMDCK\_DWE}$/ $T_{MMCMCKD\_DWE}$	DWE Setup/Hold	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	1.40/0.15	1.43/0.00	ns, Min
$T_{MMCMCKO\_DRDY}$	CLK to out of DRDY	0.65	0.72	0.99	0.99	0.72	0.70	ns, Max
F_{DCK}	DCLK frequency	200.00	200.00	200.00	200.00	200.00	100.00	MHz, Max

Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_F_{OUTMIN} is 0.036 MHz.

PLL Switching Characteristics

Table 42: **PLL Specification**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
PLL_F_{INMAX}	Maximum Input Clock Frequency	1066.00	933.00	800.00	800.00	933.00	800.00	MHz
PLL_F_{INMIN}	Minimum Input Clock Frequency	19.00	19.00	19.00	19.00	19.00	19.00	MHz
PLL_$F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max						
PLL_F_{INDUTY}	Allowable Input Duty Cycle: 19–49 MHz	25.00	25.00	25.00	25.00	25.00	25.00	%
	Allowable Input Duty Cycle: 50–199 MHz	30.00	30.00	30.00	30.00	30.00	30.00	%
	Allowable Input Duty Cycle: 200–399 MHz	35.00	35.00	35.00	35.00	35.00	35.00	%
	Allowable Input Duty Cycle: 400–499 MHz	40.00	40.00	40.00	40.00	40.00	40.00	%
	Allowable Input Duty Cycle: >500 MHz	45.00	45.00	45.00	45.00	45.00	45.00	%
PLL_F_{VCOMIN}	Minimum PLL VCO Frequency	800.00	800.00	800.00	800.00	800.00	800.00	MHz
PLL_F_{VCOMAX}	Maximum PLL VCO Frequency	2133.00	1866.00	1600.00	1600.00	1866.00	1600.00	MHz
PLL_$F_{BANDWIDTH}$	Low PLL Bandwidth at Typical(1)	1.00	1.00	1.00	1.00	1.00	1.00	MHz
	High PLL Bandwidth at Typical(1)	4.00	4.00	4.00	4.00	4.00	4.00	MHz
PLL_$T_{STATPHAOFFSET}$	Static Phase Offset of the PLL Outputs(2)	0.12	0.12	0.12	0.12	0.12	0.12	ns
PLL_$T_{OUTJITTER}$	PLL Output Jitter	Note 3						
PLL_$T_{OUTDUTY}$	PLL Output Clock Duty Cycle Precision(4)	0.20	0.20	0.20	0.20	0.20	0.25	ns
PLL_$T_{LOCKMAX}$	PLL Maximum Lock Time	100	100	100	100	100	100	µs
PLL_F_{OUTMAX}	PLL Maximum Output Frequency	1066.00	933.00	800.00	800.00	933.00	800.00	MHz
PLL_F_{OUTMIN}	PLL Minimum Output Frequency(5)	6.25	6.25	6.25	6.25	6.25	6.25	MHz
PLL_$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max						
PLL_$RST_{MINPULSE}$	Minimum Reset Pulse Width	5.00	5.00	5.00	5.00	5.00	5.00	ns
PLL_F_{PFDMAX}	Maximum Frequency at the Phase Frequency Detector	550.00	500.00	450.00	450.00	500.00	450.00	MHz
PLL_F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	19.00	19.00	19.00	19.00	19.00	19.00	MHz
PLL_$T_{FBDELAY}$	Maximum Delay in the Feedback Path	3 ns Max or one CLKIN cycle						
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK								
T_{PLLCCK_DADDR}/ T_{PLLCKC_DADDR}	Setup and hold of D address	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	1.40/0.15	1.43/0.00	ns, Min
T_{PLLCCK_DI}/ T_{PLLCKC_DI}	Setup and hold of D input	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	1.40/0.15	1.43/0.00	ns, Min
T_{PLLCCK_DEN}/ T_{PLLCKC_DEN}	Setup and hold of D enable	1.76/0.00	1.97/0.00	2.29/0.00	2.29/0.00	1.97/0.00	2.40/0.00	ns, Min

Table 42: **PLL Specification *(Cont'd)***

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
T_{PLLCCK_DWE}/ T_{PLLCKC_DWE}	Setup and hold of D write enable	1.25/0.15	1.40/0.15	1.63/0.15	1.63/0.15	1.40/0.15	1.43/0.00	ns, Min
T_{PLLCKO_DRDY}	CLK to out of DRDY	0.65	0.72	0.99	0.99	0.72	0.70	ns, Max
F_{DCK}	DCLK frequency	200.00	200.00	200.00	200.00	200.00	100.00	MHz, Max

Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as F_{VCO}/128 assuming output duty cycle is 50%.

Device Pin-to-Pin Output Parameter Guidelines

Table 43: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)**

Symbol	Description	Device	Speed Grade						Units
			1.0V				0.95V	0.9V	
			-3	-2/-2LE	-1	-1M	-2LI	-2LE	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.									
T_{ICKOF}	Clock-capable clock input and OUTFF at pins/banks closest to the BUFGs *without* MMCM/PLL (near clock region)	XC7K70T	4.98	5.49	6.17	N/A	N/A	7.04	ns
		XC7K160T	5.23	5.77	6.48	N/A	5.77	7.38	ns
		XC7K325T	5.72	6.31	7.09	N/A	6.31	8.07	ns
		XC7K355T	5.34	5.87	6.57	N/A	5.87	7.51	ns
		XC7K410T	5.84	6.44	7.22	N/A	6.44	8.21	ns
		XC7K420T	5.50	6.04	6.77	N/A	6.04	7.73	ns
		XC7K480T	5.50	6.04	6.77	N/A	6.04	7.73	ns
		XQ7K325T	N/A	6.31	7.09	7.09	N/A	8.07	ns
		XQ7K410T	N/A	6.44	7.22	7.22	N/A	8.21	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the Die Level Bank Numbering Overview section of the *7 Series FPGA Packaging and Pinout Specification* (UG475).

Table 44: **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)**

Symbol	Description	Device	Speed Grade						Units
			1.0V				0.95V	0.9V	
			-3	-2/-2LE	-1	-1M	-2LI	-2LE	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL.									
$T_{ICKOFFAR}$	Clock-capable clock input and OUTFF at pins/banks farthest from the BUFGs *without* MMCM/PLL (far clock region)	XC7K70T	5.29	5.83	6.55	N/A	N/A	7.47	ns
		XC7K160T	5.84	6.45	7.24	N/A	6.45	8.24	ns
		XC7K325T	6.33	6.99	7.84	N/A	6.99	8.92	ns
		XC7K355T	5.95	6.55	7.32	N/A	6.55	8.36	ns
		XC7K410T	6.45	7.12	7.97	N/A	7.12	9.07	ns
		XC7K420T	6.41	7.06	7.90	N/A	7.06	9.01	ns
		XC7K480T	6.41	7.06	7.90	N/A	7.06	9.01	ns
		XQ7K325T	N/A	6.99	7.84	7.84	N/A	8.92	ns
		XQ7K410T	N/A	7.12	7.97	7.97	N/A	9.07	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the Die Level Bank Numbering Overview section of the *7 Series FPGA Packaging and Pinout Specification* (UG475).

Table 45: **Clock-Capable Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grade						Units
			1.0V				0.95V	0.9V	
			-3	-2/-2LE	-1	-1M	-2LI	-2LE	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* MMCM.									
$T_{ICKOFMMCMCC}$	Clock-capable clock input and OUTFF *with* MMCM	XC7K70T	0.95	0.95	0.95	N/A	N/A	1.74	ns
		XC7K160T	0.96	0.96	0.96	N/A	0.96	1.78	ns
		XC7K325T	1.00	1.00	1.00	N/A	1.00	1.82	ns
		XC7K355T	1.00	1.00	1.00	N/A	1.00	1.78	ns
		XC7K410T	1.00	1.00	1.00	N/A	1.00	1.82	ns
		XC7K420T	1.07	1.07	1.07	N/A	1.07	1.82	ns
		XC7K480T	1.07	1.07	1.07	N/A	1.07	1.82	ns
		XQ7K325T	N/A	1.00	1.00	1.00	N/A	1.82	ns
		XQ7K410T	N/A	1.00	1.00	1.00	N/A	1.82	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 46: **Clock-Capable Clock Input to Output Delay With PLL**

Symbol	Description	Device	Speed Grade						Units
			1.0V				0.95V	0.9V	
			-3	-2/-2LE	-1	-1M	-2LI	-2LE	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* PLL.									
$T_{ICKOFPLLCC}$	Clock-capable clock input and OUTFF *with* PLL	XC7K70T	0.84	0.84	0.84	N/A	N/A	1.45	ns
		XC7K160T	0.89	0.89	0.89	N/A	0.89	1.54	ns
		XC7K325T	0.89	0.89	0.89	N/A	0.89	1.54	ns
		XC7K355T	0.89	0.89	0.89	N/A	0.89	1.50	ns
		XC7K410T	0.89	0.89	0.89	N/A	0.89	1.54	ns
		XC7K420T	0.96	0.96	0.96	N/A	0.96	1.54	ns
		XC7K480T	0.96	0.96	0.96	N/A	0.96	1.54	ns
		XQ7K325T	N/A	0.89	0.89	0.89	N/A	1.54	ns
		XQ7K410T	N/A	0.89	0.89	0.89	N/A	1.54	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 47: **Pin-to-Pin, Clock-to-Out using BUFIO**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* BUFIO.								
$T_{ICKOFCS}$	Clock-to-Out of I/O clock for HR I/O banks	4.93	5.52	6.20	6.20	5.52	6.97	ns
	Clock-to-Out of I/O clock for HP I/O banks	4.85	5.44	6.11	6.11	5.44	6.90	ns

Device Pin-to-Pin Input Parameter Guidelines

Table 48: **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

Symbol	Description	Device	Speed Grade						Units
			1.0V				0.95V	0.9V	
			-3	-2/-2LE	-1	-1M	-2LI	-2LE	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)									
T_{PSFD}/T_{PHFD}	Full Delay (Legacy Delay or Default Delay) Global Clock Input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks	XC7K70T	2.83/–0.29	2.95/–0.29	3.15/–0.29	N/A	N/A	4.96/–0.33	ns
		XC7K160T	3.17/–0.35	3.29/–0.35	3.55/–0.35	N/A	3.29/–0.35	5.54/–0.49	ns
		XC7K325T	2.83/–0.06	2.94/–0.06	3.15/–0.06	N/A	2.94/–0.06	5.18/–0.14	ns
		XC7K355T	3.26/–0.32	3.41/–0.32	3.67/–0.32	N/A	3.41/–0.32	5.84/–0.49	ns
		XC7K410T	3.43/–0.34	3.59/–0.34	3.88/–0.34	N/A	3.59/–0.34	6.21/–0.54	ns
		XC7K420T	3.37/–0.27	3.48/–0.27	3.76/–0.27	N/A	3.48/–0.27	6.00/–0.52	ns
		XC7K480T	3.37/–0.27	3.48/–0.27	3.76/–0.27	N/A	3.48/–0.27	6.00/–0.52	ns
		XQ7K325T	N/A	2.94/–0.06	3.15/–0.06	3.15/–0.06	N/A	5.18/–0.14	ns
		XQ7K410T	N/A	3.59/–0.34	3.88/–0.34	3.88/–0.34	N/A	6.21/–0.54	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.

Table 49: **Clock-Capable Clock Input Setup and Hold With MMCM**

Symbol	Description	Device	Speed Grade						Units
			1.0V				0.95V	0.9V	
			-3	-2/-2LE	-1	-1M	-2LI	-2LE	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1)									
$T_{PSMMCMCC}/T_{PHMMCMCC}$	No Delay clock-capable clock input and IFF(2) with MMCM	XC7K70T	2.39/–0.22	2.65/–0.22	2.94/–0.22	N/A	N/A	2.21/–0.44	ns
		XC7K160T	2.49/–0.20	2.77/–0.20	3.07/–0.20	N/A	2.77/–0.20	2.38/–0.47	ns
		XC7K325T	2.55/–0.16	2.85/–0.16	3.14/–0.16	N/A	2.85/–0.16	2.60/–0.47	ns
		XC7K355T	2.43/–0.16	2.73/–0.16	3.00/–0.16	N/A	2.73/–0.16	2.47/–0.43	ns
		XC7K410T	2.55/–0.16	2.84/–0.16	3.14/–0.16	N/A	2.84/–0.16	2.58/–0.47	ns
		XC7K420T	2.47/–0.09	2.73/–0.09	3.02/–0.09	N/A	2.73/–0.09	2.40/–0.41	ns
		XC7K480T	2.47/–0.09	2.73/–0.09	3.02/–0.09	N/A	2.73/–0.09	2.40/–0.41	ns
		XQ7K325T	N/A	2.85/–0.16	3.14/–0.16	3.14/–0.16	N/A	2.60/–0.47	ns
		XQ7K410T	N/A	2.84/–0.16	3.14/–0.16	3.14/–0.16	N/A	2.58/–0.47	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 50: **Clock-Capable Clock Input Setup and Hold With PLL**

Symbol	Description	Device	Speed Grade						Units
			1.0V				0.95V	0.9V	
			-3	-2/-2LE	-1	-1M	-2LI	-2LE	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1)									
$T_{PSPLLCC}$/ $T_{PHPLLCC}$	No Delay clock-capable clock input and IFF(2) with PLL	XC7K70T	2.75/–0.32	3.04/–0.32	3.33/–0.32	N/A	N/A	2.42/–0.54	ns
		XC7K160T	2.85/–0.31	3.16/–0.31	3.46/–0.31	N/A	3.16/–0.31	2.59/–0.56	ns
		XC7K325T	2.91/–0.27	3.24/–0.27	3.54/–0.27	N/A	3.24/–0.27	2.80/–0.56	ns
		XC7K355T	2.79/–0.27	3.12/–0.27	3.40/–0.27	N/A	3.12/–0.27	2.67/–0.52	ns
		XC7K410T	2.91/–0.27	3.24/–0.27	3.53/–0.27	N/A	3.24/–0.27	2.78/–0.56	ns
		XC7K420T	2.83/–0.20	3.12/–0.20	3.41/–0.20	N/A	3.12/–0.20	2.61/–0.50	ns
		XC7K480T	2.83/–0.20	3.12/–0.20	3.41/–0.20	N/A	3.12/–0.20	2.61/–0.50	ns
		XQ7K325T	N/A	3.24/–0.27	3.54/–0.27	3.54/–0.27	N/A	2.80/–0.56	ns
		XQ7K410T	N/A	3.24/–0.27	3.53/–0.27	3.53/–0.27	N/A	2.78/–0.56	ns

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 51: **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.								
T_{PSCS}/T_{PHCS}	Setup/Hold of I/O clock for HR I/O banks	–0.36/1.36	–0.36/1.50	–0.36/1.70	–0.36/1.70	–0.36/1.50	–0.44/1.87	ns
	Setup/Hold of I/O clock for HP I/O banks	–0.34/1.39	–0.34/1.53	–0.34/1.73	–0.34/1.73	–0.34/1.53	–0.44/1.87	ns

Table 52: **Sample Window**

Symbol	Description	Speed Grade						Units
		1.0V				0.95V	0.9V	
		-3	-2/-2LE	-1	-1M	-2LI	-2LE	
T_{SAMP}	Sampling Error at Receiver Pins(1)	0.51	0.56	0.61	0.61	0.56	0.56	ns
T_{SAMP_BUFIO}	Sampling Error at Receiver Pins using BUFIO(2)	0.30	0.35	0.40	0.40	0.35	0.35	ns

Notes:

1. This parameter indicates the total sampling error of the Kintex-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Kintex-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Kintex-7 FPGA clock transmitter and receiver data-valid windows.

Table 53: **Package Skew**

Symbol	Description	Device	Package	Value	Units
$T_{PKGSKEW}$	Package Skew(1)	XC7K70T	FBG484	108	ps
			FBG676	135	ps
		XC7K160T	FBG484	118	ps
			FBG676	136	ps
			FFG676	161	ps
		XC7K325T	FBG676	146	ps
			FFG676	154	ps
			FBG900	163	ps
			FFG900	161	ps
		XC7K355T	FFG901	149	ps
		XC7K410T	FBG676	165	ps
			FFG676	168	ps
			FBG900	151	ps
			FFG900	146	ps
		XC7K420T	FFG901	149	ps
			FFG1156	145	ps
		XC7K480T	FFG901	149	ps
			FFG1156	145	ps
		XQ7K325T	RF676	154	ps
			RF900	161	ps
		XQ7K410T	RF676	168	ps
			RF900	146	ps

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

GTX Transceiver Specifications

GTX Transceiver DC Input and Output Levels

Table 54 summarizes the DC output specifications of the GTX transceivers in Kintex-7 FPGAs. Consult the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) for further details.

Table 54: **GTX Transceiver DC Specifications**

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
DV_{PPOUT}	Differential peak-to-peak output voltage(1)	Transmitter output swing is set to maximum setting	1000	–	–	mV
$V_{CMOUTDC}$	DC common mode output voltage.	Equation based	$V_{MGTAVTT} - DV_{PPOUT}/4$			mV
R_{OUT}	Differential output resistance		–	100	–	Ω
T_{OSKEW}	Transmitter output pair (TXP and TXN) intra-pair skew		–	2	12	ps
DV_{PPIN}	Differential peak-to-peak input voltage (external AC coupled)	>10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V_{IN}	Single-ended input voltage(2)	DC coupled $V_{MGTAVTT}$ = 1.2V	–200	–	$V_{MGTAVTT}$	mV
V_{CMIN}	Common mode input voltage	DC coupled $V_{MGTAVTT}$ = 1.2V	–	2/3 $V_{MGTAVTT}$	–	mV
R_{IN}	Differential input resistance		–	100	–	Ω
C_{EXT}	Recommended external AC coupling capacitor(3)		–	100	–	nF

Notes:

1. The output swing and preemphasis levels are programmable using the attributes discussed in the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) and can result in values lower than reported in this table.
2. Voltage measured at the pin referenced to ground.
3. Other values can be used as appropriate to conform to specific protocols and standards.

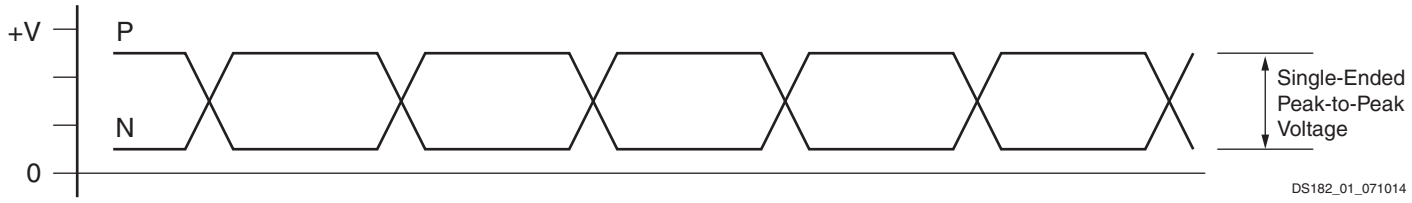


Figure 3: **Single-Ended Peak-to-Peak Voltage**

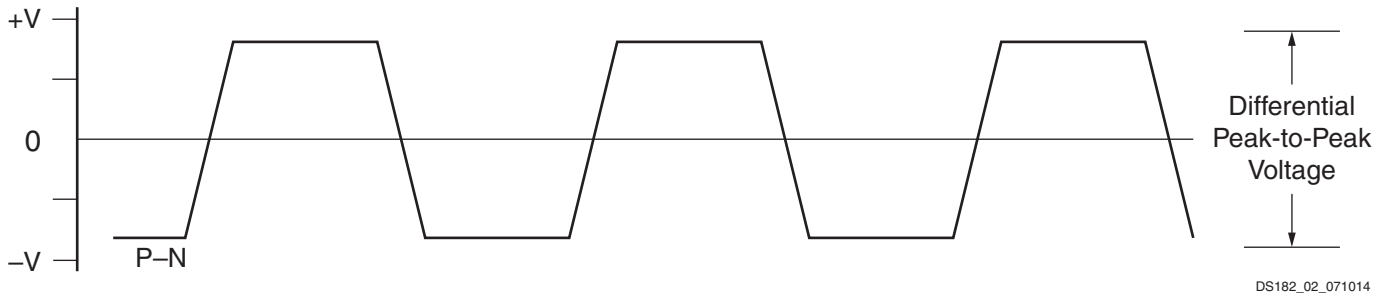


Figure 4: **Differential Peak-to-Peak Voltage**

Note: In Figure 4, differential peak-to-peak voltage = single-ended peak-to-peak voltage x 2.

Table 55 summarizes the DC specifications of the clock input of the GTX transceiver. Consult the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) for further details.

Table 55: **GTX Transceiver Clock DC Input Level Specification**

Symbol	DC Parameter	Min	Typ	Max	Units
V_{IDIFF}	Differential peak-to-peak input voltage	250	–	2000	mV
R_{IN}	Differential input resistance	–	100	–	Ω
C_{EXT}	Required external AC coupling capacitor	–	100	–	nF

GTX Transceiver Switching Characteristics

Consult the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) for further information.

Table 56: **GTX Transceiver Performance**

Symbol	Description	Output Divider	Speed Grade								Units
			-3 (1.0V)		-2 (1.0V) -2LE (1.0V) -2LI (0.95V)		-1 (1.0V)(1) -1M (1.0V)(1)		-2LE (0.9V)(2)		
			Package Type								
			FF	FB	FF RF	FB	FF RF	FB	FF RF	FB	
F_{GTXMAX}(3)	Maximum GTX transceiver data rate		12.5	6.6	10.3125	6.6	8.0	6.6	6.6	6.6	Gb/s
F_{GTXMIN}(3)	Minimum GTX transceiver data rate		0.500	0.500	0.500	0.500	0.500	0.500	0.500	0.500	Gb/s
$F_{GTXCRANGE}$	CPLL line rate range	1	3.2–6.6								Gb/s
		2	1.6–3.3								Gb/s
		4	0.8–1.65								Gb/s
		8	0.5–0.825								Gb/s
		16	N/A								Gb/s
$F_{GTXQRANGE1}$	QPLL line rate range 1	1	5.93–8.0	5.93–6.6	5.93–8.0	5.93–6.6	5.93–8.0	5.93–6.6	5.93–6.6		Gb/s
		2	2.965–4.0		2.965–4.0		2.965–4.0		2.965–3.3		Gb/s
		4	1.4825–2.0		1.4825–2.0		1.4825–2.0		1.4825–1.65		Gb/s
		8	0.74125–1.0		0.74125–1.0		0.74125–1.0		0.74125–0.825		Gb/s
		16	N/A		N/A		N/A		N/A		Gb/s
$F_{GTXQRANGE2}$	QPLL line rate range 2(4)	1	9.8–12.5	N/A	9.8–10.3125	N/A	N/A		N/A		Gb/s
		2	4.9–6.25		4.9–5.15625		N/A		N/A		Gb/s
		4	2.45–3.125		2.45–2.578125		N/A		N/A		Gb/s
		8	1.225–1.5625		1.225–1.2890625		N/A		N/A		Gb/s
		16	0.6125–0.78125		0.6125–0.64453125		N/A		N/A		Gb/s
$F_{GCPLLRANGE}$	GTX transceiver CPLL frequency range		1.6–3.3		1.6–3.3		1.6–3.3		1.6–3.3		GHz
$F_{GQPLLRANGE1}$	GTX transceiver QPLL frequency range 1		5.93–8.0		5.93–8.0		5.93–8.0		5.93–6.6		GHz

Table 56: **GTX Transceiver Performance *(Cont'd)***

Symbol	Description	Output Divider	Speed Grade								Units
			-3 (1.0V)		-2 (1.0V) -2LE (1.0V) -2LI (0.95V)		-1 (1.0V)(1) -1M (1.0V)(1)		-2LE (0.9V)(2)		
			Package Type								
			FF	FB	FF RF	FB	FF RF	FB	FF RF	FB	
$F_{GQPLLRANGE2}$	GTX transceiver QPLL frequency range 2		9.8–12.5		9.8–10.3125		N/A		N/A		GHz

Notes:

1. The -1 speed grade requires a 4-byte internal data width for operation above 5.0 Gb/s.
2. The -2LE (0.9V) speed grade requires a 4-byte internal data width for operation above 3.8 Gb/s.
3. Data rates between 8.0 Gb/s and 9.8 Gb/s are not available.
4. For QPLL line rate range 2, the maximum line rate with the divider N set to 66 is 10.3125Gb/s.

Table 57: **GTX Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

Symbol	Description	Speed Grade					Units
		1.0V			0.95V	0.9V	
		-3	-2/-2LE	-1/-1M	-2LI	-2LE	
$F_{GTXDRPCLK}$	GTXDRPCLK maximum frequency	175.01	175.01	156.25	175.01	125.00	MHz

Table 58: **GTX Transceiver Reference Clock Switching Characteristics**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
F_{GCLK}	Reference clock frequency range	-3 speed grade	60	–	700	MHz
		All other speed grades	60	–	670	MHz
T_{RCLK}	Reference clock rise time	20% – 80%	–	200	–	ps
T_{FCLK}	Reference clock fall time	80% – 20%	–	200	–	ps
T_{DCREF}	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

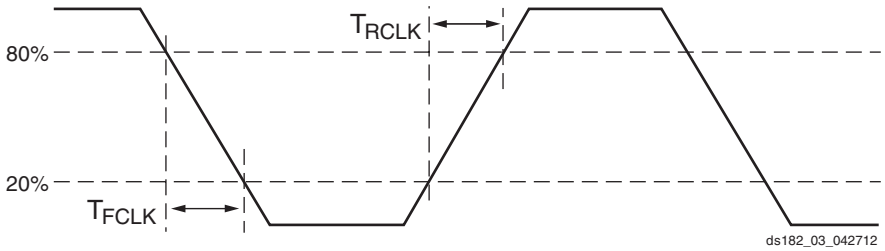


Figure 5: **Reference Clock Timing Parameters**

Table 59: **GTX Transceiver PLL /Lock Time Adaptation**

Symbol	Description	Conditions	All Speed Grades			Units
			Min	Typ	Max	
T_{LOCK}	Initial PLL lock		–	–	1	ms
T_{DLOCK}	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37 x10^6	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3 x10^6	UI

Table 60: **GTX Transceiver User Clock Switching Characteristics(1)(2)**

Symbol	Description	Conditions	Speed Grade					Units
			1.0V			0.95V	0.9V	
			-3(3)	-2/-2LE(3)	-1/-1M(4)	-2LI	-2LE(5)	
F_{TXOUT}	TXOUTCLK maximum frequency		412.500	412.500	312.500	412.500	237.500	MHz
F_{RXOUT}	RXOUTCLK maximum frequency		412.500	412.500	312.500	412.500	237.500	MHz
F_{TXIN}	TXUSRCLK maximum frequency	16-bit data path	412.500	412.500	312.500	412.500	237.500	MHz
		32-bit data path	390.625	322.266	250.000	322.266	206.250	MHz
F_{RXIN}	RXUSRCLK maximum frequency	16-bit data path	412.500	412.500	312.500	412.500	237.500	MHz
		32-bit data path	390.625	322.266	250.000	322.266	206.250	MHz
F_{TXIN2}	TXUSRCLK2 maximum frequency	16-bit data path	412.500	412.500	312.500	412.500	237.500	MHz
		32-bit data path	390.625	322.266	250.000	322.266	206.250	MHz
		64-bit data path	195.313	161.133	125.000	161.133	103.125	MHz
F_{RXIN2}	RXUSRCLK2 maximum frequency	16-bit data path	412.500	412.500	312.500	412.500	237.500	MHz
		32-bit data path	390.625	322.266	250.000	322.266	206.250	MHz
		64-bit data path	195.313	161.133	125.000	161.133	103.125	MHz

Notes:

1. Clocking must be implemented as described in the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476).
2. These frequencies are not supported for all possible transceiver configurations.
3. For speed grades -3, -2, -2LE (1.0V), -2LI (0.95V), a 16-bit data path can only be used for speeds less than 6.6 Gb/s.
4. For speed grade -1, a 16-bit data path can only be used for speeds less than 5.0 Gb/s.
5. For speed grade -2LE (0.9V), a 16-bit data path can only be used for speeds less than 3.8 Gb/s.

Table 61: **GTX Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F_{GTXTX}	Serial data rate range		0.500	–	F_{GTXMAX}	Gb/s
T_{RTX}	TX Rise time	20%–80%	–	40	–	ps
T_{FTX}	TX Fall time	80%–20%	–	40	–	ps
T_{LLSKEW}	TX lane-to-lane skew(1)		–	–	500	ps
$V_{TXOOBVDPP}$	Electrical idle amplitude		–	–	15	mV
$T_{TXOOBTRANSITION}$	Electrical idle transition time		–	–	140	ns
$TJ_{12.5}$	Total Jitter(2)(4)	12.5 Gb/s	–	–	0.28	UI
$DJ_{12.5}$	Deterministic Jitter(2)(4)		–	–	0.17	UI
$TJ_{11.18}$	Total Jitter(2)(4)	11.18 Gb/s	–	–	0.28	UI
$DJ_{11.18}$	Deterministic Jitter(2)(4)		–	–	0.17	UI

Table 61: **GTX Transceiver Transmitter Switching Characteristics *(Cont'd)***

Symbol	Description	Condition	Min	Typ	Max	Units
$TJ_{10.3125}$	Total Jitter(2)(4)	10.3125 Gb/s	–	–	0.28	UI
$DJ_{10.3125}$	Deterministic Jitter(2)(4)		–	–	0.17	UI
$TJ_{9.953}$	Total Jitter(2)(4)	9.953 Gb/s	–	–	0.28	UI
$DJ_{9.953}$	Deterministic Jitter(2)(4)		–	–	0.17	UI
$TJ_{9.8}$	Total Jitter(2)(4)	9.8 Gb/s	–	–	0.28	UI
$DJ_{9.8}$	Deterministic Jitter(2)(4)		–	–	0.17	UI
$TJ_{8.0}$	Total Jitter(2)(4)	8.0 Gb/s	–	–	0.30	UI
$DJ_{8.0}$	Deterministic Jitter(2)(4)		–	–	0.15	UI
$TJ_{6.6\_QPLL}$	Total Jitter(2)(4)	6.6 Gb/s	–	–	0.28	UI
$DJ_{6.6\_QPLL}$	Deterministic Jitter(2)(4)		–	–	0.17	UI
$TJ_{6.6\_CPLL}$	Total Jitter(3)(4)	6.6 Gb/s	–	–	0.30	UI
$DJ_{6.6\_CPLL}$	Deterministic Jitter(3)(4)		–	–	0.15	UI
$TJ_{5.0}$	Total Jitter(3)(4)	5.0 Gb/s	–	–	0.30	UI
$DJ_{5.0}$	Deterministic Jitter(3)(4)		–	–	0.15	UI
$TJ_{4.25}$	Total Jitter(3)(4)	4.25 Gb/s	–	–	0.30	UI
$DJ_{4.25}$	Deterministic Jitter(3)(4)		–	–	0.15	UI
$TJ_{3.75}$	Total Jitter(3)(4)	3.75 Gb/s	–	–	0.30	UI
$DJ_{3.75}$	Deterministic Jitter(3)(4)		–	–	0.15	UI
$TJ_{3.2}$	Total Jitter(3)(4)	3.20 Gb/s(5)	–	–	0.2	UI
$DJ_{3.2}$	Deterministic Jitter(3)(4)		–	–	0.1	UI
$TJ_{3.2L}$	Total Jitter(3)(4)	3.20 Gb/s(6)	–	–	0.32	UI
$DJ_{3.2L}$	Deterministic Jitter(3)(4)		–	–	0.16	UI
$TJ_{2.5}$	Total Jitter(3)(4)	2.5 Gb/s(7)	–	–	0.20	UI
$DJ_{2.5}$	Deterministic Jitter(3)(4)		–	–	0.08	UI
$TJ_{1.25}$	Total Jitter(3)(4)	1.25 Gb/s(8)	–	–	0.15	UI
$DJ_{1.25}$	Deterministic Jitter(3)(4)		–	–	0.06	UI
TJ_{500}	Total Jitter(3)(4)	500 Mb/s	–	–	0.1	UI
DJ_{500}	Deterministic Jitter(3)(4)		–	–	0.03	UI

Notes:

1. Using same REFCLK input with TX phase alignment enabled for up to 12 consecutive transmitters (three fully populated GTX Quads).
2. Using QPLL_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. Using CPLL_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
4. All jitter values are based on a bit-error ratio of $1e^{-12}$.
5. CPLL frequency at 3.2 GHz and TXOUT_DIV = 2.
6. CPLL frequency at 1.6 GHz and TXOUT_DIV = 1.
7. CPLL frequency at 2.5 GHz and TXOUT_DIV = 2.
8. CPLL frequency at 2.5 GHz and TXOUT_DIV = 4.

Table 62: **GTX Transceiver Receiver Switching Characteristics**

Symbol	Description		Min	Typ	Max	Units
F_{GTXRX}	Serial data rate		0.500	–	F_{GTXMAX}	Gb/s
$T_{RXELECIDLE}$	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
$RX_{OOBVDPP}$	OOB detect threshold peak-to-peak		60	–	150	mV
RX_{SST}	Receiver spread-spectrum tracking(1)	Modulated @ 33 KHz	–5000	–	0	ppm
RX_{RL}	Run length (CID)		–	–	512	UI
RX_{PPMTOL}	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
SJ Jitter Tolerance(2)						
$JT\_SJ_{12.5}$	Sinusoidal Jitter (QPLL)(3)	12.5 Gb/s	0.3	–	–	UI
$JT\_SJ_{11.18}$	Sinusoidal Jitter (QPLL)(3)	11.18 Gb/s	0.3	–	–	UI
$JT\_SJ_{10.32}$	Sinusoidal Jitter (QPLL)(3)	10.32 Gb/s	0.3	–	–	UI
$JT\_SJ_{9.95}$	Sinusoidal Jitter (QPLL)(3)	9.95 Gb/s	0.3	–	–	UI
$JT\_SJ_{9.8}$	Sinusoidal Jitter (QPLL)(3)	9.8 Gb/s	0.3	–	–	UI
$JT\_SJ_{8.0}$	Sinusoidal Jitter (QPLL)(3)	8.0 Gb/s	0.44	–	–	UI
$JT\_SJ_{6.6\_QPLL}$	Sinusoidal Jitter (QPLL)(3)	6.6 Gb/s	0.48	–	–	UI
$JT\_SJ_{6.6\_CPLL}$	Sinusoidal Jitter (CPLL)(3)	6.6 Gb/s	0.44	–	–	UI
$JT\_SJ_{5.0}$	Sinusoidal Jitter (CPLL)(3)	5.0 Gb/s	0.44	–	–	UI
$JT\_SJ_{4.25}$	Sinusoidal Jitter (CPLL)(3)	4.25 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.75}$	Sinusoidal Jitter (CPLL)(3)	3.75 Gb/s	0.44	–	–	UI
$JT\_SJ_{3.2}$	Sinusoidal Jitter (CPLL)(3)	3.2 Gb/s(4)	0.45	–	–	UI
$JT\_SJ_{3.2L}$	Sinusoidal Jitter (CPLL)(3)	3.2 Gb/s(5)	0.45	–	–	UI
$JT\_SJ_{2.5}$	Sinusoidal Jitter (CPLL)(3)	2.5 Gb/s(6)	0.5	–	–	UI
$JT\_SJ_{1.25}$	Sinusoidal Jitter (CPLL)(3)	1.25 Gb/s(7)	0.5	–	–	UI
JT_SJ_{500}	Sinusoidal Jitter (CPLL)(3)	500 Mb/s	0.4	–	–	UI
SJ Jitter Tolerance with Stressed Eye(2)						
$JT\_TJSE_{3.2}$	Total Jitter with Stressed Eye(8)	3.2 Gb/s	0.70	–	–	UI
$JT\_TJSE_{6.6}$		6.6 Gb/s	0.70	–	–	UI
$JT\_SJSE_{3.2}$	Sinusoidal Jitter with Stressed Eye(8)	3.2 Gb/s	0.1	–	–	UI
$JT\_SJSE_{6.6}$		6.6 Gb/s	0.1	–	–	UI

Notes:

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 10 MHz.
4. CPLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. CPLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. CPLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. CPLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter with RX in LPM or DFE mode.

GTX Transceiver Protocol Jitter Characteristics

For Table 63 through Table 68, the *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476) contains recommended settings for optimal usage of protocol specific characteristics.

Table 63: **Gigabit Ethernet Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
Gigabit Ethernet Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	1250	–	0.24	UI
Gigabit Ethernet Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 64: **XAUI Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
XAUI Transmitter Jitter Generation				
Total transmitter jitter (T_TJ)	3125	–	0.35	UI
XAUI Receiver High Frequency Jitter Tolerance				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 65: **PCI Express Protocol Characteristics(1)**

Standard	Description		Line Rate (Mb/s)	Min	Max	Units
PCI Express Transmitter Jitter Generation						
PCI Express Gen 1	Total transmitter jitter		2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter		5000	–	0.25	UI
PCI Express Gen 3(2)	Total transmitter jitter uncorrelated		8000	–	31.25	ps
	Deterministic transmitter jitter uncorrelated			–	12	ps
PCI Express Receiver High Frequency Jitter Tolerance						
PCI Express Gen 1	Total receiver jitter tolerance		2500	0.65	–	UI
PCI Express Gen 2(3)	Receiver inherent timing error		5000	0.40	–	UI
	Receiver inherent deterministic timing error			0.30	–	UI
PCI Express Gen 3(2)	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		Note 4	–	UI
		10 MHz–100 MHz		0.10	–	UI

Notes:

1. Tested per card electromechanical (CEM) methodology.
2. PCI-SIG 3.0 certification and compliance test boards are currently not available.
3. Using common REFCLK.
4. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20dB/decade.

Table 66: **CEI-6G and CEI-11G Protocol Characteristics**

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
CEI-6G Transmitter Jitter Generation					
Total transmitter jitter(1)	4976–6375	CEI-6G-SR	–	0.3	UI
		CEI-6G-LR	–	0.3	UI
CEI-6G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(1)	4976–6375	CEI-6G-SR	0.6	–	UI
		CEI-6G-LR	0.95	–	UI
CEI-11G Transmitter Jitter Generation					
Total transmitter jitter(2)	9950–11100	CEI-11G-SR	–	0.3	UI
		CEI-11G-LR/MR	–	0.3	UI
CEI-11G Receiver High Frequency Jitter Tolerance					
Total receiver jitter tolerance(2)	9950–11100	CEI-11G-SR	0.65	–	UI
		CEI-11G-MR	0.65	–	UI
		CEI-11G-LR	0.825	–	UI

Notes:

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

Table 67: **SFP+ Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
SFP+ Transmitter Jitter Generation				
Total transmitter jitter	9830.40(1)	–	0.28	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
SFP+ Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	9830.40(1)	0.7	–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

Notes:

1. Line rated used for CPRI over SFP+ applications.

Table 68: **CPRI Protocol Characteristics**

Description	Line Rate (Mb/s)	Min	Max	Units
CPRI Transmitter Jitter Generation				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
	9830.4	–	Note 1	UI
CPRI Receiver Frequency Jitter Tolerance				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2	0.95	–	UI
	6144.0	0.95	–	UI
	9830.4	Note 1	–	UI

Notes:

1. Tested per SFP+ specification, see Table 67.

Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
www.xilinx.com/technology/protocols/pciexpress.htm

Table 69: **Maximum Performance for PCI Express Designs(1)**

Symbol	Description	Speed Grade					Units
		1.0V			0.95V	0.9V	
		-3	-2/-2LE	-1/-1M	-2LI	-2LE	
$F_{PIPECLK}$	Pipe clock maximum frequency	250.00	250.00	250.00	250.00	250.00	MHz
$F_{USERCLK}$	User clock maximum frequency	500.00(1)	500.00(1)	250.00	500.00(1)	250.00	MHz
$F_{USERCLK2}$	User clock 2 maximum frequency	250.00	250.00	250.00	250.00	250.00	MHz
F_{DRPCLK}	DRP clock maximum frequency	250.00	250.00	250.00	250.00	250.00	MHz

Notes:

1. Refer to the *7 Series FPGAs Integrated Block for PCI Express Product Guide* (PG054) for specific supported core configurations.

XADC Specifications

Table 70: **XADC Specifications**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V_{CCADC} = 1.8V ± 5%, V_{REFP} = 1.25V, V_{REFN} = 0V, ADCCLK = 26 MHz, T_j = –40°C to 100°C, Typical values at T_j=+40°C						
ADC Accuracy(1)						
Resolution			12	–	–	Bits
Integral Nonlinearity(2)	INL		–	–	±3	LSBs
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset Error		Offset calibration enabled	–	–	±6	LSBs
Gain Error		Gain calibration disabled	–	–	±0.5	%
Offset Matching		Offset calibration enabled	–	–	4	LSBs
Gain Matching		Gain calibration disabled	–	–	0.3	%
Sample Rate			–	–	1	MS/s
Signal to Noise Ratio(2)	SNR	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	60	–	–	dB
RMS Code Noise		External 1.25V reference	–	–	2	LSBs
		On-chip reference	–	3	–	LSBs
Total Harmonic Distortion(2)	THD	F_{SAMPLE} = 500KS/s, F_{IN} = 20KHz	–	70	–	dB
ADC Accuracy at Extended Temperatures						
Resolution		T_j = –55°C to 125°C	10	–	–	Bits
Integral Nonlinearity(2)	INL	T_j = –55°C to 125°C	–	–	±1	LSB (at 10 bits)
Differential Nonlinearity	DNL	No missing codes, guaranteed monotonic, T_j = –55°C to 125°C	–	–	±1	
Analog Inputs(3)						
ADC Input Ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum External Channel Input Ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V_{CCADC}	V
Auxiliary Channel Full Resolution Bandwidth	FRBW		250	–	–	KHz
On-Chip Sensors						
Temperature Sensor Error		T_j = –40°C to 100°C	–	–	±4	°C
		T_j = –55°C to +125°C	–	–	±6	°C
Supply Sensor Error		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –40°C to +100°C	–	–	±1	%
		Measurement range of V_{CCAUX} 1.8V ±5% T_j = –55°C to +125°C	–	–	±2	%
Conversion Rate(4)						
Conversion Time - Continuous	t_{CONV}	Number of ADCCLK cycles	26	–	32	Cycles
Conversion Time - Event	t_{CONV}	Number of CLK cycles	–	–	21	Cycles
DRP Clock Frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC Clock Frequency	ADCCLK	Derived from DCLK	1	–	26	MHz

Table 70: **XADC Specifications *(Cont'd)***

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
DCLK Duty Cycle			40	–	60	%
XADC Reference(5)						
External Reference	V_{REFP}	Externally supplied reference voltage	1.20	1.25	1.30	V
On-Chip Reference		Ground V_{REFP} pin to AGND, T_j = –40°C to 100°C	1.2375	1.25	1.2625	V

Notes:

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
2. Only specified for bitstream option XADCEnhancedLinearity = ON.
3. For a detailed description, see the ADC chapter in the *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480).
4. For a detailed description, see the Timing chapter in the *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480).
5. Any variation in the reference voltage from the nominal V_{REFP} = 1.25V and V_{REFN} = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted. On-chip reference variation is ±1%.

Configuration Switching Characteristics

Table 71: **Configuration Switching Characteristics**

Symbol	Description	Speed Grade					Units
		1.0V			0.95V	0.9V	
		-3	-2/-2LE	-1/-1M	-2LI	-2LE	
Power-up Timing Characteristics							
T_{PL}(1)	Program latency	5	5	5	5	5	ms, Max
T_{POR}(1)	Power-on reset (50 ms ramp rate time)	10/50	10/50	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1 ms ramp rate time)	10/35	10/35	10/35	10/35	10/35	ms, Min/Max
$T_{PROGRAM}$	Program pulse width	250	250	250	250	250	ns, Min
CCLK Output (Master Mode)							
T_{ICCK}	Master CCLK output delay	150	150	150	150	150	ns, Min
T_{MCCKL}	Master CCLK clock Low time duty cycle	40/60	40/60	40/60	40/60	40/60	%, Min/Max
T_{MCCKH}	Master CCLK clock High time duty cycle	40/60	40/60	40/60	40/60	40/60	%, Min/Max
F_{MCCK}	Master CCLK frequency	100.00	100.00	100.00	100.00	70.00	MHz, Max
	Master CCLK frequency for AES encrypted x16	50.00	50.00	50.00	50.00	35.00	MHz, Max
F_{MCCK_START}	Master CCLK frequency at start of configuration	3.00	3.00	3.00	3.00	3.00	MHz, Typ
$F_{MCCKTOL}$	Frequency tolerance, master mode with respect to nominal CCLK	±50	±50	±50	±50	±50	%, Max
CCLK Input (Slave Modes)							
T_{SCCKL}	Slave CCLK clock minimum Low time	2.50	2.50	2.50	2.50	2.50	ns, Min
T_{SCCKH}	Slave CCLK clock minimum High time	2.50	2.50	2.50	2.50	2.50	ns, Min
F_{SCCK}	Slave CCLK frequency	100.00	100.00	100.00	100.00	70.00	MHz, Max
EMCCLK Input (Master Mode)							
T_{EMCCKL}	External master CCLK Low time	2.50	2.50	2.50	2.50	2.50	ns, Min
T_{EMCCKH}	External master CCLK High time	2.50	2.50	2.50	2.50	2.50	ns, Min

Table 71: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade					Units
		1.0V			0.95V	0.9V	
		-3	-2/-2LE	-1/-1M	-2LI	-2LE	
F_{EMCCK}	External master CCLK frequency	100.00	100.00	100.00	100.00	70.00	MHz, Max
Internal Configuration Access Port							
F_{ICAPCK}	Internal configuration access port (ICAPE2)	100.00	100.00	100.00	100.00	70.00	MHz, Max
Master/Slave Serial Mode Programming Switching							
T_{DCCK}/ T_{CCKD}	DIN Setup/Hold	4.00/0.00	4.00/0.00	4.00/0.00	4.00/0.00	5.00/0.00	ns, Min
T_{CCO}	DOUT clock to out	8.00	8.00	8.00	8.00	9.00	ns, Max
SelectMAP Mode Programming Switching							
T_{SMDCCK}/ T_{SMCCKD}	D[31:00] Setup/Hold	4.00/0.00	4.00/0.00	4.00/0.00	4.00/0.00	4.50/0.00	ns, Min
$T_{SMCSCCK}$/ $T_{SMCCKCS}$	CSI_B Setup/Hold	4.00/0.00	4.00/0.00	4.00/0.00	4.00/0.00	5.00/0.00	ns, Min
T_{SMWCCK}/ T_{SMCCKW}	RDWR_B Setup/Hold	10.00/0.00	10.00/0.00	10.00/0.00	10.00/0.00	12.00/0.00	ns, Min
$T_{SMCKCSO}$	CSO_B clock to out (330Ω pull-up resistor required)	7.00	7.00	7.00	7.00	8.00	ns, Max
T_{SMCO}	D[31:00] clock to out in readback	8.00	8.00	8.00	8.00	10.00	ns, Max
F_{RBCCK}	Readback frequency	100.00	100.00	100.00	100.00	70.00	MHz, Max
Boundary-Scan Port Timing Specifications							
T_{TAPTCK}/ T_{TCKTAP}	TMS and TDI Setup/Hold	3.00/2.00	3.00/2.00	3.00/2.00	3.00/2.00	3.00/2.00	ns, Min
T_{TCKTDO}	TCK falling edge to TDO output	7.00	7.00	7.00	7.00	8.50	ns, Max
F_{TCK}	TCK frequency	66.00	66.00	66.00	66.00	50.00	MHz, Max
BPI Flash Master Mode Programming Switching							
T_{BPICCO}[(2)]	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out	8.50	8.50	8.50	8.50	10.00	ns, Max
T_{BPIDCC}/ T_{BPICCD}	D[15:00] Setup/Hold	4.00/0.00	4.00/0.00	4.00/0.00	4.00/0.00	4.50/0.00	ns, Min
SPI Flash Master Mode Programming Switching							
T_{SPIDCC}/ T_{SPICCD}	D[03:00] Setup/Hold	3.00/0.00	3.00/0.00	3.00/0.00	3.00/0.00	3.00/0.00	ns, Min
T_{SPICCM}	MOSI clock to out	8.00	8.00	8.00	8.00	9.00	ns, Max
$T_{SPICCFC}$	FCS_B clock to out	8.00	8.00	8.00	8.00	9.00	ns, Max
STARTUPE2 Ports							
$T_{USRCCLKO}$	STARTUPE2 USRCCLKO input to CCLK output	0.50/6.00	0.50/6.70	0.50/7.50	0.50/6.70	0.50/7.50	ns, Min/Max
$F_{CFGMCLK}$	STARTUPE2 CFGMCLK output frequency	65.00	65.00	65.00	65.00	65.00	MHz, Typ
$F_{CFGMCLKTOL}$	STARTUPE2 CFGMCLK output frequency tolerance	±50	±50	±50	±50	±50	%, Max

Table 71: **Configuration Switching Characteristics *(Cont'd)***

Symbol	Description	Speed Grade					Units
		1.0V			0.95V	0.9V	
		-3	-2/-2LE	-1/-1M	-2LI	-2LE	
Device DNA Access Port							
F_{DNACK}	DNA access port (DNA_PORT)	100.00	100.00	100.00	100.00	70.00	MHz, Max

Notes:

1. To support longer delays in configuration, use the design solutions described in the *7 Series FPGA Configuration User Guide* (UG470).
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

eFUSE Programming Conditions

Table 72 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* (UG470).

Table 72: **eFUSE Programming Conditions(1)**

Symbol	Description	Min	Typ	Max	Units
I_{FS}	V_{CCAUX} supply current	–	–	115	mA
t_j	Temperature range	15	–	125	°C

Notes:

1. The FPGA must not be configured during eFUSE programming.

Revision History

The following table shows the revision history for this document:

Date	Version	Description
03/01/2011	1.0	Initial Xilinx release.
04/01/2011	1.1	Added the XC7K355T, XC7K420T, and XC7K480T devices throughout data sheet. Added the extended temperature range discussion to page 1. Updated V_{CCAUX_IO} in Table 2. Edits to clarify Power-On/Off Power Supply Sequencing power sequencing discussion. Added I_{CCAUX_IO} and I_{CCBRAM} to Table 6 and Table 7. Updated MMCM_F_{INDUTY} and added $F_{INJITTER}$, $T_{OUTJITTER}$, $T_{EXTFDVAR}$, and Note 3 to Table 41. Removed the SBG324 package from Table 53. Updated the Notice of Disclaimer.
10/04/2011	1.2	Replaced -1L with -2L throughout this data sheet. Updated Min/Max values and removed Note 5 from Table 2. Clarified Power-On/Off Power Supply Sequencing power sequencing discussion including adding $T_{VCCO2VCCAUX}$ to Table 8. Updated V_{ICM} in Table 12 and Table 13. Added Note 1 to table 12. Updated Table 72 including adding Note 1. Added *Absolute Maximum Ratings for GTX Transceivers*. Revised the reference clock maximum frequency (F_{GCLK}) in Table 58. Added Table 60. Added LVTTL and removed SSTL135_II and SSTL15_II specifications from Table 20. Removed HSTL_III from Table 21. Removed the *I/O Standard Adjustment Measurement Methodology* section. Use IBIS for more accurate information and measurements. Updated $T_{IDELAYPAT\_JIT}$ in Table 29. Added T_{AS}/T_{AH} to Table 31. Added $T_{RDCK\_DI\_WF\_NC}/T_{RCKD\_DI\_WF\_NC}$ and $T_{RDCK\_DI\_RF}/T_{RCKD\_DI\_RF}$ to Table 34. Completely updated Table 71. Updated the AC Switching Characteristics in Table 20, Table 21, Table 22, Table 25, Table 26, Table 27, Table 29 through Table 41, Table 43 though Table 40, and Table 67.
11/03/2011	1.3	Revised the V_{OCM} specification in Table 12. Updated the AC Switching Characteristics based upon the ISE 13.3 v1.02 speed specification throughout document including Table 20 and Table 21. Added MMCM_$T_{FBDELAY}$ while adding MMCM_ to the symbol names of a few specifications in Table 41 and PLL to the symbol names in Table 42. In Table 43 through Table 50, updated the pin-to-pin descriptions with the SSTL15 standard. Updated units in Table 52.

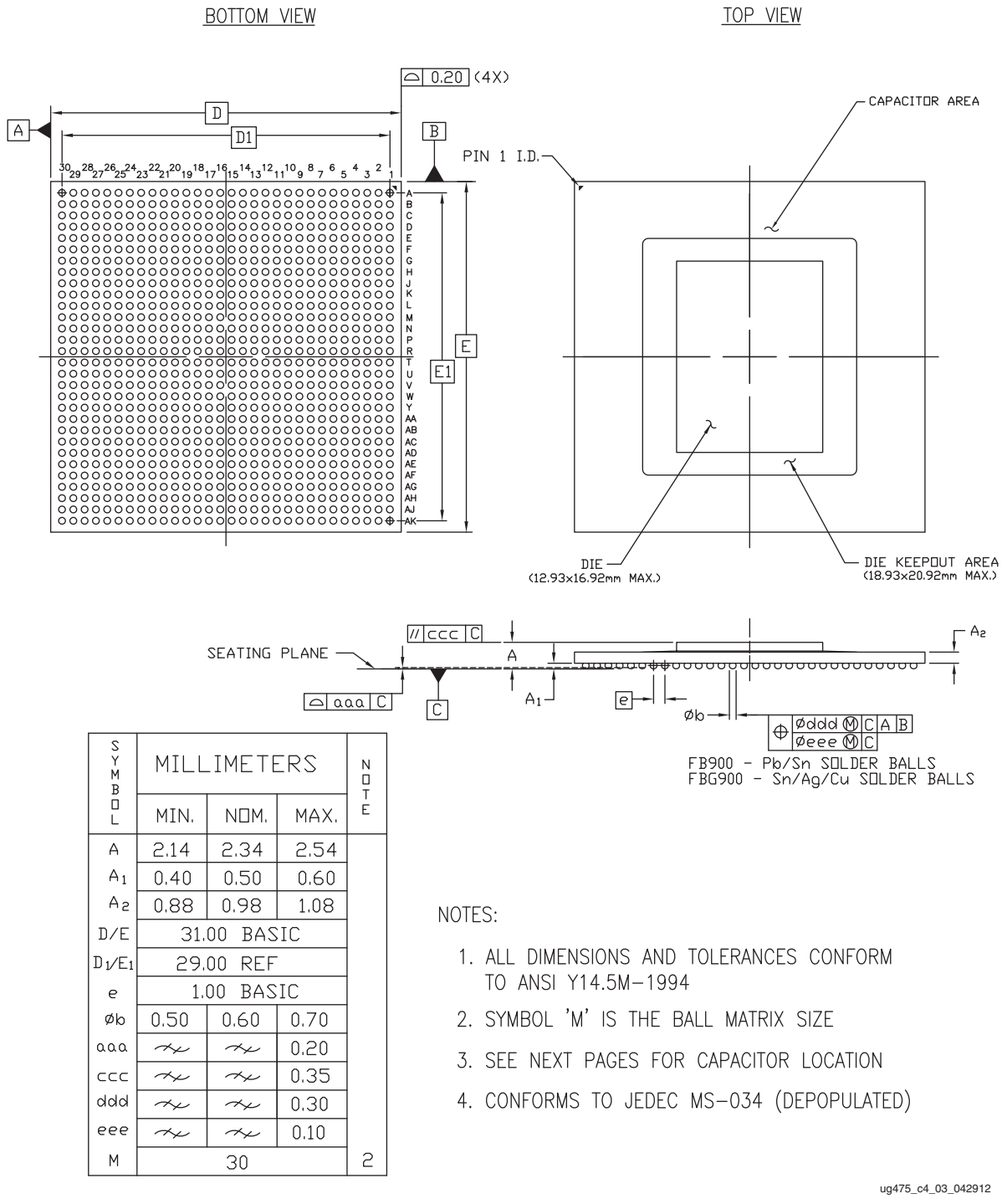
Date	Version	Description
02/13/2012	1.4	Updated summary description on page 1. In Table 2, revised V_{CCO} for the 3.3V HR I/O banks and updated T_j. Added typical values to Table 3. Updated the notes in Table 6. Added MGTAVCC, MGTAVTT, and MGTVCCAUX power supply ramp times to Table 8. Rearranged Table 9, added Mobile_DDR, HSTL_I_18, HSTL_II_18, HSUL_12, SSTL135_R, SSTL15_R, and SSTL12 and removed DIFF_SSTL135, DIFF_SSTL18_I, DIFF_SSTL18_II, DIFF_HSTL_I, and DIFF_HSTL_II. Added Table 10 and Table 11. Revised the specifications in Table 12 and Table 13. Updated the eFUSE Programming Conditions section and removed the endurance table. Added the IO_FIFO Switching Characteristics table. Revised I_{CCADC} and updated Note 1 in Table 70. Revised DDR LVDS transmitter data width in Table 17. Updated the AC Switching Characteristics based upon the ISE 13.4 v1.03 speed specification throughout document. Removed notes from Table 31 as they are no longer applicable. Updated specifications in Table 71. Updated Note 1 in Table 40. In the GTX Transceiver DC Input and Output Levels section: Revised V_{IN}, and added I_{DCIN} and I_{DCOUT} to Table 54. Added Note 4 to Table 56. In Table 58, revised F_{GCLK}, removed T_{PHASE}, and added T_{DLOCK}. Revised specifications and added Note 2 to Table 60. Added Table 61 and Table 62 along with GTX Transceiver Protocol Jitter Characteristics in Table 63 through Table 68.
05/23/2012	1.5	Reorganized entire data sheet including adding Table 47 and Table 51. Updated T_{SOL} in Table 1. Updated I_{BATT} and added R_{IN_TERM} to Table 3. Added values to Table 6 and Table 7. Updated Power-On/Off Power Supply Sequencing, page 6 with regards to GTX transceivers. Updated many parameters in Table 9 including SSTL135 and SSTL135_R. Removed V_{OX} column and added DIFF_HSUL_12 to Table 11. Updated V_{OL} in Table 12. Updated Table 17 and removed notes 2 and 3. Updated Table 18. Updated the AC Switching Characteristics based upon the ISE 14.1 v1.04 for the -3, -2, -2L (1.0V), -1, and -2L (0.9V) speed specifications throughout the document. In Table 34, updated Reset Delays section including Note 10 and Note 11. Added data for T_{LOCK} and T_{DLOCK} in Table 58. Updated many of the XADC specifications in Table 70 and added Note 2. Updated and moved *Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK* section from Table 71 to Table 41 and Table 42.
07/25/2012	1.6	Updated the descriptions, changed V_{IN} and Note 2 and added Note 4 in Table 1. In Table 2, changed descriptions and notes, removed Note 7, changed GTX transceiver parameters and values and added Note 12. Updated parameters in Table 3. Added Table 4 and Table 5. Changed the typical values for many of the devices in Table 7. Updated LVCMOS12 and the SSTLs in Table 9. Updated many of the specifications in Table 10 and Table 11. Updated speed specification to v1.06 (-3, -2, -2L(1.0V), -1) and v1.05 (-2L(0.9V)) with appropriate changes to Table 15 and Table 16 including production release of the XC7K325T and the XC7K410T in the -2, -2L(1.0V), and -1 speed designations. Added notes and specifications to Table 18 and Table 19. Updated the IOB Pad Input/Output/3-State discussion and changed Table 22 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and T_{CINCK}/T_{CKCIN} from Table 31. Rearranged Table 54 including moving some parameters to Table 1. Added Table 59. Updated Table 60. In Table 62, updated SJ Jitter Tolerance with Stressed Eye section, page 58 and Note 8. Added Note 1, Note 2, and Note 3 to Table 65. Added Note 1 and Note 2 to Table 66, and line rate ranges. Updated Table 67 including adding Note 1. Updated Table 68 including adding Note 1. In Table 70 updated Note 1 and added Note 4. In Table 71, updated T_{POR} and F_{EMCCK}.
09/04/2012	1.7	Updated Table 15 and Table 16 for production release of the XC7K160T in the -2, -2L(1.0V), and -1 speed designations.
09/26/2012	1.8	In Table 2, revised V_{CCINT} and V_{CCBRAM} and added Note 3. Updated Table 15 and Table 16 for production release of the XC7K480T in the -2, -2L(1.0V), and -1 speed designations and the XC7K325T and XC7K410T in the -3 speed designation.
10/10/2012	1.9	Updated the $I_{CCINTMIN}$ value for the XC7K355T in Table 7. Updated Table 15 and Table 16 for production release of the XC7K420T in the -2, -2L(1.0V), and -1 speed designations.
10/25/2012	2.0	Updated the AC Switching Characteristics based upon ISE 14.3 v1.07 for the -3, -2, -2L (1.0V), -1 speed specifications, and ISE 14.3 v1.06 for the -2L (0.9V) speed specifications throughout the document. Updated Table 15 and Table 16 for production release of the XC7K355T in the -2, -2L(1.0V), and -1 speed designations. Also updated Table 15 and Table 16 for production release of the XC7K325T and XC7K410T in the -2L (0.9V). Added values for Table 17 -2L (0.9V). Added package skew values to Table 53. In Table 56, increased -1 speed grade (FF package) F_{GTXMAX} value from 6.6 Gb/s to 8.0 Gb/s.

Date	Version	Description
10/31/2012	2.1	Updated Table 15 and Table 16 for production release of the XC7K70T in the -2, -2L(1.0V), and -1 speed designations.
11/26/2012	2.2	Updated Table 15 and Table 16 for production release of -3 speed designation for XC7K70T, XC7K160T, XC7K355T, XC7K420T, and XC7K480T. Removed Note 4 from Table 70.
12/05/2012	2.3	Updated Table 15 and Table 16 for production release of the -2L (0.9V) speed designation for XC7K160T, XC7K420T, and XC7K480T. Updated Note 1 in Table 53.
12/12/2012	2.4	Updated Table 15 and Table 16 for production release of the -2L (0.9V) speed designation for XC7K70T and XC7K355T. Added Internal Configuration Access Port section to Table 71.
10/04/2013	2.5	In Table 1, revised V_{IN} (I/O input voltage) to match values in Table 4 and Table 5, and combined Note 4 with old Note 5 and then added new Note 5. Also in Table 1, updated I_{DCIN} and I_{DCOUT} sections. Revised V_{IN} description and added Note 3 and Note 8 in Table 2. Updated first 3 rows in Table 4 and Table 5. Replaced XPower with Xilinx Power Estimator (XPE) in sentence before Table 7. Updated V_{IL} minimum for PCI33_3 in Table 9. Added Note 1 to Table 12. Added Note 1 to Table 13. Added Vivado Design Suite to AC Switching Characteristics. Updated titles of Table 18 and Table 19, and removed the following note: *RLDRAM III (BL = 4, BL = 8) and LPDDR2 specifications have not been validated with memory IP*. Updated T_{IOOP} and T_{IOTP} values in Table 20. Replaced "TRACE report" with "timing report" in notes for Table 28, Table 29, Table 30, Table 32, and Table 34. Removed this note: *A Zero "0" Hold Time listing indicates no hold time or a negative hold time* from Table 32, Table 33, and Table 48. Updated Note 1 in Table 38. Updated Table 60 to more accurately show transceiver user clocks for supported line rates. Updated Note 8 and description of F_{GTXRX} in Table 62. Updated Note 2, Note 3, and Note 4 in Table 70. Added $T_{USRCCLKO}$ to Table 71.
11/27/2013	2.6	Added Kintex-7Q defense-grade devices throughout. Added -1M speed grade throughout. Added reference to *7 Series FPGAs Overview* and *Defense-Grade 7 Series FPGAs Overview* inIntroduction. In Table 2, added junction temperature operating range for military (M) devices. In Table 3, removed commercial (C), industrial (I), and extended (E) from descriptions of R_{IN_TERM}. Updated temperature ranges in Table 4 and Table 5. Removed Note 1 and Note 2 from Table 7. Added T_J = 125°C to Conditions column for $T_{VCCO2VCCAUX}$ in Table 8. Added Table 14. Updated description of MMCM_F_{PFDMAX} in Table 41. Updated description of PLL_F_{PFDMAX} in Table 42. Added RF package type to Table 56. Added F_{DNACK} to Table 71.
02/07/2014	2.7	Updated the AC Switching Characteristics based upon ISE 14.7 and Vivado 2013.4. Updated Note 5 and added Note 6 to Table 2. Added Note 2 to Table 4. Added Note 2 and updated Note 3 in Table 5. Added HSUL_12_F, DIFF_HSUL_12_F, MOBILE_DDR_S, MOBILE_DDR_F, DIFF_MOBILE_DDR_S, and DIFF_MOBILE_DDR_F standards to and updated values in Table 20. Added HSUL_12_F, DIFF_HSUL_12_F, DIFF_HSUL_12_DCI_S, and DIFF_HSUL_12_DCI_F standards to and updated values in Table 21. In Table 35, corrected $F_{MAX\_CAS\_RF\_DELAYED\_WRITE}$ from 478.27 to 478.24 MHz to match software behavior. Removed introductory paragraph of Device Pin-to-Pin Output Parameter Guidelines and Device Pin-to-Pin Input Parameter Guidelines. Updated display format of "ADC Accuracy at Extended Temperatures" section in Table 70.
03/04/2014	2.8	Updated Note 2 in Table 4 and Note 2 in Table 5. For XQ7K325T and XQ7K410T in Table 15, changed -2 and -1 speed grades to -2I and -1I, respectively, and moved all XQ7K325T speed grades from Preliminary to Production. In Table 16, added production software for XQ7K325T -2/2L, -1, -1M, and (0.9V) -2L speed grades. Removed "and FB" from title of Table 19. Removed notes from Table 20 and Table 21. Added Note 1 to Table 69.
06/20/2014	2.9	In Table 4 and Table 5, updated Note 2 per the customer notice XCN14014: *7 Series FPGA and Zynq-7000 AP SoC I/O Undershoot Voltage Data Sheet Update*. In Table 15, moved all XQ7K410T speed grades from Preliminary to Production. In Table 16, added production software for XQ7K410T -2/-2L, -1, -1M, and (0.9V) -2L speed grades and removed Note 2. Added Note 3 to Table 18. In Table 29, added attribute REFCLK frequency of 400 MHz to $F_{IDELAYCTRL\_REF}$ and average tap delay at 400 MHz to Note 1. In Table 69, updated Note 1 to Gen 2 and added reference to *7 Series FPGAs Integrated Block for PCI Express Product Guide* (PG054). In Table 71, replaced USRCCLK Output with STARTUPE2 Ports and added $F_{CFGMCLK}$ and $F_{CFGMCLKTOL}$.
09/08/2014	2.10	Updated Note 3 in Table 6. In Power-On/Off Power Supply Sequencing, added sentence about there being no recommended sequence for supplies not shown. Added I/O Standard Adjustment Measurement Methodology. In Table 43, updated description of T_{ICKOF} and added Note 2. In Table 44, updated description of $T_{ICKOFFAR}$ and added Note 2. In Table 54, moved DV_{PPOUT} value of 1000 mV from Max to Min column, updated V_{IN} DC parameter description, and added Note 2. Added "peak-to-peak" to labels in Figure 3 and Figure 4.

Date	Version	Description
10/06/2014	2.11	Added -2LI (0.95V) speed grade throughout. Removed 3.3V as a descriptor of HR I/O banks and 1.8V as a descriptor of HP I/O banks throughout. Updated Introduction. Added -2LI (0.95V) to description of V_{CCINT} and V_{CCBRAM} in Table 2. Added Note 1 and updated Note 2 in Table 16. Updated Note 3 in Table 18.
11/19/2014	2.12	Replaced -2L speed grade with -2LE throughout. Updated descriptions of V_{CCINT} and V_{CCBRAM} in Table 2. Updated the AC Switching Characteristics based upon Vivado 2014.4. In Table 14, updated Vivado software version to 1.12 and added a row for V_{CCINT} = 0.95V. In Table 15, moved -2LI (0.95V) speed grade from Advance to Production. In Table 16, added Vivado 2014.4 software version to -2LI (0.95V) speed grade column and removed notes. Added Selecting the Correct Speed Grade and Voltage in the Vivado Tools. Updated speed grade heading row in Table 56. Added -2LI (0.95V) speed grade to Note 3 in Table 60. Removed sentence about PCI Express x8 Gen 2 operation from Note 1 in Table 69.
02/23/2015	2.13	In Table 12, changed maximum V_{ICM} value from 1.425V to 1.500V. Removed minimum sample rate specification from Table 70.

Notice of Disclaimer

FB/FBG900 Flip-Chip Lidless BGA (Kintex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.14	2.34	2.54	
A_1	0.40	0.50	0.60	
A_2	0.88	0.98	1.08	
D/E	31.00 BASIC			
D_1/E_1	29.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.35	
ddd	~	~	0.30	
eee	~	~	0.10	
M	30			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. SEE NEXT PAGES FOR CAPACITOR LOCATION
4. CONFORMS TO JEDEC MS–034 (DEPOPULATED)

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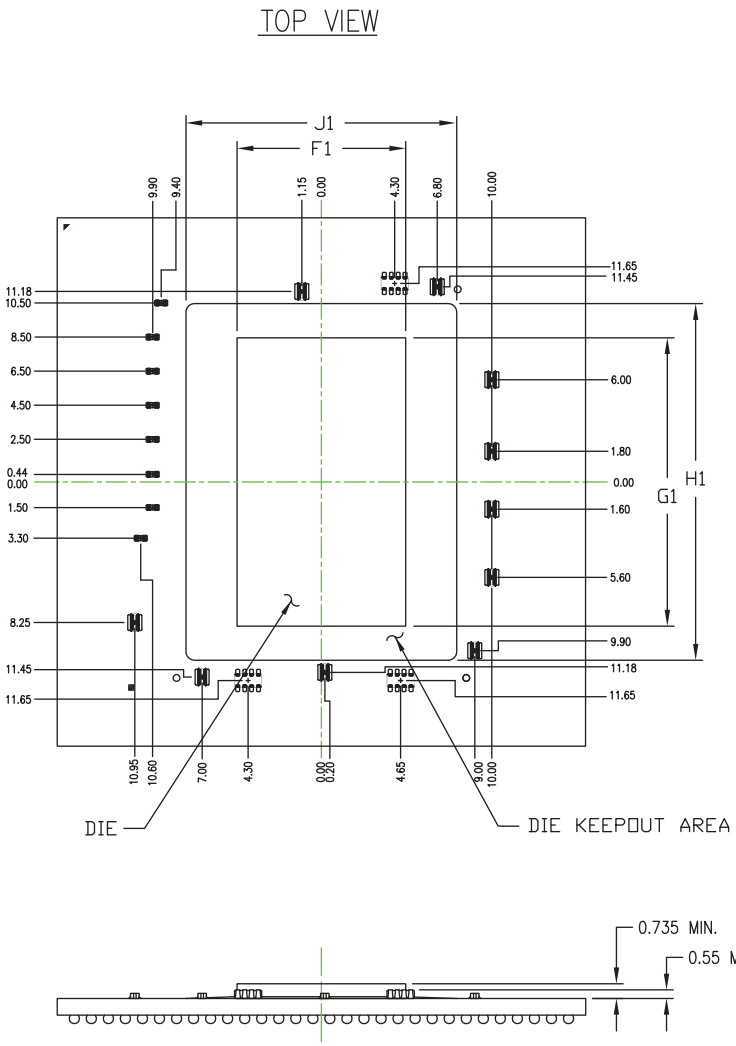
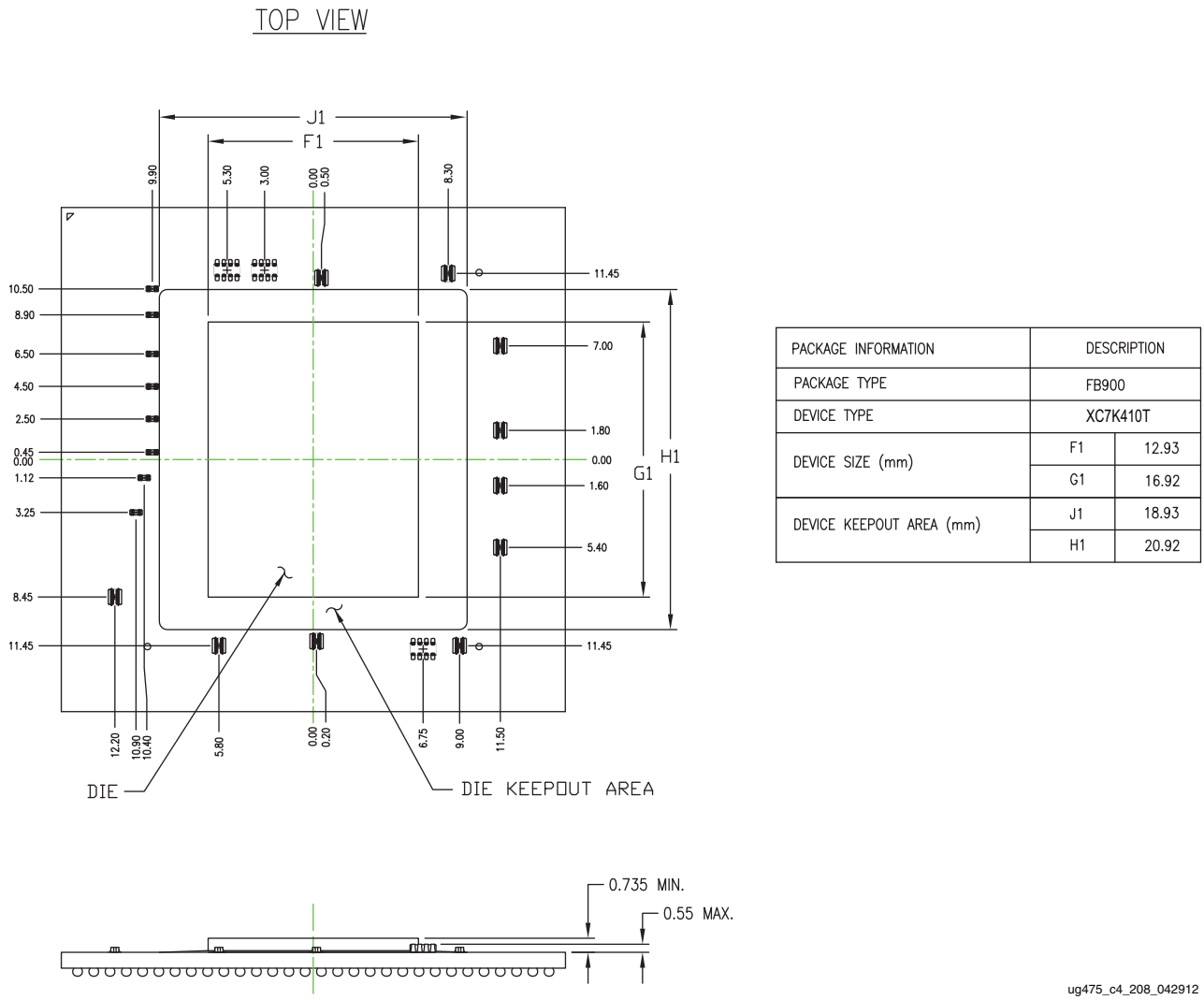
Figure 4-19: **FB/FBG900 Flip-Chip Lidless BGA Package Specifications for Kintex-7 FPGAs**



PACKAGE INFORMATION	DESCRIPTION	
PACKAGE TYPE	FB900	
DEVICE TYPE	XC7K325T	
DEVICE SIZE (mm)	F1	9.89
	G1	16.92
DEVICE KEEPOUT AREA (mm)	J1	15.89
	H1	20.92

ug475_c4_207_042912

Figure 4-20: **XC7K325T FB/FBG900 Die Dimensions with Capacitor Locations**



PACKAGE INFORMATION	DESCRIPTION	
PACKAGE TYPE	FB900	
DEVICE TYPE	XC7K410T	
DEVICE SIZE (mm)	F1	12.93
	G1	16.92
DEVICE KEEPOUT AREA (mm)	J1	18.93
	H1	20.92

Figure 4-21: **XC7K410T FB/FBG900 Die Dimensions with Capacitor Locations**