Rochester Electronics

*Datasheet*

## Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

## Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Includes FLEX 8000A

# FLEX 8000

## Programmable Logic Device Family

August 1994, ver. 4 | Data Sheet

## Features

- High-density, register-rich programmable logic device family
  - 2,500 to 16,000 usable gates
  - 282 to 1,500 registers
- FLEX 8000 devices fabricated on 0.8-micron CMOS SRAM technology
- Higher-speed FLEX 8000A devices fabricated on a 0.65-micron CMOS SRAM technology
- In-circuit reconfigurable
- FastTrack continuous routing structure for fast, predictable interconnect delays
- Dedicated carry chain that can implement fast adders and counters
- Dedicated cascade chain for efficient implementation of high-speed, high-fan-in logic functions
- Programmable output slew-rate control to reduce switching noise
- Full PCI-bus specification compliance for FLEX 8000A devices
- Built-in Joint Test Action Group (JTAG) Boundary-Scan test circuitry
- 3.3- or 5.0-V operation
  - Full 3.3-V EPF8282V
  - 3.3- or 5.0-V I/O for EPF8636A and larger devices
- Available in a variety of packages with 84 to 304 pins (see Table 1)

*Table 1. FLEX 8000 Device Features*

| Feature | EPF8282<br>EPF8282V<br>EPF8282A<br>EPF8282AV | EPF8452<br>EPF8452A | EPF8636A | EPF8820<br>EPF8820A | EPF81188<br>EPF81188A | EPF81500<br>EPF81500A |
|---|---|---|---|---|---|---|
| Available Gates | 5,000 | 8,000 | 12,000 | 16,000 | 24,000 | 32,000 |
| Usable Gates | 2,500 | 4,000 | 6,000 | 8,000 | 12,000 | 16,000 |
| Flipflops | 282 | 452 | 636 | 820 | 1,188 | 1,500 |
| Logic Elements | 208 | 336 | 504 | 672 | 1,008 | 1,296 |
| Max. User I/O Pins | 78 | 120 | 136 | 152 | 184 | 208 |
| JTAG BST Circuitry | Yes | No | Yes | Yes | No | Yes |
| Packages *(1)* | 84-pin PLCC<br>100-pin TQFP | 84-pin PLCC<br>160-pin PQFP<br>160-pin PGA | 84-pin PLCC<br>160-pin RQFP<br>192-pin PGA<br>208-pin RQFP | 160-pin RQFP<br>192-pin PGA<br>208-pin RQFP<br>225-pin BGA | 208-pin RQFP<br>232-pin PGA<br>240-pin RQFP | 240-pin RQFP<br>280-pin PGA<br>304-pin RQFP |

*Note:*
(1) Contact Altera for information on package availability.



A-DS-FLEX-04

## ... and More Features

- Software design support and automatic place-and-route with Altera's MAX+PLUS II development system for PC, Sun SPARCstation, HP 9000 Series 700, and DEC Alpha AXP platforms
- Low power consumption (less than 1 mA in standby mode)

## General Description

Altera's Flexible Logic Element MatriX (FLEX) family combines the benefits of both EPLDs and FPGAs. The fine-grained architecture and high register count characteristic of FPGAs are combined with the high speed and predictable interconnect delays of EPLDs to make the FLEX 8000 device family ideal for a wide range of applications. Logic is implemented with compact 4-input look-up tables (LUTs) and programmable registers. High performance is provided by a fast, continuous network of routing resources.

FLEX 8000 devices provide a large number of storage elements for applications such as digital signal processing, wide data-path manipulation, and data transformation. These devices are an excellent choice for bus interfaces, TTL integration, coprocessor functions, and high-speed controllers. The high-pin-count packages can integrate multiple 32-bit buses into a single device. Table 2 shows the performance of FLEX 8000 devices as shown in benchmarks of typical applications.

*Table 2. FLEX 8000 Performance* *Note (1)*

| | | FLEX 8000A Devices | | | FLEX 8000 Devices | |
|---|---|---|---|---|---|---|
| Application | Logic Elements Used | A–3 Speed Grade | A–4 Speed Grade | A–5 Speed Grade | –2 Speed Grade | –3 Speed Grade |
| 16-bit loadable counter | 16 | 95 MHz | 83 MHz | 71 MHz | 71 MHz | 45 MHz |
| 16-bit up/down counter | 16 | 95 MHz | 83 MHz | 71 MHz | 71 MHz | 45 MHz |
| 16-bit prescaled counter | 24 | 232 MHz | 185 MHz | 151 MHz | 142 MHz | 115 MHz |
| 24-bit accumulator | 24 | 67 MHz | 58 MHz | 50 MHz | 50 MHz | 32 MHz |
| 16-bit address decode | 4 | 4.9 ns | 6.3 ns | 7.7 ns | 7.8 ns | 12.0 ns |
| 16-to-1 multiplexer | 10 | 5.9 ns | 8.1 ns | 12.1 ns | 12.7 ns | 18.0 ns |

*Note:*
(1) The A–6 speed grade yields the same results as the –3 speed grade.

All FLEX 8000 device packages provide four dedicated inputs for synchronous control signals with large fan-outs. Each I/O pin has an associated register on the periphery of the device. As outputs, these registers provide fast Clock-to-output times; as inputs, they offer quick setup times.

The logic and interconnections in the FLEX 8000 architecture are configured with CMOS SRAM cells. FLEX 8000 devices are configured at system power-up with data stored in a serial Configuration EPROM device or provided by a system controller. Altera offers the EPC1213 and EPC1064 Configuration EPROMs, which configure FLEX 8000 devices via a serial data stream. Configuration data can also be stored in an industry-standard 32K × 8-bit or larger EPROM or downloaded from system RAM. After a FLEX 8000 device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Because reconfiguration requires less than 100 ms, real-time changes can be made during system operation.

You can use Altera's MAX+PLUS II development system to create FLEX 8000 logic designs with any combination of graphic, text—including the Altera Hardware Description Language (AHDL), VHSIC Hardware Description Language (VHDL), and Verilog HDL—and waveform design entry. Full simulation, worst-case timing analysis, and functional testing are available for design verification. MAX+PLUS II also provides EDIF 2 0 0 and EDIF 2 9 0 netlist interfaces for additional design entry and simulation support with industry-standard CAE tools. In addition, MAX+PLUS II can export Verilog HDL and VHDL netlist files.

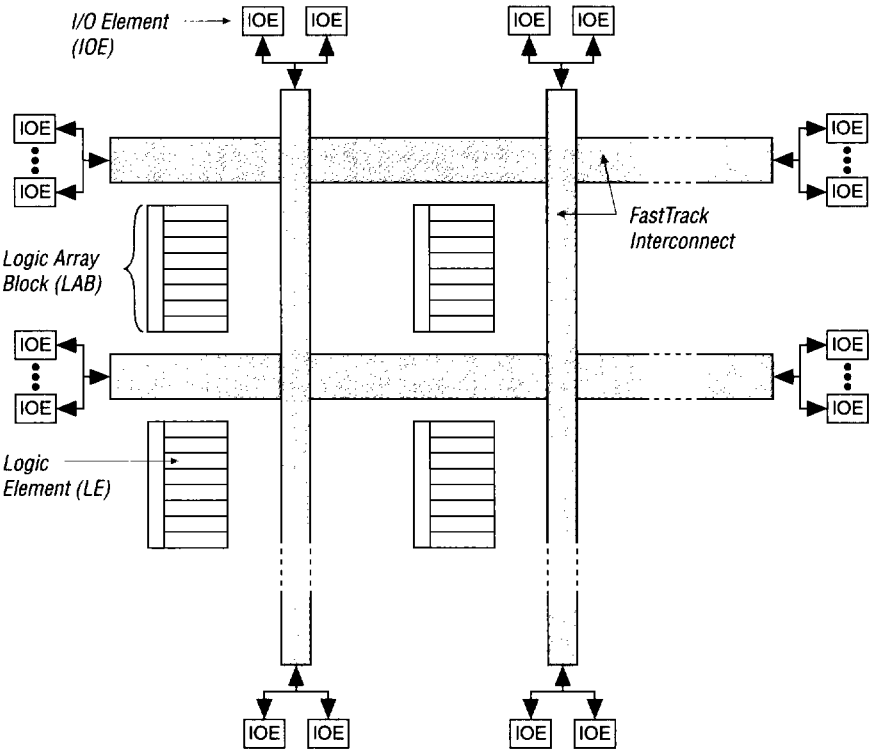
## Functional Description

The FLEX 8000 architecture incorporates a large matrix of compact building blocks called logic elements (LEs). Each LE contains a 4-input LUT that provides combinatorial logic capability and a programmable register that offers sequential logic capability. The fine-grained structure of the LE provides highly efficient logic implementation.

LEs are grouped into sets of eight to create Logic Array Blocks (LABs). Each FLEX 8000 LAB is an independent structure with common inputs, interconnections, and control signals. The LAB architecture provides a coarse-grained structure for high device performance and easy routing.

Figure 1 shows a block diagram of the FLEX 8000 architecture. Each group of eight LEs is combined into an LAB; LABs are arranged into rows and columns. The I/O pins are supported by I/O elements (IOEs) located at the ends of rows and columns. Each IOE contains a bidirectional I/O buffer and a flipflop that can be used as either an input or output register.

***Figure 1. FLEX 8000 Device Block Diagram***

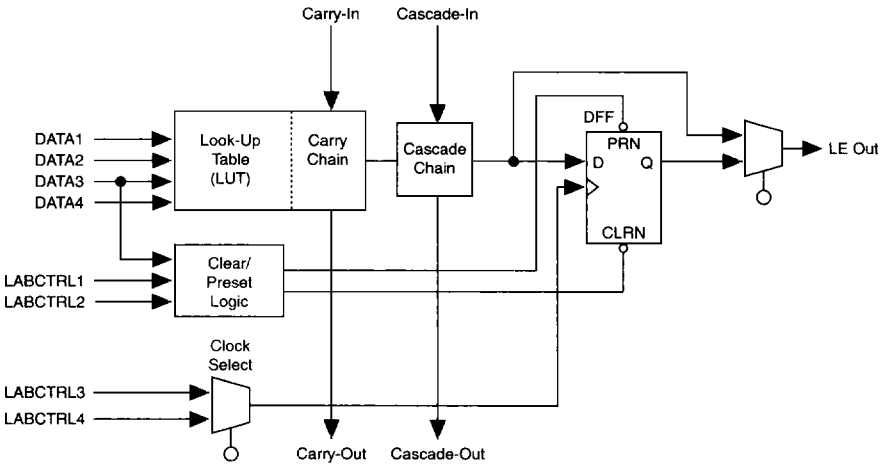



Signal interconnections within FLEX 8000 devices and to and from device pins are provided by the FastTrack Interconnect, a series of fast, continuous channels that run the entire length and width of the device. IOEs are located at the end of each row (horizontal) and column (vertical) FastTrack Interconnect path.

## Logic Element

The logic element (LE) is the smallest unit of logic in the FLEX 8000 architecture, with a compact size that provides efficient logic utilization. Each LE contains a four-input LUT, a programmable flipflop, a carry chain, and a cascade chain. Figure 2 shows a block diagram of the LE.

*Figure 2. FLEX 8000 Logic Element (LE)*




The LUT is a function generator that can quickly compute any function of four variables. The programmable flipflop in the LE can be configured for D, T, JK, or SR operation. The Clock, Clear, and Preset control signals on the flipflop can be driven by dedicated input pins, general-purpose I/O pins, or any internal logic. For purely combinatorial functions, the flipflop is bypassed and the output of the LUT goes directly to the output of the LE.

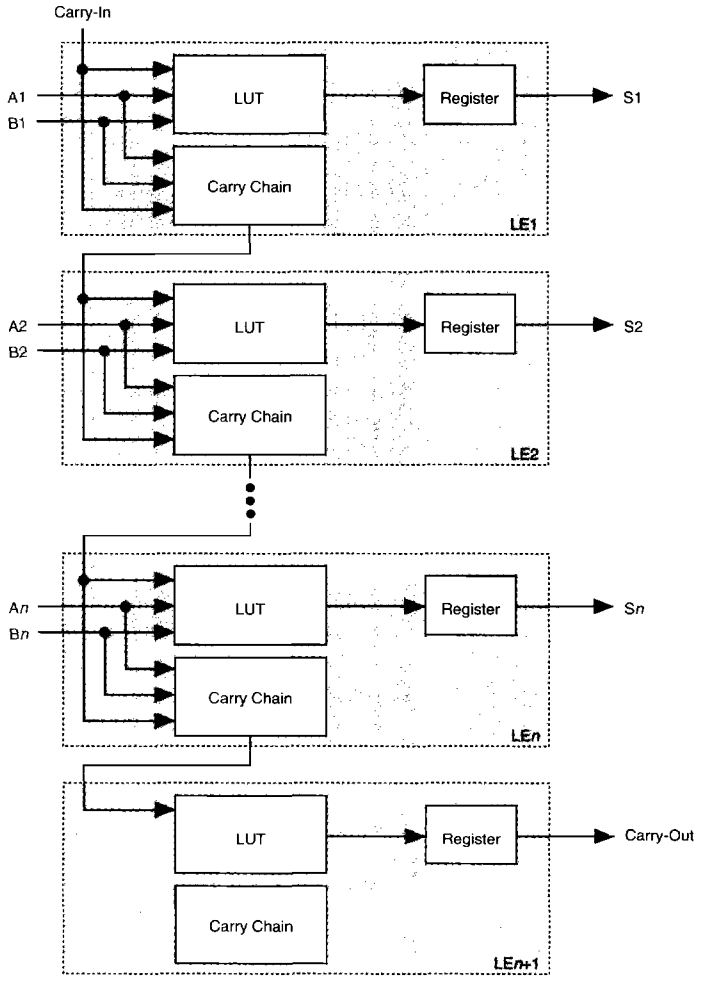
The FLEX 8000 architecture provides two dedicated high-speed data paths, carry chains and cascade chains, that connect adjacent LEs without using local interconnect paths. The carry chain supports high-speed counters and adders; the cascade chain implements wide-input functions with minimum delay. Carry and cascade chains connect all LEs in an LAB and all LABs in the same row. Heavy use of carry and cascade chains can reduce the routing resources available for implementing other logic. Therefore, the use of carry and cascade chains should be limited to speed-critical portions of a design.

## Carry Chain

The carry chain provides a very fast (less than 1 ns) carry-forward function between LEs. The carry-in signal from a lower-order bit moves forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the FLEX 8000 architecture to implement high-speed counters and adders of arbitrary width. The MAX+PLUS II Compiler can create carry chains automatically during design processing; designers can also insert carry chain logic manually during design entry.

Figure 3 shows how an *n*-bit full adder can be implemented in *n*+1 LEs by using the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register is typically bypassed for simple adders, but can be used for an accumulator function. Another portion of the LUT and the carry chain logic generate the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it can be used as a general-purpose signal. In addition to mathematical functions, carry chain logic supports very fast counters and comparators.

***Figure 3. Carry Chain Operation***

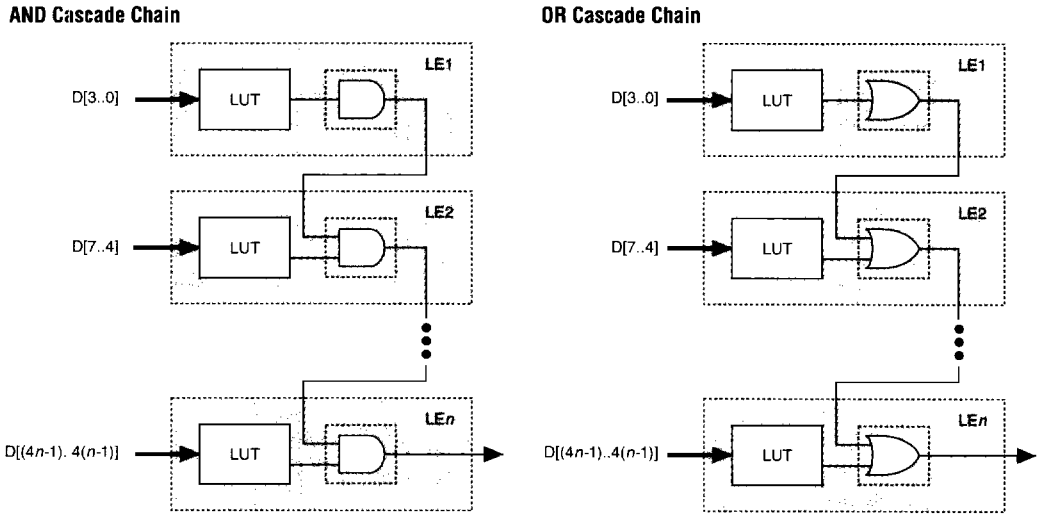


## Cascade Chain

With the cascade chain, the FLEX 8000 architecture can implement functions that have a very wide fan-in. Adjacent LUTs can be used to compute portions of the function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a delay of approximately 1 ns per LE. The MAX+PLUS II Compiler can create cascade chains automatically during design processing; designers can also insert cascade chain logic manually during design entry.

Figure 4 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in. These examples show functions of 4*n* variables implemented with *n* LEs. For a device with an A–3 speed grade, the LUT delay is approximately 1.8 ns; the cascade chain delay is 0.7 ns. With the cascade chain, 5.0 ns is needed to decode a 16-bit address.

***Figure 4. Cascade Chain Operation***



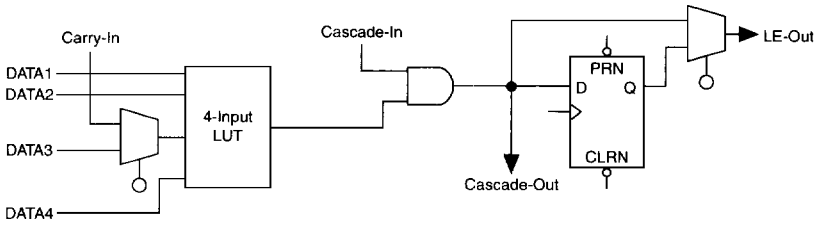

## Logic Element Operating Modes

The FLEX 8000 logic element can operate in one of four modes, shown in Figure 5, each of which uses LE resources differently. In each mode, seven of the ten available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different

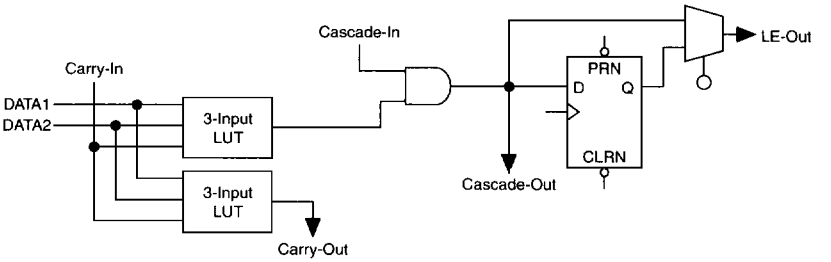
destinations to implement the desired logic function. The three remaining inputs to the LE provide Clock, Clear, and Preset control for the register. MAX+PLUS II software automatically chooses the appropriate mode for each application. Design performance can also be enhanced by designing for the operating mode that supports the desired application.

***Figure 5. FLEX 8000 Logic Element Operating Modes***

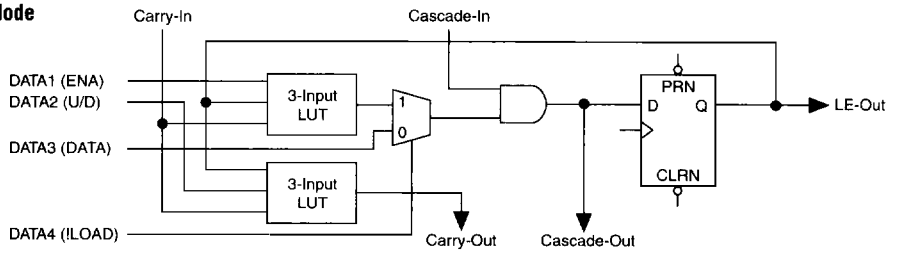
**Normal Mode**



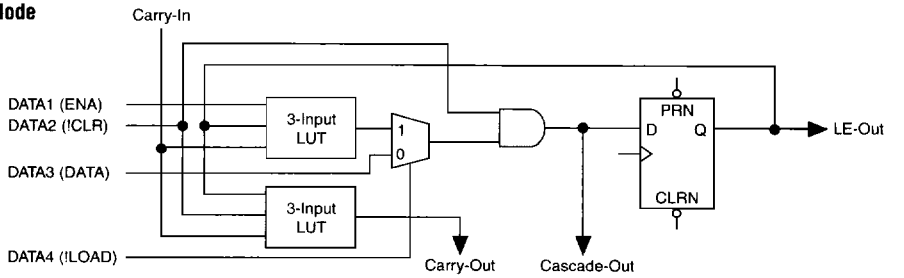

**Arithmetic Mode**




**Up/Down Counter Mode**




**Clearable Counter Mode**



### Normal Mode

The Normal mode is suitable for general logic applications and wide decode functions that can take advantage of a cascade chain. In Normal mode, four data inputs from the LAB local interconnect and the carry-in are the inputs to a 4-input LUT. Using a configurable SRAM bit, the MAX+PLUS II Compiler automatically selects the carry-in or the DATA3 signal as an input. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. The LE-out signal—the data output of the LE—is either the combinatorial output of the LUT and cascade chain, or the Q output of the programmable register.

### Arithmetic Mode

The Arithmetic mode offers two 3-input LUTs that are ideal for implementing adders, accumulators, and comparators. One LUT provides a 3-bit function; the other generates a carry bit. As shown in Figure 5, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, in an adder, this output would be the sum of three bits: A, B, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The Arithmetic mode also supports a cascade chain.

### Up/Down Counter Mode

The Up/Down Counter mode offers counter enable, synchronous up/down control, and data loading options. These control signals are generated by the data inputs from the LAB local interconnect, the carry-in signal, and output feedback from the programmable register. Two 3-input LUTs are used: one generates the counter data, the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading. Data can also be loaded asynchronously with the Clear and Preset register control signals, without using the LUT resources.

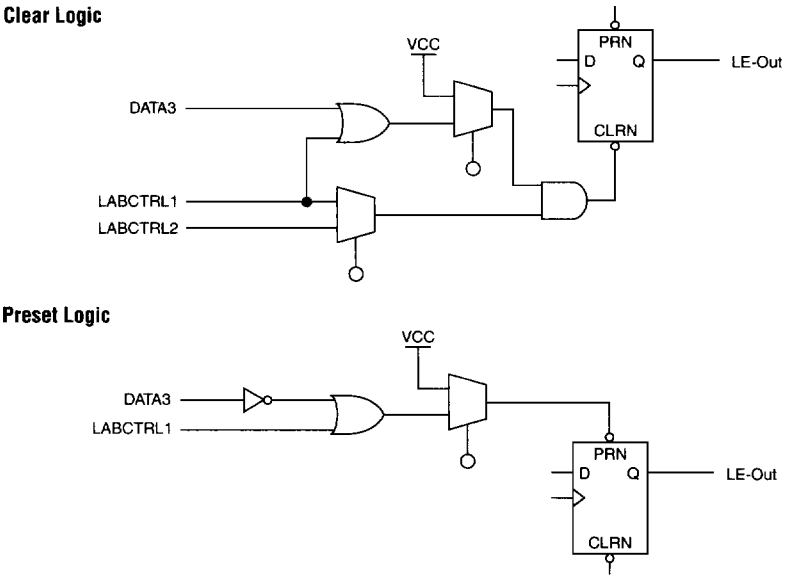
### Clearable Counter Mode

The Clearable Counter mode is similar to the Up/Down Counter mode, but supports a synchronous Clear instead of the up/down control. The Clear function is substituted for the cascade-in signal in the Up/Down Counter mode. Two 3-input LUTs are used: one generates the counter data, the other generates the fast carry bit. Synchronous loading is provided by a 2-to-1 multiplexer, the output of which is ANDed with a synchronous Clear.

### Clear/Preset Logic Control

Logic for the programmable register's Clear and Preset functions is controlled by the DATA3, LABCTRL1, and LABCTRL2 inputs to the LE. See Figure 6.

*Figure 6. Logic Element Clear & Preset Logic*

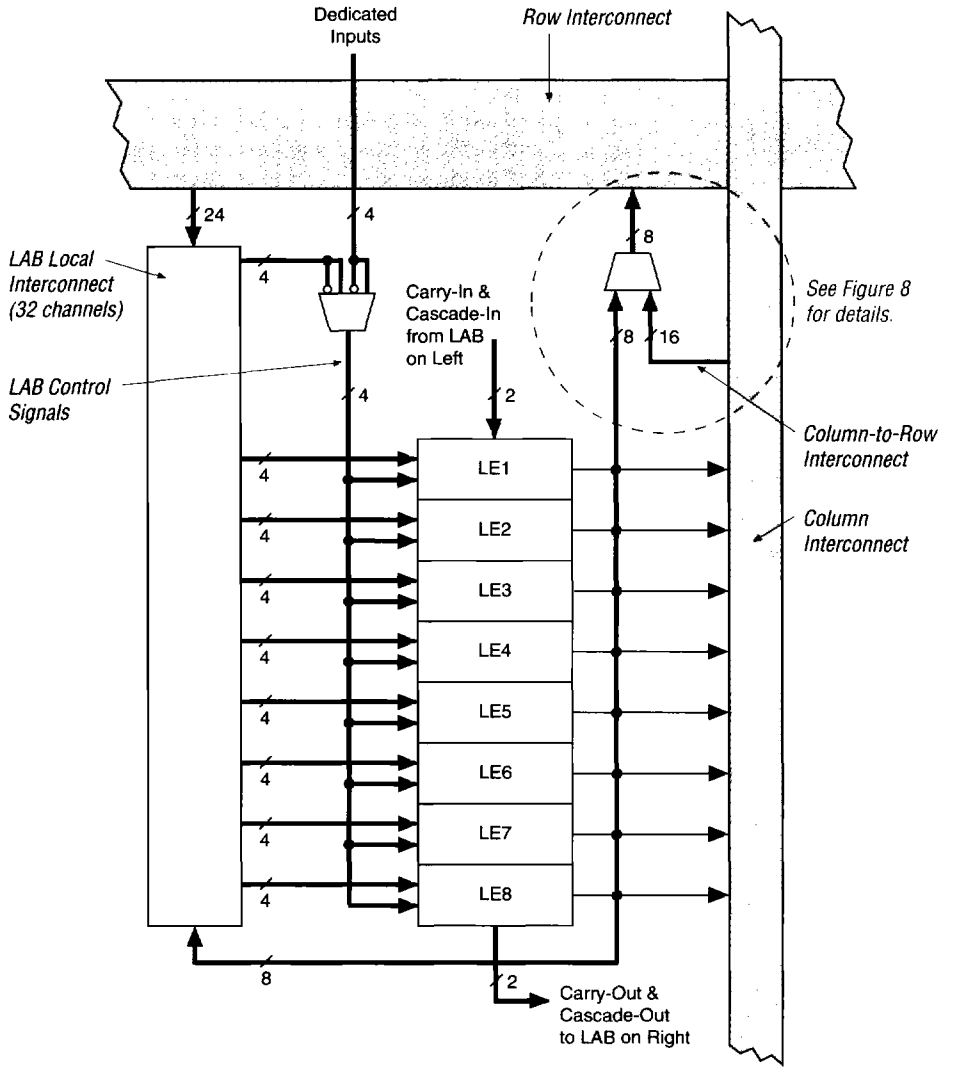



The Clear function is controlled by DATA3, LABCTRL1, and LABCTRL2; the Preset function is controlled by DATA3 and LABCTRL1. The MAX+PLUS II Compiler automatically selects the best control signal implementation during compilation. Since the Clear and Preset functions are active low, the Compiler automatically assigns a logic high to an unused Clear and/or Preset. Preset control can also be provided by using a Clear and inverting the output of the register. Inversion control is available for the inputs to both LEs and IOEs. Therefore, if a register is cleared by only one of the two LABCTRL signals, the DATA3 input is not required and can be used for one of the LE operating modes.

## Logic Array Block

A Logic Array Block (LAB) consists of eight LEs, their associated carry and cascade chains, LAB control signals, and the LAB local interconnect. The LAB provides the coarse-grained structure of the FLEX 8000 architecture for efficient routing with high device utilization and high performance. Figure 7 shows a block diagram of the FLEX 8000 LAB.

***Figure 7. Logic Array Block (LAB)***




Each LAB provides four control signals that can be used in all eight LEs. Two of these signals can be used as Clocks, the other two for Clear/Preset control. The LAB control signals can be driven directly from a dedicated input pin, an I/O pin, or any internal signal via the LAB local interconnect. The dedicated inputs are typically used for global Clock, Clear, or Preset signals because they provide synchronous control with very low skew across the device. If logic is required on a control signal, it can be generated

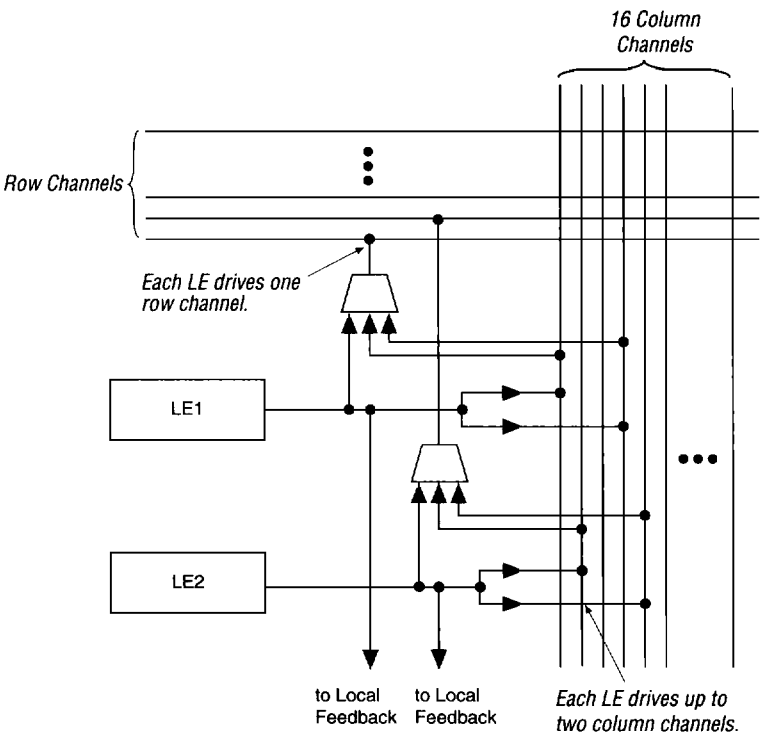
in one or more LEs in any LAB and driven into the local interconnect of the target LAB. Programmable inversion is available for all four LAB control signals.

## FastTrack Interconnect

In the FLEX 8000 architecture, connections between LEs and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the entire FLEX 8000 device. This device-wide routing structure provides predictable performance even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The LABs within FLEX 8000 devices are arranged into a matrix of columns and rows. Each row of LABs has a dedicated row interconnect that routes signals both into and out of the LABs in the row. The row interconnect can then drive I/O pins or feed other LABs in the device. Figure 8 shows how an LE drives the row and column interconnect.

***Figure 8. LAB Connections to Row & Column Interconnect***



Each LE in an LAB can drive up to two separate column interconnect channels. Therefore, all 16 available column channels can be driven by the LAB. The column channels run vertically across the entire device, and share access to LABs in the same column but in different rows. The MAX+PLUS II Compiler chooses which LEs must be connected to a column channel. A row interconnect channel can be fed by the output of the LE or by two column channels. These three signals feed a multiplexer that connects to a specific row channel. Each LE is connected to one 3-to-1 multiplexer. In an LAB, the multiplexers provide all 16 column channels with access to 8 row channels.

Each column of LABs has a dedicated column interconnect that routes signals out of the LABs into the column. The column interconnect can then drive I/O pins or feed into the row interconnect to route the signals to other LABs in the device. A signal from the column interconnect, which can be either the output of an LE or an input from an I/O pin, must transfer to the row interconnect before it can enter an LAB. Table 3 summarizes the FastTrack Interconnect resources available in each FLEX 8000 device.

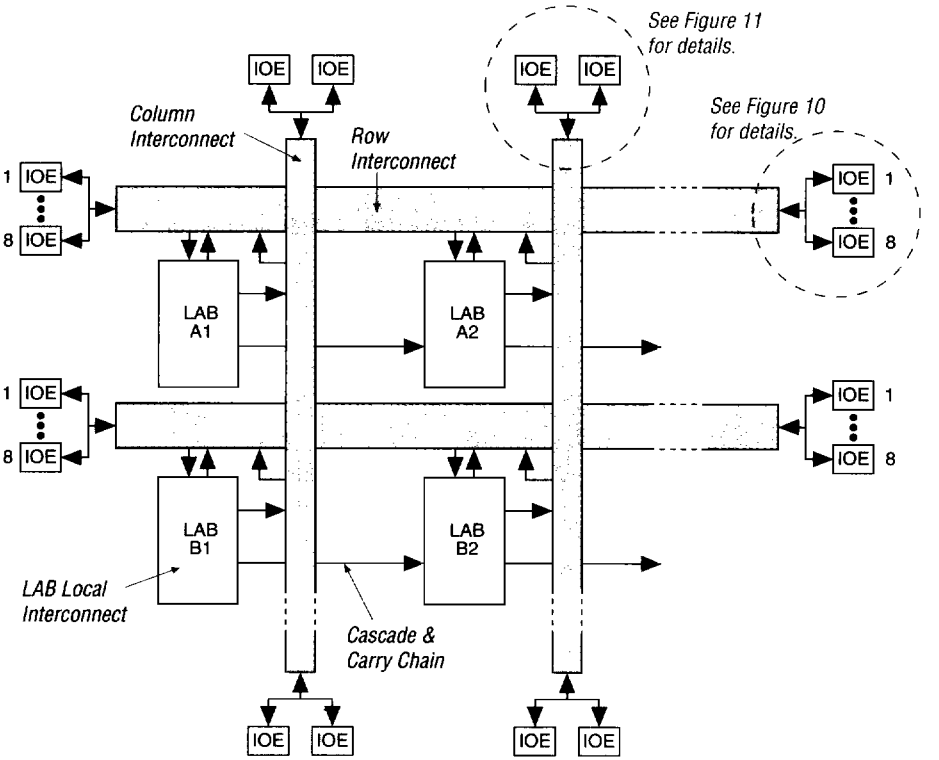
*Table 3. FLEX 8000 FastTrack Interconnect Resources*

| Device | Rows | Channels per Row | Columns | Channels per Column |
|---|---|---|---|---|
| EPF8282<br>EPF8282V<br>EPF8282A<br>EPF8282AV | 2 | 168 | 13 | 16 |
| EPF8452<br>EPF8452A | 2 | 168 | 21 | 16 |
| EPF8636A | 3 | 168 | 21 | 16 |
| EPF8820<br>EPF8820A | 4 | 168 | 21 | 16 |
| EPF81188<br>EPF81188A | 6 | 168 | 21 | 16 |
| EPF81500<br>EPF81500A | 6 | 216 | 27 | 16 |

Figure 9 shows the interconnection of four adjacent LABs, with row, column, and local interconnects, as well as the associated cascade and carry chains.

***Figure 9. FLEX 8000 Device Interconnect Resources***

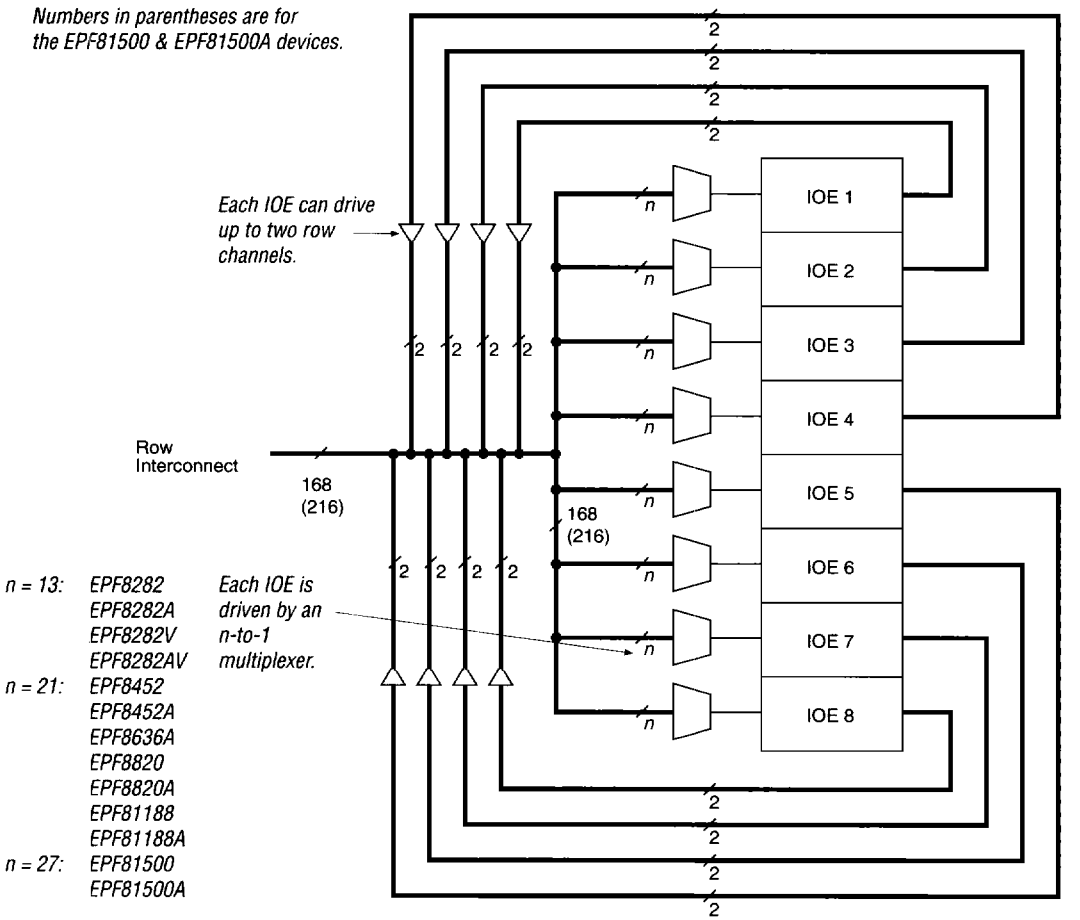
*Each LAB is named on the basis of its physical row (A, B, C, etc.) and column (1, 2, 3, etc.) position within the device.*




## Row-to-IOE Connections

Figure 10 illustrates the connection between row interconnect channels and IOEs. An input signal from an IOE can drive two separate row channels. When an IOE is used as an output, the signal is driven by an *n*-to-1 multiplexer that selects the row channels. The size of the multiplexer varies with the number of columns in a device. The EPF81500 and EPF81500A use a 27-to-1 multiplexer; the EPF81188, EPF81188A, EPF8820, EPF8820A, EPF8636A, EPF8452, and EPF8452A use a 21-to-1 multiplexer; and the EPF8282, EPF8282A, EPF8282V and EPF8282AV use a 13-to-1 multiplexer. Eight IOEs are connected to each side of the row channels.

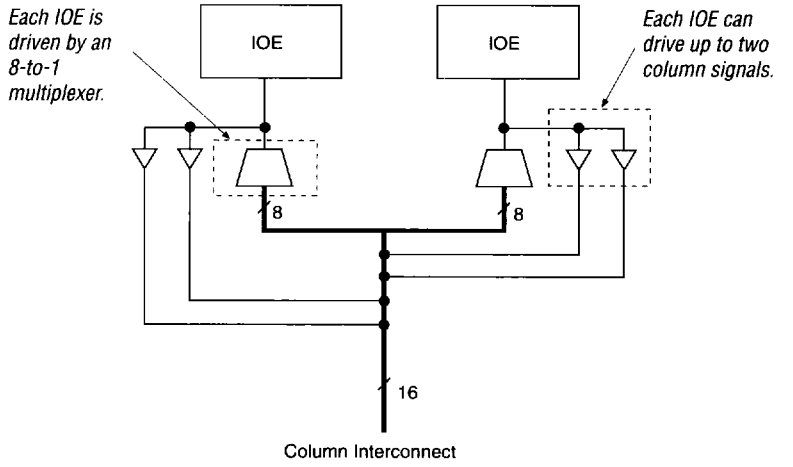
***Figure 10. FLEX 8000 Row-to-IOE Connection***




## Column-to-IOE Connections

On the top and bottom of the column channels are two IOEs (see Figure 11). When an IOE is used as an input, it can drive up to 2 separate column channels. The output signal to an IOE can choose from 8 of the 16 column channels through an 8-to-1 multiplexer.

***Figure 11. FLEX 8000 Column-to-IOE Connection***

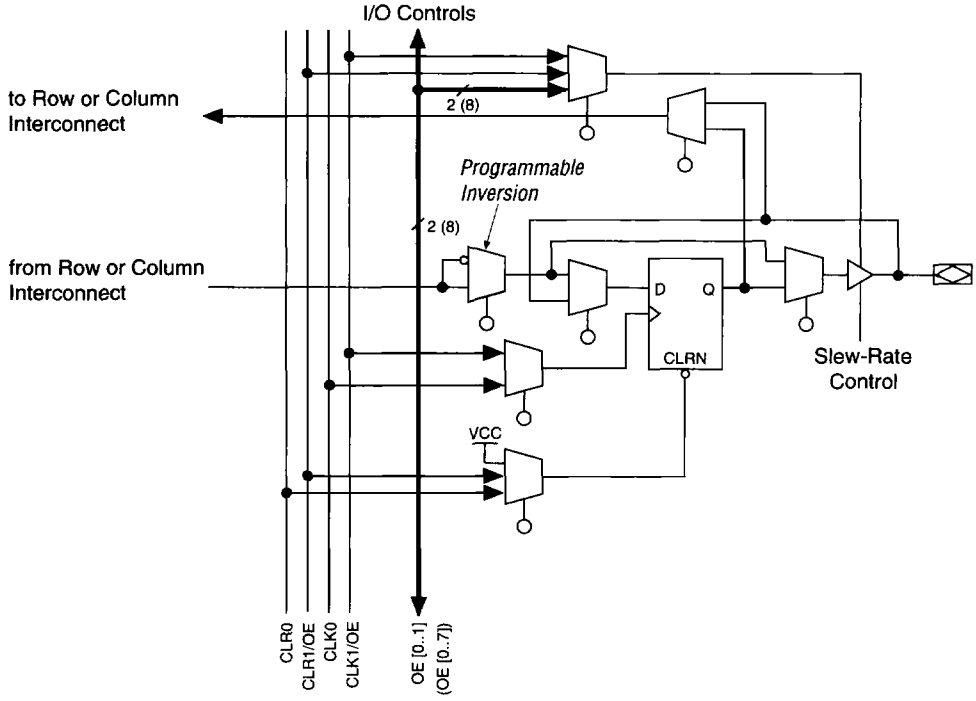



In addition to the general-purpose I/O pins, FLEX 8000 devices have four dedicated input pins. These dedicated inputs provide low-skew, device-wide signal distribution, and are typically used for global Clock, Clear, and Preset control signals. The signals from the dedicated inputs are available as control signals for all LABs and I/O elements in the device. The dedicated inputs can also be used as general-purpose data inputs because they can feed the local interconnect of each LAB in the device.

Figure 12 shows the I/O element (IOE) block diagram. Signals enter the FLEX 8000 device either from the I/O pins that provide general-purpose input capability or from the four dedicated inputs. The IOEs are located at the ends of the row and column interconnect channels.

***Figure 12. I/O Element (IOE)***

*Numbers in parentheses are for EPF81500 and EPF81500A devices.*




I/O pins can be used as input, output, or bidirectional pins. Each I/O pin has a register that can be used either as an input register for external data that requires fast setup times, or as an output register for data that requires fast Clock-to-output performance. The MAX+PLUS II Compiler uses the programmable inversion option to automatically invert signals from the row and column interconnect when appropriate.

The output buffer in each IOE has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces system noise and adds a maximum delay of 4 ns. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis.

The Clock, Clear, and Output Enable controls for the IOEs are provided by a network of I/O control signals. These signals can be supplied by either the dedicated input pins or internal logic. The IOE control-signal paths are designed to minimize the skew across the device. All control-signal sources are buffered onto high-speed drivers that drive the signals around the periphery of the device. This "peripheral bus" can be configured to provide up to four Output Enable signals (ten in the EPF81500 and EPF81500A), and up to two Clock or Clear signals. Figure 12 illustrates how two Output Enable signals are shared with one Clock (CLK1) and one Clear (CLR1) signal.

The signals for the peripheral bus can be generated by any of the 4 dedicated inputs or signals on the row interconnect channels, as shown in Figure 13. The number of row channels used correlates to the number of columns in the FLEX 8000 device. The EPF8282, EPF8282A, EPF8282V, and EPF8282AV, for example, use 13 channels; the EPF8452, EPF8452A, EPF8636A, EPF8820, EPF8820A, EPF81188, and EPF81188A use 21 channels; and the EPF81500 and EPF81500A use 27 channels. The first LE in each LAB is the source of the row channel signal. The 6 peripheral control signals (12 in the EPF81500 and EPF81500A) can be accessed by every I/O element.

***Figure 13. FLEX 8000 Peripheral Bus***

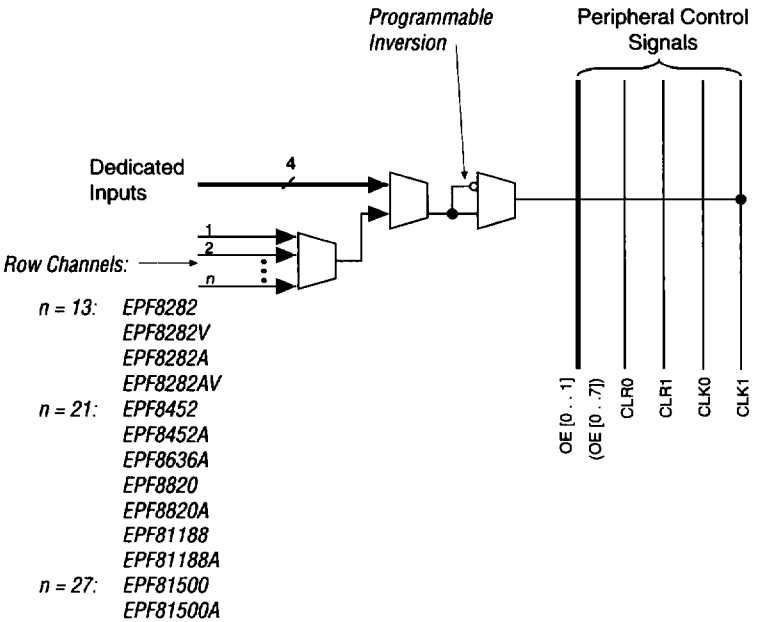


Table 4 lists the row source of the peripheral control signal for each FLEX 8000 device.

*Table 4. Row Sources of Peripheral Control Signals*

| Peripheral Control Signal | EPF8282 EPF8282V EPF8282A EPF8282AV | EPF8452 EPF8452A | EPF8636A | EPF8820 EPF8820A | EPF81188 EPF81188A | EPF81500 EPF81500A |
|---|---|---|---|---|---|---|
| CLK0 | Row A | Row A | Row A | Row A | Row E | Row E |
| CLK1 | Row B | Row B | Row C | Row C | Row B | Row B |
| CLR0 | Row A | Row A | Row B | Row B | Row F | Row F |
| CLR1 | Row B | Row B | Row C | Row D | Row C | Row C |
| OE0 | Row A | Row A | Row A | Row A | Row D | Row A |
| OE1 | Row B | Row B | Row B | Row B | Row A | Row A |
| OE2 | – | – | – | – | – | Row B |
| OE3 | – | – | – | – | – | Row C |
| OE4 | – | – | – | – | – | Row D |
| OE5 | – | – | – | – | – | Row D |
| OE6 | – | – | – | – | – | Row E |
| OE7 | – | – | – | – | – | Row F |

## 3.3- or 5.0-V I/O Operation

Some members of the FLEX 8000 family, including EPF81500, EPF81500A, EPF81188, EPF81188A, EPF8820, EPF8820A, and EPF8636A devices (except the 84-pin PLCC EPF8636A) can be set for 3.3-V or 5.0-V operation. These devices have one set of $V_{CC}$ pins for internal operation and input buffers ($V_{CCINT}$), and another set for I/O output drivers ($V_{CCIO}$).

The $V_{CCINT}$ pins must always be connected to a 5.0-V power supply. With a 5.0-V $V_{CCINT}$ level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs. The $V_{CCIO}$ pins can be connected to either a 3.3-V or 5.0-V power supply, depending on the output requirements. When the $V_{CCIO}$ pins are connected to a 5.0-V power supply, the output levels are compatible with 5.0-V systems. When the $V_{CCIO}$ pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V systems. Devices operating with a $V_{CCIO}$ levels lower than 4.75 V incur a nominal timing delay adder for the $t_{OD}$ parameter.

## JTAG Operation

The EPF8282, EPF8282A, EPF8282V, EPF8282AV, EPF8636A, EPF8820, EPF8820A, EPF81500, and EPF81500A devices support the Joint Test Action Group (JTAG) boundary-scan testing. For detailed information on JTAG operation in these FLEX 8000 devices, refer to *Application Note 39 (JTAG Boundary-Scan Testing in FLEX 8000 Devices).*

## Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard CAE tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and system-level performance analysis.

The FLEX 8000 timing model in Figure 14 shows the delays that correspond to various paths and functions in the circuit. This model contains three distinct parts: the LE; the IOE; and the interconnect, including the row and column FastTrack Interconnect, LAB local interconnect, and carry and cascade interconnect paths. Each parameter shown in Figure 14 is expressed as a worst-case value in the "Internal Timing Characteristics" tables in this data sheet. Hand-calculations that use the FLEX 8000 timing model and these timing parameters can be used to estimate FLEX 8000 device performance. Timing simulation or timing analysis after compilation is required to determine final worst-case performance.

*Figure 14. FLEX 8000 Timing Model*

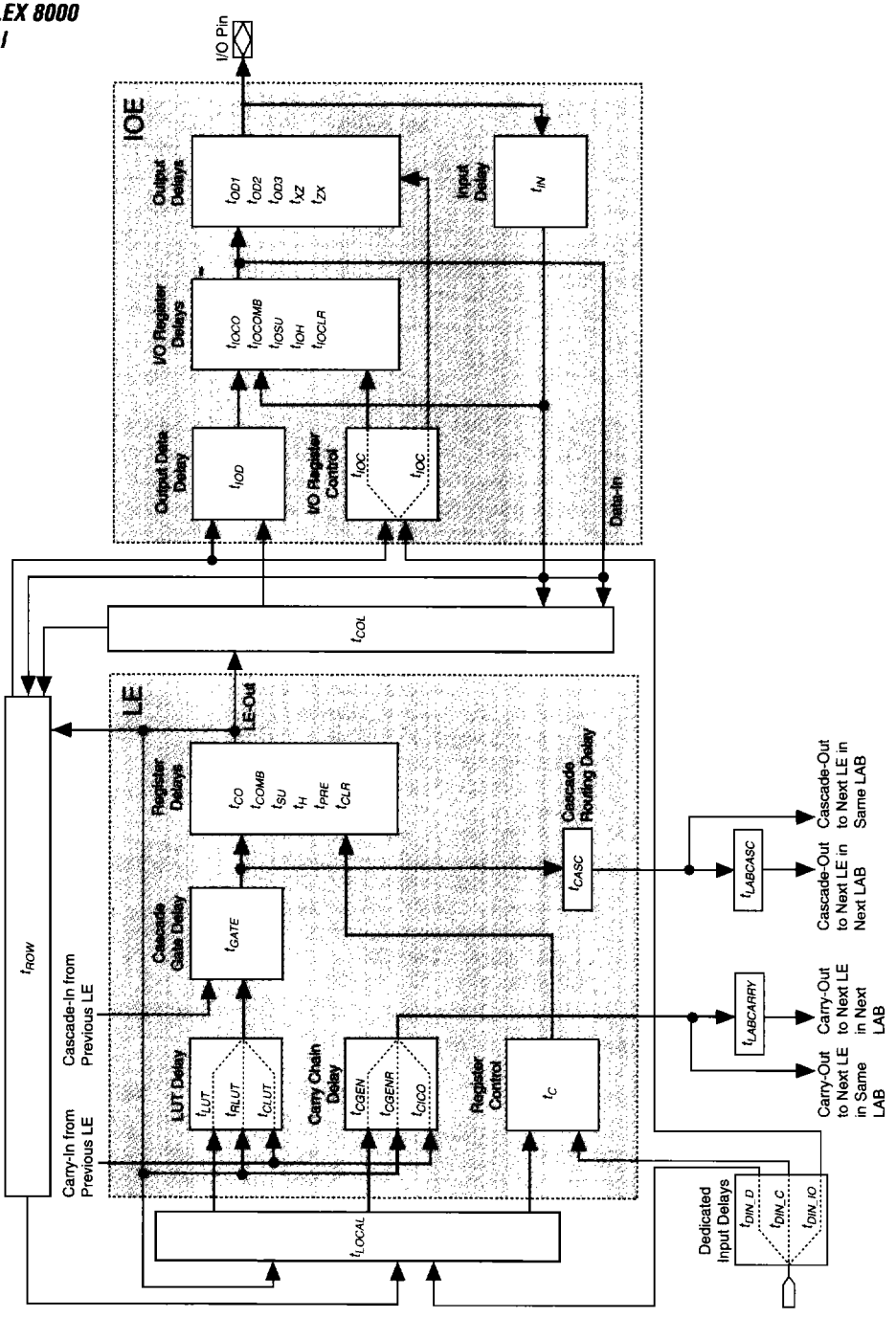


Table 5 outlines the interconnect paths shown in Figure 14.

*Table 5. FLEX 8000 Timing Model Interconnect Paths*

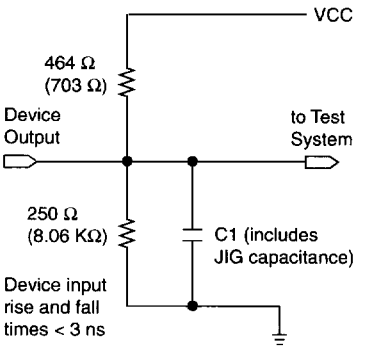
| Source | Destination | Total Delay |
|---|---|---|
| LE-out | LE in same LAB | $t_{LOCAL}$ |
| LE-out | LE in same row, different LAB | $t_{ROW} + t_{LOCAL}$ |
| LE-out | LE in different row | $t_{COL} + t_{ROW} + t_{LOCAL}$ |
| LE-out | IOE on column | $t_{COL}$ |
| LE-out | IOE on row | $t_{ROW}$ |
| IOE on row | LE in same row | $t_{ROW} + t_{LOCAL}$ |
| IOE on column | Any LE | $t_{COL} + t_{ROW} + t_{LOCAL}$ |

## Generic Testing

Each FLEX 8000 device is functionally tested and guaranteed. Complete testing of each configurable SRAM bit and all logic functionality ensures 100% configuration yield. AC test measurements for FLEX 8000 devices are made under conditions equivalent to those shown in Figure 15. Multiple test patterns can be used to configure devices during all stages of the production flow.

*Figure 15. FLEX 8000 AC Test Conditions*

*Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for 3.3-V devices.*




*FLEX 8000 5.0-V Device Absolute Maximum Ratings*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to GND | –2.0 | 7.0 | V |
| $V_I$ | DC input voltage | *Note (1)* | –2.0 | 7.0 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | °C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | °C |
| $T_J$ | Junction temperature | Under bias | | 150 | °C |

### FLEX 8000 5.0-V Device Recommended Operating Conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | With respect to GND, *Note (2)* | 4.75 (4.50) | 5.25 (5.50) | V |
| $V_{CCIO}$ | Supply voltage for output buffers | 5.0-V operation, *Note (2)* | 4.75 (4.50) | 5.25 (5.50) | V |
| | | 3.3-V operation | 3.00 | 3.60 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating temperature | For commercial use | 0 | 70 | °C |
| $T_A$ | Operating temperature | For industrial use | –40 | 85 | °C |
| $T_C$ | Case temperature | For military use | –55 | 125 | °C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

### FLEX 8000 5.0-V Device DC Operating Conditions *Notes (3), (4)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2.0 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | 0.8 | V |
| $V_{OH}$ | 5.0-V high-level TTL output voltage | $I_{OH}$ = –4 mA DC, $V_{CCIO}$ = 4.75 V | 2.4 | | | V |
| | 3.3-V high-level TTL output voltage | $I_{OH}$ = –4 mA DC, $V_{CCIO}$ = 3.00 V | 2.4 | | | V |
| $V_{OL}$ | 5.0-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC, $V_{CCIO}$ = 4.75 V | | | 0.45 | V |
| | 3.3-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC, $V_{CCIO}$ = 3.00 V | | | 0.45 | V |
| $I_I$ | Input leakage current | $V_I$ = $V_{CC}$ or GND | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-state output off-state current | $V_O$ = $V_{CC}$ or GND | –40 | | 40 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) | $V_I$ = GND, No load | | 500 | | µA |

### FLEX 8000 5.0-V Device Capacitance *Note (5)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 10 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 10 | pF |

*Notes to tables:*

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.

(2) Numbers in parentheses are for military- and industrial-temperature-range versions.

(3) Typical values are for $T_A$ = 25° C and $V_{CC}$ = 5.0 V.

(4) Operating conditions:
$V_{CCINT}$ = 5 V ± 5%, $T_A$ = 0° C to 70° C for commercial use.
$V_{CCINT}$ = 5 V ± 10%, $T_A$ = –40° C to 85° C for industrial use.
$V_{CCINT}$ = 5 V ± 10%, $T_A$ = –55° C to 125° C for military use.

(5) Capacitance is sample-tested only.

Figure 16 shows the typical output drive characteristics of 5.0-V FLEX 8000 devices with 5.0-V $V_{CCIO}$. The output driver is compatible with the PCI local bus specification.

*Figure 16. Ouput Drive Characteristics for 5.0-V Devices, 5.0-V $V_{CCIO}$*

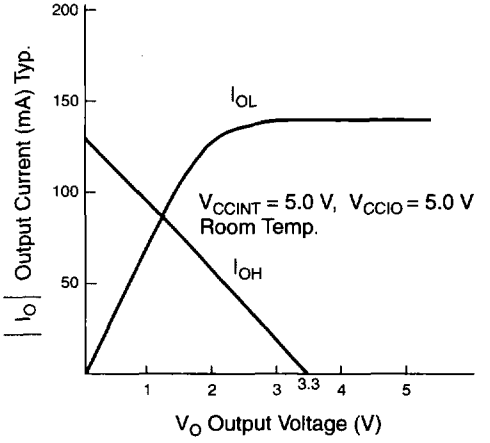
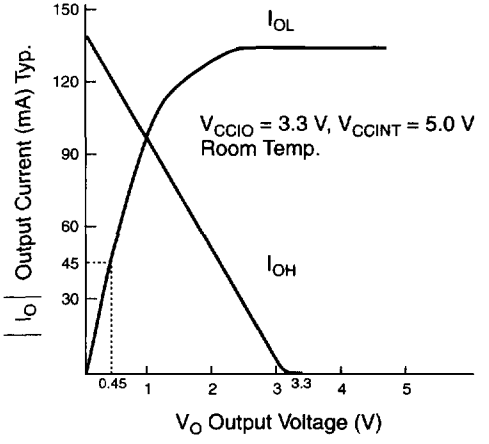



Figure 17 shows the typical output drive characteristics of 5.0-V FLEX 8000 devices with 3.3-V $V_{CCIO}$. The output driver is compatible with the PCI local bus specification.

*Figure 17. Ouput Drive Characteristics for 5.0-V Devices, 3.3-V $V_{CCIO}$*



## FLEX 8000 Internal Timing Characteristics *Note (1)*

| FLEX 8000 I/O Element Timing Parameters (27-Column Devices) | | | EPF81500-2 | | EPF81500-3 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{IOD}$ | IOE register data delay | | | 1.0 | | 2.0 | ns |
| $t_{IOC}$ | IOE register control signal delay | | | 1.0 | | 2.0 | ns |
| $t_{IOE}$ | Output enable delay | | | 1.0 | | 2.0 | ns |
| $t_{IOCO}$ | IOE register clock-to-output delay | | | 1.0 | | 1.0 | ns |
| $t_{IOCOMB}$ | IOE combinatorial delay | | | 0.0 | | 0.0 | ns |
| $t_{IOSU}$ | IOE register setup time before clock | | 2.0 | | 2.0 | | ns |
| $t_{IOH}$ | IOE register hold time after clock | | 0.0 | | 0.0 | | ns |
| $t_{IOCLR}$ | IOE register clear delay | | | 1.2 | | 1.2 | ns |
| $t_{IN}$ | Input pad and buffer delay | | | 1.8 | | 2.8 | ns |
| $t_{OD1}$ | Output buffer and pad delay<br>Slow slew rate = off, $V_{CCIO}$ = 5.0 V | *Note (2)* | | 2.0 | | 2.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay<br>Slow slew rate = off, $V_{CCIO}$ = 3.3 V | *Note (3)* | | 3.0 | | 3.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay<br>Slow slew rate = on | | | 6.0 | | 6.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | | | 2.0 | | 2.0 | ns |
| $t_{ZX}$ | Output buffer enable delay | | | 2.0 | | 2.0 | ns |

| FLEX 8000 Logic Element Timing Parameters (27-Column Devices) | | | EPF81500-2 | | EPF81500-3 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{LUT}$ | LUT delay for data-in | | | 4.1 | | 5.1 | ns |
| $t_{CLUT}$ | LUT delay for carry-in | | | 0.2 | | 1.0 | ns |
| $t_{RLUT}$ | LUT delay for LE register feedback | | | 1.9 | | 3.4 | ns |
| $t_{GATE}$ | Cascade gate delay | | | 0.0 | | 0.0 | ns |
| $t_{CASC}$ | Cascade chain routing delay | | | 1.1 | | 2.0 | ns |
| $t_{CICO}$ | Carry-in to carry-out delay | | | 0.7 | | 1.1 | ns |
| $t_{CGEN}$ | Data-in to carry-out delay | | | 0.7 | | 1.4 | ns |
| $t_{CGENR}$ | LE register feedback to carry-out delay | | | 1.7 | | 2.4 | ns |
| $t_{C}$ | LE register control signal delay | | | 2.8 | | 3.1 | ns |
| $t_{CH}$ | Clock high time | | | 3.5 | | 4.3 | ns |
| $t_{CL}$ | Clock low time | | | 3.5 | | 4.3 | ns |
| $t_{CO}$ | LE register clock-to-output delay | | | 0.4 | | 0.9 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.4 | | 0.9 | ns |
| $t_{SU}$ | LE register setup time before clock | | 1.5 | | 1.7 | | ns |
| $t_{H}$ | LE register hold time after clock | | 2.3 | | 4.0 | | ns |
| $t_{PRE}$ | LE register preset delay | | | 0.7 | | 1.2 | ns |
| $t_{CLR}$ | LE register clear delay | | | 0.7 | | 1.2 | ns |

| FLEX 8000 Interconnect Timing Parameters (27-Column Devices) | | | EPF81500-2 | | EPF81500-3 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{LABCASC}$ | Cascade delay between LEs in different LABs | | | 0.5 | | 0.9 | ns |
| $t_{LABCARRY}$ | Carry delay between LEs in different LABs | | | 0.5 | | 0.6 | ns |
| $t_{LOCAL}$ | LAB local interconnect delay | | | 1.0 | | 1.0 | ns |
| $t_{ROW}$ | Row interconnect routing delay | *Note (4)* | | 6.2 | | 6.2 | ns |
| $t_{COL}$ | Column interconnect routing delay | | | 3.0 | | 3.0 | ns |
| $t_{DIN\_C}$ | Dedicated input to LE control delay | | | 6.0 | | 7.0 | ns |
| $t_{DIN\_D}$ | Dedicated input to LE data delay | *Note (4)* | | 8.0 | | 9.0 | ns |
| $t_{DIN\_IO}$ | Dedicated input to IOE control delay | | | 8.0 | | 9.0 | ns |

### FLEX 8000 External Reference Timing Characteristics (27-Column Devices) *Note (5)*

| | | | EPF81500-2 | | EPF81500-3 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{DRR}$ | Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects | Test circuit CKT1 *Note (6)* | | 34.0 | | 40.2 | ns |

*Notes to tables:*

(1) Internal timing parameters cannot be measured explicitly. The values in these tables are worst-case delays based on testable and guaranteed external parameters. These internal parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(2) $V_{CCIO}$ = 5.0 V ± 5% for commercial use.
$V_{CCIO}$ = 5.0 V ± 10% for industrial use.
$V_{CCIO}$ = 5.0 V ± 10% for military use.

(3) $V_{CCIO}$ = 3.3 V ± 10% for commercial use.
$V_{CCIO}$ = 3.3 V ± 10% for industrial use.
$V_{CCIO}$ = 3.3 V ± 10% for military use.

(4) The $t_{ROW}$ and $t_{DIN\_D}$ delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(5) External reference timing characteristics are factory-tested, guaranteed worst-case values. A representative subset of signal paths is tested to approximate typical device applications.

(6) Contact Altera Applications at (800) 800-EPLD for more information on test conditions.

## *FLEX 8000 Internal Timing Characteristics* *Note (1)*

| ***FLEX 8000 I/O Element Timing Parameters (21-Column Devices)*** | | | EPF81188-2 EPF8820-2 EPF8452-2 | | EPF81188-3 EPF8820-3 EPF8452-3 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{IOD}$ | IOE register data delay | | | 1.0 | | 2.0 | ns |
| $t_{IOC}$ | IOE register control signal delay | | | 1.0 | | 2.0 | ns |
| $t_{IOE}$ | Output enable delay | | | 1.0 | | 2.0 | ns |
| $t_{IOCO}$ | IOE register clock-to-output delay | | | 1.0 | | 1.0 | ns |
| $t_{IOCOMB}$ | IOE combinatorial delay | | | 0.0 | | 0.0 | ns |
| $t_{IOSU}$ | IOE register setup time before clock | | 2.0 | | 2.0 | | ns |
| $t_{IOH}$ | IOE register hold time after clock | | 0.0 | | 0.0 | | ns |
| $t_{IOCLR}$ | IOE register clear delay | | | 1.2 | | 1.2 | ns |
| $t_{IN}$ | Input pad and buffer delay | | | 1.8 | | 2.8 | ns |
| $t_{OD1}$ | Output buffer and pad delay<br>Slow slew rate = off, $V_{CCIO}$ = 5.0 V | *Note (2)* | | 2.0 | | 2.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay<br>Slow slew rate = off, $V_{CCIO}$ = 3.3 V | *Note (3)* | | 3.0 | | 3.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay<br>Slow slew rate = on | | | 6.0 | | 6.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | | | 2.0 | | 2.0 | ns |
| $t_{ZX}$ | Output buffer enable delay | | | 2.0 | | 2.0 | ns |

| ***FLEX 8000 Logic Element Timing Parameters (21-Column Devices)*** | | | EPF81188-2 EPF8820-2 EPF8452-2 | | EPF81188-3 EPF8820-3 EPF8452-3 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{LUT}$ | LUT delay for data-in | | | 4.1 | | 5.1 | ns |
| $t_{CLUT}$ | LUT delay for carry-In | | | 0.2 | | 1.0 | ns |
| $t_{RLUT}$ | LUT delay for LE register feedback | | | 1.9 | | 3.4 | ns |
| $t_{GATE}$ | Cascade gate delay | | | 0.0 | | 0.0 | ns |
| $t_{CASC}$ | Cascade chain routing delay | | | 1.1 | | 2.0 | ns |
| $t_{CICO}$ | Carry-in to carry-out delay | | | 0.7 | | 1.1 | ns |
| $t_{CGEN}$ | Data-in to carry-out delay | | | 0.7 | | 1.4 | ns |
| $t_{CGENR}$ | LE register feedback to carry-out delay | | | 1.7 | | 2.4 | ns |
| $t_{C}$ | LE register control signal delay | | | 2.8 | | 3.1 | ns |
| $t_{CH}$ | Clock high time | | | 3.5 | | 4.3 | ns |
| $t_{CL}$ | Clock low time | | | 3.5 | | 4.3 | ns |
| $t_{CO}$ | LE register clock-to-output delay | | | 0.4 | | 0.9 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.4 | | 0.9 | ns |
| $t_{SU}$ | LE register setup time before clock | | 1.5 | | 1.7 | | ns |
| $t_{H}$ | LE register hold time after clock | | 2.3 | | 4.0 | | ns |
| $t_{PRE}$ | LE register preset delay | | | 0.7 | | 1.2 | ns |
| $t_{CLR}$ | LE register clear delay | | | 0.7 | | 1.2 | ns |

| FLEX 8000 Interconnect Timing Parameters (21-Column Devices) | | | EPF81188-2 EPF8820-2 EPF8452-2 | | EPF81188-3 EPF8820-3 EPF8452-3 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{LABCASC}$ | Cascade delay between LEs in different LABs | | | 0.5 | | 0.9 | ns |
| $t_{LABCARRY}$ | Carry delay between LEs in different LABs | | | 0.5 | | 0.6 | ns |
| $t_{LOCAL}$ | LAB local interconnect delay | | | 1.0 | | 1.0 | ns |
| $t_{ROW}$ | Row interconnect routing delay | *Note (4)* | | 5.0 | | 5.0 | ns |
| $t_{COL}$ | Column interconnect routing delay | | | 3.0 | | 3.0 | ns |
| $t_{DIN\_C}$ | Dedicated input to LE control delay | | | 6.0 | | 7.0 | ns |
| $t_{DIN\_D}$ | Dedicated input to LE data delay | *Note (4)* | | 8.0 | | 9.0 | ns |
| $t_{DIN\_IO}$ | Dedicated input to IOE control delay | | | 8.0 | | 9.0 | ns |

**FLEX 8000 External Reference Timing Characteristics** *Note (5)*

| | | | EPF81188-2 EPF8820-2 EPF8452-2 | | EPF81188-3 EPF8820-3 EPF8452-3 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{DRR}$ | Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects | Test circuit CKT1 *Note (6)* | | 32.0 | | 38.2 | ns |

*Notes to tables:*

(1) Internal timing parameters cannot be measured explicitly. The values in these tables are worst-case delays based on testable and guaranteed external parameters. These internal parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(2) $V_{CCIO}$ = 5.0 V ± 5% for commercial use.
$V_{CCIO}$ = 5.0 V ± 10% for industrial use.
$V_{CCIO}$ = 5.0 V ± 10% for military use.

(3) $V_{CCIO}$ = 3.3 V ± 10% for commercial use.
$V_{CCIO}$ = 3.3 V ± 10% for industrial use.
$V_{CCIO}$ = 3.3 V ± 10% for military use. Not valid for the EPF8282, EPF8282A, EPF8452, or EPF8452A devices.

(4) The $t_{ROW}$ and $t_{DIN\_D}$ delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(5) External reference timing characteristics are factory-tested, guaranteed worst-case values. A representative subset of signal paths is tested to approximate typical device applications.

(6) Contact Altera Applications at (800) 800-EPLD for more information on test conditions.

## *FLEX 8000 Internal Timing Characteristics* *Note (1)*

| *FLEX 8000 I/O Element Timing Parameters (13-Column Devices)* | | | EPF8282-2 | | EPF8282-3 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{IOD}$ | IOE register data delay | | | 1.0 | | 2.0 | ns |
| $t_{IOC}$ | IOE register control signal delay | | | 1.0 | | 2.0 | ns |
| $t_{IOE}$ | Output enable delay | | | 1.0 | | 2.0 | ns |
| $t_{IOCO}$ | IOE register clock-to-output delay | | | 1.0 | | 1.0 | ns |
| $t_{IOCOMB}$ | IOE combinatorial delay | | | 0.0 | | 0.0 | ns |
| $t_{IOSU}$ | IOE register setup time before clock | | 2.0 | | 2.0 | | ns |
| $t_{IOH}$ | IOE register hold time after clock | | 0.0 | | 0.0 | | ns |
| $t_{IOCLR}$ | IOE register clear delay | | | 1.3 | | 1.3 | ns |
| $t_{IN}$ | Input pad and buffer delay | | | 1.8 | | 2.8 | ns |
| $t_{OD1}$ | Output buffer and pad delay<br>Slow slew rate = off, $V_{CCIO}$ = 5.0 V | *Note (2)* | | 2.5 | | 3.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay<br>Slow slew rate = off, $V_{CCIO}$ = 3.3 V | *Note (3)* | | – | | – | ns |
| $t_{OD3}$ | Output buffer and pad delay<br>Slow slew rate = on | | | 6.5 | | 7.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | | | 2.5 | | 3.0 | ns |
| $t_{ZX}$ | Output buffer enable delay | | | 2.5 | | 3.0 | ns |

| *FLEX 8000 Logic Element Timing Parameters (13-Column Devices)* | | | EPF8282-2 | | EPF8282-3 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{LUT}$ | LUT delay for data-in | | | 4.1 | | 5.1 | ns |
| $t_{CLUT}$ | LUT delay for carry-In | | | 0.2 | | 1.0 | ns |
| $t_{RLUT}$ | LUT delay for LE register feedback | | | 1.9 | | 3.4 | ns |
| $t_{GATE}$ | Cascade gate delay | | | 0.0 | | 0.0 | ns |
| $t_{CASC}$ | Cascade chain routing delay | | | 1.1 | | 2.0 | ns |
| $t_{CICO}$ | Carry-in to carry-out delay | | | 0.7 | | 1.1 | ns |
| $t_{CGEN}$ | Data-in to carry-out delay | | | 0.7 | | 1.4 | ns |
| $t_{CGENR}$ | LE register feedback to carry-out delay | | | 1.7 | | 2.4 | ns |
| $t_{C}$ | LE register control signal delay | | | 2.8 | | 3.1 | ns |
| $t_{CH}$ | Clock high time | | | 3.5 | | 4.3 | ns |
| $t_{CL}$ | Clock low time | | | 3.5 | | 4.3 | ns |
| $t_{CO}$ | LE register clock-to-output delay | | | 0.4 | | 0.9 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.4 | | 0.9 | ns |
| $t_{SU}$ | LE register setup time before clock | | 1.5 | | 1.7 | | ns |
| $t_{H}$ | LE register hold time after clock | | 2.3 | | 4.0 | | ns |
| $t_{PRE}$ | LE register preset delay | | | 0.7 | | 1.2 | ns |
| $t_{CLR}$ | LE register clear delay | | | 0.7 | | 1.2 | ns |

| FLEX 8000 Interconnect Timing Parameters (13-Column Devices) | | | EPF8282-2 | | EPF8282-3 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{LABCASC}$ | Cascade delay between LEs in different LABs | | | 0.5 | | 0.9 | ns |
| $t_{LABCARRY}$ | Carry delay between LEs in different LABs | | | 0.5 | | 0.6 | ns |
| $t_{LOCAL}$ | LAB local interconnect delay | | | 1.0 | | 1.0 | ns |
| $t_{ROW}$ | Row interconnect routing delay | *Note (4)* | | 4.2 | | 4.2 | ns |
| $t_{COL}$ | Column interconnect routing delay | | | 2.5 | | 2.5 | ns |
| $t_{DIN\_C}$ | Dedicated input to LE control delay | | | 6.0 | | 7.0 | ns |
| $t_{DIN\_D}$ | Dedicated input to LE data delay | *Note (4)* | | 7.2 | | 8.2 | ns |
| $t_{DIN\_IO}$ | Dedicated input to IOE control delay | | | 7.0 | | 8.0 | ns |

### FLEX 8000 External Reference Timing Characteristics (13-Column Devices) *Note (5)*

| | | | EPF8282-2 | | EPF8282-3 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{DRR}$ | Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects | Test circuit CKT1 *Note (6)* | | 29.3 | | 35.5 | ns |

*Notes to tables:*

(1) Internal timing parameters cannot be measured explicitly. The values in these tables are worst-case delays based on testable and guaranteed external parameters. These internal parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(2) $V_{CCIO}$ = 5.0 V ± 5% for commercial use.
$V_{CCIO}$ = 5.0 V ± 10% for industrial use.
$V_{CCIO}$ = 5.0 V ± 10% for military use.

(3) $V_{CCIO}$ = 3.3 V ± 10% for commercial use.
$V_{CCIO}$ = 3.3 V ± 10% for industrial use.
$V_{CCIO}$ = 3.3 V ± 10% for military use. Not valid for the EPF8282, EPF8282A, EPF8452, or EPF8452A devices.

(4) The $t_{ROW}$ and $t_{DIN\_D}$ delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(5) External reference timing characteristics are factory-tested, guaranteed worst-case values. A representative subset of signal paths is tested to approximate typical device applications.

(6) Contact Altera Applications at (800) 800-EPLD for more information on test conditions.

## *FLEX 8000A Internal Timing Characteristics* *Note (1)*

| ***FLEX 8000A I/O Element Timing Parameters (21-Column Devices)*** | | | EPF81188A-3 EPF8636A-3 EPF8452A-3 | | EPF81188A-4 EPF8636A-4 EPF8452A-4 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{IOD}$ | IOE register data delay | | | 0.8 | | 0.9 | ns |
| $t_{IOC}$ | IOE register control signal delay | | | 0.8 | | 0.9 | ns |
| $t_{IOE}$ | Output enable delay | | | 0.8 | | 0.9 | ns |
| $t_{IOCO}$ | IOE register clock-to-output delay | | | 0.2 | | 0.2 | ns |
| $t_{IOCOMB}$ | IOE combinatorial delay | | | 0.0 | | 0.0 | ns |
| $t_{IOSU}$ | IOE register setup time before clock | | 1.6 | | 1.8 | | ns |
| $t_{IOH}$ | IOE register hold time after clock | | 0.0 | | 0.0 | | ns |
| $t_{IOCLR}$ | IOE register clear delay | | | 1.2 | | 1.2 | ns |
| $t_{IN}$ | Input pad and buffer delay | | | 1.6 | | 1.7 | ns |
| $t_{OD1}$ | Output buffer and pad delay<br>Slow slew rate = off, $V_{CCIO}$ = 5.0 V | *Note (2)* | | 1.0 | | 1.5 | ns |
| $t_{OD2}$ | Output buffer and pad delay<br>Slow slew rate = off, $V_{CCIO}$ = 3.3 V | *Note (3)* | | 2.0 | | 2.5 | ns |
| $t_{OD3}$ | Output buffer and pad delay<br>Slow slew rate = on | | | 4.0 | | 4.5 | ns |
| $t_{XZ}$ | Output buffer disable delay | | | 1.0 | | 1.8 | ns |
| $t_{ZX}$ | Output buffer enable delay | | | 1.0 | | 1.8 | ns |

| ***FLEX 8000A Logic Element Timing Parameters (21-Column Devices)*** | | | EPF81188A-3 EPF8636A-3 EPF8452A-3 | | EPF81188A-4 EPF8636A-4 EPF8452A-4 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{LUT}$ | LUT delay for data-in | | | 2.3 | | 3.0 | ns |
| $t_{CLUT}$ | LUT delay for carry-In | | | 0.2 | | 0.1 | ns |
| $t_{RLUT}$ | LUT delay for LE register feedback | | | 1.6 | | 1.6 | ns |
| $t_{GATE}$ | Cascade gate delay | | | 0.0 | | 0.0 | ns |
| $t_{CASC}$ | Cascade chain routing delay | | | 0.7 | | 0.9 | ns |
| $t_{CICO}$ | Carry-in to carry-out delay | | | 0.5 | | 0.6 | ns |
| $t_{CGEN}$ | Data-in to carry-out delay | | | 0.9 | | 0.8 | ns |
| $t_{CGENR}$ | LE register feedback to carry-out delay | | | 1.4 | | 1.5 | ns |
| $t_{C}$ | LE register control signal delay | | | 1.8 | | 2.4 | ns |
| $t_{CH}$ | Clock high time | | | 1.7 | | 2.7 | ns |
| $t_{CL}$ | Clock low time | | | 1.7 | | 2.7 | ns |
| $t_{CO}$ | LE register clock-to-output delay | | | 0.5 | | 0.6 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.5 | | 0.6 | ns |
| $t_{SU}$ | LE register setup time before clock | | 1.0 | | 1.1 | | ns |
| $t_{H}$ | LE register hold time after clock | | 1.1 | | 1.4 | | ns |
| $t_{PRE}$ | LE register preset delay | | | 0.7 | | 0.8 | ns |
| $t_{CLR}$ | LE register clear delay | | | 0.7 | | 0.8 | ns |

| FLEX 8000A Interconnect Timing Parameters (21-Column Devices) | | | EPF81188A-3 EPF8636A-3 EPF8452A-3 | | EPF81188A-4 EPF8636A-4 EPF8452A-4 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{LABCASC}$ | Cascade delay between LEs in different LABs | | | 0.4 | | 0.4 | ns |
| $t_{LABCARRY}$ | Carry delay between LEs in different LABs | | | 0.4 | | 0.4 | ns |
| $t_{LOCAL}$ | LAB local interconnect delay | | | 0.5 | | 0.7 | ns |
| $t_{ROW}$ | Row interconnect routing delay | *Note (4)* | | 5.0 | | 5.0 | ns |
| $t_{COL}$ | Column interconnect routing delay | | | 3.0 | | 3.0 | ns |
| $t_{DIN\_C}$ | Dedicated input to LE control delay | | | 5.0 | | 5.5 | ns |
| $t_{DIN\_D}$ | Dedicated input to LE data delay | *Note (4)* | | 7.0 | | 7.5 | ns |
| $t_{DIN\_IO}$ | Dedicated input to IOE control delay | | | 7.0 | | 7.5 | ns |

**FLEX 8000A External Reference Timing Characteristics (21-Column Devices)** *Note (5)*

| | | | EPF81188A-3 EPF8636A-3 EPF8452A-3 | | EPF81188A-4 EPF8636A-4 EPF8452A-4 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{DRR}$ | Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects | Test circuit CKT1 *Note (6)* | | 20.0 | | 25.0 | ns |

*Notes to tables:*

(1) Internal timing parameters cannot be measured explicitly. The values in these tables are worst-case delays based on testable and guaranteed external parameters. These internal parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(2) $V_{CCIO}$ = 5.0 V ± 5% for commercial use.
$V_{CCIO}$ = 5.0 V ± 10% for industrial use.
$V_{CCIO}$ = 5.0 V ± 10% for military use.

(3) $V_{CCIO}$ = 3.3 V ± 10% for commercial use.
$V_{CCIO}$ = 3.3 V ± 10% for industrial use.
$V_{CCIO}$ = 3.3 V ± 10% for military use. Not valid for the EPF8282, EPF8282A, EPF8452, or EPF8452A devices.

(4) The $t_{ROW}$ and $t_{DIN\_D}$ delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(5) External reference timing characteristics are factory-tested, guaranteed worst-case values. A representative subset of signal paths is tested to approximate typical device applications.

(6) Contact Altera Applications at (800) 800-EPLD for more information on test conditions.

## *FLEX 8000A Internal Timing Characteristics* *Note (1)*

| ***FLEX 8000A I/O Element Timing Parameters (21-Column Devices)*** | | | EPF81188A-5 EPF8636A-5 EPF8452A-5 | | EPF81188A-6 EPF8452A-6 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{IOD}$ | IOE register data delay | | | 1.0 | | 2.0 | ns |
| $t_{IOC}$ | IOE register control signal delay | | | 1.0 | | 2.0 | ns |
| $t_{IOE}$ | Output enable delay | | | 1.0 | | 2.0 | ns |
| $t_{IOCO}$ | IOE register clock-to-output delay | | | 1.0 | | 1.0 | ns |
| $t_{IOCOMB}$ | IOE combinatorial delay | | | 0.0 | | 0.0 | ns |
| $t_{IOSU}$ | IOE register setup time before clock | | 2.0 | | 2.0 | | ns |
| $t_{IOH}$ | IOE register hold time after clock | | 0.0 | | 0.0 | | ns |
| $t_{IOCLR}$ | IOE register clear delay | | | 1.2 | | 1.2 | ns |
| $t_{IN}$ | Input pad and buffer delay | | | 1.8 | | 2.8 | ns |
| $t_{OD1}$ | Output buffer and pad delay<br>Slow slew rate = off, $V_{CCIO}$ = 5.0 V | *Note (2)* | | 2.0 | | 2.0 | ns |
| $t_{OD2}$ | Output buffer and pad delay<br>Slow slew rate = off, $V_{CCIO}$ = 3.3 V | *Note (3)* | | 3.0 | | 3.0 | ns |
| $t_{OD3}$ | Output buffer and pad delay<br>Slow slew rate = on | | | 5.0 | | 6.0 | ns |
| $t_{XZ}$ | Output buffer disable delay | | | 2.0 | | 2.0 | ns |
| $t_{ZX}$ | Output buffer enable delay | | | 2.0 | | 2.0 | ns |

| ***FLEX 8000A Logic Element Timing Parameters (21-Column Devices)*** | | | EPF81188A-5 EPF8636A-5 EPF8452A-5 | | EPF81188A-6 EPF8452A-6 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{LUT}$ | LUT delay for data-in | | | 3.7 | | 5.1 | ns |
| $t_{CLUT}$ | LUT delay for carry-in | | | 0.1 | | 1.0 | ns |
| $t_{RLUT}$ | LUT delay for LE register feedback | | | 1.9 | | 3.4 | ns |
| $t_{GATE}$ | Cascade gate delay | | | 0.0 | | 0.0 | ns |
| $t_{CASC}$ | Cascade chain routing delay | | | 1.1 | | 2.0 | ns |
| $t_{CICO}$ | Carry-in to carry-out delay | | | 0.7 | | 1.1 | ns |
| $t_{CGEN}$ | Data-in to carry-out delay | | | 0.9 | | 1.4 | ns |
| $t_{CGENR}$ | LE register feedback to carry-out delay | | | 1.8 | | 2.4 | ns |
| $t_{C}$ | LE register control signal delay | | | 2.9 | | 3.1 | ns |
| $t_{CH}$ | Clock high time | | | 3.4 | | 4.3 | ns |
| $t_{CL}$ | Clock low time | | | 3.4 | | 4.3 | ns |
| $t_{CO}$ | LE register clock-to-output delay | | | 0.7 | | 0.9 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.7 | | 0.9 | ns |
| $t_{SU}$ | LE register setup time before clock | | 1.2 | | 1.7 | | ns |
| $t_{H}$ | LE register hold time after clock | | 1.8 | | 4.0 | | ns |
| $t_{PRE}$ | LE register preset delay | | | 0.9 | | 1.2 | ns |
| $t_{CLR}$ | LE register clear delay | | | 0.9 | | 1.2 | ns |

| FLEX 8000A Interconnect Timing Parameters (21-Column Devices) | | | EPF81188A-5 EPF8636A-5 EPF8452A-5 | | EPF81188A-6 EPF8452A-6 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{LABCASC}$ | Cascade delay between LEs in different LABs | | | 0.5 | | 0.9 | ns |
| $t_{LABCARRY}$ | Carry delay between LEs in different LABs | | | 0.5 | | 0.6 | ns |
| $t_{LOCAL}$ | LAB local interconnect delay | | | 0.9 | | 1.0 | ns |
| $t_{ROW}$ | Row interconnect routing delay | *Note (4)* | | 5.0 | | 5.0 | ns |
| $t_{COL}$ | Column interconnect routing delay | | | 3.0 | | 3.0 | ns |
| $t_{DIN\_C}$ | Dedicated input to LE control delay | | | 6.0 | | 7.0 | ns |
| $t_{DIN\_D}$ | Dedicated input to LE data delay | *Note (4)* | | 8.0 | | 9.0 | ns |
| $t_{DIN\_IO}$ | Dedicated input to IOE control delay | | | 7.0 | | 9.0 | ns |

**FLEX 8000A External Reference Timing Characteristics (21-Column Devices)** *Note (5)*

| | | | EPF81188A-5 EPF8636A-5 EPF8452A-5 | | EPF81188A-6 EPF8452A-6 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{DRR}$ | Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects | Test circuit CKT1 *Note (6)* | | 30.0 | | 38.2 | ns |

*Notes to tables:*

(1) Internal timing parameters cannot be measured explicitly. The values in these tables are worst-case delays based on testable and guaranteed external parameters. These internal parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(2) $V_{CCIO}$ = 5.0 V ± 5% for commercial use.
$V_{CCIO}$ = 5.0 V ± 10% for industrial use.
$V_{CCIO}$ = 5.0 V ± 10% for military use.

(3) $V_{CCIO}$ = 3.3 V ± 10% for commercial use.
$V_{CCIO}$ = 3.3 V ± 10% for industrial use.
$V_{CCIO}$ = 3.3 V ± 10% for military use. Not valid for the EPF8282, EPF8282A, EPF8452, or EPF8452A devices.

(4) The $t_{ROW}$ and $t_{DIN\_D}$ delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(5) External reference timing characteristics are factory-tested, guaranteed worst-case values. A representative subset of signal paths is tested to approximate typical device applications.

(6) Contact Altera Applications at (800) 800-EPLD for more information on test conditions.

## Calculating Supply Current for 5.0-V FLEX 8000 Devices

The $V_{CC}$ supply current for 5.0-V FLEX 8000 devices, $I_{CC}$, can be calculated with the following equation:

$$I_{CC} = I_{CCSTANDBY} + I_{CCOUTPUT} + I_{CCACTIVE}$$

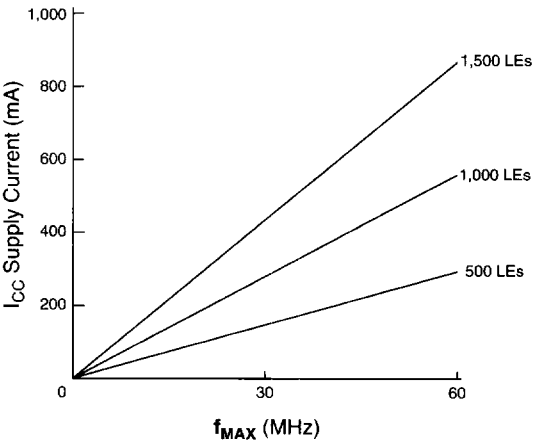
Typical $I_{CCSTANDBY}$ values are shown as $I_{CC0}$ in the "FLEX 8000 5.0-V Device DC Operating Conditions" table earlier in this data sheet. The $I_{CCOUTPUT}$ value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Operating Requirements for Altera Devices* in the current ***Data Book***. The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value can be calculated on the basis of the relationship that each LE typically consumes 75 µA/MHz. The following equation shows the general formula for calculating $I_{CCACTIVE}$:

$$I_{CCACTIVE} = 75 \times \frac{\mu A}{MHz \bullet LE} \times F \times N \times 0.125$$

In this equation, F is the maximum operating frequency in MHz; N is the number of LEs used in the device. The total is multiplied by 0.125, which is based on a 16-bit counter in which 2 out of 16 (12.5%) of the output bits switch on each Clock edge.

Figure 18 shows the relationship between $I_{CC}$ and operating frequency for LE utilization values ranging from 500 to 1,500 LEs.

***Figure 18. FLEX 8000 $I_{CCACTIVE}$ vs. Operating Frequency***



### FLEX 8000 3.3-V Device Absolute Maximum Ratings

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to GND | –2.0 | 7.0 | V |
| $V_I$ | DC input voltage | *Note (1)* | –2.0 | 7.0 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | °C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | °C |
| $T_J$ | Junction temperature | Under bias | | 150 | °C |

### FLEX 8000 3.3-V Device Recommended Operating Conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to GND | 3.0 | 3.6 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating temperature | For commercial use | 0 | 70 | °C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

### FLEX 8000 3.3-V Device DC Operating Conditions *Note (2)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2.0 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 0.1 mA DC | $V_{CC}$ – 0.2 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 4 mA DC | | | 0.45 | V |
| $I_I$ | Input leakage current | $V_I$ = $V_{CC}$ or GND | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-state output off-state current | $V_O$ = $V_{CC}$ or GND | –40 | | 40 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) | $V_I$ = GND, No load, *Note (3)* | | 300 | | µA |

### FLEX 8000 3.3-V Device Capacitance *Note (4)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 10 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 10 | pF |

## *FLEX 8000 3.3-Volt Device Internal Timing Characteristics* *Note (1)*

| ***EPF8282V I/O Element (IOE) Timing Parameters*** | | | EPF8282V-3 | | EPF8282V-4 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{IOD}$ | IOE register data delay | | | 2.2 | | 3.5 | ns |
| $t_{IOC}$ | IOE register control signal delay | | | 2.0 | | 3.4 | ns |
| $t_{IOE}$ | Output enable delay | | | 2.0 | | 3.4 | ns |
| $t_{IOCO}$ | IOE register clock-to-output delay | | | 2.0 | | 3.0 | ns |
| $t_{IOCOMB}$ | IOE combinatorial delay | | | 0.0 | | 0.0 | ns |
| $t_{IOSU}$ | IOE register setup time before clock | | 2.8 | | 4.7 | | ns |
| $t_{IOH}$ | IOE register hold time after clock | | 0.2 | | 0.1 | | ns |
| $t_{IOCLR}$ | IOE register clear delay | | | 2.3 | | 3.5 | ns |
| $t_{IN}$ | Input pad and buffer delay | | | 3.4 | | 5.4 | ns |
| $t_{OD1}$ | Output buffer and pad delay<br>Slow slew rate = off, $V_{CCIO}$ = 3.3 V | *Note (2)* | | 3.1 | | 5.6 | ns |
| $t_{OD2}$ | Output buffer and pad delay<br>Slow slew rate = off, $V_{CCIO}$ = 5.0 V | *Note (5)* | | – | | – | ns |
| $t_{OD3}$ | Output buffer and pad delay<br>Slow slew rate = on | | | 7.1 | | 9.6 | ns |
| $t_{XZ}$ | Output buffer disable delay | | | 4.3 | | 6.7 | ns |
| $t_{ZX}$ | Output buffer enable delay | | | 4.3 | | 6.7 | ns |

| ***EPF8282V Logic Element (LE) Timing Parameters*** | | | EPF8282V-3 | | EPF8282V-4 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{LUT}$ | LUT delay for data-in | | | 7.3 | | 14.3 | ns |
| $t_{CLUT}$ | LUT delay for carry-in | | | 1.4 | | 1.3 | ns |
| $t_{RLUT}$ | LUT delay for LE register feedback | | | 5.1 | | 7.3 | ns |
| $t_{GATE}$ | Cascade gate delay | | | 0.0 | | 0.0 | ns |
| $t_{CASC}$ | Cascade chain routing delay | | | 2.8 | | 4.2 | ns |
| $t_{CICO}$ | Carry-in to carry-out delay | | | 1.5 | | 2.2 | ns |
| $t_{CGEN}$ | Data-in to carry-out delay | | | 2.2 | | 4.5 | ns |
| $t_{CGENR}$ | LE register feedback to carry-out delay | | | 3.7 | | 6.0 | ns |
| $t_{C}$ | LE register control signal delay | | | 4.7 | | 9.5 | ns |
| $t_{CH}$ | Clock high time | | | 6.0 | | 10.5 | ns |
| $t_{CL}$ | Clock low time | | | 6.0 | | 10.5 | ns |
| $t_{CO}$ | LE register clock-to-output delay | | | 0.9 | | 0.9 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 0.9 | | 0.9 | ns |
| $t_{SU}$ | LE register setup time before clock | | 2.4 | | 4.4 | | ns |
| $t_{H}$ | LE register hold time after clock | | 4.6 | | 6.8 | | ns |
| $t_{PRE}$ | LE register preset delay | | | 1.3 | | 1.6 | ns |
| $t_{CLR}$ | LE register clear delay | | | 1.3 | | 1.6 | ns |

| EPF8282V Interconnect Timing Parameters | | | EPF8282V-3 | | EPF8282V-4 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{LABCASC}$ | Cascade delay between LEs in different LABs | | | 1.3 | | 2.0 | ns |
| $t_{LABCARRY}$ | Carry delay between LEs in different LABs | | | 0.8 | | 1.2 | ns |
| $t_{LOCAL}$ | LAB local interconnect delay | | | 1.5 | | 1.5 | ns |
| $t_{ROW}$ | Row interconnect routing delay | *Note (3)* | | 6.3 | | 6.3 | ns |
| $t_{COL}$ | Column interconnect routing delay | | | 3.8 | | 3.8 | ns |
| $t_{DIN\_C}$ | Dedicated input to LE control delay | | | 8.0 | | 10.3 | ns |
| $t_{DIN\_D}$ | Dedicated input to LE data delay | | | 9.8 | | 12.3 | ns |
| $t_{DIN\_IO}$ | Dedicated input to IOE control delay | | | 10.0 | | 12.3 | ns |

### FLEX 8000 3.3-V External Reference Timing Characteristics (13-Column Devices) *Note (4)*

| | | | EPF8282V-3 | | EPF8282V-4 | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{DRR}$ | Register-to-register delay via 4 LEs, 3 row interconnects, and 4 local interconnects | Test circuit CKT1 *Note (6)* | | 50.4 | | 80.4 | ns |

*Notes to tables:*

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.

(2) $V_{CCIO}$ = 3.3 V ± 10% for commercial use.
$V_{CCIO}$ = 3.3 V ± 10% for industrial use.
$V_{CCIO}$ = 3.3 V ± 10% for military use.

(3) The $t_{ROW}$ and $t_{DIN\_D}$ delays are worst-case values for typical applications. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

(4) Capacitance is sample-tested only.

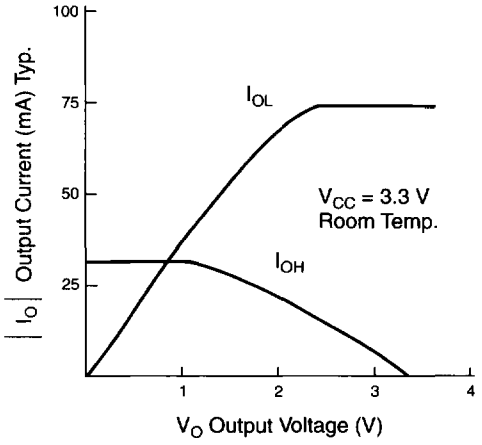
(5) Not valid for the EPF8282V device.

(6) Internal timing parameters cannot be measured explicitly. The values in these tables are worst-case delays based on testable and guaranteed external parameters. These internal parameters should be used for estimating device performance. Post-compilation timing simulation or timing analysis is required to determine actual worst-case performance.

## Calculating Supply Current for 3.3-V FLEX 8000 Devices

Figure 19 shows the typical output drive characteristics of EPF8282V I/O pins.

***Figure 19. EPF8282V Typical Output Drive Characteristics***




The $V_{CC}$ supply current for 3.3-V FLEX 8000 devices, $I_{CC}$, can be calculated with the following equation:

$$I_{CC} = I_{CCSTANDBY} + I_{CCOUTPUT} + I_{CCACTIVE}$$

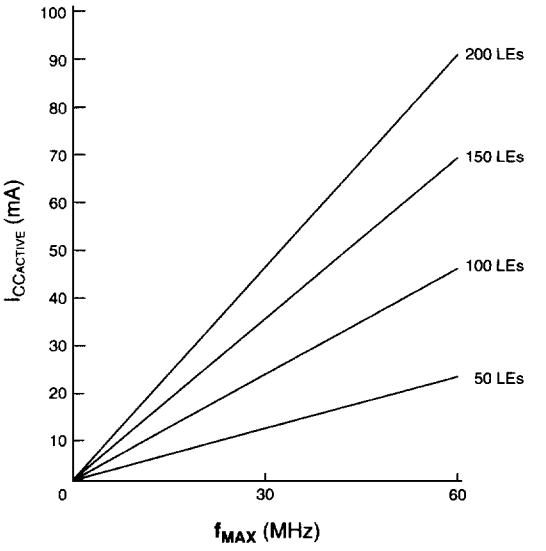
Typical $I_{CCSTANDBY}$ values are shown as $I_{CC0}$ in the "FLEX 8000 3.3-V Device DC Operating Conditions" table earlier in this data sheet. The $I_{CCOUTPUT}$ value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Operating Requirements for Altera Devices* in the current ***Data Book.*** The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. This value can be based on a typical current consumption of 60 µA/MHz per LE. The following equation shows the general formula for calculating $I_{CCACTIVE}$:

$$I_{CCACTIVE} = 60 \times \frac{\mu A}{MHz \bullet LE} \times F \times N \times 0.125$$

In this equation, F is the maximum operating frequency in MHz and N is the number of LEs used in the device. The equation is multiplied by the typical percentage of LEs that switch on each Clock edge. The value 0.125 is based on a 16-bit counter in which 2 out of 16 (12.5%) of the bits switch on each Clock edge.

Figure 20 shows the relationship between $I_{CCACTIVE}$ and the operating frequency for LE utilization values ranging from 50 to 200 LEs.

*Figure 20. EPF8282V $I_{CCACTIVE}$ vs. Operating Frequency*




# Configuration & Operation

The FLEX 8000 architcture supports several configuration schemes to load a design into the device(s) on the circuit board. This data sheet summarizes the device operating modes and available device configuration schemes. Refer to *Application Note 33 (Configuring FLEX 8000 Devices)* and *Application Note 38 (Configuring Multiple FLEX 8000 Devices)* for detailed descriptions of device configuration options; device configuration pins; and information on configuring FLEX 8000 devices, including sample schematics, timing diagrams, and configuration parameters.

## Operating Modes

The FLEX 8000 architecture uses SRAM technology that requires configuration data to be loaded whenever the circuit powers up and begins operation. The process of physically loading the SRAM programming data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The configuration and initialization processes together are called "command mode"; normal device operation is called "user mode."

The SRAM technology allows FLEX 8000 devices to be reconfigured in-circuit by loading new programming data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different programming data, reinitializing the device, and resuming user-mode operation. The entire reconfiguration process requires less than 100 ms and can be used to dynamically reconfigure an entire system. In-field upgrades can be performed by distributing new configuration files.

## Configuration Schemes

The configuration data for a FLEX 8000 device can be loaded with one of six configuration schemes, chosen on the basis of the target application. Both active and passive schemes are available. In the active configuration schemes, the FLEX 8000 device functions as the controller, directing the loading operation, controlling external EPROM devices, and completing the loading process. The Clock source for all active configuration schemes is an oscillator on the FLEX 8000 device that operates between 2 MHz and 6 MHz. In the passive configuration schemes, an external controller guides the FLEX 8000 device, which operates as a slave. Table 6 shows the source of data for each of the six configuration schemes.

*Table 6. Configuration Schemes*

| Configuration Scheme | Acronym | Data Source |
|---|---|---|
| Active serial | AS | Altera Configuration EPROM |
| Active parallel up | APU | Parallel EPROM |
| Active parallel down | APD | Parallel EPROM |
| Passive serial | PS | Serial data path |
| Passive parallel synchronous | PPS | Intelligent host |
| Passive parallel asynchronous | PPA | Intelligent host |

## MAX+PLUS II Development System

FLEX 8000 devices are supported by Altera's MAX+PLUS II development system. MAX+PLUS II also supports the Altera Classic, MAX 5000, and MAX 7000 device families.

Designs can be entered as logic schematics with the Graphic Editor; as state machines, truth tables, conditional logic, and Boolean equations with the Altera Hardware Description Language (AHDL), VHSIC Hardware Description Language (VHDL), or Verilog HDL; or as waveforms with the Waveform Editor. Logic synthesis and minimization automatically optimize the logic of a design. MAX+PLUS II also provides automatic design partitioning into multiple devices from the same family. Design verification and timing analysis are performed with the built-in Simulator and Timing Analyzer. Errors in a design can be automatically located and highlighted in the original design files.

MAX+PLUS II software runs on 486- and Pentium-based PCs, as well as Sun SPARCstations, HP 9000 Series 700, and DEC Alpha AXP workstations. It gives designers the tools to create complex logic designs quickly and efficiently. MAX+PLUS II provides an EDIF netlist interface for additional design entry and simulation support with popular CAE tools from Cadence, Mentor Graphics, Synopsys, Viewlogic, Intergraph, Logic Modeling, and others. MAX+PLUS II also exports Verilog HDL and VHDL netlist files for use with other industry-standard design verification tools.

Altera's FLEX 8000-compatible programming hardware includes the Altera Logic Programmer card, the Master Programming Unit (MPU), and various device adapters. The MPU supports continuity checking to ensure adequate electrical contact between the adapter and the device. Configuration EPROM device adapters are shipped with the FLEX Download Cable, which allows users to configure FLEX 8000 devices in-circuit with Altera programming hardware and the MAX+PLUS II Programmer. For more information on programming hardware, see *Altera Programming Hardware* in the current Altera ***Data Book***. FLEX 8000 devices can also be configured in-circuit via a standard RS-232 serial port from a workstation or PC using the BitBlaster, a hardware box that provides a download cable to a FLEX 8000 device. For more information on the BitBlaster, refer to the *BitBlaster Serial Download Cable Data Sheet*. Further details about the MAX+PLUS II development system are available in the current *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*.

## Thermal Characteristics

The following formulas are used to calculate the maximum allowed power ($P_{MAX}$) for a device:

$$P_{MAX} = \frac{150°C - T_{AMB}}{\theta_{JA}}$$

or

$$P_{MAX} = \frac{150°C - T_C}{\theta_{JC}}$$

The maximum allowable power is dependent on the maximum allowable junction temperature of the silicon ($T_J$), the ambient temperature of operation ($T_{AMB}$), and the package's thermal resistance ($\theta_J$) when operating in the system. $\theta_{JC}$ is a measure of the lowest possible thermal resistance and is used to calculate maximum power when the case temperature ($T_{CASE}$) of the device is known. The maximum junction temperature for all FLEX 8000 devices is 150° C. The ambient temperature is dependent on the application. Table 7 lists the thermal resistance values for junction-to-case ($\theta_{JC}$), and junction-to-ambient ($\theta_{JA}$) over different air-flow conditions.

*Table 7. Thermal Resistance for FLEX 8000 Devices* *Note (1)*

| Device | Pin Count | Package | $\theta_{JC}$ (C/W) | $\theta_{JA}$ (C/W) Still Air | $\theta_{JA}$ (C/W) 100 ft./min. | $\theta_{JA}$ (C/W) 200 ft./min. | $\theta_{JA}$ (C/W) 400 ft./min. |
|---|---|---|---|---|---|---|---|
| EPF8282 | 84 | PLCC | 11 | 35 | 23, *Note (2)* | 18, *Note (2)* | 14, *Note (2)* |
| EPF8282V | 100 | TQFP | C.F. | C.F. | C.F. | C.F. | C.F. |
| EPF8452 | 84 | PLCC | 11 | 35 | 23, *Note (2)* | 18, *Note (2)* | 14, *Note (2)* |
| EPF8452A | 160 | PQFP | 7 | 40 | 26, *Note (2)* | 20, *Note (2)* | 16, *Note (2)* |
| | 160 | PGA | 6 | 20 | 13, *Note (2)* | 10, *Note (2)* | 8, *Note (2)* |
| EPF8636A | 84 | PLCC | 11, *Note (2)* | 35, *Note (2)* | 23, *Note (2)* | 18, *Note (2)* | 14, *Note (2)* |
| | 192 | PGA | 6 | 16 | 11, *Note (2)* | 8, *Note (2)* | 6, *Note (2)* |
| | 208 | RQFP | 2 | 18 | 12 | 9 | 7 |
| EPF8820 | 192 | PGA | 6 | 16 | 11, *Note (2)* | 8, *Note (2)* | 6, *Note (2)* |
| | 208 | RQFP | 2 | 18 | 12 | 9 | 7 |
| | 225 | BGA | 6 | 28 | 19 | 14 | 11 |
| EPF81188 | 232 | PGA | 2 | 14 | 10 | 7 | 5 |
| EPF81188A | 240 | RQFP | 2 | 20 | 13, *Note (2)* | 10, *Note (2)* | 8, *Note (2)* |
| EPF81500 | 280 | PGA | 2, *Note (2)* | 14, *Note (2)* | 10, *Note (2)* | 7, *Note (2)* | 5, *Note (2)* |
| | 304 | RQFP | 2, *Note (2)* | 20, *Note (2)* | 13, *Note (2)* | 10, *Note (2)* | 8, *Note (2)* |

*Notes:*
(1) This table is based on an ambient temperature ($T_{AMB}$) of 25° C.
(2) This information is preliminary.

## Device Pin-Outs

Tables 8 through 10 show the pin names and numbers for each FLEX 8000 device package.

*Table 8. FLEX 8000 84-, 100- & 160-Pin Package Pin-Outs (Part 1 of 2)*

| Pin Name | 84-Pin PLCC EPF8452 EPF8452A EPF8636A | 84-Pin PLCC EPF8282 | 100-Pin TQFP EPF8282 | 160-Pin PGA EPF8452 EPF8452A | 160-Pin PQFP EPF8452 EPF8452A |
|---|---|---|---|---|---|
| nSP *(1)* | 75 | 75 | 75 | R1 | 120 |
| MSEL0 *(1)* | 74 | 74 | 74 | P2 | 117 |
| MSEL1 *(1)* | 53 | 53 | 51 | A1 | 84 |
| nSTATUS *(1)* | 32 | 32 | 24 | C13 | 37 |
| nCONFIG *(1)* | 33 | 33 | 25 | A15 | 40 |
| DCLK *(1)* | 10 | 10 | 100 | P14 | 1 |
| nWS | 30 | 30 | 22 | F13 | 30 |
| CONF_DONE *(1)* | 11 | 11 | 1 | N13 | 4 |
| nRS | 48 | 48 | 42 | C6 | 71 |
| RDCLK | 49 | 49 | 45 | B5 | 73 |
| nCS | 29 | 29 | 21 | D15 | 29 |
| CS | 28 | 28 | 19 | E15 | 27 |
| RDYnBUSY | 77 | 77 | 77 | P3 | 125 |
| CLKUSR | 50 | 50 | 47 | C5 | 76 |
| ADD17 | 51 | 51 | 49 | B4 | 78 |
| ADD16 | 55 | 36 | 28 | E2 | 91 |
| ADD15 | 56 | 56 | 55 | D1 | 92 |
| ADD14 | 57 | 57 | 57 | E1 | 94 |
| ADD13 | 58 | 58 | 58 | F3 | 95 |
| ADD12 | 60 | 60 | 59 | F2 | 96 |
| ADD11 | 61 | 61 | 60 | F1 | 97 |
| ADD10 | 62 | 62 | 61 | G2 | 98 |
| ADD9 | 63 | 63 | 62 | G1 | 99 |
| ADD8 | 64 | 64 | 64 | H1 | 101 |
| ADD7 | 65 | 65 | 65 | H2 | 102 |
| ADD6 | 66 | 66 | 66 | J1 | 103 |
| ADD5 | 67 | 67 | 67 | J2 | 104 |
| ADD4 | 69 | 69 | 68 | K2 | 105 |
| ADD3 | 70 | 70 | 69 | K1 | 106 |
| ADD2 | 71 | 71 | 71 | K3 | 109 |
| ADD1 | 72 | 76 | 76 | M1 | 110 |

*Table 8. FLEX 8000 84-, 100- & 160-Pin Package Pin-Outs (Part 2 of 2)*

| Pin Name | 84-Pin PLCC EPF8452 EPF8452A EPF8636A | 84-Pin PLCC EPF8282 | 100-Pin TQFP EPF8282 | 160-Pin PGA EPF8452 EPF8452A | 160-Pin PQFP EPF8452 EPF8452A |
|---|---|---|---|---|---|
| ADD0 | 76 | 78 | 78 | N3 | 123 |
| DATA7 | 2 | 3 | 90 | P8 | 144 |
| DATA6 | 4 | 4 | 91 | P10 | 150 |
| DATA5 | 6 | 6 | 92 | R12 | 152 |
| DATA4 | 7 | 7 | 95 | R13 | 154 |
| DATA3 | 8 | 8 | 97 | P13 | 157 |
| DATA2 | 9 | 9 | 99 | R14 | 159 |
| DATA1 | 13 | 13 | 4 | N15 | 11 |
| DATA0 | 14 | 14 | 5 | K13 | 12 |
| TDI *(2)* | 45 *(3)* | 55 | 54 | – | – |
| TDO *(2)* | 27 *(3)* | 27 | 18 | – | – |
| TCLK *(2)* | 44 *(3)* | 72 | 72 | – | – |
| TMS *(2)* | 43 *(3)* | 20 | 11 | – | – |
| nTRST *(1)* | 52 *(4)* | 52 | 50 | – | – |
| Dedicated Inputs | 12, 31, 54, 73 | 12, 31, 54, 73 | 3, 23, 53, 73 | C3, D14, N2, R15 | 5, 36, 85, 116 |
| VCC | 17, 38, 59, 80 | 17, 38, 59, 80 | 6, 20, 37, 56, 70, 87 | B2, C4, D3, D8, D12, G3, G12, H4, H13, J3, J12, M4, M7, M9, M13, N12 | 21, 41, 53, 67, 80, 81, 100, 121, 133, 147, 160 |
| GND | 5, 26, 47, 68 | 5, 26, 47, 68 | 2, 13, 30, 44, 52, 63, 80, 94 | C12, D4, D7, D9, D13, G4, G13, H3, H12, J4, J13, L1, M3, M8, M12, M15, N4 | 13, 14, 28, 46, 60, 75, 93, 107, 108, 126, 140, 155 |
| No Connect (N.C.) | – | – | – | – | 2, 3, 38, 39, 70, 82, 83, 118, 119, 148 |
| Total User I/O Pins | 64 | 64 | 74 | 116 | 116 |

*Notes to Table 8:*

(1) Dedicated pin (not available as a user I/O pin).
(2) If the device is not configured to use the JTAG BST circuitry, this pin is available as a user I/O pin.
(3) Dedicated JTAG pins are available for EPF8636A devices only. No dedicated JTAG pins are available for EPF8452 and EPF8452A devices.
(4) Pin 52 is a $V_{CC}$ pin on EPF8452 and EPF8452A devices only.

*Table 9. FLEX 8000 192-, 208- & 225-Pin Package Pin-Outs (Part 1 of 3)*

| Pin Name | 192-Pin PGA EPF8636A EPF8820 | 208-Pin RQFP EPF8636A | 208-Pin RQFP EPF8820 | 225-Pin BGA EPF8820 |
|---|---|---|---|---|
| nSP *(1)* | R15 | 207 | 207 | A15 |
| MSEL0 *(1)* | T15 | 4 | 4 | B14 |
| MSEL1 *(1)* | T3 | 49 | 49 | R15 |
| nSTATUS *(1)* | B3 | 108 | 108 | P2 |
| nCONFIG *(1)* | C3 | 103 | 103 | R1 |
| DCLK *(1)* | C15 | 158 | 158 | B2 |
| CONF_DONE *(1)* | B15 | 153 | 153 | A1 |
| nWS | C5 | 114 | 114 | L4 |
| nRS | B5 | 66 | 116 | K5 |
| RDCLK | C11 | 64 | 137 | F1 |
| nCS | B13 | 116 | 145 | D1 |
| CS | A16 | 118 | 148 | C1 |
| RDYnBUSY | A8 | 201 | 127 | J3 |
| CLKUSR | A10 | 59 | 134 | G2 |
| ADD17 | R5 | 57 | 43 | M14 |
| ADD16 | U3 | 43 | 42 | L12 |
| ADD15 | T5 | 41 | 41 | M15 |
| ADD14 | U4 | 39 | 40 | L13 |
| ADD13 | R6 | 37 | 39 | L14 |
| ADD12 | T6 | 31 | 35 | K13 |
| ADD11 | R7 | 30 | 33 | K15 |
| ADD10 | T7 | 29 | 31 | J13 |

*Table 9. FLEX 8000 192-, 208- & 225-Pin Package Pin-Outs (Part 2 of 3)*

| Pin Name | 192-Pin PGA EPF8636A EPF8820 | 208-Pin RQFP EPF8636A | 208-Pin RQFP EPF8820 | 225-Pin BGA EPF8820 |
|---|---|---|---|---|
| ADD9 | T8 | 28 | 29 | J15 |
| ADD8 | U9 | 24 | 25 | G14 |
| ADD7 | U10 | 23 | 23 | G13 |
| ADD6 | U11 | 22 | 21 | G11 |
| ADD5 | U12 | 21 | 19 | F14 |
| ADD4 | R12 | 14 | 14 | E13 |
| ADD3 | U14 | 12 | 13 | D15 |
| ADD2 | U15 | 10 | 11 | D14 |
| ADD1 | R13 | 8 | 10 | E12 |
| ADD0 | U16 | 203 | 9 | C15 |
| DATA7 | H17 | 178 | 178 | A7 |
| DATA6 | G17 | 172 | 176 | D7 |
| DATA5 | F17 | 169 | 174 | A6 |
| DATA4 | E17 | 165 | 172 | A5 |
| DATA3 | G15 | 162 | 171 | B5 |
| DATA2 | F15 | 160 | 167 | E6 |
| DATA1 | E16 | 149 | 165 | D5 |
| DATA0 | C16 | 147 | 162 | C4 |
| TDI *(2)* | R11 | 72 | 20 | F15 |
| TDO *(2)* | B9 | 120 | 129 | J2 |
| TCLK *(2)* | U8 | 74 | 30 | J14 |
| TMS *(2)* | U7 | 76 | 32 | J12 |
| nTRST *(1)* | R3 | 54 | 54 | P14 |

*Table 9. FLEX 8000 192-, 208- & 225-Pin Package Pin-Outs (Part 3 of 3)*

| Pin Name | 192-Pin PGA EPF8636A EPF8820 | 208-Pin RQFP EPF8636A | 208-Pin RQFP EPF8820 | 225-Pin BGA EPF8820 |
|---|---|---|---|---|
| Dedicated Inputs | A5, U5, U13, A13 | 7, 45, 112, 150 | 17, 36, 121, 140 | F4, L1, K12, E15 |
| $V_{CCINT}$ (5.0 V) | C8, C9, C10, R8, R9, R10, R14 | 5, 6, 33, 110, 137, | 5, 6, 27, 48, 119, 141 | F5, F10, E1, L2, K4, M12, P15, H13, H14, B15, C13 |
| $V_{CCIO}$ (5.0 V or 3.3 V) | D3, D4, D9, D14, D15, G4, G14, L4, L14, P4, P9, P14 | 32, 55 ,78, 91, 102, 138, 159, 182, 193, 206 | 26, 55, 69, 87, 102, 131, 159, 173, 191, 206 | H3, H2, P6, R6, P10, N10, R14, N13, H15, H12, D12, A14, B10, A10, B6, C6, A2, C3, M4, R2 |
| GND | C4, D7, D8, D10, D11, H4, H14, K4, K14, P7, P8, P10, P11 | 19, 20, 46, 47, 60, 67, 96, 109, 111, 124, 125, 151, 164, 171, 200 | 15, 16, 37, 38, 60, 78, 96, 109, 110, 120, 130, 142, 152, 164, 182, 200 | B1, D4, E14, F7, F8, F9, F12, G6, G7, G8, G9, G10, H1, H4, H5, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, K6, K7, K8, K9, K11, L15, N3, P1 |
| No Connect (N.C.) | C6, C12, C13, C14, E3, E15, F3, J3, J4, J14, J15, N3, N15, P3, P15, R4 *(3)* | 1, 2, 3, 16, 17, 18, 25, 26, 27, 34, 35, 36, 50, 51, 52, 53, 104, 105, 106, 107, 121, 122, 123, 130, 131, 132, 139, 140, 141, 154, 155, 156, 157, 208 | 1, 2, 3, 50, 51, 52, 53, 104, 105, 106, 107, 154, 155, 156, 157, 208 | – |
| Total User I/O Pins | 132 *(4)* | 132 | 148 | 148 |

*Notes to Table 9:*
(1) Dedicated pin (not available as a user I/O pin).
(2) Available as a user I/O pin if device is not configured to use JTAG BST circuitry.
(3) These pins are No Connect pins only for EPF8636A devices, not for EPF8820 devices.
(4) The EPF8636A device has 132 user I/O pins; the EPF8820 device has 148 user I/O pins.

*Table 10. FLEX 8000 232-, 240-, 280 & 304-Pin Package Pin-Outs (Part 1 of 3)*

| Pin Name | 232-Pin PGA EPF81188 EPF81188A | 240-Pin QFP EPF81188 EPF81188A | 280-Pin PGA EPF85100 | 304-Pin RQFP EPF81500 |
|---|---|---|---|---|
| nSP *(1)* | C14 | 237 | W1 | 304 |
| MSEL0 *(1)* | G15 | 21 | N1 | 26 |
| MSEL1 *(1)* | L15 | 40 | H3 | 51 |
| nSTATUS *(1)* | L3 | 141 | G19 | 178 |
| nCONFIG *(1)* | R4 | 117 | B18 | 152 |
| CONF_DONE *(1)* | G3 | 160 | M16 | 204 |
| DCLK *(1)* | C4 | 184 | U18 | 230 |
| nWS | P1 | 133 | F18 | 167 |
| nRS | N1 | 137 | G18 | 171 |
| RDCLK | G2 | 158 | M17 | 202 |
| nCS | E2 | 166 | N16 | 212 |
| CS | E3 | 169 | N18 | 215 |
| RDYnBUSY | K2 | 146 | J17 | 183 |
| CLKUSR | H2 | 155 | K19 | 199 |
| ADD17 | R15 | 58 | E3 | 73 |
| ADD16 | T17 | 56 | E2 | 71 |
| ADD15 | P15 | 54 | F4 | 69 |
| ADD14 | M14 | 47 | G1 | 60 |
| ADD13 | M15 | 45 | H2 | 58 |
| ADD12 | M16 | 43 | H1 | 56 |
| ADD11 | K15 | 36 | J3 | 47 |
| ADD10 | K17 | 34 | K3 | 45 |
| ADD9 | J14 | 32 | K4 | 43 |
| ADD8 | J15 | 29 | L1 | 34 |
| ADD7 | H17 | 27 | L2 | 32 |
| ADD6 | H15 | 25 | M1 | 30 |
| ADD5 | F16 | 18 | N2 | 20 |
| ADD4 | F15 | 16 | N3 | 18 |
| ADD3 | F14 | 14 | N4 | 16 |
| ADD2 | D15 | 7 | U1 | 8 |
| ADD1 | B17 | 5 | U2 | 6 |
| ADD0 | C15 | 3 | V1 | 4 |

*Table 10. FLEX 8000 232-, 240-, 280 & 304-Pin Package Pin-Outs (Part 2 of 3)*

| Pin Name | 232-Pin PGA EPF81188 EPF81188A | 240-Pin QFP EPF81188 EPF81188A | 280-Pin PGA EPF81500 | 304-Pin RQFP EPF81500 |
|---|---|---|---|---|
| DATA7 | A7 | 205 | W13 | 254 |
| DATA6 | D8 | 203 | W14 | 252 |
| DATA5 | B7 | 200 | W15 | 250 |
| DATA4 | C7 | 198 | W16 | 248 |
| DATA3 | D7 | 196 | W17 | 246 |
| DATA2 | B5 | 194 | V16 | 243 |
| DATA1 | A3 | 191 | U16 | 241 |
| DATA0 | A2 | 189 | V17 | 239 |
| TDI *(2)* | – | – | B1 | 80 |
| TDO *(2)* | – | – | C17 | 149 |
| TCLK *(2)* | – | – | A19 | 148 |
| TMS *(2)* | – | – | C2 | 81 |
| nTRST *(2)* | – | – | A18 | 145 |

*Table 10. FLEX 8000 232-, 240-, 280 & 304-Pin Package Pin-Outs (Part 3 of 3)*

| Pin Name | 232-Pin PGA EPF81188 EPF81188A | 240-Pin QFP EPF81188 EPF81188A | 280-Pin PGA EPF81500 | 304-Pin RQFP EPF81500 |
|---|---|---|---|---|
| Dedicated Inputs | C1, C17, R1, R17 | 10, 51, 130, 171 | F1, F16, P3, P19 | 12, 64, 164, 217 |
| $V_{CCINT}$ (5.0 V) | E4, H4, L4, P12, L14, H14, E14, R14, U1 | 20, 42, 64, 66, 114, 128, 150, 172, 236 | B17, D3, D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14 | 24, 54, 77, 144, 79, 115, 162, 191, 218, 266, 301 |
| $V_{CCIO}$ (5.0 V or 3.3 V) | N10, M13, M5, K13, K5, H13, H5, F5, E10, E8, N8, F13 | 19, 41, 65, 81, 99, 116, 140, 162, 186, 202, 220, 235 | D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15 | 22, 53, 78, 99, 119, 137, 163, 193, 220, 244, 262, 282, 300 |
| GND | A1, D6, E11, E7, E9, G4, G5, G13, G14, J5, J13, K4, K14, L5, L13, N4, N7, N9, N11, N14 | 8, 9, 30, 31, 52, 53, 72, 90, 108, 115, 129, 139, 151, 161, 173, 185, 187, 193, 211, 229 | D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16, | 9, 11, 36, 38, 65, 67, 90, 108, 116, 128, 150, 151, 175, 177, 206, 208, 231, 232, 237, 253, 265, 273, 291 |
| No Connect (N.C.) | – | 61, 62, 119, 120, 181, 182, 239, 240 | | 10, 21, 23, 25, 35, 37, 39, 40, 41, 42, 52, 55, 66, 68, 146, 147, 161, 173, 174, 176, 187, 188, 189, 190, 192, 194, 195, 205, 207, 219, 221, 233, 234, 235, 236, 302, 303 |
| Total User I/O Pins | 180 | 180 | 204 | 204 |

*Notes to Table 10:*
(1) Dedicated pin (not available as a user I/O pin).
(2) Dedicated JTAG pin (not available as a user I/O pin).

## Package Outlines

Figures 21 through 31 show the package outlines for all FLEX 8000 devices. Package outlines are listed here in ascending pin count order. Maximum lead coplanarity is 0.004 in. (0.10 mm). For information on device package ordering codes, see *Ordering Information* in the current data book. Package outline dimensions are shown in the following formats:

$$\frac{\text{min. inches (min. millimeters)}}{\text{max. inches (max. millimeters)}}$$

or:

$$\frac{\text{nominal inches} \pm \text{tolerance}}{(\text{nominal millimeters} \pm \text{tolerance})}$$

or:

$$\frac{\text{inches}}{(\text{millimeters})}\ \text{BSC, Min., Max., Ref., Typ.}$$

### *Figure 21. 84-Pin Plastic J-Lead Chip Carrier (PLCC)*

*See introduction to "Package Outlines" section for dimension formats. Controlling measurement is in inches.*

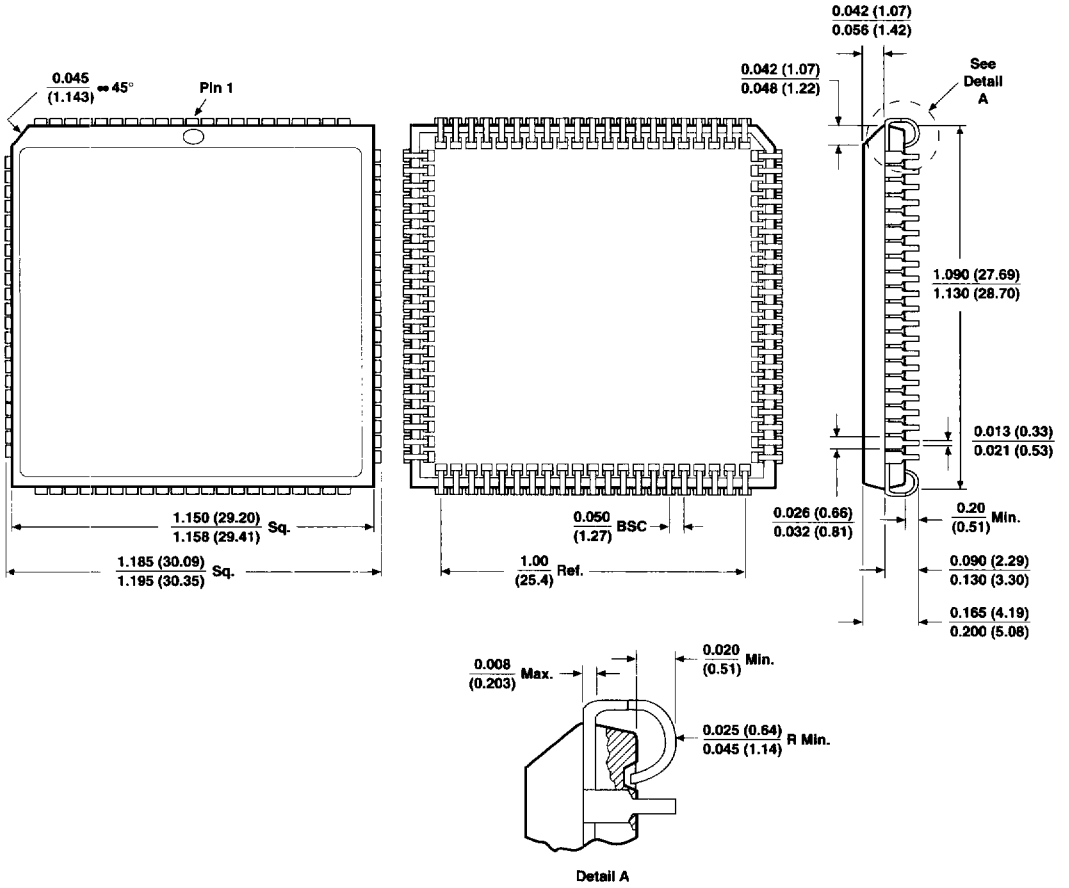
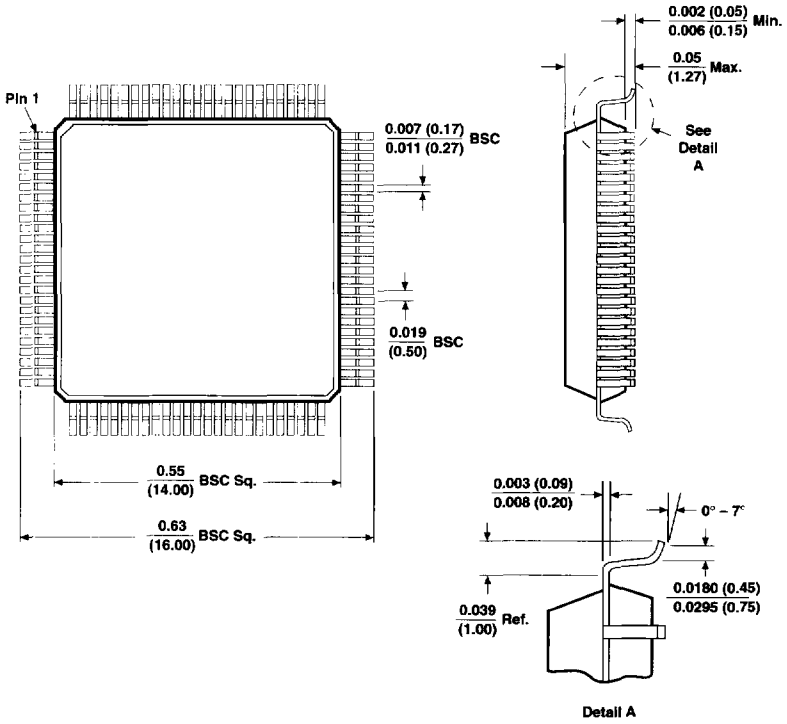


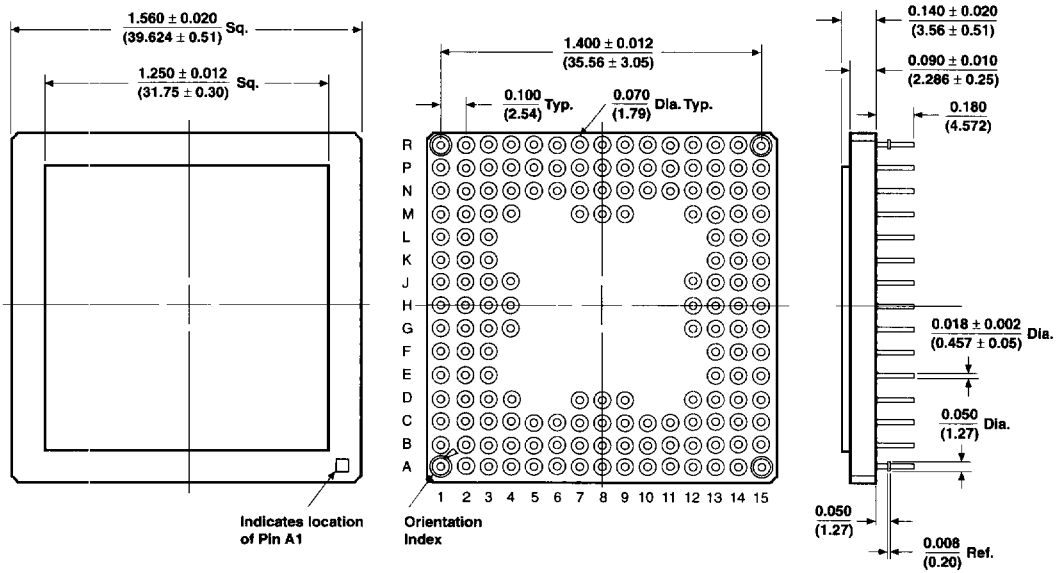
***Figure 22. 100-Pin Thin Plastic Quad Flat Pack (TQFP)***

*See introduction to "Package Outlines" section for dimension formats. Controlling measurement is in millimeters.*



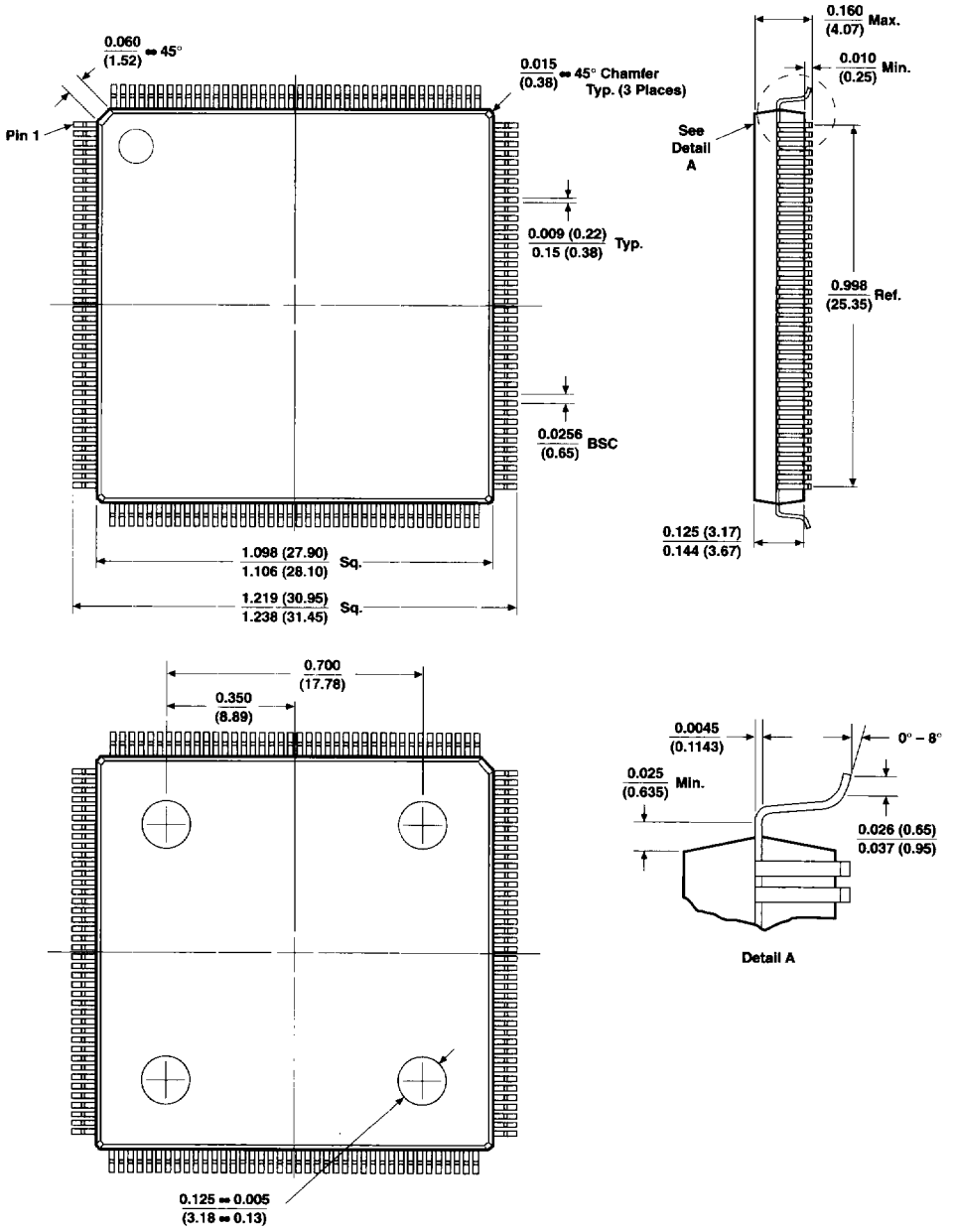
### *Figure 23. 160-Pin Ceramic Pin-Grid Array (PGA)*

*See introduction to "Package Outlines" section for dimension formats. Controlling measurement is in inches.*



### *Figure 24. 160-Pin Plastic Quad Flat Pack (PQFP)*

*See introduction to "Package Outlines" section for dimension formats. Controlling measurement is in millimeters.*



### *Figure 25. 192-Pin Ceramic Pin-Grid Array (PGA)*

*See introduction to "Package Outlines" section for dimension formats. Controlling measurement is in inches.*

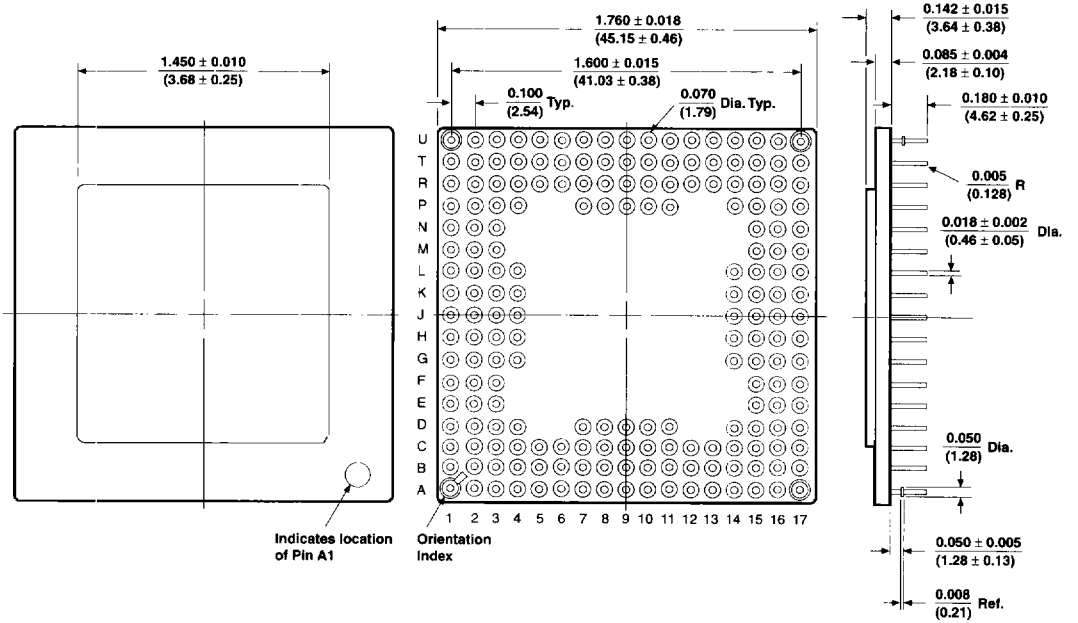
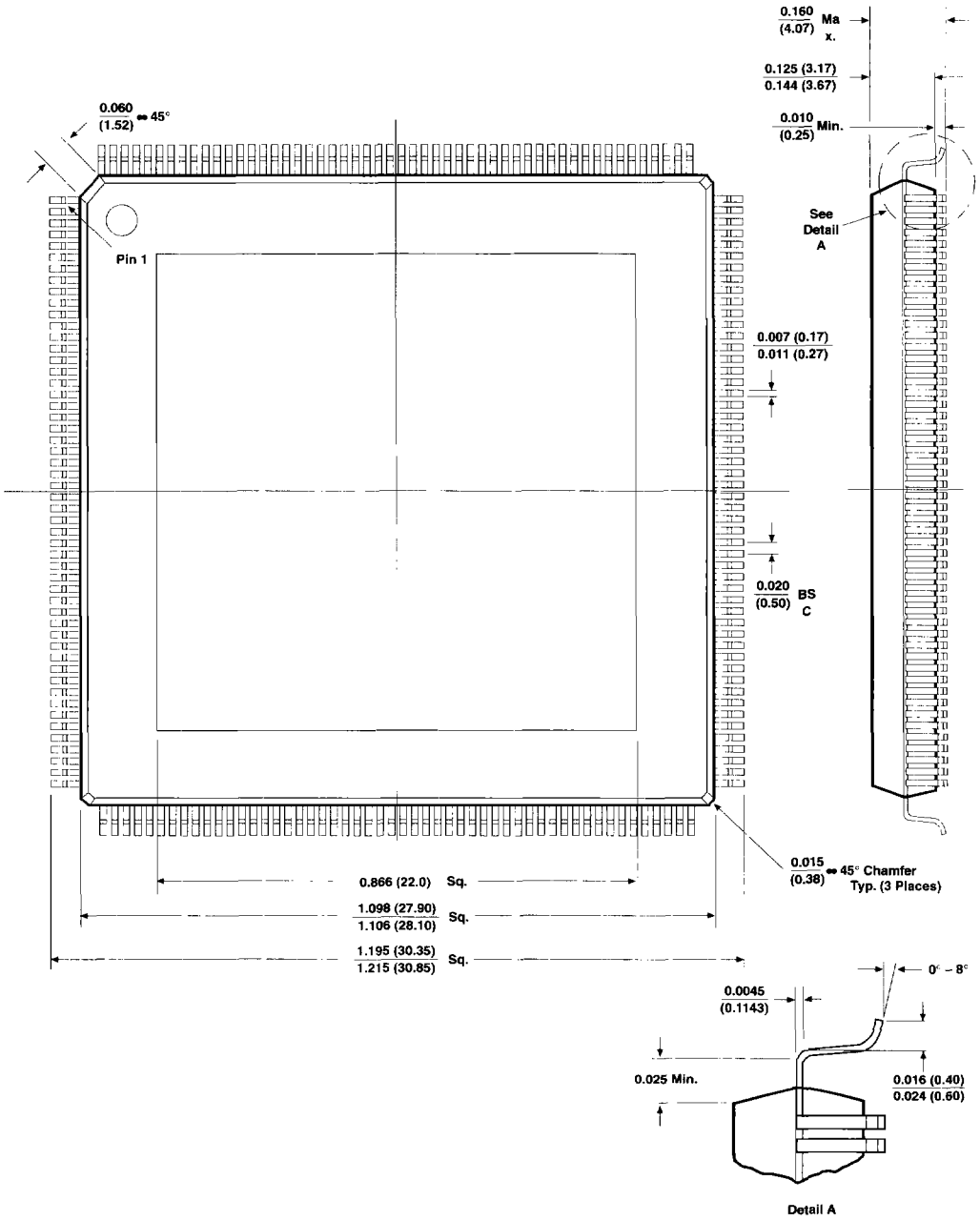


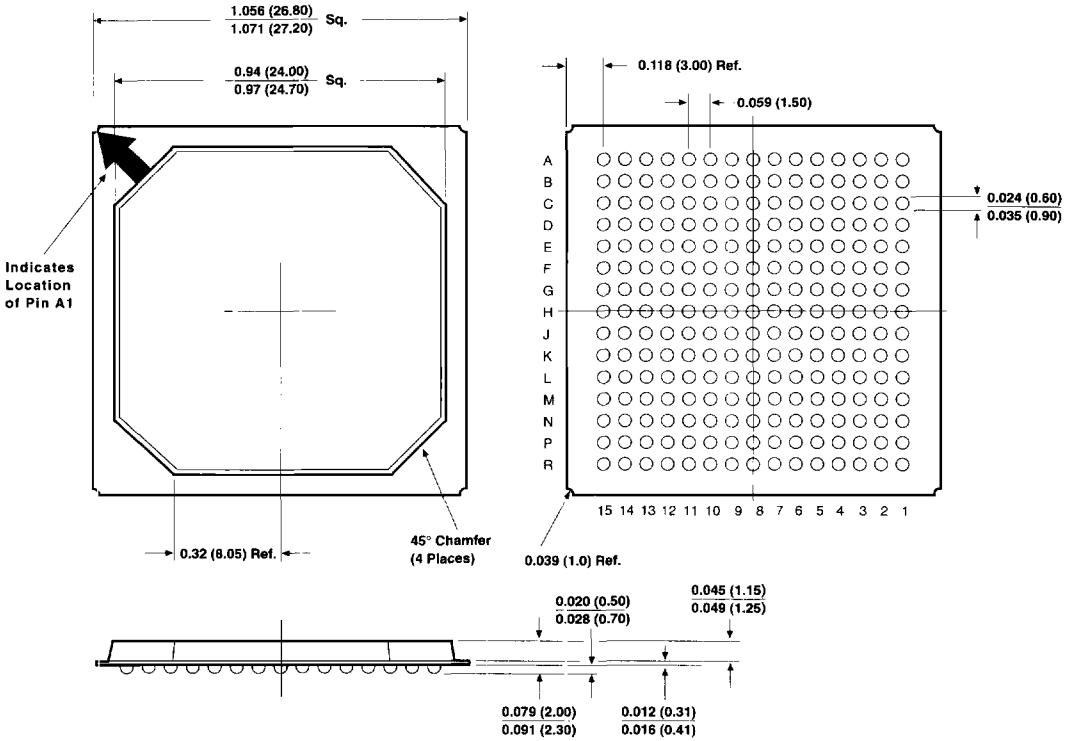
***Figure 26. 208-Pin Power Quad Flat Pack (RQFP)***

*See introduction to "Package Outlines" section for dimension formats. Controlling measurement is in millimeters.*



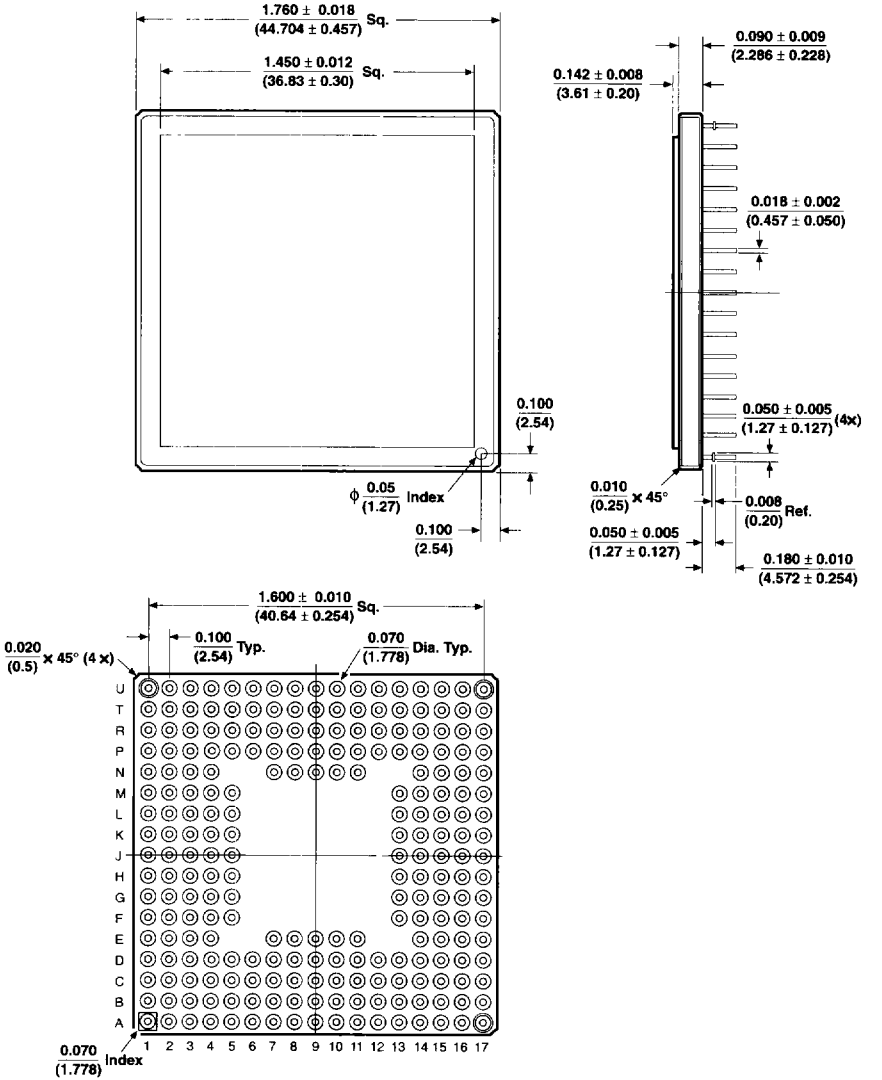
### *Figure 27. 225-Pin Ball-Grid Array (BGA)*

*See introduction to "Package Outlines" section for dimension formats. Controlling measurement is in millimeters.*



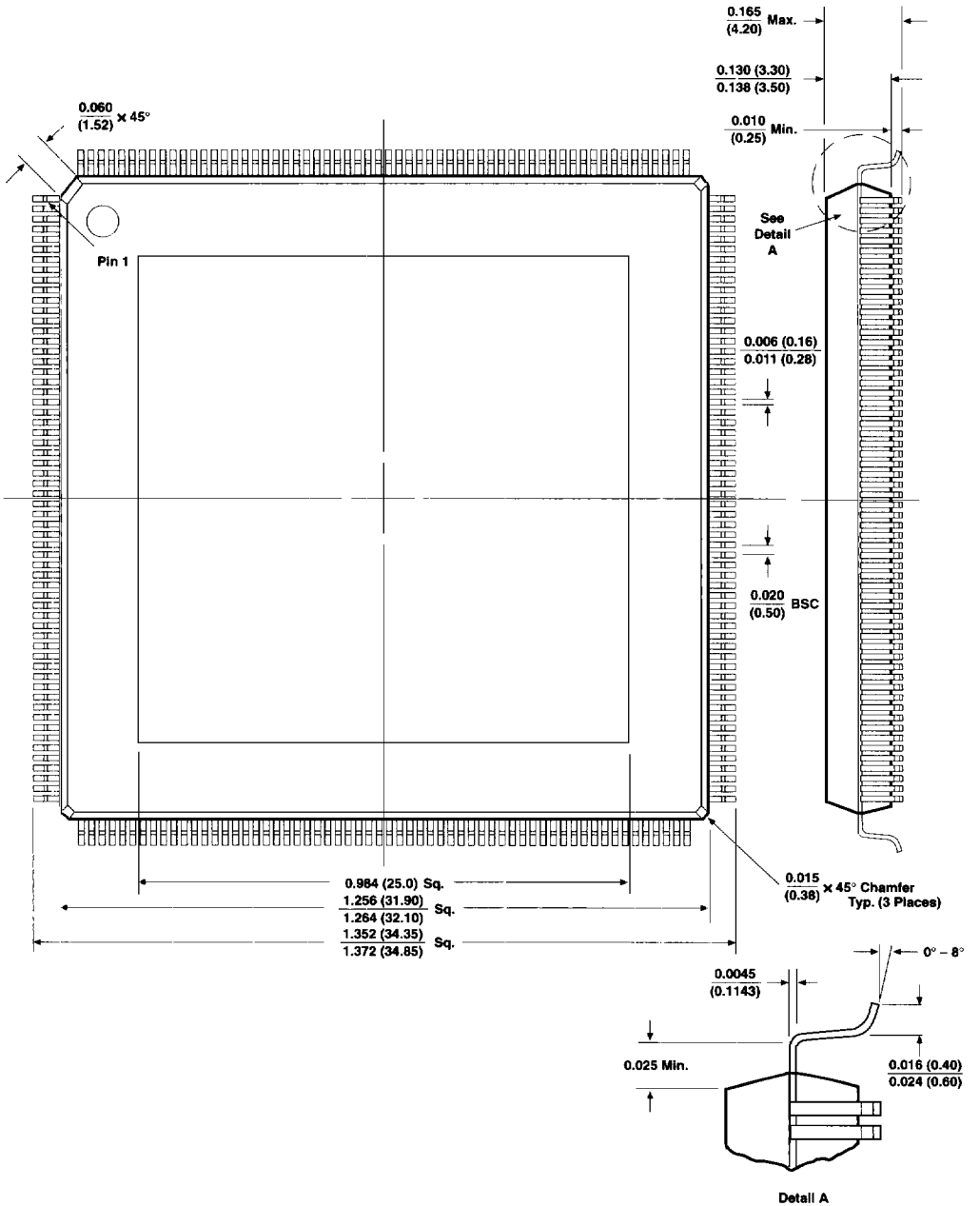
### *Figure 28. 232-Pin Ceramic Pin-Grid Array (PGA)*

*See introduction to "Package Outlines" section for dimension formats. Controlling measurement is in inches.*



### *Figure 29. 240-Pin Power Quad Flat Pack (RQFP)*

*See introduction to "Package Outlines" section for dimension formats. Controlling measurement is in millimeters.*



## *Figure 30. 280-Pin Pin-Grid Array (PGA)*

*See introduction to "Package Outlines" section for dimension formats. Controlling measurement is in millimeters.*

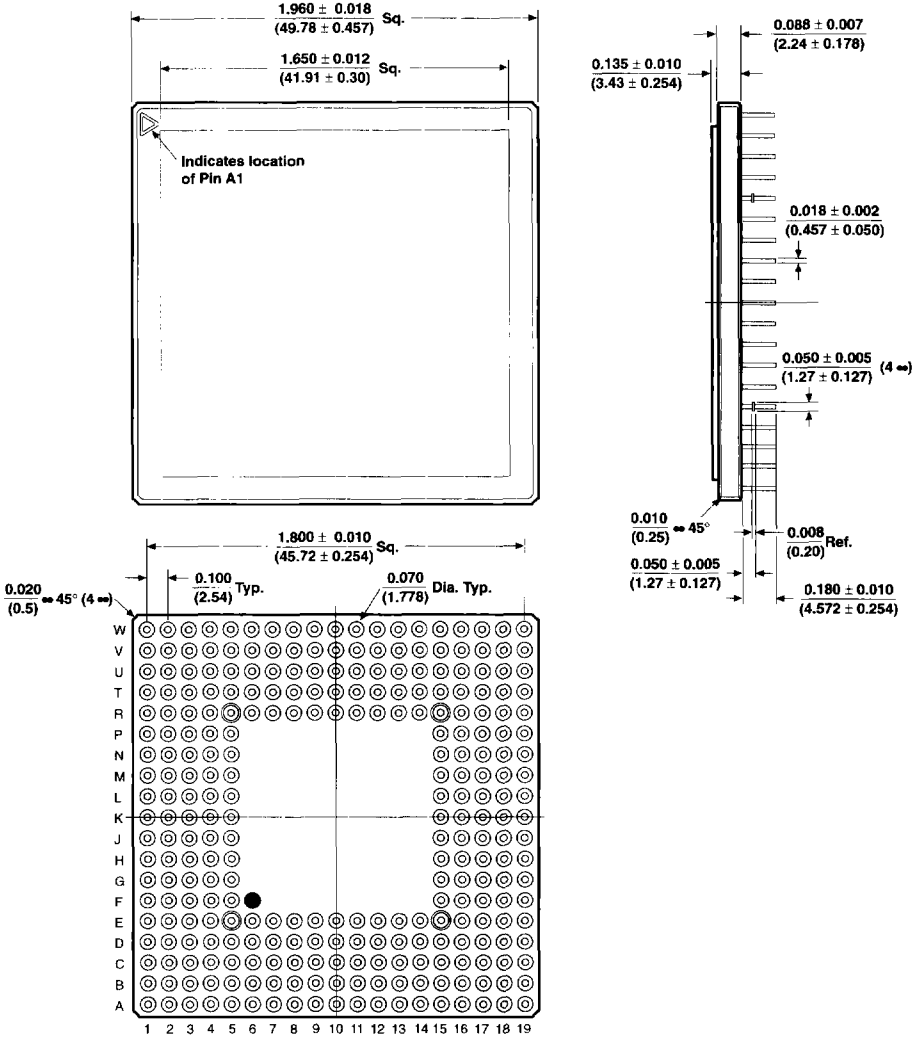
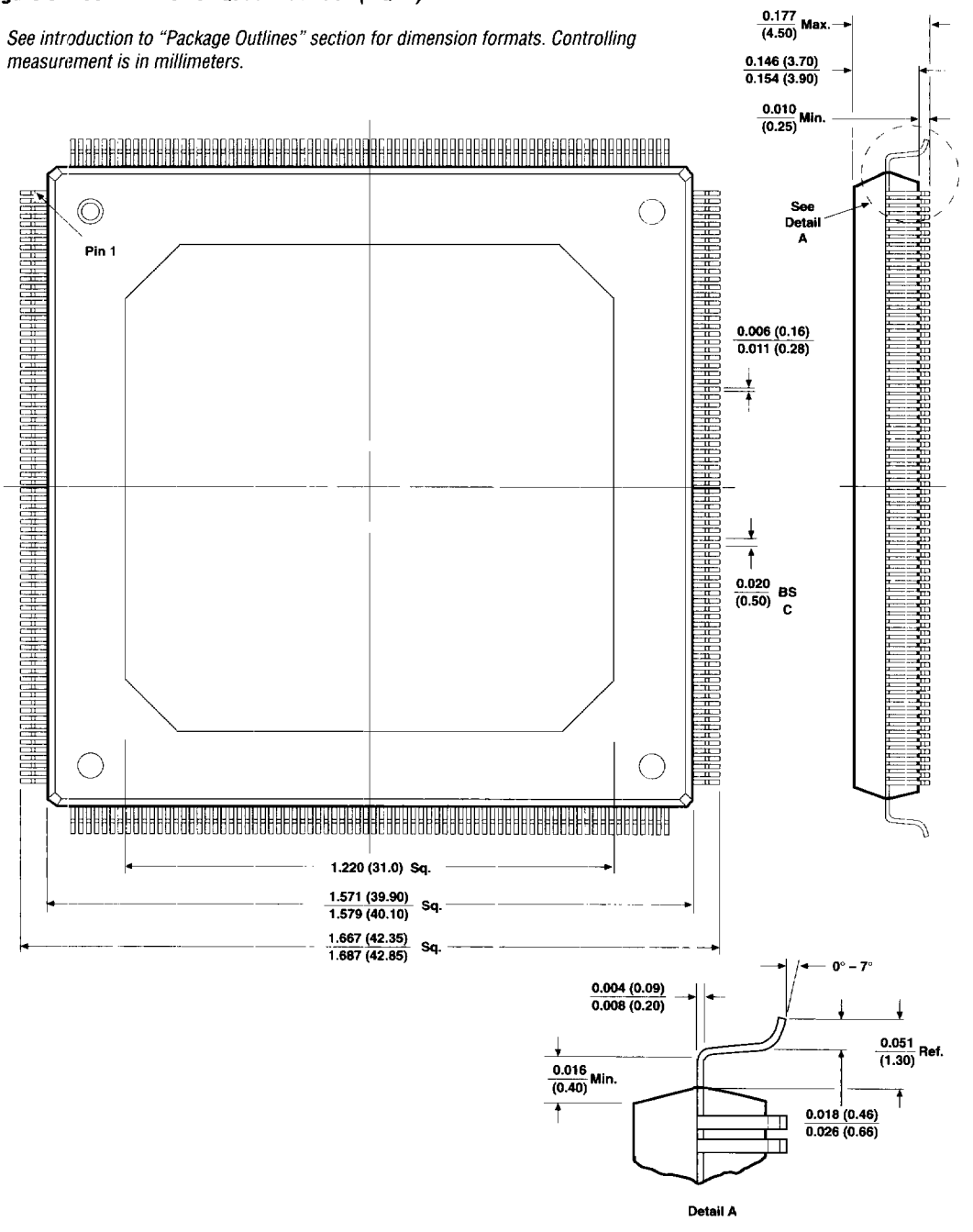


***Figure 31. 304-Pin Power Quad Flat Pack (RQFP)***

*See introduction to "Package Outlines" section for dimension formats. Controlling measurement is in millimeters.*



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