Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Features

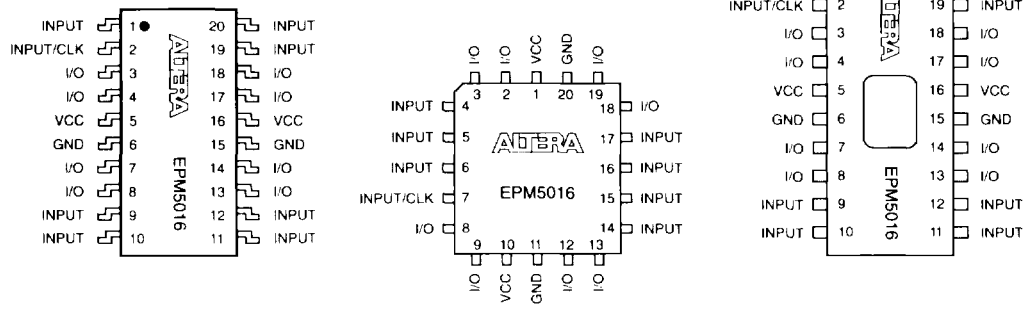
- High-speed 20-pin DIP, J-lead, or SOIC single-LAB MAX 5000 EPLD
  - Combinatorial speeds with t_{PD} = 15 ns
  - Counter frequencies up to 100 MHz
  - Pipelined data rates up to 100 MHz
- 16 individually configurable macrocells
- 32 expander product terms (expanders) that allow 34 product terms in a single macrocell
- Up to 21 flip-flops or 32 latches
- Up to 10 input latches that can be constructed with cross-coupled expanders
- 24-mA output drivers to allow direct interfacing to system buses
- Programmable I/O architecture allowing up to 16 inputs and 8 outputs
- Available in 20-pin windowed ceramic DIP package, or plastic one-time-programmable (OTP) DIP, J-lead (PLCC), and 300-mil SOIC packages

General Description

The Altera EPM5016 EPLD is a Multiple Array MatriX (MAX) 5000-family CMOS EPLD that is optimized for speed. It can integrate multiple SSI and MSI TTL and 74HC devices. In addition, it can replace any 20-pin PAL or PLA device with logic left over for further integration. See Figure 9.

Figure 9. EPM5016 Package Pin-Out Diagrams

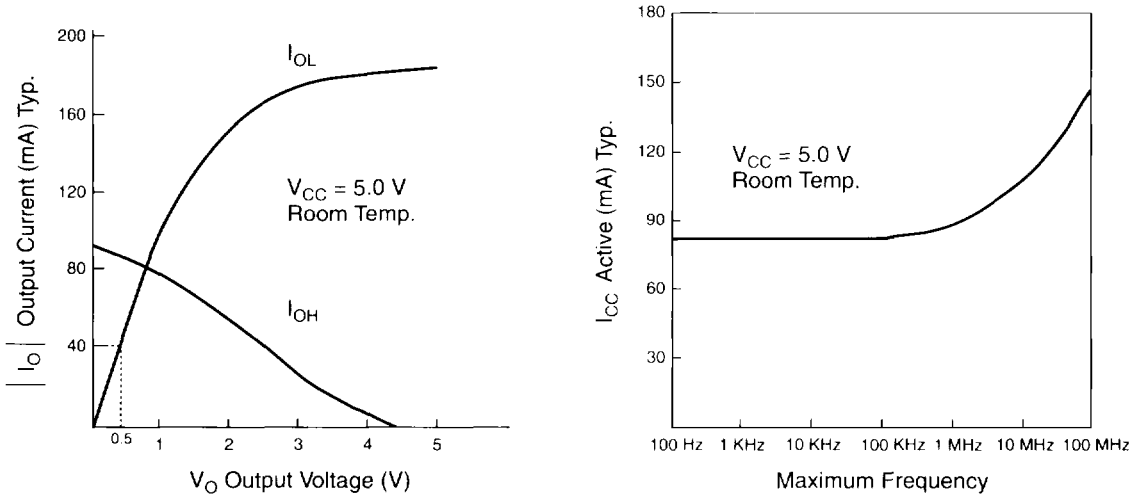
Package outlines not drawn to scale.



SOIC J-Lead DIP

Figure 10 shows output drive characteristics of EPM5016 I/O pins and typical supply current versus frequency for the EPM5016 EPLD.

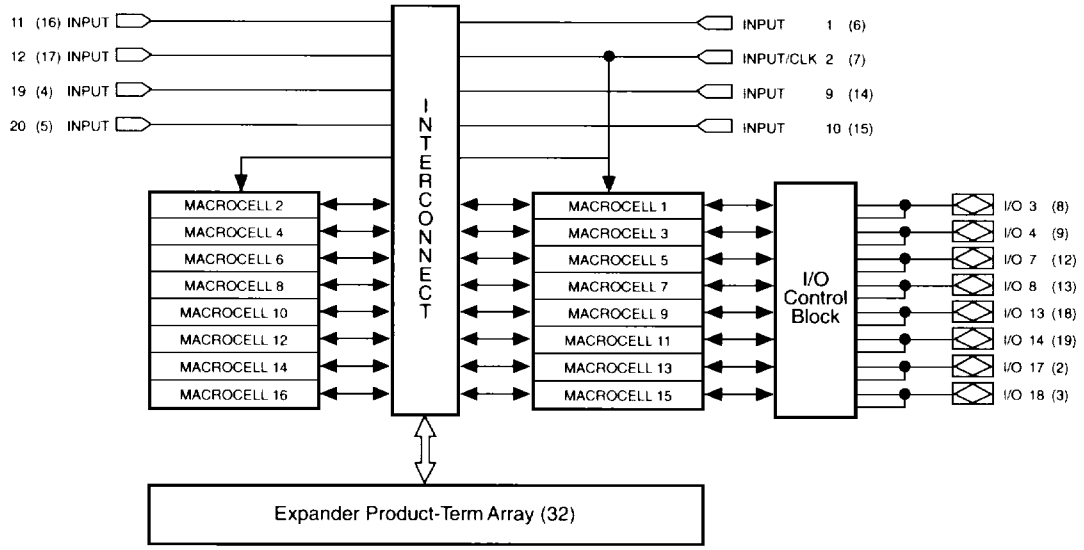
Figure 10. EPM5016 Output Drive Characteristics and I_{CC} vs. Frequency



The EPM5016 EPLD contains 16 macrocells (see Figure 11). The expander product-term array for the EPM5016 EPLD contains 32 expanders. The I/O control block contains 8 bidirectional I/O pins that can be configured for dedicated input, dedicated output, or bidirectional operation. All I/O pins feature dual feedback for maximum pin flexibility.

Figure 11. EPM5016 Block Diagram

The EPM5016 has 16 macrocells and 32 expanders. Numbers in parentheses are for the PLCC package.



Absolute Maximum Ratings

Note: See *Operating Requirements for EPLDs* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (1)*	–2.0	13.5	V
V_I	DC input voltage		–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			200	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			1000	mW
T_{STG}	Storage temperature	No bias	–65	150	°C
T_{AMB}	Ambient temperature	Under bias	–65	135	°C
T_J	Junction temperature	Under bias		150	°C

Recommended Operating Conditions

See Note (2)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75 (4.5)	5.25 (5.5)	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	°C
T_A	Operating temperature	For industrial use	–40	85	°C
t_R	Input rise time			100	ns
t_F	Input fall time			100	ns

DC Operating Conditions

See Notes (2), (3), (4)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –12 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 24 mA DC			0.5	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (standby)	$V_I = V_{CC}$ or GND		80	110 (150)	mA
I_{CC3}	V_{CC} supply current (active)	$V_I = V_{CC}$ or GND, No load, f = 1.0 MHz, *See Note (5)*		85	115 (175)	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *See Note (4)*

External Timing Parameters			EPM5016-15		EPM5016-17		EPM5016-20		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{PD1}	Input to non-registered output	C1 = 35 pF		15		17		20	ns
t_{PD2}	I/O input to non-registered output			15		17		20	ns
t_{SU}	Global clock setup time		6		8		11		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		9		11		13	ns
t_{CH}	Global clock high time		5		6		8		ns
t_{CL}	Global clock low time		5		6		8		ns
t_{ASU}	Array clock setup time		5		7		9		ns
t_{AH}	Array clock hold time		5		7		8		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		15		17		20	ns
t_{ACH}	Array clock high time	*See Note (6)*	4		5		7		ns
t_{ACL}	Array clock low time		6		7		9		ns
t_{CNT}	Minimum global clock period			10		12		16	ns
f_{CNT}	Max. internal global clock frequency	*See Note (5)*	100		83.3		62.5		MHz
t_{ACNT}	Minimum array clock period			10		12		16	ns
f_{ACNT}	Max. internal array clock frequency	*See Note (5)*	100		83.3		62.5		MHz
f_{MAX}	Maximum clock frequency	*See Note (7)*	100		83.3		62.5		MHz

Internal Timing Parameters *See Note (8)*			EPM5016-15		EPM5016-17		EPM5016-20		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{IN}	Input pad and buffer delay			4		5		5	ns
t_{IO}	I/O input pad and buffer delay			4		5		5	ns
t_{EXP}	Expander array delay			5		8		10	ns
t_{LAD}	Logic array delay			6		7		9	ns
t_{LAC}	Logic control array delay			4		5		7	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		4		4		5	ns
t_{ZX}	Output buffer enable delay			7		7		8	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		7		7		8	ns
t_{SU}	Register setup time		2		5		8		ns
t_{LATCH}	Flow-through latch delay			1		1		1	ns
t_{RD}	Register delay			1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1	ns
t_{H}	Register hold time		6		8		9		ns
t_{IC}	Array clock delay			6		6		8	ns
t_{ICS}	Global clock delay			0		1		2	ns
t_{FD}	Feedback delay			1		1		1	ns
t_{PRE}	Register preset time			3		6		6	ns
t_{CLR}	Register clear time			3		6		6	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Numbers in parentheses are for military and industrial temperature-range versions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(4) Operating conditions: V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5 V ± 10%, T_A = –40° C to 85° C for industrial use.
(5) Measured with a device programmed as a 16-bit counter.
(6) This parameter is measured with a positive-edge-triggered clock at the register. For negative-edge clocking, the t_{ACH} and t_{ACL} parameters must be swapped.
(7) The f_{MAX} values represent the highest frequency for pipelined data.
(8) For information on internal timing parameters, refer to *Application Brief 75*.

Product Availability

Operating Temperature		Availability
Commercial	(0° C to 70° C)	EPM5016-15, EPM5016-17, EPM5016-20
Industrial	(–40° C to 85° C)	EPM5016-20
Military	(–55° C to 125° C)	Consult factory