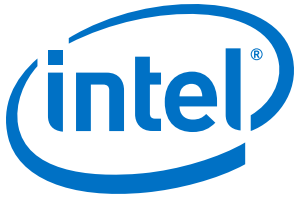

Intel® Stratix® 10 Device Datasheet

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Intel® Stratix® 10 Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and timing for Intel® Stratix® 10 devices.

Table 1. Intel Stratix 10 Device Grades and Speed Grades Supported

Device Grade	Speed Grade Supported
Extended	• –E1V (fastest) • –E2V • –E2L • –E3V • –E3X
Industrial	• –I1V • –I2V • –I2L • –I3V • –I3X

The suffix after the speed grade denotes the power options offered in Intel Stratix 10 devices.

- V—SmartVID with standard static power
- L—0.85 V fixed voltage with low static power
- X—0.85 V fixed voltage with lowest static power

Table 2. Datasheet Status for Intel Stratix 10 Devices

Variant	Datasheet Status
Intel Stratix 10 GX	Final
Intel Stratix 10 SX	Final
Intel Stratix 10 TX	Final
Intel Stratix 10 MX	Final

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Intel Stratix 10 devices.

Operating Conditions

Intel Stratix 10 devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Intel Stratix 10 devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Intel Stratix 10 devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 3. Absolute Maximum Ratings for Intel Stratix 10 Devices

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CC}	Core voltage power supply	—	–0.50	1.26	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	—	–0.50	1.26	V
V_{CCERAM}	Embedded memory and digital transceiver power supply	—	–0.50	1.24	V
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	—	–0.50	2.46	V

continued...

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CCBAT}	Battery back-up power supply for design security volatile key register	—	–0.50	2.46	V
V_{CCIO_SDM}	Configuration pins power supply	—	–0.50	2.19	V
V_{CCIO}	I/O buffers power supply	3 V I/O	–0.50	4.10	V
		LVDS I/O (1)	–0.50	2.19	V
V_{CCA_PLL}	Phase-locked loop (PLL) analog power supply	—	–0.50	2.46	V
V_{CCT_GXB}	Transmitter analog power supply	—	–0.50	1.47	V
V_{CCR_GXB}	Receiver analog power supply	—	–0.50	1.47	V
V_{CCH_GXB}	Transmitter output buffer power supply	—	–0.50	2.46	V
V_{CCL_HPS}	HPS core voltage and periphery circuitry power supply	—	–0.50	1.30	V
V_{CCIO_HPS}	HPS I/O buffers power supply	LVDS I/O (1)	–0.50	2.19	V
V_{CCPLL_HPS}	HPS PLL power supply	—	–0.50	2.46	V
V_I	DC input voltage	3 V I/O	–0.30	3.80	V
		LVDS I/O	–0.30	2.19	V
I_{OUT}	DC output current per pin	—	–15 (2)(3)(4)(5)(6)	15	mA

continued...

(1) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

(2) The maximum current allowed through any LVDS I/O bank pin when the device is not turned on or during power-up/power-down conditions is 10 mA.

(3) Total current per LVDS I/O bank must not exceed 100 mA.

(4) Voltage level must not exceed 1.89 V.

(5) Applies to all I/O standards and settings supported by LVDS I/O banks, including single-ended and differential I/Os.

(6) Applies only to LVDS I/O banks. 3 V I/O banks are not covered under this specification and must be implemented as per the power sequencing requirement. For more details, refer to *AN 692: Power Sequencing Considerations for Intel Cyclone® 10 GX, Intel Arria® 10, and Intel Stratix 10 Devices* and *Intel Stratix 10 Power Management User Guide*.

Symbol	Description	Condition	Minimum	Maximum	Unit
T_J	Absolute junction temperature for Intel Stratix 10 MX devices	—	–55	120	°C
	Absolute junction temperature for all other Intel Stratix 10 devices	—	-55	125	°C
T_{STG}	Storage temperature (no bias) for Intel Stratix 10 MX devices	—	–55	120	°C
	Storage temperature (no bias) for all other Intel Stratix 10 devices	—	-55	150	°C

Related Information

- AN 692: Power Sequencing Considerations for Intel Cyclone 10 GX, Intel Arria 10, and Intel Stratix 10 Devices
  Provides the power sequencing requirements for Intel Stratix 10 devices.
- Power Sequencing Considerations for Intel Stratix 10 Devices, Intel Stratix 10 Power Management User Guide
  Provides the power sequencing requirements for Intel Stratix 10 devices.

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –1.1 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, when using V_{CCIO} = 1.8 V, a signal that overshoots to 2.44 V for LVDS I/O can only be at 2.44 V for ~6% over the lifetime of the device.

Table 4. Maximum Allowed Overshoot During Transitions for Intel Stratix 10 Devices (for LVDS I/O)

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

Symbol	Description	LVDS I/O (V) [7]	Overshoot Duration as % at T_J = 100°C	Unit
Vi (AC)	AC input voltage	V_{CCIO} + 0.30	100	%
		V_{CCIO} + 0.35	60	%
		V_{CCIO} + 0.40	30	%

continued...

(7) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Symbol	Description	LVDS I/O (V) (7)	Overshoot Duration as % at T_J = 100°C	Unit
		V_{CCIO} + 0.45	20	%
		V_{CCIO} + 0.50	10	%
		V_{CCIO} + 0.55	6	%
		> V_{CCIO} + 0.55	No overshoot allowed	%

Table 5. Maximum Allowed Overshoot During Transitions for Intel Stratix 10 Devices (for 3 V I/O)

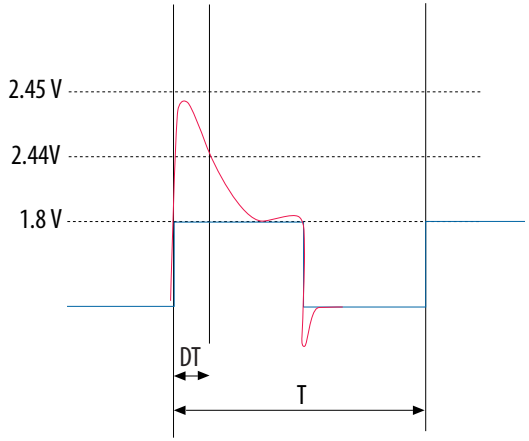
This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

Symbol	Description	3 V I/O (V)	Overshoot Duration as % at T_J = 100°C	Unit
Vi (AC)	AC input voltage	V_{CCIO} + 0.65	100	%
		V_{CCIO} + 0.70	42	%
		V_{CCIO} + 0.75	18	%
		V_{CCIO} + 0.80	9	%
		V_{CCIO} + 0.85	4	%
		> V_{CCIO} + 0.85	No overshoot allowed	%

For an overshoot of 2.5 V, the percentage of high time for the overshoot can be as high as 100% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal.

(7) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Figure 1. Intel Stratix 10 Devices Overshoot Duration



Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Intel Stratix 10 devices.

Recommended Operating Conditions

Table 6. Recommended Operating Conditions for Intel Stratix 10 Devices

This table lists the steady-state voltage values expected for Intel Stratix 10 devices. Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum (8)	Typical	Maximum (8)	Unit
V_{CC}	Core voltage power supply	–E1V, –I1V, –E2V, –I2V, –E3V, –I3V (9)	(Typical) – 30 mV	0.8 – 0.94	(Typical) + 30 mV	V
		–E2L, –I2L, –E3X, –I3X	0.82	0.85	0.88	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	–E1V, –I1V, –E2V, –I2V, –E3V, –I3V (9)	(Typical) – 30 mV	0.8 – 0.94	(Typical) + 30 mV	V
		–E2L, –I2L, –E3X, –I3X	0.82	0.85	0.88	V
V_{CCIO_SDM}	Configuration pins power supply	1.8 V	1.71	1.8	1.89	V
$V_{CCPLLDIG\_SDM}$	Secure Device Manager (SDM) block PLL digital power supply	—	0.87	0.9	0.93	V
V_{CCPLL_SDM}	SDM block PLL analog power supply	—	1.71	1.8	1.89	V
$V_{CCFUSEWR\_SDM}$	Fuse block writing power supply	—	2.35	2.4	2.45	V
V_{CCADC}	ADC voltage sensor power supply	—	1.71	1.8	1.89	V
V_{CCERAM}	Embedded memory and digital transceiver power supply	0.9 V	0.87	0.9	0.93	V
V_{CCBAT} (10)	Battery back-up power supply (For design security volatile key register)	—	1.2	—	1.8	V

continued...

(8) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise. Refer to power distribution network (PDN) tool for PCB power distribution network design.

(9) The use of Power Management Bus (PMBus™) voltage regulator dedicated to Intel Stratix 10 SmartVID devices is mandatory. The PMBus voltage regulator and Intel Stratix 10 SmartVID devices are connected via PMBus.

(10) You need to always power up V_{CCBAT}. If you do not use the design security feature in Intel Stratix 10 devices, connect V_{CCBAT} to a 1.8 V power supply. Intel Stratix 10 power-on reset (POR) circuitry monitors V_{CCBAT}.

Symbol	Description	Condition	Minimum (8)	Typical	Maximum (8)	Unit
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	1.8 V	1.71	1.8	1.89	V
V_{CCIO}	I/O buffers power supply	3.0 V (for 3 V I/O only)	2.85	3	3.15	V
		2.5 V (for 3 V I/O only)	2.375	2.5	2.625	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.2 V	1.14	1.2	1.26	V
V_{CCIO_UIB}	Power supply for the Universal Interface Bus between the core and embedded HBM2 memory	1.2 V	1.17	1.2	1.23	V
V_{CCM_WORD}	Power supply for the embedded HBM2 memory	—	2.4	2.5	2.6	V
V_{CCA_PLL}	PLL analog voltage regulator power supply	—	1.71	1.8	1.89	V
V_I (11)(12)	DC input voltage	3 V I/O	–0.3	—	3.8	V
		LVDS I/O	–0.3	—	2.19	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature for Intel Stratix 10 MX devices	Extended	0 (13)	—	100 (14)	°C

continued...

(8) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise. Refer to power distribution network (PDN) tool for PCB power distribution network design.

(11) The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

(12) This value applies to both input and tri-stated output configuration. Pin voltage should not be externally pulled higher than the maximum value.

(13) For use cases that require FPGA configuration at temperatures less than 0°C, contact Intel Premier Support to enable non-cold start applications.

(14) Recommended maximum operating temperature for HBM2 is 95°C.

Symbol	Description	Condition	Minimum (8)	Typical	Maximum (8)	Unit
	Operating junction temperature for all other Intel Stratix 10 devices	Extended	0	—	100	°C
		Industrial	-20 (–40) (15)	—	100	°C
t_{RAMP} (16)(17)(18)(19)	Power supply ramp time	Standard POR	200 µs	—	100 ms	—

Related Information

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(8) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise. Refer to power distribution network (PDN) tool for PCB power distribution network design.

(15) E-tile supports an operating temperature range of -40°C to 100°C. However, the E-tile transceivers may experience a higher error rate from -40°C to -20°C because of the calibration procedure when starting at a low temperature. Therefore, the recommended operating temperature range for E-tile protocol-compliant transceiver links is -20°C to 100°C. Additionally, for best results, extensive debug should be performed at 25°C or above.

(16) This is also applicable to HPS power supply. For HPS power supply, refer to t_{RAMP} specifications for standard POR when HPS_PORSEL = 0 and t_{RAMP} specifications for fast POR when HPS_PORSEL = 1.

(17) t_{RAMP} is the ramp time of each individual power supply, not the ramp time of all combined power supplies.

(18) To support AS fast mode, all power supplies to the Intel Stratix 10 device must be fully ramped-up within 10 ms to the recommended operating conditions.

(19) To support AS normal mode, V_{CCIO_SDM} of the Intel Stratix 10 device must be fully ramped-up within 10 ms to the recommended operating condition.

Transceiver Power Supply Operating Conditions

Table 7. Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L-Tile Devices in a Non-Bonded Configuration

Symbol	Description	Datarate	Minimum	Typical	Maximum	Unit
$V_{CCT\_GXB[L,R]}$ and $V_{CCR\_GXB[L,R]}$	Chip-to-chip (20)	1.0 Gbps to 26.6 Gbps (21) (22)	1.1	1.12	1.14	V
		1.0 Gbps to 17.4 Gbps (21) (22)	1.0	1.03 (23)	1.06	V
	Backplane (24)	1.0 Gbps to 12.5 Gbps (21)	1.0	1.03 (25), (23)	1.06	V
$V_{CCH\_GXB[L,R]}$	Transceiver high voltage power	—	1.71 (26)	1.8	1.89	V

(20) Chip-to-chip refers to transceiver links that are short reach and do not require advanced equalization such as decision feedback equalization (DFE).

(21) Stratix 10 transceivers can support data rates below 1.0 Gbps through over sampling.

(22) Bonded channels operating at datarates above 16.0 Gbps require 1.12 V ±20 mV at the pin. For channels that are placed on the same tile as the channels that require 1.12 V ±20 mV, V_{CCR_GXB} and V_{CCT_GXB} = 1.12 V ±20 mV.

(23) For a 1.03-V typical voltage, the maximum/minimum should be ± 30 mV; hence, V_{MAX} = 1.06 V. However, when these channels share the power supply with channels requiring a 1.12-V typical voltage, these channels should increase typical voltage to 1.12 V, with a maximum/minimum ± 20 mV; hence V_{MAX} = 1.14 V.

(24) Backplane applications refer to ones which require advanced equalization, such as DFE enabled, to compensate for channel loss.

(25) Refer to the Intel Quartus® Prime Pro Edition software for the typical nominal value.

(26) In an optical transfer network (OTN) application, the minimum VCCH voltage specification at the package pin is 1.77 V.

Table 8. Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L-Tile Devices in a Bonded Configuration

Symbol	Description	Datarate	Minimum	Typical	Maximum	Unit
$V_{CCT\_GXB[L,R]}$ and $V_{CCR\_GXB[L,R]}$	Chip-to-chip (20)	1.0 Gbps to 16.0 Gbps (21)	1.0	1.03 (23)	1.06	V
		> 16.0 Gbps to 17.4 Gbps (21) (22)	1.1	1.12	1.14	V
	Backplane (24)	1.0 Gbps to 12.5 Gbps (21)	1.0	1.03 (25), (23)	1.06	V
$V_{CCH\_GXB[L,R]}$	Transceiver high voltage power	—	1.71 (26)	1.8	1.89	V

Table 9. Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX/MX/TX H-Tile Devices in a Non-Bonded Configuration

Symbol	Description	Datarate	Minimum	Typical	Maximum	Unit
$V_{CCT\_GXB[L,R]}$ and $V_{CCR\_GXB[L,R]}$	Chip-to-chip (20)and Backplane (24)	1.0 Gbps to 28.3 Gbps (GXT) (21)	1.1	1.12	1.14	V
		1.0 Gbps to 17.4 Gbps (GX) (21)	1.0	1.03 (23)	1.06	V
$V_{CCH\_GXB[L,R]}$	Transceiver high voltage power	—	1.71 (26)	1.8	1.89	V

Table 10. Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX/MX/TX H-Tile Devices in a Bonded Configuration

Symbol	Description	Datarate	Minimum	Typical	Maximum	Unit
$V_{CCT\_GXB[L,R]}$ and $V_{CCR\_GXB[L,R]}$	Chip-to-chip (20) and Backplane (24)	1.0 Gbps to 16.0 Gbps (21)	1.0	1.03 (23)	1.06	V
		> 16.0 Gbps to 17.4 Gbps (21)	1.1	1.12	1.14	V
$V_{CCH\_GXB[L,R]}$	Transceiver high voltage power	—	1.71 (26)	1.8	1.89	V

Note: Most VCCR_GXB and VCCT_GXB pins associated with unused transceiver channels can be grounded on a per-tile basis to minimize power consumption. Refer to the *Intel Stratix 10 Device Family Pin Connection Guidelines* and the Intel Quartus Prime pin report for information about pinning out the package to minimize power consumption for your specific design.

Table 11. Transceiver Power Supply Operating Conditions for Intel Stratix 10 TX/MX E-Tile Devices

Symbol	Description	Minimum (27)	Typical	Maximum (27)	Unit	Noise Mask (at ball grid array (BGA))
V_{CCRT_GXE} (28)	Transceiver power supply	0.87	0.9	0.93	V	20 mVpp (100 kHz to 400 kHz) 3 mVpp (3 MHz to 500 MHz) 10 mVpp at 1 GHz
$V_{CCRTPLL\_GXE}$ (28)	Transceiver PLL power supply	0.87	0.9	0.93	V	6 mVpp at 100 kHz 1 mVpp (600 kHz to 10 MHz) 10 mVpp at 1 GHz
V_{CCH_GXE}	Analog power supply	1.067	1.1	1.133	V	10 mVpp (800 kHz to 500 MHz
V_{CCCLK_GXE}	LVPECL REFCLK power supply	2.375	2.5	2.625	V	—

Related Information

Intel Stratix 10 Device Family Pin Connection Guidelines

HPS Power Supply Operating Conditions

Table 12. HPS Power Supply Operating Conditions for Intel Stratix 10 Devices

This table lists the steady-state voltage and current values expected for Intel Stratix 10 system-on-a-chip (SoC) devices with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to Recommended Operating Conditions for Intel Stratix 10 Devices table for the steady-state voltage values expected from the FPGA portion of the Intel Stratix 10 SoC devices.

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CCL_HPS}	HPS core voltage and periphery circuitry power supply	–E2L, –I2L, –E3X, –I3X	0.87	0.9	0.93	V
			0.91	0.94	0.97	V

continued...

(27) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(28) The difference between V_{CCRT}/$V_{CCRTPLL}$ and V_{CCH} should be no less than 200 mV.

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
		–E1V, –I1V, –E2V, –I2V, –E3V, –I3V (29)	0.77 – 0.91	0.8 – 0.94	0.83 – 0.97	V
$V_{CCPLLDIG\_HPS}$	HPS PLL digital power supply	–E2L, –I2L, –E3X, –I3X	0.87	0.9	0.93	V
			0.91	0.94	0.97	V
		–E1V, –I1V, –E2V, –I2V, –E3V, –I3V (29)	0.77 – 0.91	0.8 – 0.94	0.83 – 0.97	V
V_{CCPLL_HPS}	HPS PLL analog power supply	1.8 V	1.71	1.8	1.89	V
V_{CCIO_HPS}	HPS I/O buffers power supply	1.8 V	1.71	1.8	1.89	V

Related Information

- Recommended Operating Conditions on page 9
  Provides the steady-state voltage values for the FPGA portion of the device.
- HPS Clock Performance on page 65

DC Characteristics

Supply Current and Power Consumption

Intel offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Intel Quartus Prime Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the usage of the resources.

The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yield very accurate power estimates.

(29) The use of Power Management Bus (PMBus) voltage regulator dedicated to Intel Stratix 10 SmartVID devices is mandatory. The PMBus voltage regulator and Intel Stratix 10 SmartVID devices are connected via PMBus.

I/O Pin Leakage Current

Table 13. I/O Pin Leakage Current for Intel Stratix 10 Devices

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–80	80	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–80	80	µA

Bus Hold Specifications

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Table 14. Bus Hold Parameters for Intel Stratix 10 Devices

Parameter	Symbol	Condition	V_{CCIO} (V)										Unit
			1.2		1.5		1.8		2.5		3.0		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max)	8	—	12	—	30	—	60	—	70	—	µA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min)	–8	—	–12	—	–30	—	–60	—	–70	—	µA
Bus-hold, low, overdrive current	I_{ODL}	0 V < V_{IN} < V_{CCIO}	—	125	—	175	—	200	—	300	—	500	µA
Bus-hold, high, overdrive current	I_{ODH}	0 V < V_{IN} < V_{CCIO}	—	–125	—	–175	—	–200	—	–300	—	–500	µA
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	0.38	1.13	0.68	1.07	0.7	1.7	0.8	2	V

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 15. OCT Calibration Accuracy Specifications for Intel Stratix 10 Devices

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (V)	Calibration Accuracy			Unit
			–E1, –I1	–E2, –I2	–E3, –I3	
34-Ω, 48-Ω, 60-Ω, 80-Ω, 120-Ω, and 240-Ω R_S	Internal series termination with calibration (34-Ω, 48-Ω, 60-Ω, 80-Ω, 120-Ω, and 240-Ω setting)	V_{CCIO} = 1.2	±15	±15	±15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	±15	±15	±15	%
25-Ω and 50-Ω R_S	Internal series termination with calibration (25-Ω and 50-Ω setting)	V_{CCIO} = 1.8, 1.5, 1.2	±15	±15	±15	%
34-Ω, 40-Ω, 48-Ω, 60-Ω, 80-Ω, 120-Ω, and 240-Ω R_T	Internal parallel termination with calibration (34-Ω, 40-Ω, 48-Ω, 60-Ω, 80-Ω, 120-Ω, and 240-Ω setting)	POD12 I/O standard, V_{CCIO} = 1.2	±15	±15	±15	%
48-Ω, 50-Ω, 60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (48-Ω, 50-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.2	–10 to +60	–10 to +60	–10 to +60	%
48-Ω, 60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (48-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.25	–10 to +70	–10 to +70	–10 to +70	%
48-Ω, 60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (48-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.35	–10 to +65	–10 to +65	–10 to +65	%
50-Ω R_T	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8	–10 to +50	–10 to +50	–10 to +50	%

OCT Without Calibration Resistance Tolerance Specifications

Table 16. OCT Without Calibration Resistance Tolerance Specifications for Intel Stratix 10 Devices

This table lists the Intel Stratix 10 OCT without calibration resistance tolerance to PVT changes.

Symbol	Description	I/O Buffer Type	Condition (V)	Resistance Tolerance			Unit
				–E1, –I1	–E2, –I2	–E3, –I3	
25-Ω and 50-Ω R_S	Internal series termination without calibration (25-Ω and 50-Ω setting)	3 V I/O	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	–40 to +30	±40	±40	%
25-Ω and 50-Ω R_S	Internal series termination without calibration (25-Ω and 50-Ω setting)	LVDS I/O	V_{CCIO} = 1.8, 1.5, 1.2	–20 to +35	–20 to +35	–20 to +35	%
34-Ω and 40-Ω R_S	Internal series termination without calibration (34-Ω and 40-Ω setting)	LVDS I/O	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	–20 to +35	–20 to +35	–20 to +35	%
48-Ω, 60-Ω, 80-Ω, and 240-Ω R_S	Internal series termination without calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting)	LVDS I/O	V_{CCIO} = 1.2	–20 to +35	–20 to +35	–20 to +35	%
100-Ω R_D	Internal differential termination (100-Ω setting)	LVDS I/O	V_{CCIO} = 1.8	±25	±35	±40	%

Pin Capacitance

Table 17. Pin Capacitance for Intel Stratix 10 Devices

Symbol	Description	Maximum	Unit
C_{IO_COLUMN}	Input capacitance on column I/O pins	3.5	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins	3.5	pF

Internal Weak Pull-Up Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up. For SDM and HPS, the configuration I/O and peripheral I/O are supported with weak pull-up and weak pull-down options.

Table 18. Internal Weak Pull-Up Resistor Values for Intel Stratix 10 Devices

Symbol	Description	Condition (V)	Nominal Value	Resistance Tolerance	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V_{CCIO} = 3.0 ±5%	25	±25%	kΩ
		V_{CCIO} = 2.5 ±5%	25	±25%	kΩ
		V_{CCIO} = 1.8 ±5%	25	±25%	kΩ
		V_{CCIO} = 1.5 ±5%	25	±25%	kΩ
		V_{CCIO} = 1.35 ±5%	25	±25%	kΩ
		V_{CCIO} = 1.25 ±5%	25	±25%	kΩ
		V_{CCIO} = 1.2 ±5%	25	±25%	kΩ

Related Information

Intel Stratix 10 Device Family Pin Connection Guidelines
Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.

I/O Standard Specifications

Tables in this section list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Intel Stratix 10 devices.

For minimum voltage values, use the minimum V_{CCIO} values. For maximum voltage values, use the maximum V_{CCIO} values.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

Related Information

Recommended Operating Conditions on page 9

Single-Ended I/O Standards Specifications

Table 19. Single-Ended I/O Standards Specifications for Intel Stratix 10 Devices

I/O Standard	V_{CCIO} (V)			V_{IL}(V)		V_{IH}(V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (30) (mA)	I_{OH} (30) (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.0-V LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
3.0-V LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.3	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	-0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
Schmitt Trigger Input	1.71	1.8	1.89	—	0.35 × V_{CCIO}	0.65 × V_{CCIO}	—	—	—	—	—

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 20. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel Stratix 10 Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-135	1.283	1.35	1.45	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-125	1.19	1.25	1.31	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-12	1.14	1.2	1.26	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}

continued...

(30) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 1.8- V LVCMOS specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	$V_{CCIO}/2$	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	$V_{CCIO}/2$	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}	—	$V_{CCIO}/2$	—
HSUL-12	1.14	1.2	1.3	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	—	—	—
POD12	1.14	1.2	1.26	—	Internally calibrated	—	—	V_{CCIO}	—

Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 21. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Intel Stratix 10 Devices

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL} (31) (mA)	I_{OH} (31) (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-18 Class I	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	V_{TT} – 0.603	V_{TT} + 0.603	6.7	–6.7
SSTL-18 Class II	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} –0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	16	–16
SSTL-135	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
SSTL-125	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
SSTL-12	—	V_{REF} – 0.10	V_{REF} + 0.10	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—

continued...

(31) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL} (31) (mA)	I_{OH} (31) (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
HSTL-18 Class I	—	V_{REF} –0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} –0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 × V_{CCIO}	0.9 × V_{CCIO}	—	—
POD12	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	—	—	—	—

Differential SSTL I/O Standards Specifications

Table 22. Differential SSTL I/O Standards Specifications for Intel Stratix 10 Devices

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{SWING(AC)}$ (V)		$V_{IX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	0.5	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.175	—	$V_{CCIO}/2$ + 0.175
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(32)	$2(V_{IH(AC)} – V_{REF})$	$2(V_{REF} – V_{IL(AC)})$	$V_{CCIO}/2$ – 0.15	—	$V_{CCIO}/2$ + 0.15

continued...

(31) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

(32) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{SWING(AC)}$ (V)		$V_{IX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max
SSTL-135	1.283	1.35	1.45	0.18	(32)	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$
SSTL-125	1.19	1.25	1.31	0.18	(32)	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$
SSTL-12	1.14	1.2	1.26	0.16	(32)	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$	$V_{REF} - 0.15$	$V_{CCIO}/2$	$V_{REF} + 0.15$

Differential HSTL and HSUL I/O Standards Specifications

Table 23. Differential HSTL and HSUL I/O Standards Specifications for Intel Stratix 10 Devices

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{DIF(AC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.4	—	0.78	—	1.12	0.78	—	1.12
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.4	—	0.68	—	0.9	0.68	—	0.9
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	$V_{CCIO} + 0.3$	0.3	$V_{CCIO} + 0.48$	—	$0.5 \times V_{CCIO}$	—	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$
HSUL-12	1.14	1.2	1.3	$2(V_{IH(DC)} - V_{REF})$	$2(V_{REF} - V_{IH(DC)})$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{REF} - V_{IH(AC)})$	$0.5 \times V_{CCIO} - 0.12$	$0.5 \times V_{CCIO}$	$0.5 \times V_{CCIO} + 0.12$	$0.4 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	$0.6 \times V_{CCIO}$

Differential I/O Standards Specifications

Table 24. Differential I/O Standards Specifications for Intel Stratix 10 Devices

I/O Standard	V_{CCIO} (V)			V_{ID} (mV) (33)		$V_{ICM(DC)}$ (V)			V_{OD} (V) (34) (35)			V_{OCM} (V) (34)		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVDS (36)	1.71	1.8	1.89	100	—	0.05	Data rate ≤700 Mbps	1.65	0.247	—	0.6	1.125	1.25	1.375
						1	Data rate >700 Mbps	1.6						
RSDS (37)	1.71	1.8	1.89	100	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (38)	1.71	1.8	1.89	200	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL (39)	1.71	1.8	1.89	300	—	0.6	Data rate ≤700 Mbps	1.7	—	—	—	—	—	—
						1	Data rate >700 Mbps	1.6						

Switching Characteristics

This section provides the performance characteristics of Intel Stratix 10 core and periphery blocks.

(33) The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

(34) R_L range: $90 \leq R_L \leq 110\ \Omega$.

(35) The specification is only applicable to default V_{OD} setting.

(36) For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rates above 700 Mbps and 0.05 V to 1.65 V for data rates below 700 Mbps.

(37) For optimized RSDS receiver performance, the receiver voltage input range must be within 0.3 V to 1.4 V.

(38) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be within 0.4 V to 1.325 V.

(39) For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rates above 700 Mbps and 0.45 V to 1.95 V for data rates below 700 Mbps.

Periphery Performance Specifications

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specifications

Table 25. High-Speed I/O Specifications for Intel Stratix 10 Devices

When serializer/deserializer (SERDES) factor J = 3 to 10, use the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

Symbol		Condition	–E1V, –I1V			–E2V, –E2L, –I2L, –I2V			–E3V, –E3X, –I3X, –I3V			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards		Clock boost factor W = 1 to 40 (40)	10	—	800	10	—	700	10	—	625	MHz
f_{HSCLK_in} (input clock frequency) Single-Ended I/O Standards		Clock boost factor W = 1 to 40 (40)	10	—	625	10	—	625	10	—	525	MHz
f_{HSCLK_OUT} (output clock frequency)		—	—	—	800 (41)	—	—	700 (41)	—	—	625 (41)	MHz
Transmitter	True Differential I/O Standards - f_{HSDR} (data rate) (42)	SERDES factor J = 4 to 10 (43)(45) (44)	(45)	—	1600	(45)	—	1434	(45)	—	1250	Mbps

continued...

(40) Clock Boost Factor (W) is the ratio between the input data rate and the input clock rate.

(41) This is achieved by using the PHY clock network.

(42) Requires package skew compensation with PCB trace length.

(43) The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

Symbol		Condition	–E1V, –I1V			–E2V, –E2L, –I2L, –I2V			–E3V, –E3X, –I3X, –I3V			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		SERDES factor J = 3 (43)(45)(44)	(45)	—	1,000	(45)	—	1,000	(45)	—	938	Mbps
		SERDES factor J = 2, uses DDR registers	(45)	—	840 (46)	(45)	—	(46)	(45)	—	(46)	Mbps
		SERDES factor J = 1, uses DDR registers	(45)	—	420 (46)	(45)	—	(46)	(45)	—	(46)	Mbps
	$t_{x\ Jitter}$ - True Differential I/O Standards	Total jitter for data rate, 600 Mbps – 1.6 Gbps	—	—	160	—	—	200	—	—	250	ps
		Total jitter for data rate, < 600 Mbps	—	—	0.1	—	—	0.12	—	—	0.15	UI
	t_{DUTY} (47)	TX output clock duty cycle for Differential I/O Standards	45	50	55	45	50	55	45	50	55	%
	t_{RISE} & t_{FALL} (44)(48)	True Differential I/O Standards	—	—	160	—	—	180	—	—	200	ps
	TCCS (47)(42)	True Differential I/O Standards	—	—	330	—	—	330	—	—	330	ps

continued...

(44) The V_{CC} and V_{CCP} must be on a combined power layer and a maximum load of 5 pF for chip-to-chip interface.

(45) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and serializer do not have a minimum toggle rate.

(46) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity meets the interface requirements.

(47) Not applicable for DIVCLK = 1.

(48) This applies to default pre-emphasis and V_{OD} settings only.

Symbol		Condition	–E1V, –I1V			–E2V, –E2L, –I2L, –I2V			–E3V, –E3X, –I3X, –I3V			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Receiver	True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 to 10 (43)(45)(44)	—	—	1600	—	—	1434	—	—	1250	Mbps
		SERDES factor J = 3 (43)(45)(44)	—	—	1,000	—	—	1,000	—	—	938	Mbps
	f_{HSDR} (data rate) (without DPA) (42)	SERDES factor J = 3 to 10	(45)	—	(49)	(45)	—	(49)	(45)	—	(49)	Mbps
		SERDES factor J = 2, uses DDR registers	(45)	—	(46)	(45)	—	(46)	(45)	—	(46)	Mbps
		SERDES factor J = 1, uses DDR registers	(45)	—	(46)	(45)	—	(46)	(45)	—	(46)	Mbps
DPA (FIFO mode)	DPA run length	—	—	—	10000	—	—	10000	—	—	10000	UI
DPA (soft CDR mode)	DPA run length	SGMII/GbE protocol	—	—	5	—	—	5	—	—	5	UI
		All other protocols	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—
Soft CDR mode	Soft-CDR ppm tolerance	—	–300	—	300	–300	—	300	–300	—	300	ppm
Non DPA mode	Sampling Window	—	—	—	330	—	—	330	—	—	330	ps

(49) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

DPA Lock Time Specifications

Figure 2. DPA Lock Time Specifications with DPA PLL Calibration Enabled

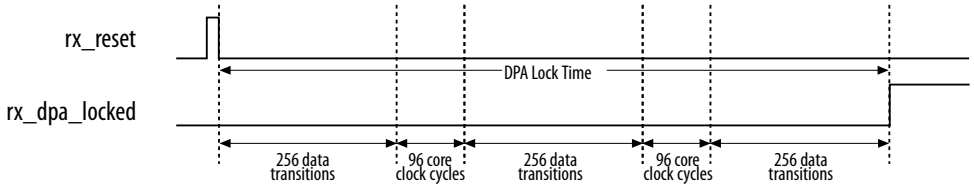


Table 26. DPA Lock Time Specifications for Intel Stratix 10 Devices

The specifications are applicable to both commercial and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions (50)	Maximum Data Transition
SPI-4	00000000001111111111	2	128	640
Parallel Rapid I/O	00001111	2	128	640
	10010000	4	64	640
Miscellaneous	10101010	8	32	640
	01010101	8	32	640

(50) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications

Figure 3. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Equal to 1.6 Gbps

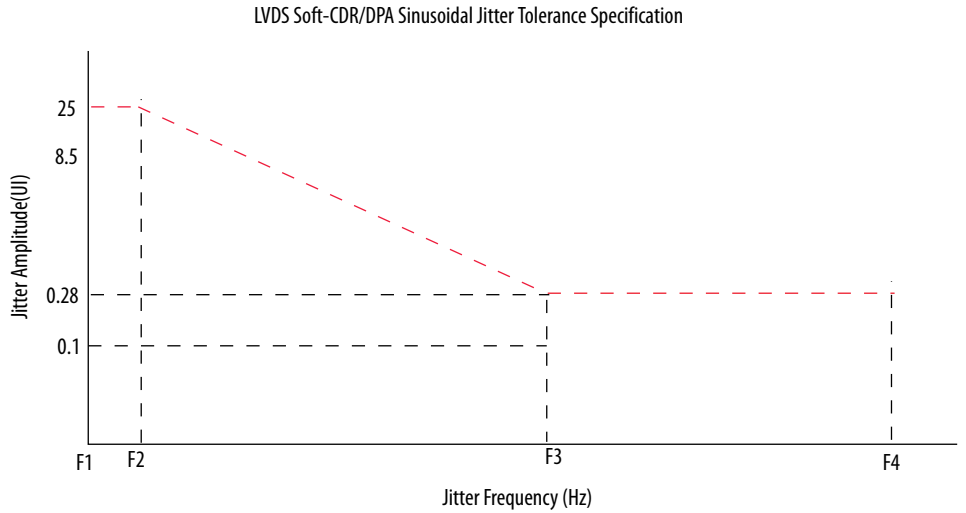
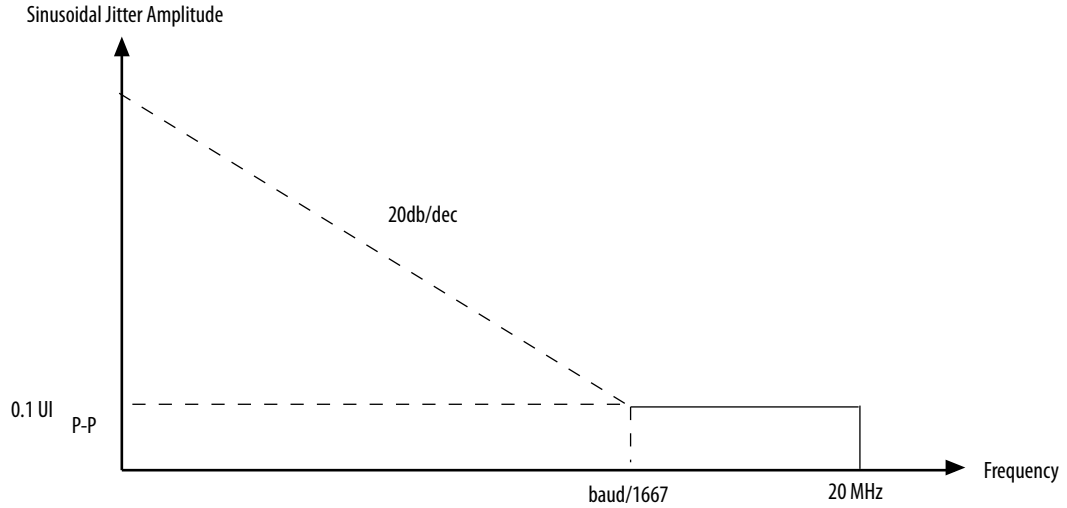


Table 27. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.6 Gbps

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.00
F2	17,565	25.00
F3	1,493,000	0.28
F4	50,000,000	0.28

Figure 4. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Less than 1.6 Gbps



Memory Standards Supported by the Hard Memory Controller

Table 28. Memory Standards Supported by the Hard Memory Controller for Intel Stratix 10 Devices

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator.

Memory Standard	Rate Support	Ping Pong PHY Support	Maximum Frequency (MHz)
DDR4 SDRAM	Quarter rate	Yes	1,333
DDR3 SDRAM	Quarter rate (51)	Yes	1,066
DDR3L SDRAM	Quarter rate	Yes	1,066

Related Information

External Memory Interface Spec Estimator
Provides the specific details of the memory standards supported.

(51) Half rate support is only up to 667 MHz.

Memory Standards Supported by the Soft Memory Controller

Table 29. Memory Standards Supported by the Soft Memory Controller for Intel Stratix 10 Devices

This table lists the overall capability of the soft memory controller. For specific details, refer to the External Memory Interface Spec Estimator.

Memory Standard	Rate Support	Maximum Frequency (MHz)
RLDRAM 3 (52)	Quarter rate	1,200
QDR IV SRAM	Quarter rate	1,066
QDR II SRAM	Half rate (53)	350
QDR II+ SRAM	Half rate	550
QDR II+ Xtreme SRAM	Half rate	633

Related Information

External Memory Interface Spec Estimator
Provides the specific details of the memory standards supported.

Memory Standards Supported by the HPS Hard Memory Controller

Table 30. Memory Standards Supported by the HPS Hard Memory Controller for Intel Stratix 10 Devices

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator.

Memory Standard	Rate Support	Maximum Frequency (MHz)
DDR4 SDRAM	Half rate	1,066
DDR3 SDRAM	Half rate	1,066
DDR3L SDRAM	Half rate	1,066

Related Information

External Memory Interface Spec Estimator
Provides the specific details of the memory standards supported.

(52) For Intel Stratix 10 RLDRAM 3, Intel only provides the PHY-only option.

(53) Full rate support is only up to 334 MHz.

Performance Specifications of the HBM2 Interface in Intel Stratix 10 MX Devices

Table 31. Performance Specifications of the HBM2 Interface in Intel Stratix 10 MX Devices

Intel Stratix 10 MX Device Speed Grade	Maximum HBM2 Interface Frequency (MHz)
-1	1000
-2	800
-3	600

HBM2 Interface Performance

Figure 5. HBM2 Performance in a 4GB4H HBM2 Device (64B access)

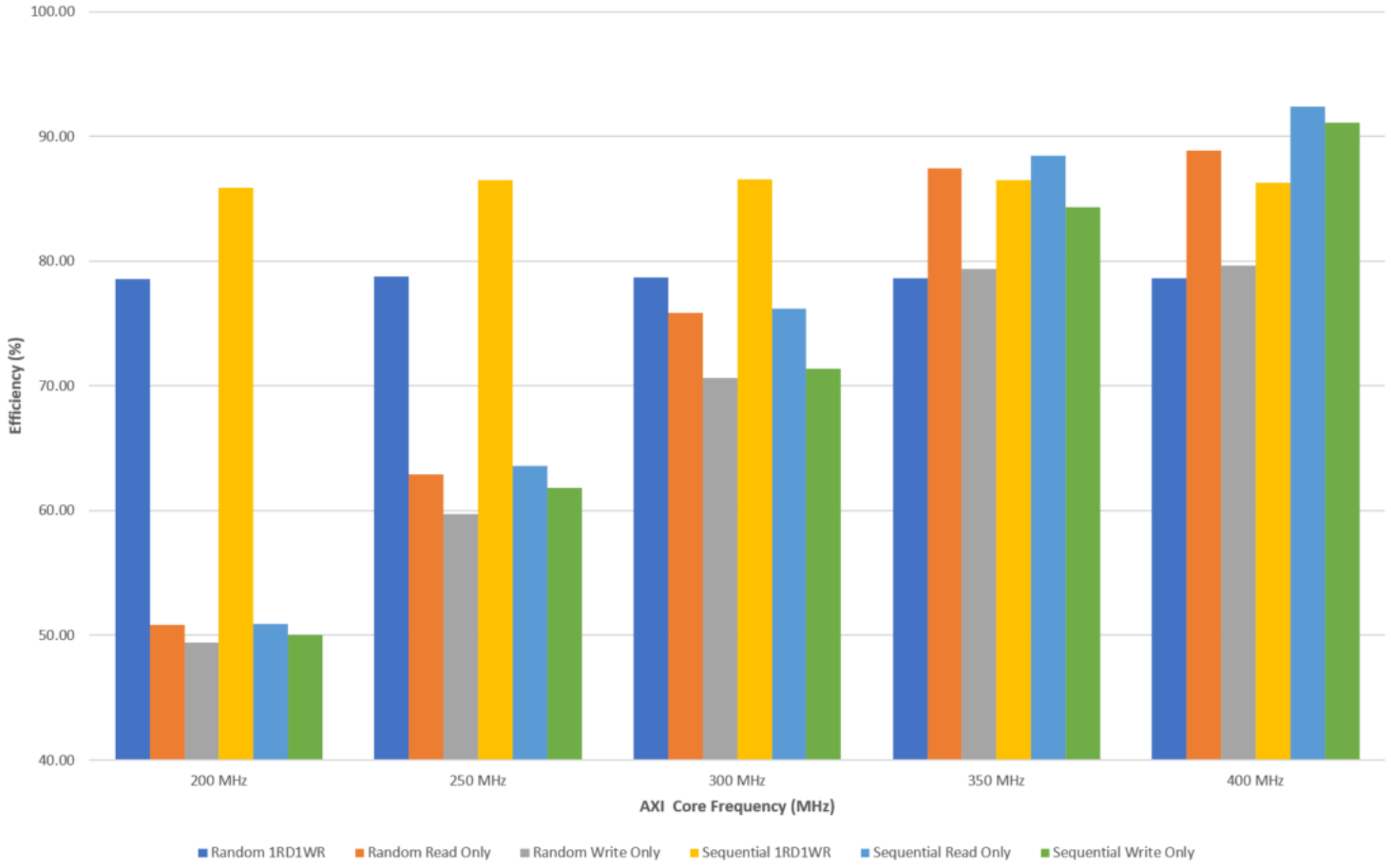
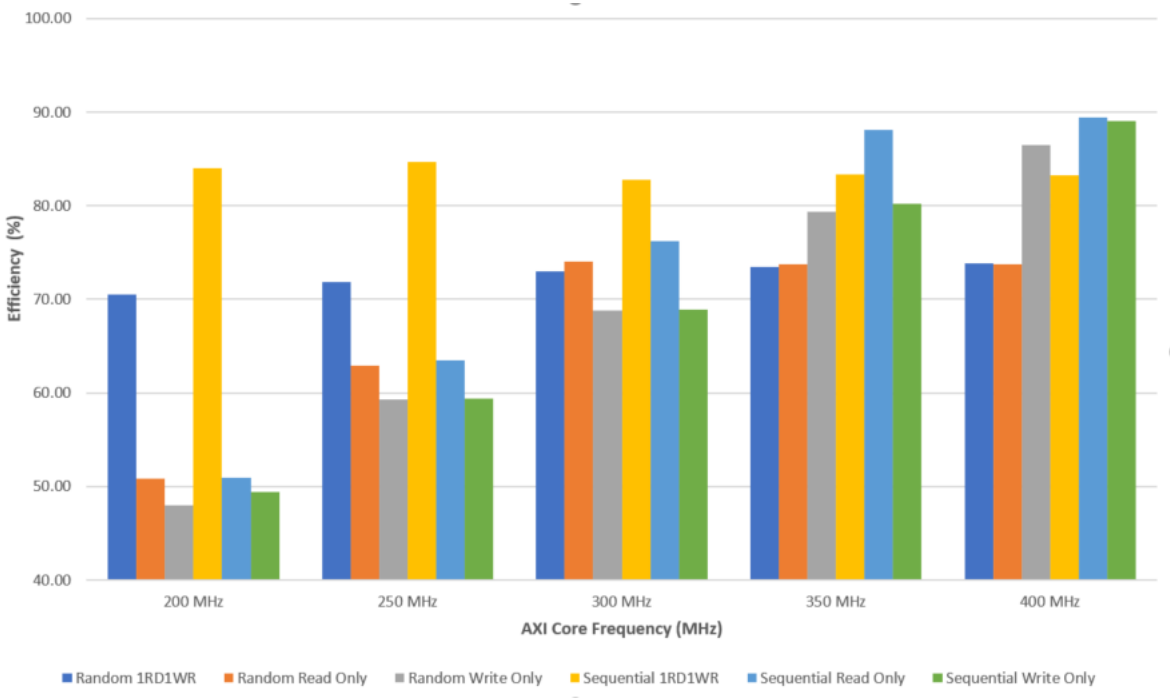


Figure 6. HBM2 Performance in a 8GB8H HBM2 Device (64B access)



Note:

- These graphs show the Efficiency information for the HBM2 interface running at 800 MHz in an Intel Stratix 10 MX device with -2 Speed Grade using 64B access, with the re-order buffer turned off and different AXI Transaction IDs enabled. Contact Factory to get the Efficiency information for other Access Configurations.
- Final timing closure available in Intel Quartus Prime 19.1.

DLL Range Specifications

Table 32. DLL Frequency Range Specifications for Intel Stratix 10 Devices

Parameter	Performance (for All Speed Grades)	Unit
DLL operating frequency range	600 – 1,333 (54)	MHz
DLL reference clock input	Minimum 600	MHz

Memory Output Clock Jitter Specifications

The clock jitter specification applies to the memory output clock pins clocked by an I/O PLL, or generated using differential signal-splitter and double data I/O circuits clocked by a PLL output routed on a PHY clock network as specified. Intel recommends using PHY clock networks for better jitter performance.

The memory clock output jitter is within the JEDEC specifications with an input of 10 ps peak-to-peak jitter.

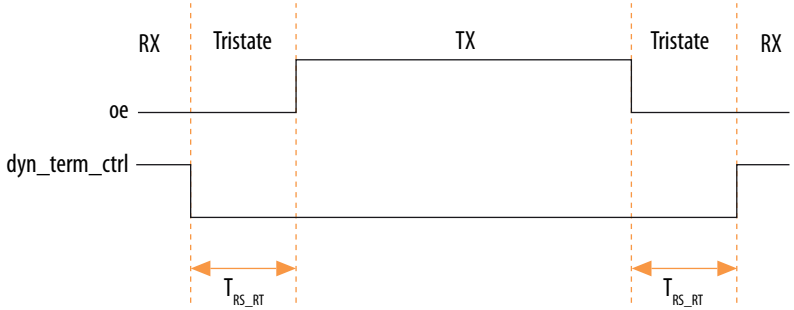
OCT Calibration Block Specifications

Table 33. OCT Calibration Block Specifications for Intel Stratix 10 Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for R_S OCT /R_T OCT calibration	> 2000	—	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	—	8	—	Full-rate cycle

(54) In the SX device family, if the HPS EMIF is instantiated, the maximum speed for that instantiation is 1,066 MHz.

Figure 7. Timing Diagram for on oe and dyn_term_ctrl Signals



L-Tile Transceiver Performance Specifications

Transceiver Performance for Intel Stratix 10 GX/SX L-Tile Devices

Table 34. Intel Stratix 10 GX/SX L-Tile Transmitter and Receiver Datarate Performance

Symbol/Description	Transceiver Speed Grade		
	-1	-2	-3
Chip-to-chip	N/A	26.6 Gbps 8 channels per tile (55)	17.4 Gbps
Backplane	N/A	12.5 Gbps	12.5 Gbps

Note: Refer to the *Transceiver Power Supply Operating Conditions* for V_{CCR_GXB} and V_{CCT_GXB} specifications when using bonded and non-bonded transceiver channels in Intel Stratix 10 L-Tile devices.

(55) Refer to *AN-778: Intel Stratix 10 Transceiver Usage* for more details on channel selection requirements.

Table 35. L-Tile ATX PLL Performance

Symbol/Description	Condition	Transceiver Speed Grade 2	Transceiver Speed Grade 3	Unit
Supported Output Frequency	Maximum Frequency	13.3	8.7	GHz
	Minimum Frequency	500		MHz
t_{LOCK} (56)	Maximum Frequency	1		ms
t_{ARESET} Required Reset Time (57) (58)	—	25		Avalon Clock Cycles

Note: TX jitter specifications for the SerialLite III protocol at 17.4 Gbps are as low as: TJ = 0.32 UI, RJ = 0.15 UI, DJ = 0.18 UI, and DCD = 0.05 UI.

Table 36. L-Tile fPLL Performance

Symbol/Description	Condition	Mode	All Transceiver Speed Grades	Unit
Supported Output Frequency (VCO frequency based)	Maximum datarate	Transceiver - HDMI	12.5	Gbps
		Transceiver - General	12.5	
		Transceiver - OTN, SDI Cascade	14.025	
	Minimum datarate	Transceiver - HDMI	4.6	Gbps
		Transceiver - General	6	
		Transceiver - OTN, SDI Cascade	7	
t_{LOCK} (56)	Maximum Frequency		1	ms
t_{ARESET} Required Reset Time (57) (58)	—		25	Avalon Clock Cycles

(56) This specification applies after the ATX PLL, fPLL, or CMU PLL has completed calibration.

(57) You must use the Avalon-MM interface to hold the PLLs in reset for the specified cycles by writing to the ATX PLL, fPLL, or CMU PLL `pll_powerdown` register.

(58) You must assert `pll_powerdown` for a minimum of 25 cycles are required if you are using a 250-MHz AVMM clock.

Table 37. L-Tile CMU PLL Performance

Symbol/Description	Condition	All Transceiver Speed Grades	Unit
Supported Output Frequency (VCO frequency based)	Maximum Frequency	5.15625	GHz
	Minimum Frequency	2.3	GHz
t_{LOCK} (56)	Maximum Frequency	1	ms
t_{ARESET} Required Reset Time (57) (58)	—	25	Avalon Clock Cycles

Related Information

AN-778: Intel Stratix 10 Transceiver Usage

Transceiver Specifications for Intel Stratix 10 GX/SX L-Tile Devices

Table 38. L-Tile Reference Clock Specifications

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
Supported I/O Standards	Dedicated reference clock pin	CML, Differential LVPECL, LVDS, and HCSL			
	RX reference clock pin	CML, Differential LVPECL, and LVDS			
Input Reference Clock Frequency (CMU PLL)		50	—	800	MHz
Input Reference Clock Frequency (ATX PLL)		100	—	800	MHz
Input Reference Clock Frequency (fPLL)		50 (59)	—	800	MHz
Rise time	20% to 80%	—	—	350	ps
Fall time	80% to 20%	—	—	350	ps
Duty cycle	—	45	—	55	%

continued...

(59) The f_{MIN} is 25 MHz when the fPLL is used for the HDMI protocol.

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
Spread-spectrum modulating clock frequency	PCIe	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5	—	%
On-chip termination resistors	—	—	100	—	Ω
Absolute V_{MAX}	Dedicated reference clock pin	—	—	1.6	V
	RX reference clock pin	—	—	1.2	V
Absolute V_{MIN}	—	–0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	mV
V_{ICM} (AC coupled)	V_{CCR_GXB} =1.03 V	—	0	—	V
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	mV
Transmitter REFCLK Phase Noise (800 MHz) (60)	100 Hz	—	—	–70	dBc/Hz
	1 kHz	—	—	–90	dBc/Hz
	10 kHz	—	—	–100	dBc/Hz
	100 kHz	—	—	–110	dBc/Hz
	≥ 1 MHz	—	—	–120	dBc/Hz
R_{REF}	—	2.0 k ±1%	—	2.0 k ±1%	Ω
$T_{SSC-MAX-PERIOD-SLEW}$	Max spread spectrum clocking (SSC) df/dt			0.75	

Note: When using PCI Express, you must meet the reference clock phase jitter requirements as specified in the *4.3.7 Refclk Specifications for 2.5 GT/s and 5.0 GT/s* and *4.3.8 Refclk Specification for 8.0 GT/s* sections of the *PCI Express Base Specification* Revision 3.0.

(60) To calculate the REFCLK phase noise requirement at frequencies other than 800 MHz, use the following formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 800 MHz + 20*log(f/800).

Table 39. L-Tile Transceiver Clock Network Maximum Data Rate Specifications

Clock Network	Maximum Performance (61)			Channel Span	Unit
	ATX	fPLL	CMU		
x1	17.4	12.5	10.3125	6 channels	Gbps
x6	17.4	12.5	N/A	6 channels	Gbps
x24	17.4 (65)	12.5	N/A	2 banks up and 1 bank down (total 24 channels) or 2 banks down and 1 bank up (total 24 channels)	Gbps
GXT clock lines	26.6	N/A	N/A	4 GXT channels within the same transceiver bank and 2 from the bank above or 2 from the bank below. (62)	Gbps

Table 40. L-Tile Receiver Specifications

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	—	High Speed Differential I/O, CML, Differential LVPECL, and LVDS			
Absolute V_{MAX} for a receiver pin (63)	—	—	—	1.2	V
Absolute V_{MIN} for a receiver pin (63) (64)	—	-0.4	—	—	V

continued...

(61) The maximum data rate depends on speed grade.

(62) If the upper ATX PLL in a bank is used as the main GXT PLL, then the channel span includes two GXT channels from the bank above. If the lower ATX PLL in a bank is used as the main GXT PLL, then the channel span includes two GXT channels from the bank below.

(63) The device cannot tolerate prolonged operation at this absolute maximum.

(64) A passive pull up resistance prevents a 0-V common mode voltage on AC coupled receiver pins before the FPGA is configured.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p)	V_{CCR_GXB} = 1.03 V (65)	—	—	2.0	V
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	Ω
	100-Ω setting	—	100 ± 20%	—	Ω
V_{ICM} (AC coupled)	V_{CCR_GXB} = 1.03 V	—	700	—	mV
	V_{CCR_GXB} = 1.12 V	—	750	—	mV
t_{LTR} (66)	—	—	—	1	ms
t_{LTD} (67)	—	4	—	—	µs
t_{LTD_manual} (68)	—	4	—	—	µs
$t_{LTR\_LTD\_manual}$ (69)	—	15	—	—	µs
Run Length	—	—	—	200	UI
CDR ppm tolerance	PCIe-only	-300	—	300	ppm
	All other protocols	-1000	—	1000	ppm

(65) Bonded channels operating at data rates above 16 Gbps require 1.12 V ± 20 mV at the pin. For a given L-Tile, if there are channels that need the higher power supply, tie all the channels on that side to the higher power supply.

(66) t_{LTR} is the time required for the receiver CDR to lock to the input reference clock frequency after coming out of reset, or after the CDR's calibration is complete.

(67) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(68) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(69) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

Table 41. L-Tile Transmitter Specifications

Symbol/Description	Condition	Transceiver Speed Grade 2 and 3			Unit
		Min	Typ	Max	
Supported I/O Standards	—	High Speed Differential I/O (70)			—
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	Ω
	100-Ω setting	—	100 ± 20%	—	Ω
V_{OCM} (AC coupled)	V_{CCT_GXB} = 1.03 V	—	515	—	mV
Rise time (71)	20% to 80%	20	—	130	ps
Fall time (71)	80% to 20%	20	—	130	ps
Intra-differential pair skew	TX V_{CM} = 0.5 V and slew rate of 15 ps	—	—	15 (72)	ps

Table 42. L-Tile Typical Transmitter V_{OD} Settings

Symbol	V_{OD} Setting (73)	V_{OD}/V_{CCT_GXB} Ratio
V_{OD} differential value = V_{OD}/V_{CCT_GXB} ratio x V_{CCT_GXB}	31	1.00
	30	0.97
	29	0.93
	28	0.90
	27	0.87
	26	0.83

continued...

(70) High Speed Differential I/O is the dedicated I/O standard for the transmitter in Intel Stratix 10 L-/H-Tile transceivers.

(71) The Intel Quartus Prime software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

(72) This specification pertains to Hyper Memory Cube.

(73) Intel recommends a V_{OD} ranging from 31 to 17.

Symbol	V_{OD} Setting [73]	V_{OD}/V_{CCT_GXB} Ratio
	25	0.80
	24	0.77
	23	0.73
	22	0.70
	21	0.67
	20	0.63
	19	0.60
	18	0.57
	17	0.53
	16	0.50
	15	0.47
	14	0.43
	13	0.40
	12	0.37

Table 43. L-Tile Transmitter Channel-to-channel Skew Specifications

Mode	Channel Span	Maximum Skew	Unit
x6 Clock	Up to 6 channels in one bank	61	ps
x24 Clock	Up to 24 channels in one tile	500 [74]	ps

(73) Intel recommends a V_{OD} ranging from 31 to 17.

(74) 500 ps is not supported for all configurations and depends upon the Master CGB placement.

Table 44. Transceiver Clocks Specifications for Intel Stratix 10 L-Tile Devices

Clock	Value	Unit
reconfig_clk	≤ 150	MHz
fixed_clk for the RX detect circuit	250 ± 20%	MHz

For OSC_CLK_1 specifications, refer to the External Configuration Clock Source Requirements section.

Related Information

- External Configuration Clock Source Requirements on page 96
- PLLs and Clock Networks

H-Tile Transceiver Performance Specifications

Transceiver Performance for Intel Stratix 10 GX/SX/MX/TX H-Tile Devices

Table 45. Intel Stratix 10 GX/SX/MX/TX H-Tile Transmitter and Receiver Datarate Performance

Symbol	Description	Transceiver Speed Grade		
		-1	-2	-3
GX channels	Chip-to-chip and Backplane	17.4 Gbps		
GXT channels	Chip-to-chip and Backplane	28.3 Gbps (75)	26.6 Gbps	N/A

Note: Refer to the *Transceiver Power Supply Operating Conditions* for V_{CCR_GXB} and V_{CCT_GXB} specifications when using bonded and non-bonded transceiver channels in Intel Stratix 10 H-Tile devices.

(75) Only four GXT channels per bank are supported for backplane applications operating at 28.3 Gbps.

Table 46. H-Tile ATX PLL Performance

Symbol/Description	Condition	Transceiver Speed Grade 1	Transceiver Speed Grade 2	Transceiver Speed Grade 3	Unit
Supported Output Frequency	Maximum Frequency	14.15	12.9	8.7	GHz
	Minimum Frequency	500			MHz
t_{LOCK} (76)	Maximum Frequency	1			ms
t_{ARESET} (77)	—	25			Avalon Clock Cycles

Note: TX jitter specifications for the SerialLite III protocol at 17.4 Gbps are as low as: TJ = 0.32 UI, RJ = 0.15 UI, DJ = 0.18 UI, and DCD = 0.05 UI.

Table 47. H-Tile Fractional PLL Performance

Symbol/Description	Condition	Mode	All Transceiver Speed Grades	Unit
Supported Output Frequency (VCO frequency based)	Maximum datarate	Transceiver - HDMI	12.5	Gbps
		Transceiver - General	12.5	
		Transceiver - OTN, SDI Cascade	14.025	
	Minimum datarate	Transceiver - HDMI	4.6	Gbps
		Transceiver - General	6	
		Transceiver - OTN, SDI Cascade	7	
t_{LOCK} (76)	Maximum Frequency		1	ms
t_{ARESET} (77)	—		25	Avalon Clock Cycles

(76) This specification applies after the ATX PLL, fPLL, or CMU PLL has completed calibration.

(77) You must use the Avalon-MM interface to hold the PLLs in reset for the specified cycles by writing to the ATX PLL, fPLL, or CMU PLL `pll_powerdown` register.

Table 48. H-Tile CMU PLL Performance

Symbol/Description	Condition	All Transceiver Speed Grades	Unit
Supported Output Frequency	Maximum Frequency	5.15625	GHz
	Minimum Frequency	2.450	GHz
t_{LOCK} (76)	Maximum Frequency	1	ms
t_{ARESET} (77)	—	25	Avalon Clock Cycles

Transceiver Specifications for Intel Stratix 10 GX/SX H-Tile Devices

Table 49. H-Tile Reference Clock Specifications

Symbol/Description	Condition	Min	Typ	Max	Unit
Supported I/O Standards	Dedicated reference clock pin	CML, Differential LVPECL, LVDS, and HCSL			
	RX reference clock pin	CML, Differential LVPECL, and LVDS			
Input Reference Clock Frequency (CMU PLL)		50	—	800	MHz
Input Reference Clock Frequency (ATX PLL)		100	—	800	MHz
Input Reference Clock Frequency (fPLL PLL)		50 (78)	—	800	MHz
Rise time	20% to 80%	—	—	350	ps
Fall time	80% to 20%	—	—	350	ps
Duty cycle	—	45	—	55	%
Spread-spectrum modulating clock frequency	PCIe	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5	—	%
On-chip termination resistors	—	—	100	—	Ω
Absolute V_{MAX}	Dedicated reference clock pin	—	—	1.6	V
	RX reference clock pin	—	—	1.2	V
Absolute V_{MIN}	—	–0.4	—	—	V

continued...

(78) The f_{MIN} is 25 MHz when the fPLL is used for the HDMI protocol.

Symbol/Description	Condition	Min	Typ	Max	Unit
Peak-to-peak differential input voltage	—	200	—	1600	mV
V_{ICM} (AC coupled)	V_{CCR_GXB} =1.03 V	—	0	—	V
	V_{CCR_GXB} = 1.12 V	—	0	—	V
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	mV
Transmitter REFCLK Phase Noise (800 MHz) (79) (80)	100 Hz	—	—	–70	dBc/Hz
	1 kHz	—	—	–90	dBc/Hz
	10 kHz	—	—	–100	dBc/Hz
	100 kHz	—	—	–110	dBc/Hz
	≥ 1 MHz	—	—	–120	dBc/Hz
R_{REF}	—	—	2.0 k ±1%	—	Ω
$T_{SSC-MAX-PERIOD-SLEW}$	Max SSC df/dt			0.75	

Note: When using PCI Express, you must meet the reference clock phase jitter requirements as specified in the *4.3.7 Refclk Specifications for 2.5 GT/s and 5.0 GT/s* and *4.3.8 Refclk Specification for 8.0 GT/s* sections of the *PCI Express Base Specification* Revision 3.0.

(79) To calculate the REFCLK phase noise requirement at frequencies other than 800 MHz, use the following formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 800 MHz + 20*log(f/800).

(80) A phase noise (PN) mask overrides the REFCLK noise.

Table 50. H-Tile Transceiver Clock Network Maximum Data Rate Specifications

Clock Network	Maximum Performance (81)			Channel Span	Unit
	ATX	fPLL	CMU		
x1	17.4	12.5	10.3125	6 channels	Gbps
x6	17.4	12.5	N/A	6 channels	Gbps
x24	17.4 (86)	12.5	N/A	2 banks up and 1 bank down (total 24 channels) or 2 banks down and 1 bank up (total 24 channels)	Gbps
GXT clock lines	28.3	N/A	N/A	4 GXT channels within the same transceiver bank and 2 from the bank above or 2 from the bank below. (82)	Gbps

Table 51. H-Tile Receiver Specifications

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
Supported I/O Standards	—	High Speed Differential I/O, CML, Differential LVPECL, and LVDS			
Absolute V_{MAX} for a receiver pin (83)	—	—	—	1.2	V
Absolute V_{MIN} for a receiver pin (84)	—	-0.4	—	—	V

continued...

(81) The maximum data rate depends on speed grade.

(82) If the upper ATX PLL in a bank is used as the main GXT PLL, then the channel span includes two GXT channels from the bank above. If the lower ATX PLL in a bank is used as the main GXT PLL, then the channel span includes two GXT channels from the bank below.

(83) The device cannot tolerate prolonged operation at this absolute maximum.

(84) A passive pull up resistance prevents a 0-V common mode voltage on AC coupled receiver pins before the FPGA is configured.

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration (85)	—	—	—	2.0	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration (85)	V_{CCR_GXB} = 1.03 V, 1.12 V (86), (87)	—	—	2.0	V
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	Ω
	100-Ω setting	—	100 ± 20%	—	Ω
V_{ICM} (AC coupled)	V_{CCR_GXB} = 1.03 V (87)	—	700	—	mV
	V_{CCR_GXB} = 1.12 V (87)	—	750	—	mV
t_{LTR} (88)	—	—	—	1	ms
t_{LTD} (89)	—	4	—	—	µs
t_{LTD_manual} (90)	—	4	—	—	µs

continued...

(85) DC coupling specifications are pending silicon characterization.

(86) Bonded channels operating at data rates above 16 Gbps require 1.12 V ± 20 mV at the pin. For channels that are placed in the same H-Tile as the channels that required 1.12 V ± 20 mV, V_{CCR_GXB} = 1.12 V ± 20 mV.

(87) For GXT channels, V_{CCR_GXB} must be 1.12 V. For GX channels, V_{CCR_GXB} must be 1.03 V. V_{CCR_GXB} must be 1.12 V for the transceiver on the same H-Tile when using GX and GXT channels together.

(88) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset or after CDR calibration is completed.

(89) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(90) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
$t_{LTR\_LTD\_manual}$ (91)	—	15	—	—	µs
Run Length	—	—	—	200	UI
CDR ppm tolerance	PCIe-only	-300	—	300	ppm
	All other protocols	-1000	—	1000	ppm

Table 52. H-Tile Transmitter Specifications

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	—	High Speed Differential I/O (92)			—
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	Ω
	100-Ω setting	—	100 ± 20%	—	Ω
V_{OCM} (AC coupled)	V_{CCT_GXB} = 1.03 V (93)	—	515	—	mV
V_{OCM} (AC coupled)	V_{CCT_GXB} = 1.12 V (93)	—	560		mV
V_{OCM} (DC coupled)	V_{CCT_GXB} = 1.03 V (93)	—	515	—	mV
V_{OCM} (DC coupled)	V_{CCT_GXB} = 1.12 V (93)	—	560	—	mV

continued...

(91) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

(92) High Speed Differential I/O is the dedicated I/O standard for the transmitter in Intel Stratix 10 transceivers.

(93) For GXT channels, V_{CCT_GXB} must be 1.12 V. For GX channels, V_{CCT_GXB} must be 1.03 V. V_{CCT_GXB} must be 1.12 V when using GX and GXT channels together within the same H-Tile.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Rise time (94)	20% to 80%	20	—	130	ps
Fall time (94)	80% to 20%	20	—	130	ps
Intra-differential pair skew	TX V_{CM} = 0.5 V and slew rate of 15 ps	—	—	15 (95)	ps

Table 53. H-Tile Typical Transmitter V_{OD} Settings

Symbol	V_{OD} Setting (96)	V_{OD}/V_{CCT_GXB} Ratio
V_{OD} differential value = V_{OD}/V_{CCT_GXB} ratio x V_{CCT_GXB}	31	1.00
	30	0.97
	29	0.93
	28	0.90
	27	0.87
	26	0.83
	25	0.80
	24	0.77
	23	0.73
	22	0.70
	21	0.67
	20	0.63

continued...

(94) The Intel Quartus Prime software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

(95) This specification pertains to Hyper Memory Cube.

(96) Intel recommends a V_{OD} ranging from 31 to 17.

Symbol	V_{OD} Setting (96)	V_{OD}/V_{CCT_GXB} Ratio
	19	0.60
	18	0.57
	17	0.53
	16	0.50
	15	0.47
	14	0.43
	13	0.40
	12	0.37

Table 54. H-Tile Transmitter Channel-to-channel Skew Specifications

Mode	Channel Span	Maximum Skew	Unit
x6 Clock	Up to 6 channels in one bank	61	ps
x24 Clock	Up to 24 channels in one bank	500 (97)	ps

Table 55. Transceiver Clocks Specifications for Intel Stratix 10 GX/SX H-Tile Devices

Clock	Value	Unit
`reconfig_clk`	≤ 150	MHz
`fixed_clk` for the RX detect circuit	250 ± 20%	MHz

For OSC_CLK_1 specifications, refer to the External Configuration Clock Source Requirements section.

Related Information

- External Configuration Clock Source Requirements on page 96
- PLLs and Clock Networks

(96) Intel recommends a V_{OD} ranging from 31 to 17.

(97) 500 ps is not supported for all configurations and depends upon the Master CGB placement.

E-Tile Transceiver Performance Specifications

Transceiver Performance for Intel Stratix 10 E-Tile Devices

Table 56. E-Tile Transmitter and Receiver Data Rate Performance Specifications

Symbol/Description	Condition	Minimum	Typical	Maximum	Unit
Supported datarate(98)	NRZ	1		28.9	Gbps
	PAM-4	2		57.8(99)	Gbps

Transceiver Reference Clock Specifications

Table 57. E-Tile Reference Clock LVPECL DC Electrical Characteristics

Symbol	Refclk Parameter	Minimum	Typical	Maximum	Unit
VTT	Termination Voltage (2.5V compliant)	0.4	0.5	0.6	V
VTT	Termination Voltage (3.3V compliant)	1.04	1.3	1.56	V
RTT	Termination Resistor	40	50	60	Ohm
V_{DIFF}	Differential Voltage	0.4	0.8	1.2	V
V_{CM}	Input Common Mode Voltage (2.5V compliant, no internal termination resistor)	$V_{DIFF}/2$		$V_{CCCLK\_GXE}-V_{DIFF}/2$	V

continued...

(98) The supported datarate is for chip-to-chip and backplane links.

(99) Two channels are combined to support up to 57.8 Gbps.

Symbol	Refclk Parameter	Minimum	Typical	Maximum	Unit
V_{CM}	Input Common Mode Voltage (2.5V compliant, internal termination resistor)	V_{CCCLK_GXE} - 1.6	V_{CCCLK_GXE} - 1.3	V_{CCCLK_GXE} - 1.0	V
V_{CM}	Input Common Mode Voltage (3.3V compliant, no internal termination resistor)	$V_{DIFF}/2$		V_{CCCLK_GXE}-$V_{DIFF}/2$	V
V_{CM}	Input Common Mode Voltage (3.3V compliant, internal termination resistor)	1.4	2	2.6	V

Table 58. E-Tile Reference Clock Electrical & Jitter Requirements

Parameter	Condition	Minimum	Typical	Maximum	Unit
Frequency	-	125	156.25	700	MHz
Frequency Tolerance	-	-100		100	PPM
Clock Duty Cycle	-	45	50	55	%
Rise & Fall Times	20% - 80%	40		300	ps
Phase Jitter	12 KHz - 20 MHz		0.375	0.5	ps rms
Phase Noise (100)	10 KHz			-130	dBc/Hz
	100 KHz			-138	dBc/Hz
	500 KHz			-138	dBc/Hz
	3 MHz			-140	dBc/Hz
	10 MHz			-144	dBc/Hz
	20 MHz			-146	dBc/Hz

(100) The phase noise numbers in the table above are the maximum acceptable phase noise values measured at a carrier frequency of 156.25 MHz. To calculate the phase noise requirement at any other frequency, use the formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 156.25 MHz + $20*\log_{10}(f/156.25)$

Transmitter Specifications for Intel Stratix 10 E-Tile Devices

Table 59. E-Tile Transmitter Specifications

Symbol/Description	Condition	Minimum	Typical	Maximum	Unit
Transmitter differential output voltage peak-to-peak	No precursor/postcursor de-emphasis		0.965		V
Transmitter common mode voltage		$V_{CCRT\_GXE}/2$			V

Receiver Specifications for Intel Stratix 10 E-Tile Devices

Table 60. E-Tile Receiver Specifications

Symbol/Description	Condition	Minimum	Typical	Maximum	Unit
Receiver run length(101)				100(102)	symbols
DC input impedance		40		60	ohm
DC differential input impedance		80	100	120	ohm
Powered down DC input impedance	Receiver pin impedance when the receiver termination is powered down	100k			ohm
Electrical Idle detection voltage	-	65		175	mV
Differential termination	From DC to 100 MHz	80	100	120	ohm
PPM tolerance	Allowed frequency mismatch between REFCLK and RX data			750	ppm

(101) No additional transition density requirements apply.

(102) The incoming data must be statistically DC-balanced.

Core Performance Specifications

Clock Tree Specifications

Table 61. Clock Tree Performance for Intel Stratix 10 Devices

Parameter	Performance			Unit
	–E1V, –I1V	–E2V, –E2L, –I2V, –I2L	–E3V, –E3X, –I3V, –I3X	
Programmable clock routing	1,000	900	780	MHz

PLL Specifications

Fractional PLL Specifications

Table 62. Fractional PLL Specifications for Intel Stratix 10 Devices

These specifications are applicable when fPLL is used in core mode.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	—	29	—	800 (103)	MHz
f_{INPFD}	Input clock frequency to the phase frequency detector (PFD)	—	29	—	700	MHz
f_{VCO}	PLL voltage-controlled oscillator (VCO) operating range for core applications	—	6	—	14.025	GHz
$t_{EINDUTY}$	Input clock duty cycle	—	40	—	60	%
f_{OUT}	Output frequency for internal clock	—	—	—	1	GHz
$f_{DYCONFIGCLK}$	Dynamic configuration clock for `reconfig_clk`	—	—	—	125	MHz
t_{LOCK}	Time required to lock from end-of-device configuration	—	—	—	1	ms

continued...

(103) This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is dependent on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
f_{CLBW}	PLL closed-loop bandwidth	—	0.3	—	4	MHz
t_{INCCJ} (104), (105)	Input clock cycle-to-cycle jitter	$F_{REF} \geq 100$ MHz	—	—	0.13	UI (p-p)
		$F_{REF} < 100$ MHz	—	—	±650	ps (p-p)
t_{OUTPJ} (106)	Period jitter for clock output	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
t_{OUTCCJ} (106)	Cycle-to-cycle jitter for clock output	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	—	32	—	bit

Related Information

Memory Output Clock Jitter Specifications on page 35
Provides more information about the external memory interface clock output jitter specifications.

(104) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(105) F_{REF} is f_{IN}/N, specification applies when $N = 1$.

(106) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specifications for Intel Stratix 10 Devices table.

I/O PLL Specifications

Table 63. I/O PLL Specifications for Intel Stratix 10 Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	–1 speed grade	10	—	1,100 (107)	MHz
		–2 speed grade	10	—	900 (107)	MHz
		–3 speed grade	10	—	750 (107)	MHz
f_{INPFD}	Input clock frequency to the PFD	—	10	—	325	MHz
f_{VCO}	PLL VCO operating range	–1 speed grade	600	—	1,600	MHz
		–2 speed grade	600	—	1,434	MHz
		–3 speed grade	600	—	1,280 (108)	MHz
f_{CLBW}	PLL closed-loop bandwidth	—	0.5	—	10	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	—	40	—	60	%
f_{OUT}	Output frequency for internal clock (C counter)	–1 speed grade	—	—	1,100	MHz
		–2 speed grade	—	—	900	MHz
		–3 speed grade	—	—	750	MHz
f_{OUT_EXT}	Output frequency for external clock output	–1 speed grade	—	—	800	MHz
		–2 speed grade	—	—	720	MHz
		–3 speed grade	—	—	650	MHz

continued...

(107) This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is dependent on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

(108) This specification is only applicable when the I/O PLL is instantiated with the IOPLL Intel FPGA IP core. For I/O PLL instantiated with LVDS SERDES Intel FPGA IP core, PHY Lite for Parallel Interfaces Intel Stratix 10 FPGA IP core, External Memory Interfaces Intel Stratix 10 FPGA IP core, and High Bandwidth Memory (HBM-2) Interface Intel FPGA IP core, the maximum f_{VCO} is 1,250 MHz.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{OUTDUTY}$	Duty cycle for dedicated external clock output (when set to 50%)	—	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	—	5	ns
$f_{DYCONFIGCLK}$	Dynamic configuration clock for `mgmt_clk` and `scanclk`	—	—	—	200	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `areset`	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the `areset` signal	—	10	—	—	ns
t_{INCCJ} (109)(110)	Input clock cycle-to-cycle jitter	$F_{REF} \geq 100$ MHz	—	—	0.15	UI (p-p)
		$F_{REF} < 100$ MHz	—	—	±750	ps (p-p)
t_{OUTPJ_DC}	Period jitter for dedicated clock output	$F_{OUT} \geq 100$ MHz	—	—	175	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	17.5	mUI (p-p)
t_{OUTCCJ_DC}	Cycle-to-cycle jitter for dedicated clock output	$F_{OUT} \geq 100$ MHz	—	—	175	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	17.5	mUI (p-p)
t_{OUTPJ_IO} (111)	Period jitter for clock output on the regular I/O	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)

continued...

(109) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(110) F_{REF} is f_{IN}/N, specification applies when $N = 1$.

(111) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specifications for Intel Stratix 10 Devices table.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{OUTCCJ_IO} (111)	Cycle-to-cycle jitter for clock output on the regular I/O	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
$t_{CASC\_OUTPJ\_DC}$	Period jitter for dedicated clock output in cascaded PLLs through dedicated cascade path and core clock fabric	$F_{OUT} \geq 100$ MHz	—	—	175	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	17.5	mUI (p-p)

Related Information

Memory Output Clock Jitter Specifications on page 35
Provides more information about the external memory interface clock output jitter specifications.

DSP Block Specifications

Table 64. DSP Block Performance Specifications for Intel Stratix 10 Devices

Mode	Performance			Unit
	–E1V, –I1V	–E2V, –E2L, –I2V, –I2L	–E3V, –E3X, –I3V, –I3X	
Fixed-point 18 × 19 multiplication mode	1,000	771	667	MHz
Fixed-point 27 × 27 multiplication mode (112)	1,000	771	667	MHz
Fixed-point 18 × 18 multiplier adder mode (112)	1,000	771	667	MHz
Fixed-point 18 × 18 multiplier adder summed with 36-bit input mode (112)	1,000	771	667	MHz
Fixed-point 18 × 19 systolic mode	1,000	771	667	MHz
Complex 18 × 19 multiplication mode	1,000	771	667	MHz
Floating point multiplication mode	750	579	500	MHz

continued...

(112) When `chainin` or `chainout` is enabled, the performance specifications for the following speed grades are as follows:
- –E1V and –I1V: 750 MHz
- –E2V, –E2L, –I2V, and –I2L: 578 MHz
- –E3V, –E3X, –I3V, and –I3X: 507 MHz

Mode	Performance			Unit
	–E1V, –I1V	–E2V, –E2L, –I2V, –I2L	–E3V, –E3X, –I3V, –I3X	
Floating point adder or subtract mode	750	579	500	MHz
Floating point multiplier adder or subtract mode	750	579	500	MHz
Floating point multiplier accumulate mode	750	579	500	MHz
Floating point vector one mode	750	579	500	MHz
Floating point vector two mode	750	579	500	MHz

Memory Block Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to **50%** output duty cycle. Use the Intel Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

Table 65. Memory Block Performance Specifications for Intel Stratix 10 Devices

Memory	Mode	Performance			Unit
		–E1V, –I1V	–E2V, –E2L, –I2V, –I2L	–E3V, –E3X, –I3V, –I3X	
MLAB	Single port, all supported widths (×16/×32)	1,000	782	667	MHz
	Simple dual-port, all supported widths (×16/×32)	1,000	782	667	MHz
	Simple dual-port with read-during-write option	550	450	400	MHz
	ROM, all supported width (×16/×32)	1,000	782	667	MHz
M20K Block	Single-port, all supported widths	1,000	782	667	MHz
	Simple dual-port, all supported widths	1,000	782	667	MHz
	Simple dual-port, coherent read enabled	1,000	782	667	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	800	640	560	MHz

continued...

Memory	Mode	Performance			
		–E1V, –I1V	–E2V, –E2L, –I2V, –I2L	–E3V, –E3X, –I3V, –I3X	Unit
	Simple dual-port with ECC enabled, 512 × 32	600	480	420	MHz
	Simple dual-port with ECC, optional pipeline registers enabled, and fast write mode, 512 × 32	1,000	782	667	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, with the read-during-write option set to **Old Data**, 512 × 32	1,000	750	667	MHz
	True dual port, all supported widths	600	500	420	MHz
	Simple quad-port, all supported widths	600	480	420	MHz
	ROM, all supported widths	1,000	782	667	MHz
eSRAM (113)(114)	Simple dual-port	200–750	200–640	200–500	MHz

Internal Temperature Sensing Diode Specifications

Table 66. Internal Temperature Sensing Diode Specifications for Intel Stratix 10 Devices

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time
–40 to 125 °C (115)	±5 °C	No	1 KSPS	< 1 ms

(113) The input clock source for eSRAM must not exceed 20 ps peak-to-peak, or 1.42 ps RMS at $1e^{-12}$ BER or 1.22 ps at $1e^{-16}$ BER.

(114) For speed grade –3 devices, the following clock frequency ranges are not supported:
- 466.51 MHz – 499.99 MHz
- 233.26 MHz – 249.99 MHz

(115) Temperature range refers to junction temperature.

External Temperature Sensing Diode Specifications

Table 67. External Temperature Sensing Diode Specifications for Intel Stratix 10 Devices

- The typical value is at 25°C.
- Diode accuracy improves with lower injection current.
- Absolute accuracy is dependent on third-party external diode ADC and integration specifics.

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	10	—	100	µA
V_{bias}, voltage across diode	0.35	—	0.9	V
Series resistance (core fabric TSD)	—	—	< 3	Ω
Series resistance (L-Tile and H-Tile TSD)	—	—	< 1	Ω
Series resistance (E-Tile TSD)	—	—	(116)	Ω
Diode ideality factor (core fabric TSD)	—	1.006	—	—
Diode ideality factor (L-Tile and H-Tile TSD)	—	1.03	—	—
Diode ideality factor (E-Tile TSD)	—	(116)	—	—

Internal Voltage Sensor Specifications

Table 68. Internal Voltage Sensor Specifications for Intel Stratix 10 Devices

Parameter	Minimum	Typical	Maximum	Unit
Resolution	—	8	—	Bit
Sampling rate	—	—	1.0	KSPS
Differential non-linearity (DNL)	—	—	±1	LSB
Integral non-linearity (INL)	—	—	±1	LSB
Input capacitance	—	—	40	pF

continued...

(116) Pending silicon characterization.

Parameter		Minimum	Typical	Maximum	Unit
Voltage sensor accuracy, V_{in} range: 0 V to 1.24 V		–3	—	3	%
Unipolar Input Mode	Input signal range for Vsigp	0	—	1.49	V
	Common mode voltage on Vsign	0	—	0.25	V
	Input signal range for Vsigp – Vsign	0	—	1.24	V

HPS Performance Specifications

This section provides hard processor system (HPS) specifications and timing for Intel Stratix 10 devices.

HPS Clock Performance

Table 69. Maximum HPS Clock Frequencies for Intel Stratix 10 Devices

Performance	V_{CCL_HPS} (V)	MPU Frequency (MHz)	SDRAM Interconnect Frequency(117) (MHz)	L3 Interconnect Frequency (MHz)
–E1V, –I1V	SmartVID	1,200	533	400
	0.9	1,200	533	400
	0.94	1,350	533	400 (118)
–E2V, –I2V	SmartVID	1,000	467	400
	0.9	1,000	467	400
	0.94	1,000	467	400
–E3V, –I3V	SmartVID	800	400	333
	0.9	800	400	333
	0.94	800	400	400
–E2L, –I2L(119)	0.9	1200	467	400
	0.94	1,350	467	400 (118)
–E3X, –I3X (119)	0.9	1,200	400	400
	0.94	1,350	400	400 (118)

(117) This frequency is for the `hmc_free_clk`, which is half the frequency of the HPS external memory interface (EMIF).

(118) If MPU frequency is 1,350 MHz, the L3 interconnect frequency is 385 MHz because of the clock ratios.

(119) Note that V_{CCL_HPS} can not be connected to SmartVID for –E2L, –I2L, –E3X, and –I3X devices.

Related Information

External Memory Interface Spec Estimator
Provides the specific details of the maximum allowed SDRAM operating frequency.

HPS Internal Oscillator Frequency

Table 70. HPS Internal Oscillator Frequency for Intel Stratix 10 Devices

Description	Min	Typ	Max	Unit
Internal Oscillator Frequency	100	200	300	MHz

HPS PLL Specifications

HPS PLL Input Requirements

Table 71. HPS PLL Input Requirements for Intel Stratix 10 Devices

The main HPS PLL receives its clock signals from the HPS_OSC_CLK pin. Refer to the *Intel Stratix 10 Device Family Pin Connection Guidelines* for information about assigning this pin.

Description	Min	Typ	Max	Unit
Clock input range	25	—	125	MHz
Clock input accuracy	—	—	50	PPM
Clock input duty cycle	45	50	55	%

HPS PLL Performance

Table 72. HPS PLL Performance for Intel Stratix 10 Devices

Description	Min	Max	Unit
Main PLL VCO output	—	3000	MHz
Peripheral PLL VCO output	—	3000	MHz
h2f_user0_clk (120)	—	500	MHz
h2f_user1_clk (120)	—	500	MHz

(120) The HPS PLL provides this clock to the FPGA fabric.

HPS SPI Timing Characteristics

Table 73. SPI Master Timing Requirements for Intel Stratix 10 Devices

You can adjust the input delay timing by programming the `rx_sample_dly` register.

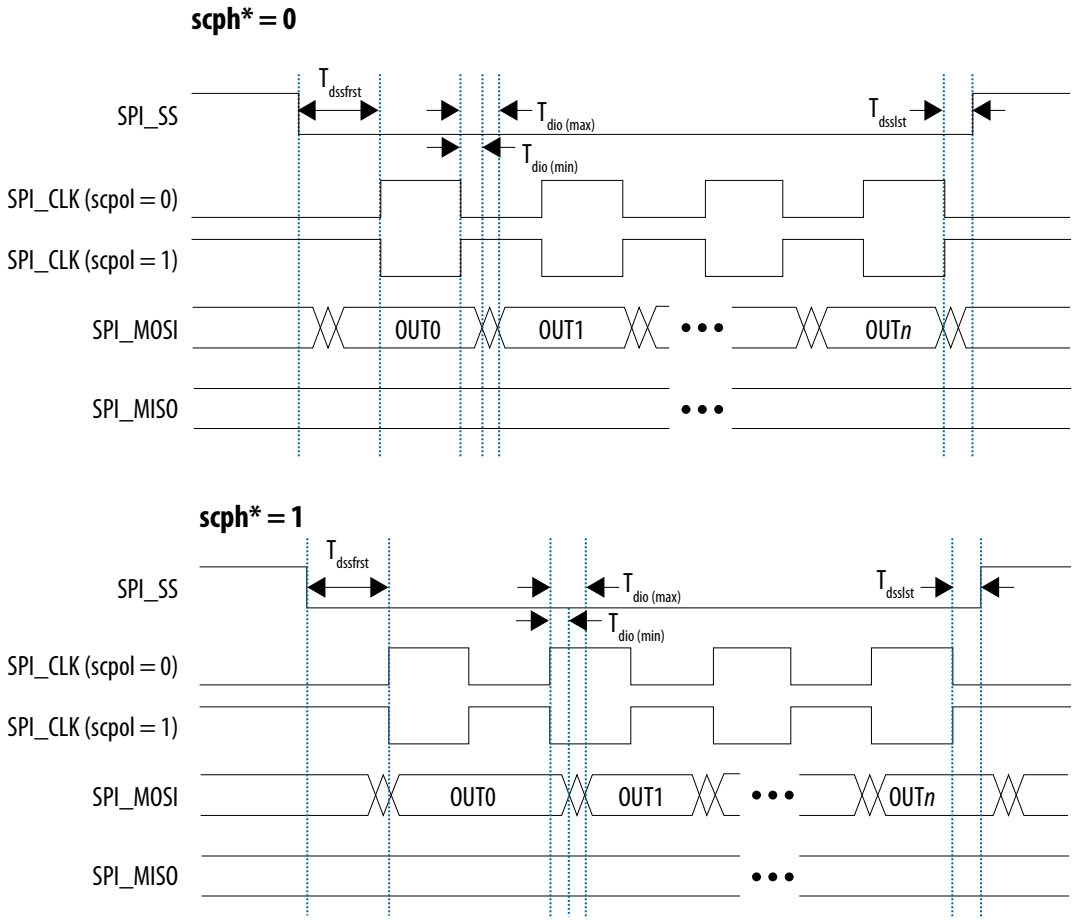
Symbol	Description	Min	Typ	Max	Unit
$T_{spi\_ref\_clk}$	The period of the SPI internal reference clock, sourced from `l4_main_clk`	2.5	—	—	ns
T_{clk}	SPIM_CLK clock period	16.67	—	—	ns
$T_{dutycycle}$	SPIM_CLK duty cycle	45	50	55	%
T_{ck_jitter}	SPIM_CLK output jitter	—	—	2	%
T_{dio}	Master-out slave-in (MOSI) output skew	–3	—	2	ns
$T_{dssfrst}$ (121)	SPI_SS_N asserted to first SPIM_CLK edge	$(1.5 \times T_{clk}) - 2$	—	—	ns
T_{dsslst} (121)	Last SPIM_CLK edge to SPI_SS_N deasserted	$T_{clk} - 2$	—	—	ns
T_{su} (122)	SPIM_MISO setup time with respect to SPIM_CLK capture edge	4 .5 – (`rx_sample_dly` × $T_{spi\_ref\_clk}$) (123)	—	—	ns
T_h (122)	Input hold in respect to SPIM_CLK capture edge	1.3 + (`rx_sample_dly`× $T_{spi\_ref\_clk}$)	—	—	ns

(121) SPI_SS_N behavior differs depending on Motorola SPI, TI SSP or Microwire operational mode.

(122) The capture edge differs depending on the operational mode. For Motorola SPI, the capture edge can be the rising or falling edge depending on the `scpol` register bit; for TI SSP, the capture edge is the falling edge; for Microwire, the capture edge is the rising edge.

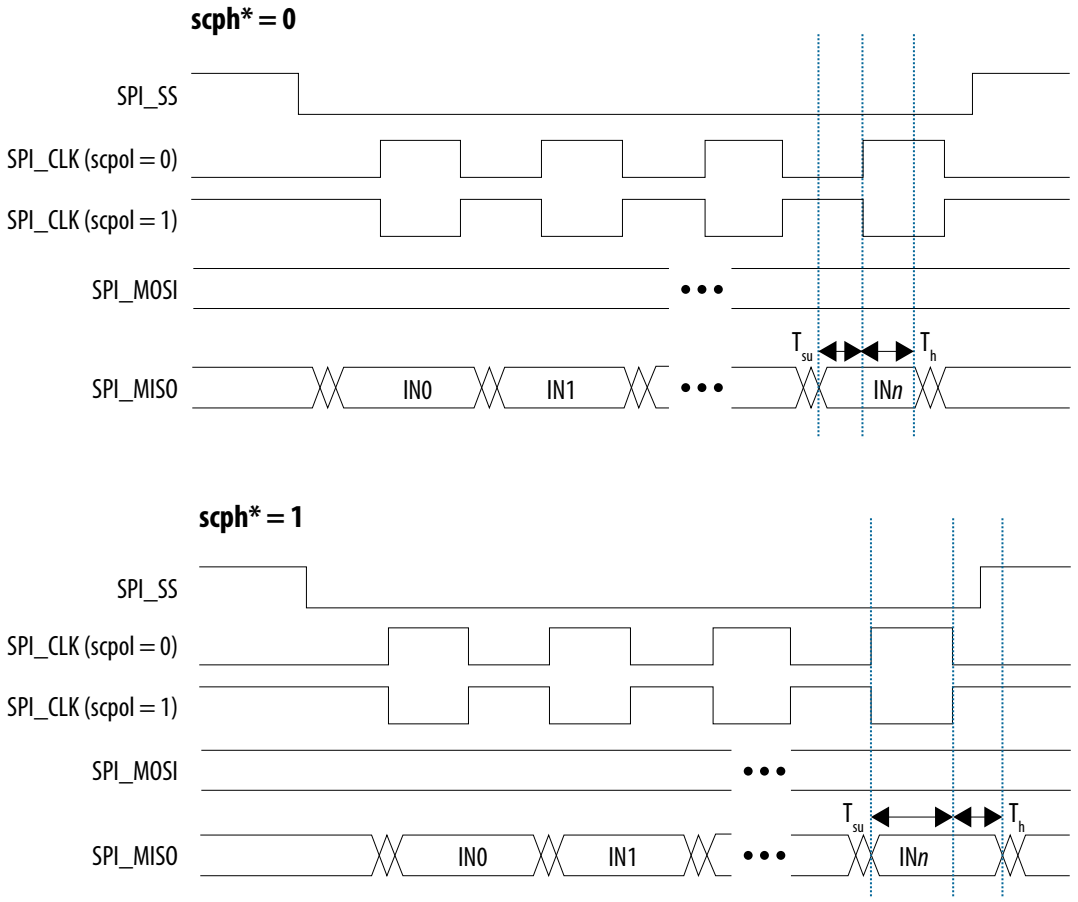
(123) Valid values of `rx_sample_dly` range from 1 to 64 (units are in $T_{spi\_ref\_clk}$ steps)

Figure 8. SPI Master Output Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Figure 9. SPI Master Input Timing Diagram

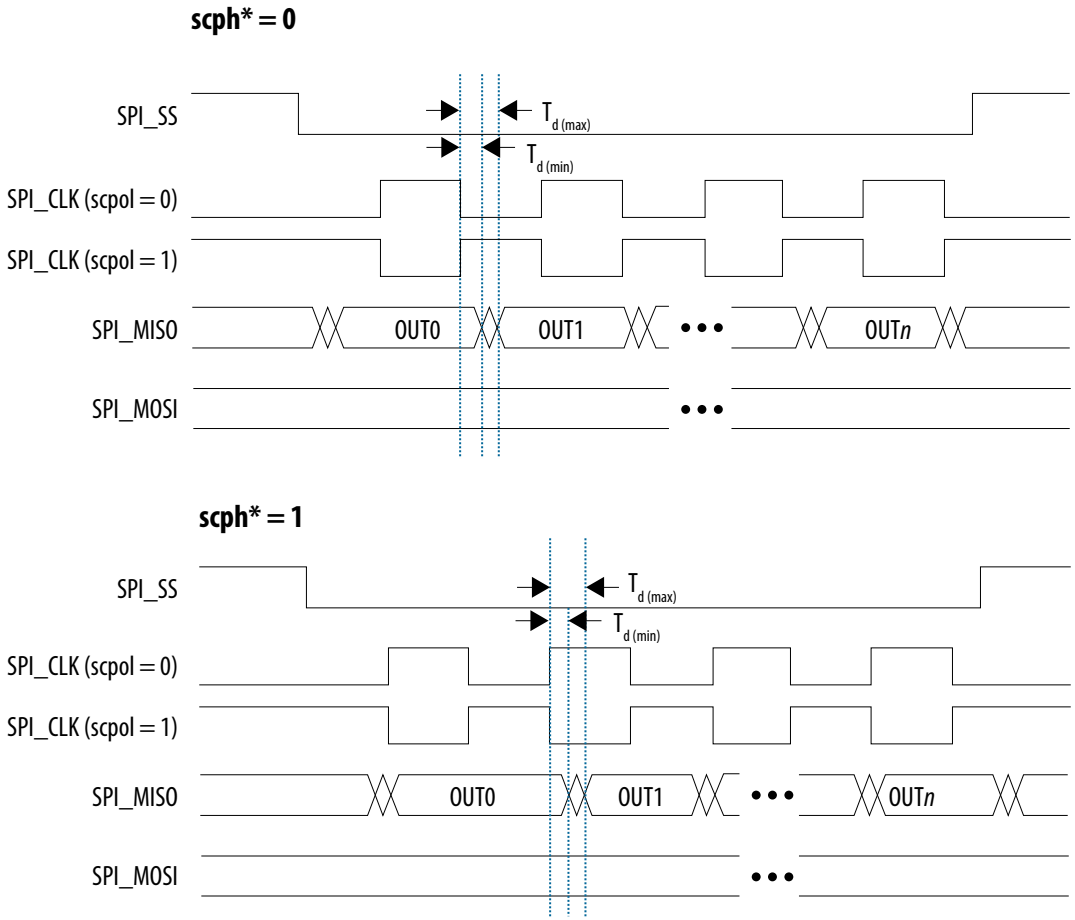


*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Table 74. SPI Slave Timing Requirements for Intel Stratix 10 Devices

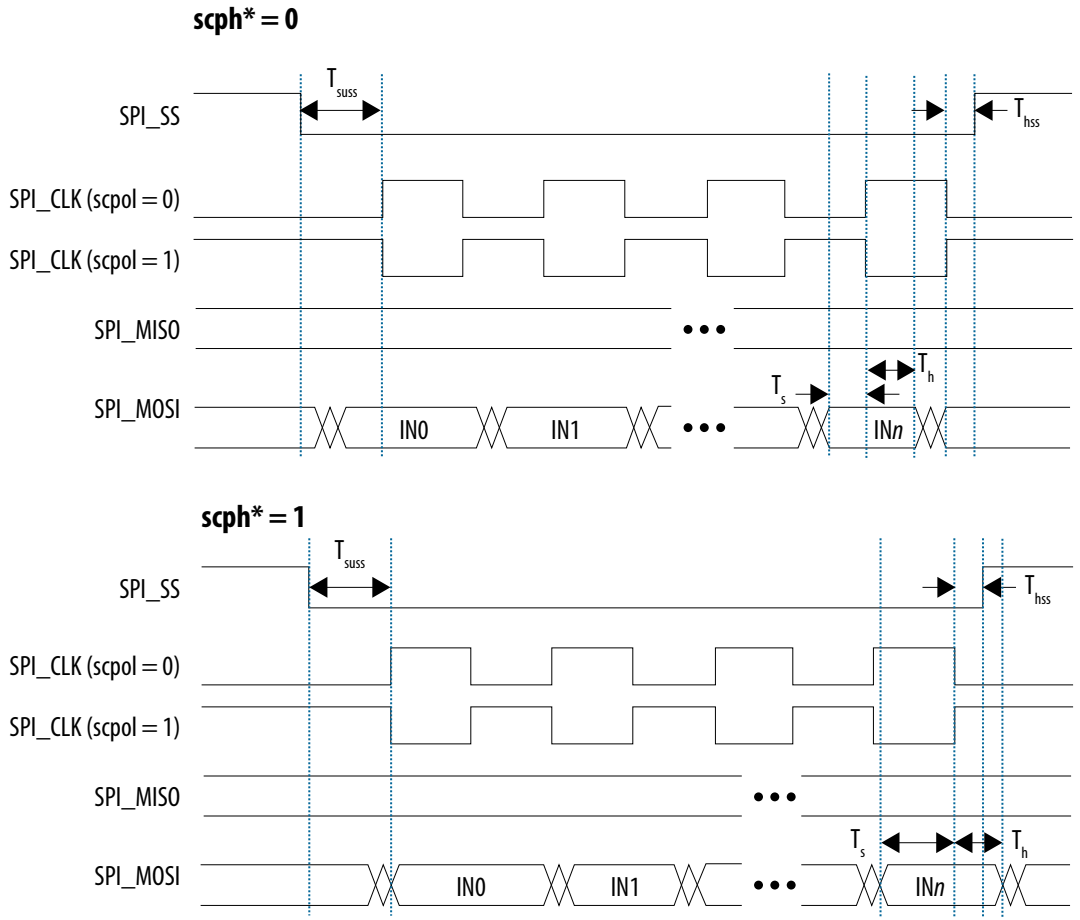
Symbol	Description	Min	Typ	Max	Unit
$T_{spi\_ref\_clk}$	The period of the SPI internal reference clock, sourced from `l4_main_clk`	2.5	—	—	ns
T_{clk}	SPIM_CLK clock period	30	—	—	ns
$T_{dutycycle}$	SPIM_CLK duty cycle	45	50	55	%
T_d	Master-in slave-out (MISO) output skew	$(2 \times T_{spi\_ref\_clk}) + 3$	—	$(3 \times T_{spi\_ref\_clk}) + 11$	ns
T_{su}	Master-out slave-in (MOSI) setup time	4	—	—	ns
T_h	Master-out slave-in (MOSI) hold time	9	—	—	ns
T_{suss}	SPI_SS_N asserted to first SPIM_CLK edge	$T_{spi\_ref\_clk} + 4$	—	—	ns
T_{hss}	Last SPIM_CLK edge to SPI_SS_N deasserted	$T_{spi\_ref\_clk} + 4$	—	—	ns

Figure 10. SPI Slave Output Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Figure 11. SPI Slave Input Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register

Related Information

SPI Controller

For more information about the SPI controller and timing, refer to the *SPI Controller* chapter in the *Intel Stratix 10 Hard Processor System Technical Reference Manual*

HPS SD/MMC Timing Characteristics

Table 75. HPS Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Intel Stratix 10 Devices

These timings apply to SD, MMC, and embedded MMC (eMMC) cards operating at 1.8 V.

Symbol	Description	Min	Typ	Max	Unit
T_{sdmmc_cclk}	SDMMC_CCLK clock period (Identification mode)	2500	—	—	ns
	SDMMC_CCLK clock period (SDR12)	40	—	—	ns
	SDMMC_CCLK clock period (SDR25)	20	—	—	ns
$T_{dutycycle}$	SDMMC_CCLK duty cycle	45	50	55	%
$T_{sdmmc\_cclk\_jitter}$	SDMMC_CCLK output jitter	—	—	2	%
T_{sdmmc_clk}	Internal reference clock before division by 4	5	—	—	ns
T_d	SDMMC_CMD/SDMMC_DATA[7:0] output delay (124)	$T_{sdmmc\_clk} \times$ drvsel/2	—	3 + ($T_{sdmmc\_clk} \times$ drvsel/2)	ns
T_{su}	SDMMC_CMD/SDMMC_DATA[7:0] input setup (125)	6 – ($T_{sdmmc\_clk} \times$ smplsel/2)	—	—	ns
T_h	SDMMC_CMD/SDMMC_DATA[7:0] input hold (125)	0.5 + ($T_{sdmmc\_clk} \times$ smplsel/2)	—	—	ns

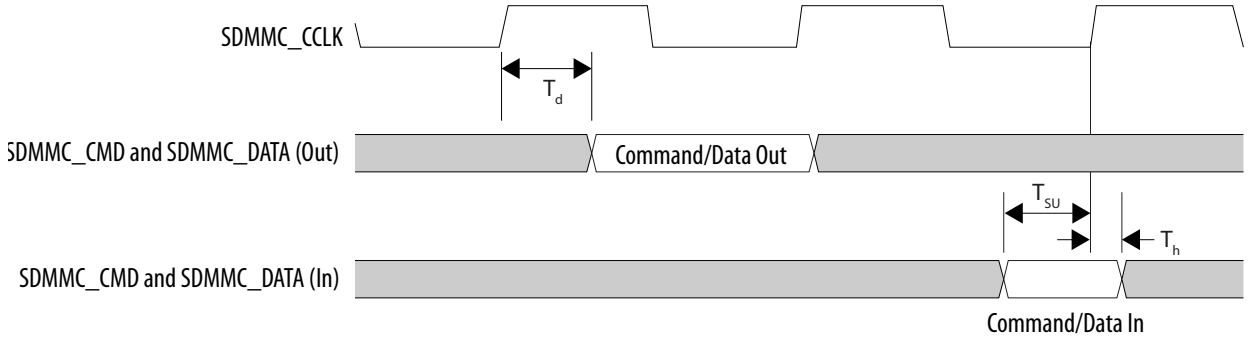
None of the HPS I/Os supports 3 V mode, while SD/MMC cards must operate at 3 V at power on. eMMC devices can operate at 1.8 V at power on.

Note: SD cards power up at 3 V. To support SD, your design must include a level shifter between the SD card and the HPS SD/MMC interface.

(124) When the drvsel bitfield in the sdmmc register is set to 3 (in the system manager) and the reference clock (sdmmc_clk) is 200 MHz for example, the output delay time is 7.5 to 10.5 ns.

(125) When the smplsel bitfield in the sdmmc register is set to 2 (in the system manager) and the reference clock (sdmmc_clk) is 200 MHz for example, the setup time is 1 ns and the hold time is 5.5 ns.

Figure 12. SD/MMC Timing Diagram



Related Information

SD/MMC Controller

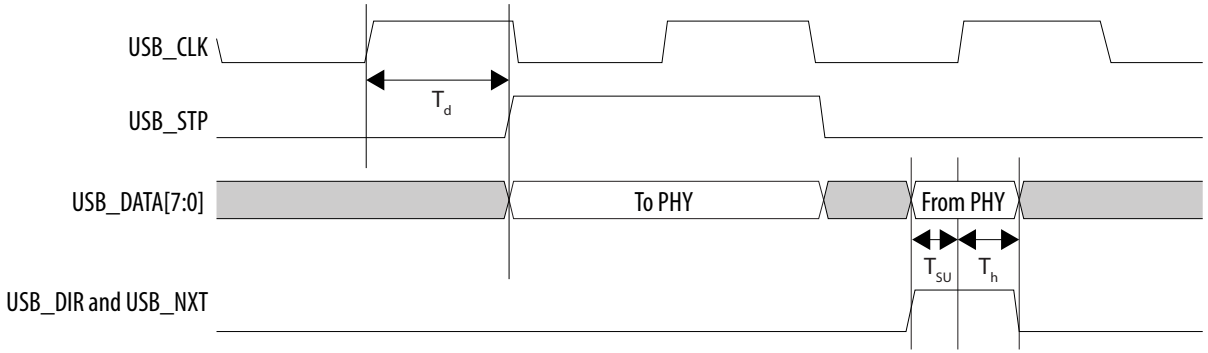
For more information about the SD/MMC controller and timing, refer to the *SD/MMC Controller* chapter in the *Intel Stratix 10 Hard Processor System Technical Reference Manual*

HPS USB UPLI Timing Characteristics

Table 76. HPS USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) Low Pin Interface (ULPI) Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Min	Typ	Max	Unit
T_{usb_clk}	USB_CLK clock period	—	16.667	—	ns
T_d	Clock to USB_STP/USB_DATA[7:0] output delay	2	—	7	ns
T_{su}	Setup time for USB_DIR/USB_NXT/USB_DATA[7:0]	4	—	—	ns
T_h	Hold time for USB_DIR/USB_NXT/USB_DATA[7:0]	1	—	—	ns

Figure 13. USB ULPI Timing Diagram



Note: The USB interface supports single data rate (SDR) timing only.

Related Information

USB 2.0 OTG Controller

For more information about the USB 2.0 OTG controller and timing, refer to the *USB 2.0 OTG Controller* chapter in the *Intel Stratix 10 Hard Processor System Technical Reference Manual*

HPS Ethernet Media Access Controller (EMAC) Timing Characteristics

Table 77. Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	TX_CLK clock period	—	8	—	ns
T_{clk} (100Base-T)	TX_CLK clock period	—	40	—	ns
T_{clk} (10Base-T)	TX_CLK clock period	—	400	—	ns
$T_{dutycycle}$ (1000Base-T)	TX_CLK duty cycle	45	50	55	%
$T_{dutycycle}$(10/100Base-T)	TX_CLK duty cycle	40	50	60	%
T_d (126) (127)	TXD/TX_CTL to TX_CLK output skew	–0.5	—	0.5	ns

Figure 14. RGMII TX and RMII TX Timing Diagram

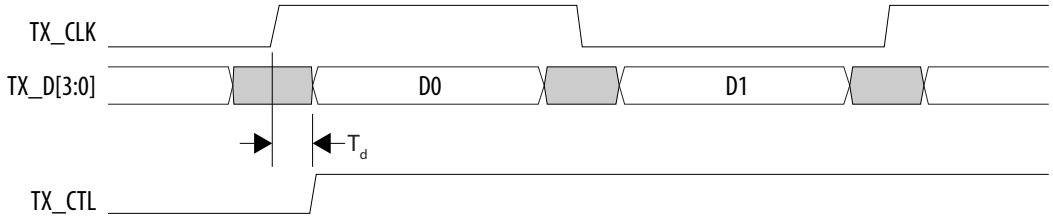


Table 78. RGMII RX Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	RX_CLK clock period	—	8	—	ns
T_{clk} (100Base-T)	RX_CLK clock period	—	40	—	ns

continued...

(126) Rise and fall times depend on the I/O standard, drive strength, and loading. Intel recommends simulating your configuration.

(127) If you connect a PHY that does not implement clock-to-data skew, you can delay TX_CLK by 1.5—2.0 ns with the HPS I/O programmable delay, to meet the PHY's 1-ns data-to-clock skew requirement.

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (10Base-T)	RX_CLK clock period	—	400	—	ns
$T_{dutycycle}$(1000Base-T)	RX_CLK duty cycle	45	50	55	%
$T_{dutycycle}$(10/100Base-T)	RX_CLK duty cycle	40	50	60	%
T_{su}	RX_D/RX_CTL to RX_CLK setup time	1	—	—	ns
T_h (128)	RX_CLK to RX_D/RX_CTL hold time	1	—	—	ns

Figure 15. RGMII RX and RMII RX Timing Diagram

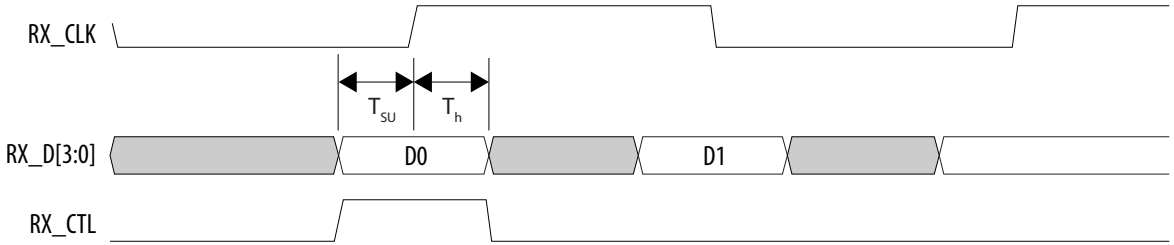


Table 79. Reduced Media Independent Interface (RMII) Clock Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	REF_CLK clock period, sourced by HPS TX_CLK	—	20	—	ns
	REF_CLK clock period, sourced by external clock source	—	20	—	ns
$T_{dutycycle\_int}$	Clock duty cycle, REF_CLK sourced by TX_CLK	35	50	65	%
$T_{dutycycle\_ext}$	Clock duty cycle, REF_CLK sourced by external clock source	35	50	65	%

Table 80. RMII TX Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Min	Typ	Max	Unit
T_d	TX_CLK to TXD/TX_CTL output data delay	2	—	10	ns

(128) If you connect a PHY that does not implement clock-to-data skew, you can meet the HPS EMAC's 1 ns setup time by delaying RX_CLK by 1.5-2 ns, using the HPS I/O programmable delay.

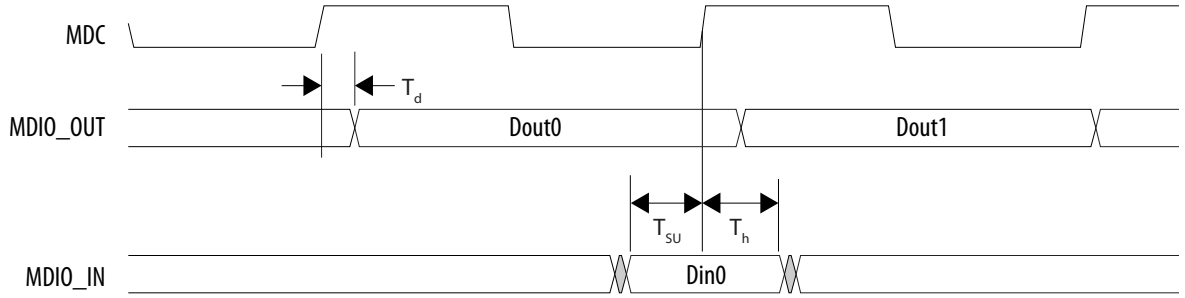
Table 81. RMII RX Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Min	Typ	Max	Unit
T_{su}	RX_D/RX_CTL setup time	2	—	—	ns
T_h	RX_D/RX_CTL hold time	1	—	—	ns

Table 82. Management Data Input/Output (MDIO) Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	MDC clock period	400	—	—	ns
T_d	MDC to MDIO output data delay	10	—	300	ns
T_{su}	Setup time for MDIO data	10	—	—	ns
T_h	Hold time for MDIO data	0	—	—	ns

Figure 16. MDIO Timing Diagram



Related Information

Ethernet Media Access Controller

For more information about the Ethernet MAC and timing, refer to the *Ethernet Media Access Controller* chapter in the *Intel Stratix 10 Hard Processor System Technical Reference Manual*

HPS I²C Timing Characteristics

Table 83. HPS I²C Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T_{clk}	Serial clock (SCL) clock period	10	—	2.5	—	µs
T_{clk_jitter}	I2C clock output jitter	—	2	—	2	%
T_{HIGH} (129)	SCL high period	4 (130)	—	0.6 (131)	—	µs
T_{LOW} (132)	SCL low period	4.7 (133)	—	1.3 (134)	—	µs
$T_{SU;DAT}$	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1	—	µs
$T_{HD;DAT}$ (135)	Hold time for SCL to SDA data	0	3.15	0	0.6	µs
$T_{VD;DAT}$ and $T_{VD;ACK}$ (136)	SCL to SDA output data delay	—	3.45 (137)	—	0.9 (138)	µs

continued...

(129) You can adjust T_{high} using the `ic_ss_scl_hcnt` or `ic_fs_scl_hcnt` register.

(130) The recommended minimum setting for `ic_ss_scl_hcnt` is 440.

(131) The recommended minimum setting for `ic_fs_scl_hcnt` is 71.

(132) You can adjust T_{low} using the `ic_ss_scl_lcnt` or `ic_fs_scl_lcnt` register.

(133) The recommended minimum setting for `ic_ss_scl_lcnt` is 500.

(134) The recommended minimum setting for `ic_fs_scl_lcnt` is 141.

(135) $T_{HD;DAT}$ is affected by the rise and fall time.

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
$T_{SU;STA}$	Setup time for a repeated start condition	4.7	—	0.6	—	µs
$T_{HD;STA}$	Hold time for a repeated start condition	4	—	0.6	—	µs
$T_{SU;STO}$	Setup time for a stop condition	4	—	0.6	—	µs
T_{BUF}	SDA high pulse duration between STOP and START	4.7	—	1.3	—	µs
$T_{scl:r}$ (139)	SCL rise time	—	1000	20	300	ns
$T_{scl:f}$ (139)	SCL fall time	—	300	6.54	300	ns
$T_{sda:r}$ (139)	SDA rise time	—	1000	20	300	ns
$T_{sda:f}$ (139)	SDA fall time	—	300	6.54	300	ns

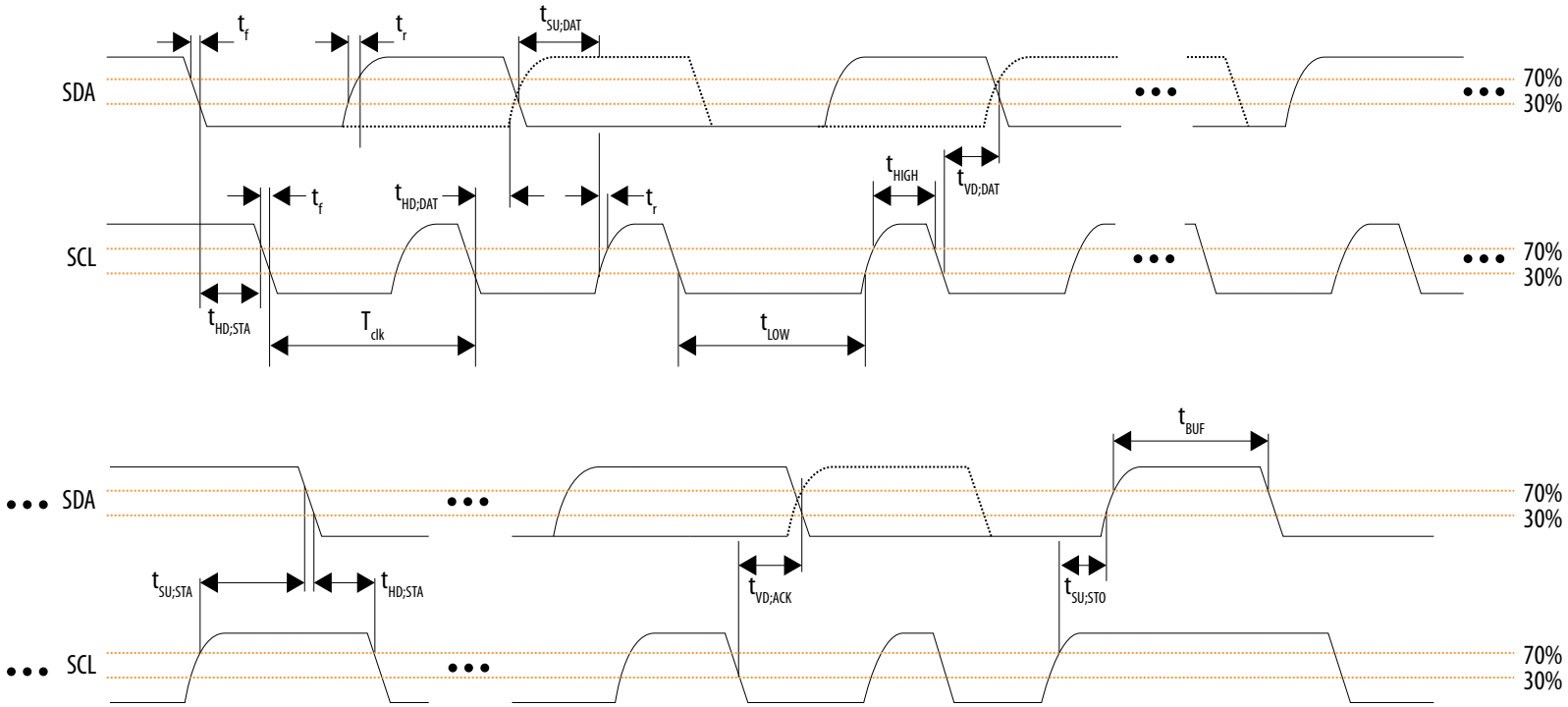
(136) $T_{VD;DAT}$ and $T_{VD;ACK}$ are affected by the rise and fall time, as well as the SDA hold time (set by adjusting the `ic_sda_hold` register).

(137) Use maximum SDA_HOLD = 240 to be within the specification.

(138) Use maximum SDA_HOLD = 60 to be within the specification.

(139) Rise and fall time parameters vary depending on external factors such as the characteristics of the IO driver, pull-up resistor value, and total capacitance on the transmission line.

Figure 17. I²C Timing Diagram



Related Information

I²C Controller

For more information about the I²C controller and timing, refer to the *I²C Controller* chapter in the *Intel Stratix 10 Hard Processor System Technical Reference Manual*

HPS NAND Timing Characteristics

Table 84. HPS NAND ONFI 1.0 Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Min	Max	Unit
T_{WP} (140)	Write enable pulse width	10	—	ns
T_{WH} (140)	Write enable hold time	7	—	ns
T_{RP} (140)	Read enable pulse width	10	—	ns
T_{REH} (140)	Read enable hold time	7	—	ns
T_{CLS} (140)	Command latch enable to write enable setup time	10	—	ns
T_{CLH} (140)	Command latch enable to write enable hold time	5	—	ns
T_{CS} (140)	Chip enable to write enable setup time	15	—	ns
T_{CH} (140)	Chip enable to write enable hold time	5	—	ns
T_{ALS} (140)	Address latch enable to write enable setup time	10	—	ns
T_{ALH} (140)	Address latch enable to write enable hold time	5	—	ns
T_{DS} (140)	Data to write enable setup time	7	—	ns
T_{DH} (140)	Data to write enable hold time	5	—	ns
T_{WB} (140)	Write enable high to R/B low	—	200	ns
T_{CEA}	Chip enable to data access time	—	100	ns
T_{REA}	Read enable to data access time	—	40	ns
T_{RHZ}	Read enable to data high impedance	—	200	ns
T_{RR}	Ready to read enable low	20	—	ns

(140) This timing is software programmable. Refer to the *NAND Flash Controller* chapter in the *Stratix 10 Hard Processor System Technical Reference Manual* for more information about software-programmable timing in the NAND flash controller.

Figure 18. NAND Command Latch Timing Diagram

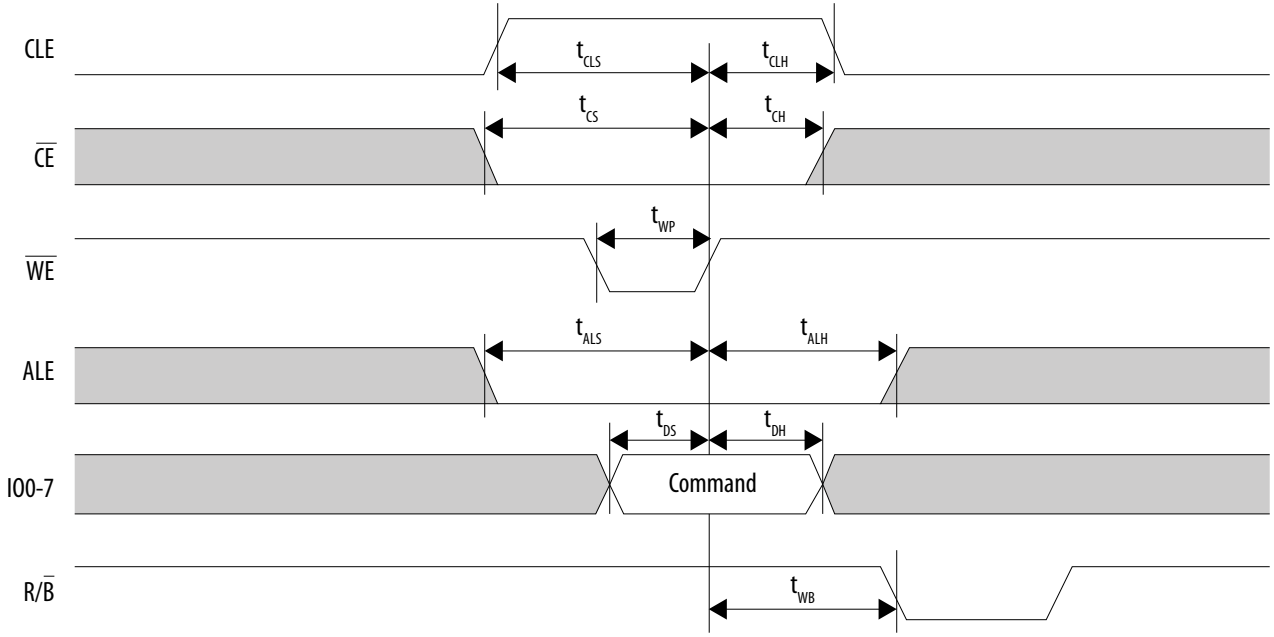


Figure 19. NAND Address Latch Timing Diagram

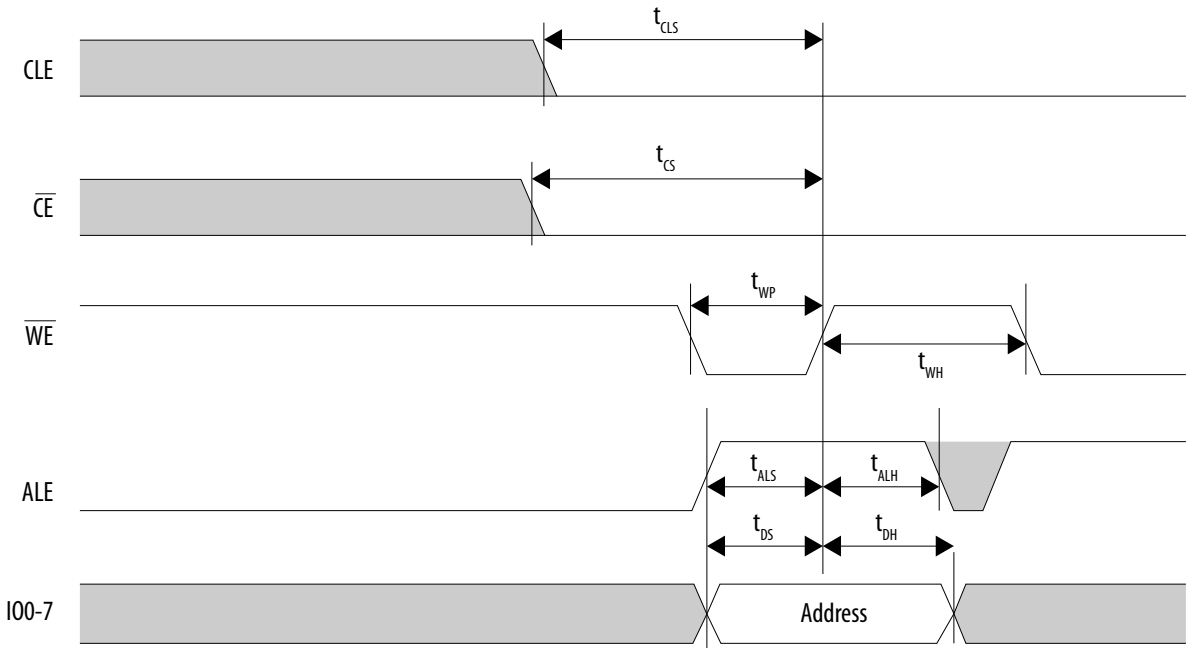


Figure 20. NAND Data Output Cycle Timing Diagram

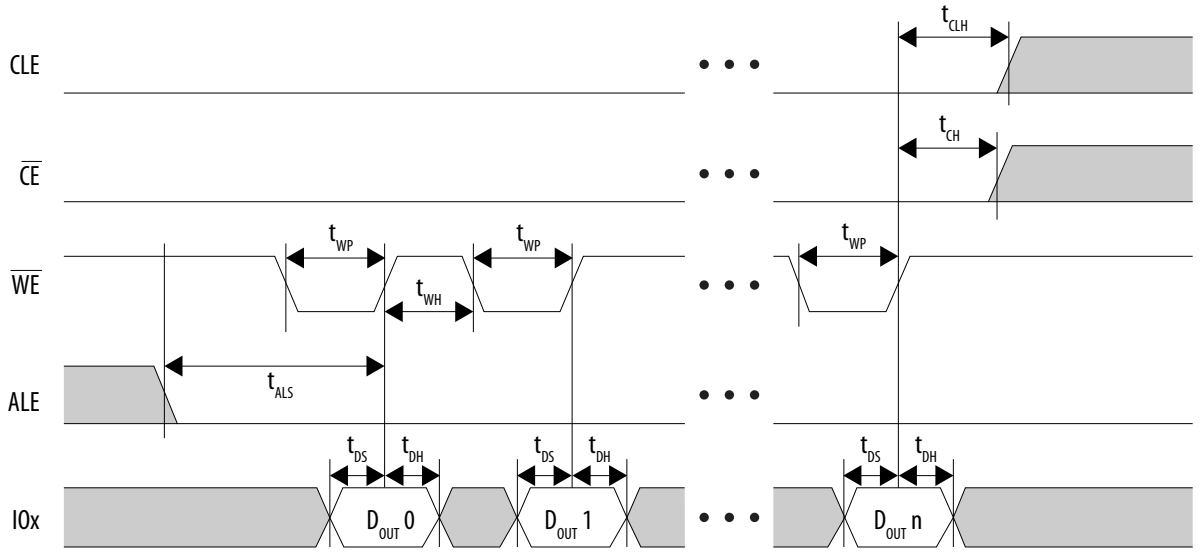


Figure 21. NAND Data Input Cycle Timing Diagram

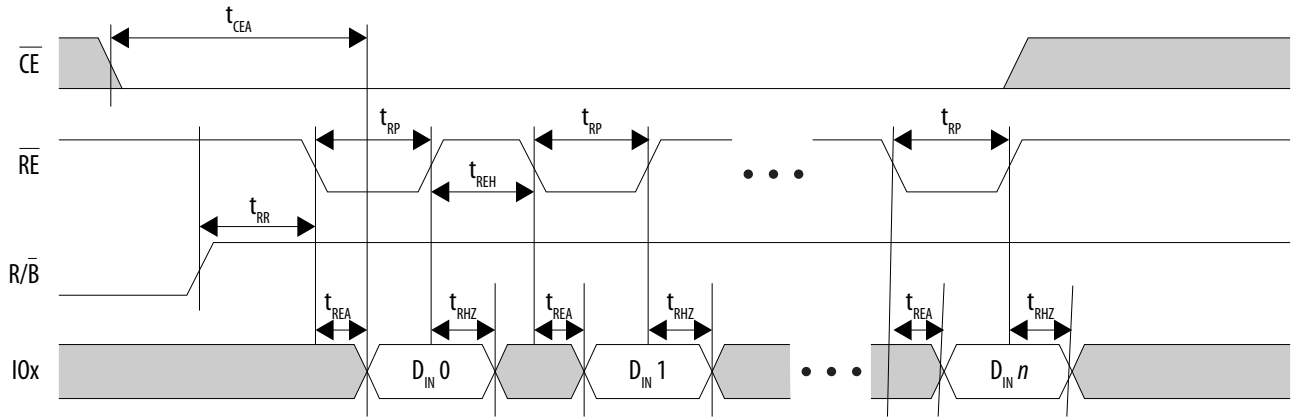


Figure 22. NAND Data Input Timing Diagram for Extended Data Output (EDO) Cycle

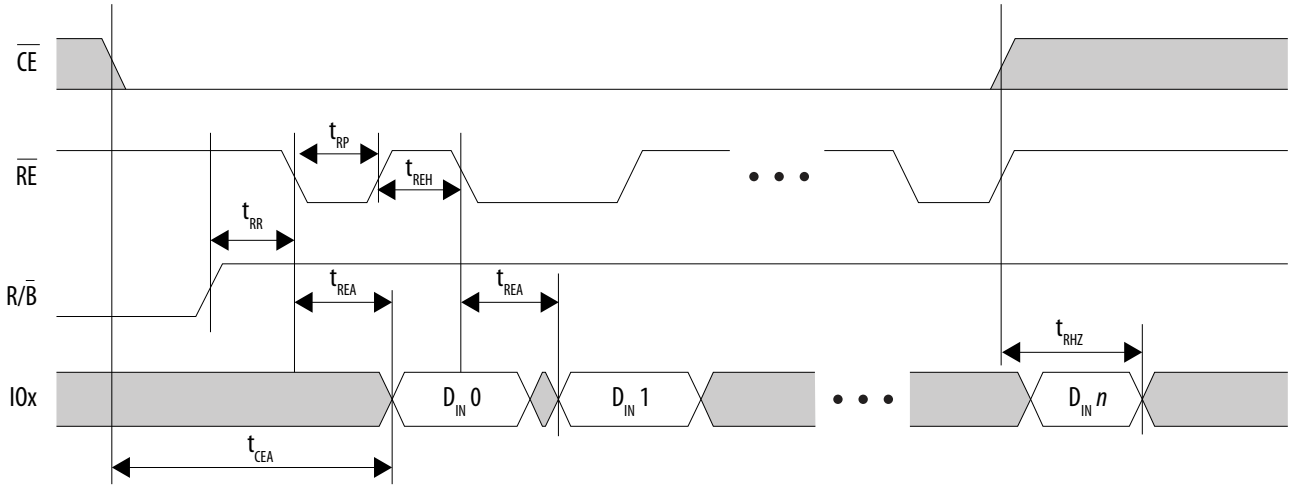


Figure 23. NAND Read Status Timing Diagram

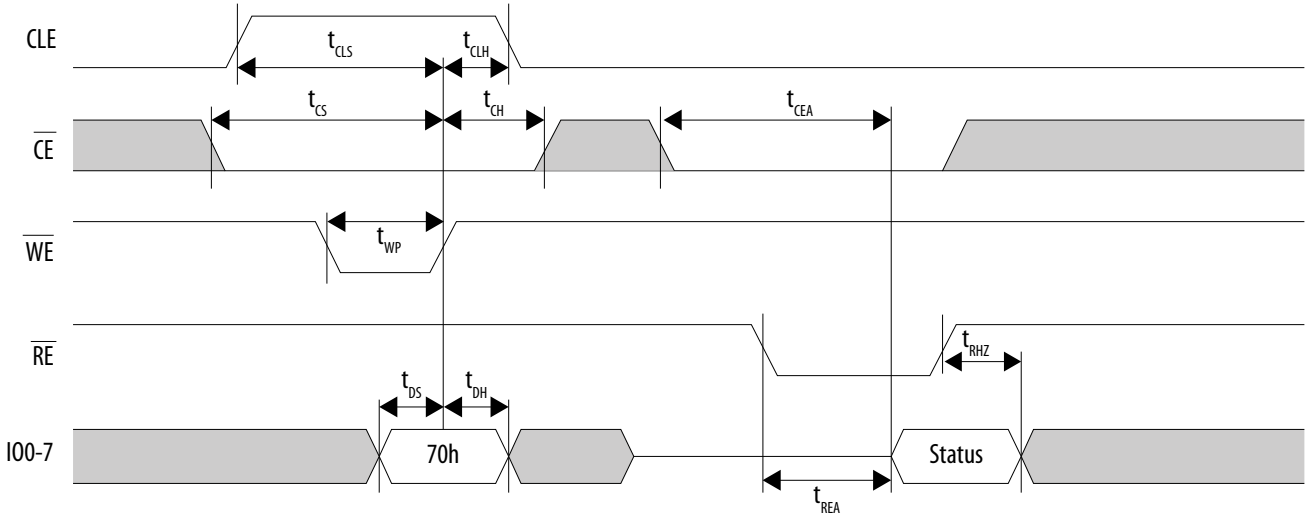
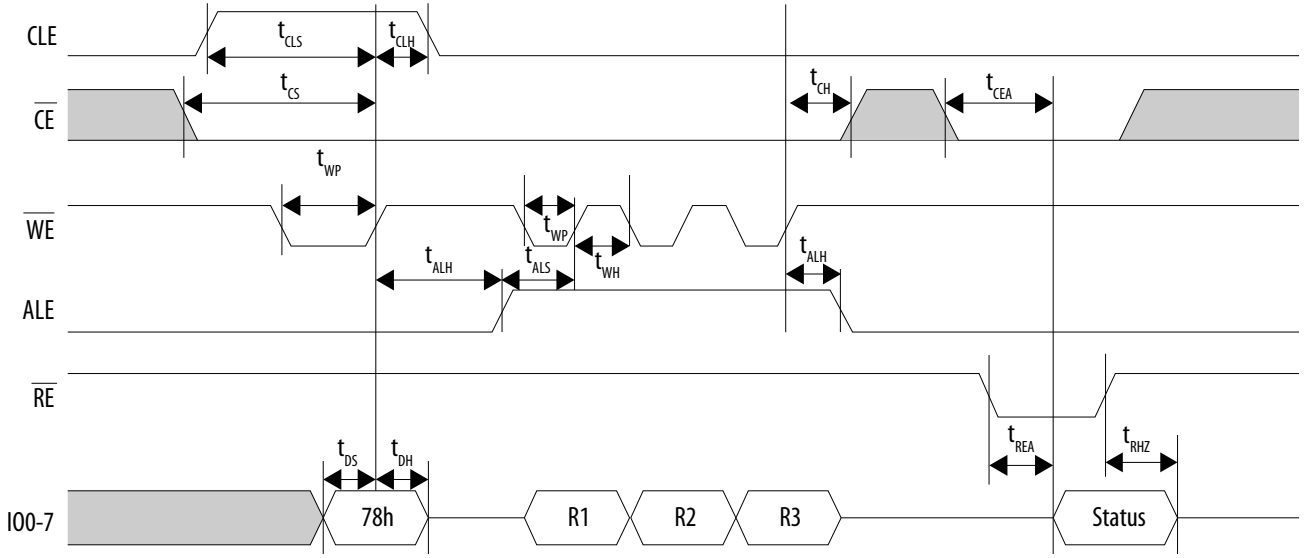


Figure 24. NAND Read Status Enhanced Timing Diagram



Related Information

NAND Flash Controller

Refer to the *NAND Flash Controller* chapter in the *Intel Stratix 10 Hard Processor System Technical Reference Manual* for more information about the NAND flash controller and timing, particularly software-programmable timing.

HPS Trace Timing Characteristics

Table 85. Trace Timing Requirements for Intel Stratix 10 Devices

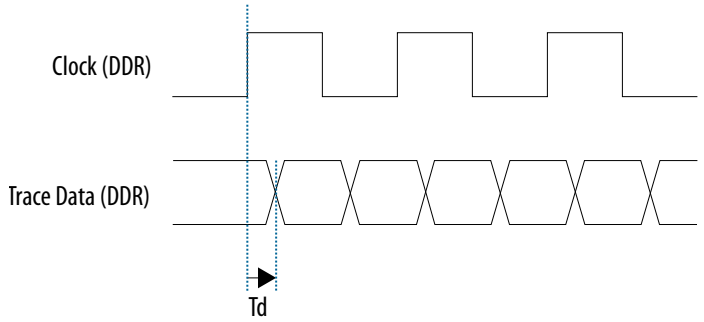
To increase the trace bandwidth, Intel recommends routing the trace interface to the FPGA in the HPS Platform Designer (Standard) component. The FPGA trace interface offers a 64-bit single data rate path that can be converted to double data rate to minimize FPGA I/O usage.

Depending on the trace module that you connect to the HPS trace interface, you may need to include board termination to achieve the maximum sampling speed possible. Refer to your trace module datasheet for termination recommendations.

Most trace modules implement programmable clock and data skew, to improve trace data timing margins. Alternatively, you can change the clock-to-data timing relationship with the HPS programmable I/O delay.

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	Trace clock period	6.667	—	—	ns
T_{clk_jitter}	Trace clock output jitter	—	—	2	%
$T_{dutycycle}$	Trace clock maximum duty cycle	45	50	55	%
T_d	T_{clk} to D0–D15 output data delay	0	—	1.8	ns

Figure 25. Trace Timing Diagram



HPS GPIO Interface

The general-purpose I/O (GPIO) interface has debounce circuitry included to remove signal glitches. The debounce clock frequency ranges from 125 Hz to 32 kHz. The minimum pulse width is 1 debounce clock cycle and the minimum detectable GPIO pulse width is 62.5 µs (at 32 kHz). Any pulses shorter than 2 debounce clock cycles are filtered by the GPIO peripheral.

If the external signal is driven into the GPIO for less than one clock cycle, the external signal is filtered. If the external signal is between one and two clock cycles, the external signal may or may not be filtered depending on the phase of the signal. If the external signal is more than two clock cycles, the external signal is not filtered.

Related Information

General-Purpose I/O Interface

For more information about the GPIO interface and timing, refer to the *General-Purpose I/O Interface* chapter in the *Intel Stratix 10 Hard Processor System Technical Reference Manual*

HPS JTAG Timing Characteristics

Table 86. HPS JTAG Timing Requirements for Intel Stratix 10 Devices

Symbol	Description	Min	Typ	Max	Unit
t_{JCP}	TCK clock period	41.66	—	—	ns
t_{JCH}	TCK clock high time	20	—	—	ns
t_{JCL}	TCK clock low time	20	—	—	ns
t_{JPSU} (TDI)	TDI JTAG port setup time	5	—	—	ns
t_{JPSU} (TMS)	TMS JTAG port setup time	5	—	—	ns
t_{JPH}	JTAG port hold time	0	—	—	ns
t_{JPCO}	JTAG port clock to output	0	—	8	ns
t_{JPZX}	JTAG port high impedance to valid output	—	—	10	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	—	10	ns

HPS Programmable I/O Timing Characteristics

Table 87. HPS Programmable I/O Delay for Intel Stratix 10 Device

Programmable Delay	Description	Min	Typ	Max	Unit
0, 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30	No delay enabled	—	0	—	ps
1	Delay Step 1	—	120	—	ps
3	Delay Step 2	—	240	—	ps
5	Delay Step 3	—	360	—	ps
7	Delay Step 4	—	480	—	ps
9	Delay Step 5	—	600	—	ps
11	Delay Step 6	—	720	—	ps
13	Delay Step 7	—	840	—	ps
15	Delay Step 8	—	960	—	ps
17	Delay Step 9	—	1080	—	ps
19	Delay Step 10	—	1200	—	ps
21	Delay Step 11	—	1320	—	ps
23	Delay Step 12	—	1440	—	ps
25	Delay Step 13	—	1560	—	ps
27	Delay Step 14	—	1680	—	ps
29	Delay Step 15	—	1800	—	ps
31	Delay Step 16	—	1920	—	ps

You can program the number of delay steps by adjusting the I/O Delay register (`io0_delay` through `io47_delay` for I/Os 0 through 47).

Configuration Specifications

General Configuration Timing Specifications

Table 88. General Configuration Timing Specifications for Intel Stratix 10 Devices

Symbol	Description		Requirement			Unit
			Min	Typ	Max	
$t_{CF12ST1}$ (141)	nCONFIG high to nSTATUS high		—	10	—	ms
$t_{CF02ST0}$	nCONFIG low to nSTATUS low	Device is empty or not yet configured	—	10	100	ms
		Device is configured	—	200	400	ms
t_{ST0}	nSTATUS low pulse during configuration error		0.5	—	1.5	ms
t_{CD2UM} (142)	CONF_DONE high to user mode		—	—	2	ms

POR Specifications

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.

Table 89. POR Delay Specification for Intel Stratix 10 Devices

POR Delay	Minimum	Maximum	Unit
AS (Normal mode), AVST ×8, AVST ×16, AVST ×32, SD/MMC	12	20	ms
AS (Fast mode)	2	6.5	ms

(141) The maximum time does not exceed 2× of the typical value.

(142) This specification is the initialization time that indicates the time from CONF_DONE signal goes high to INIT_DONE signal goes high.

External Configuration Clock Source Requirements

Table 90. External Configuration Clock Source (OSC_CLK_1) Clock Input Requirements

Description	External Clock Source	Min	Typ	Max	Unit
Clock input frequency (143)	Powered by V_{CCIO_SDM}		25/100/125		MHz
Clock input jitter tolerance		—	—	2	%
Clock input duty cycle		45	50	55	%

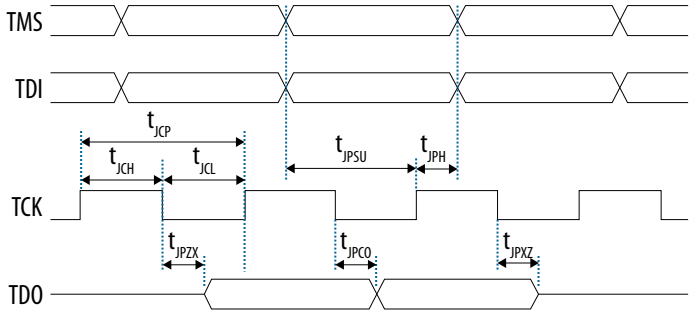
JTAG Configuration Timing

Table 91. JTAG Timing Parameters and Values for Intel Stratix 10 Devices

Symbol	Description	Requirement		Unit
		Minimum	Maximum	
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	7	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14	ns

(143) The acceptable clock frequencies are 25 MHz, 100 MHz, and 125 MHz only. You must match the external configuration clock frequency on the OSC_CLK_1 pin to the configuration clock source assignment in the Intel Quartus Prime software. Other frequencies in the range are not supported.

Figure 26. JTAG Timing Diagram



AS Configuration Timing

Table 92. AS Timing Parameters for Intel Stratix 10 Devices

Intel recommends performing trace length matching for nCSO and AS_DATA pins to AS_CLK to minimize the skew. The maximum tolerance for skew between nCSO and AS_CLK is recommended to be less than 200 ps. The tolerance for skew between AS_CLK to AS_DATA must be within 0 ps – 400 ps.

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{clk}	AS_CLK clock period	—	7.52	—	ns
$T_{dutycycle}$	AS_CLK duty cycle	45	50	55	%
T_{dcsfrs}	AS_nCSO[3:0] asserted to first AS_CLK edge	4.21 (144)	—	7.50 (144)	ns
T_{dcslst}	Last AS_CLK edge to AS_nCSO[3:0] deasserted	5.18 (144)	—	8 (144)	ns
T_{do}	AS_DATA0 output delay	–1.5	—	1.31	ns
T_{ext_delay} (145)	Total external propagation delay on AS signals	0	—	15	ns

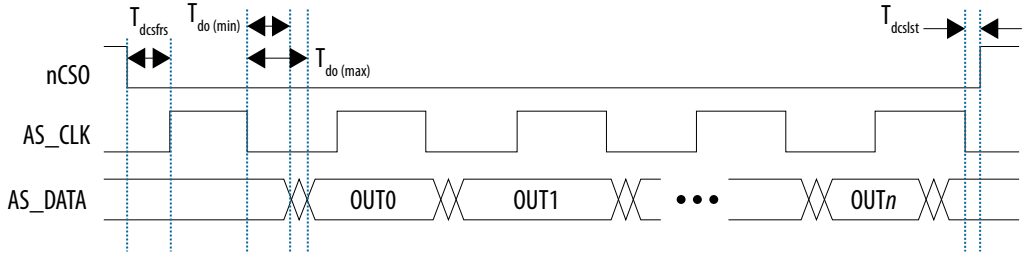
continued...

(144) AS operating at maximum clock frequency = 133 MHz. The delay is larger when operating at AS clock frequency lower than 133 MHz.

(145) $T_{ext\_delay} = T_{bd\_clk} + T_{co} + T_{bd\_data} + T_{add}$
T_{bd_clk}: Propagation delay for AS_CLK between FPGA and flash device.

Symbol	Description		Minimum	Typical	Maximum	Unit
T_{ext_skew}	Skew delay for AS_DATA signals for the specific AS_CLK frequency	133 MHz	—	—	4.61	ns
		125 MHz	—	—	5.09	ns
		115 MHz	—	—	5.79	ns
		108 MHz	—	—	6.35	ns
		100 MHz	—	—	7.09	ns
		80 MHz	—	—	9.59	ns
		77 MHz	—	—	7.92	ns
		58 MHz	—	—	10.02	ns
		50 MHz	—	—	12.09	ns
		25 MHz	—	—	22.09	ns
T_{dcsb2b}	Minimum delay of slave select deassertion between two back-to-back transfers		1	—	—	AS_CLK

Figure 27. AS Configuration Serial Output Timing Diagram

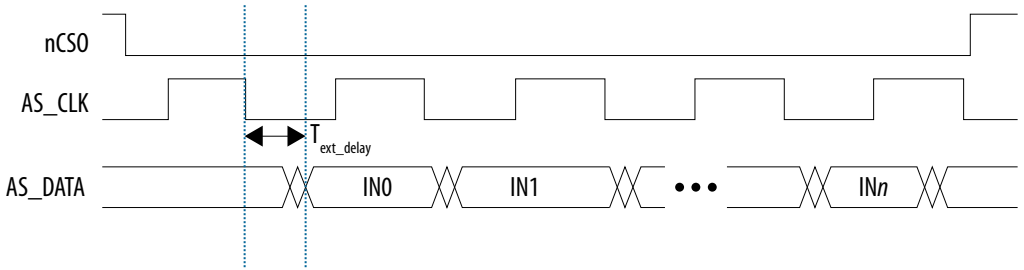


T_{co}: Output hold time and clock low to output valid of flash device. This delay must be used to ensure T_{ext_delay} is within the minimum and maximum specification values.

T_{bd_data}: Propagation delay for AS_DATA bus between FPGA and flash device.

T_{add}: Propagation delay for active/passive components on AS_DATA interfaces.

Figure 28. AS Configuration Serial Input Timing Diagram



Related Information

AS_CLK, Intel Stratix 10 Configuration User Guide
Provides the supported configuration clock source and AS_CLK frequencies in Intel Stratix 10 devices.

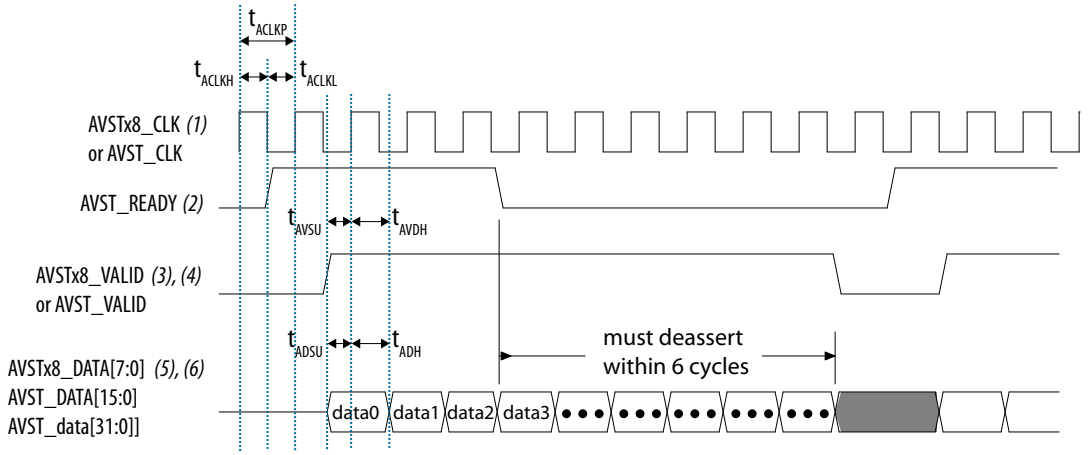
Avalon-ST Configuration Timing

Table 93. Avalon-ST Timing Parameters for ×8, ×16, and ×32 Configurations in Intel Stratix 10 Devices

Symbol	Description	Minimum	Maximum	Unit
t_{ACLKH}	AVST_CLK high time	3.6	—	ns
t_{ACLKL}	AVST_CLK low time	3.6	—	ns
t_{ACLKP}	AVST_CLK period	8	—	ns
t_{ADSU} (146)	AVST_DATA setup time before rising edge of AVST_CLK	5.5	—	ns
t_{ADH} (146)	AVST_DATA hold time after rising edge of AVST_CLK	0	—	ns
t_{AVSU}	AVST_VALID setup time before rising edge of AVST_CLK	5.5	—	ns
t_{AVDH}	AVST_VALID hold time after rising edge of AVST_CLK	0	—	ns

(146) Data sampled by the FPGA (sink) at the next rising clock edge.

Figure 29. Avalon-ST Configuration Timing Diagram



Notes:

1. For Avalon-ST x16 and x32, this signal is AVST_CLK. These clocks must be running throughout the configuration (until CONF_DONE goes high).
2. AVST_READY is valid only when nSTATUS is high. AVST_READY is an asynchronous signal to AVSTx8_CLK/AVST_CLK.
3. For Avalon-ST x16 and x32, this signal is AVST_VALID.
4. The waveforms shows the interface signals with a host which uses ready latency =2. The AVSTx8_VALID signal is delayed from AVST_READY signal by 2 clock cycles.
5. For Avalon-ST x16 and x32, this signal is AVST_DATA[15:0] and AVST_DATA[31:0] respectively.
6. Host may send up to 6 more data after AVST_READY has de-asserted.

SD/MMC Configuration Timing

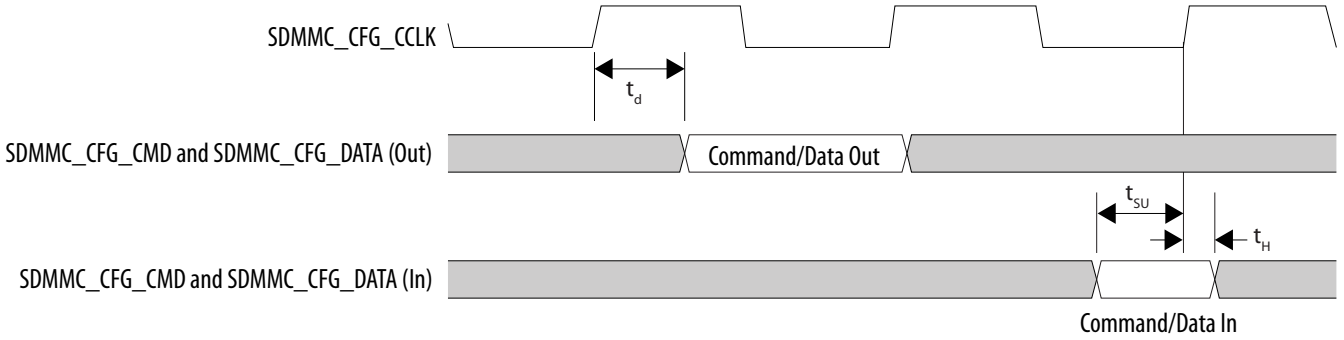
Table 94. SD/MMC Timing Parameters for Intel Stratix 10 Devices

For SD or MMC cards, a level shifter/translator is required to shift down the voltage from 3.0 V to 1.8 V when interfacing the SD/MMC card I/Os with FPGA SDM I/O.

The SD/MMC configuration scheme will be available in a future release of the Intel Quartus Prime software.

Symbol	Description	Minimum	Typical	Maximum	Unit
t_{SDCLKP}	SDMMC_CFG_CCLK clock period (Identification mode)	—	2,500	—	ns
	SDMMC_CFG_CCLK clock period (Standard SD mode)	—	40	—	ns
	SDMMC_CFG_CCLK clock period (High-speed SD mode)	—	20	—	ns
$t_{DUTYCYCLE}$	SDMMC_CFG_CCLK duty cycle	45	50	55	%
t_d	SDMMC_CFG_CMD/SDMMC_CFG_DATA output delay	7.3	—	10.1	ns
t_{SU}	SDMMC_CFG_CMD/SDMMC_CFG_DATA input setup	5	—	—	ns
t_H	SDMMC_CFG_CMD/SDMMC_CFG_DATA input hold	1.5	—	—	ns

Figure 30. SD/MMC Timing Diagram



Configuration Bit Stream Sizes

Table 95. Configuration Bit Stream Sizes for Intel Stratix 10 Devices

This table shows the estimated configuration bit stream sizes of the EPCQ-L serial configuration device or external flash size before design compilation. The sizes are for compressed bit stream. The actual sizes may vary based on your design. The actual sizes may be equal or smaller than the bit stream sizes in this table.

Variant	Product Line	Compressed Configuration Bit Stream Size (Mbits)	IOCSR Bit Stream Size (Mbits)
Intel Stratix 10 GX, SX, TX, and MX	GX 400, GX 650, SX 400, SX 650	100	0.140
	GX 850, GX 1100, SX 850, SX 1100, MX 1100	180	0.200
	GX 1650, GX 2100, SX 1650, SX 2100, TX 1650, TX 2100, MX 1650, MX 2100	310	0.297
	GX 2500, GX 2800, SX 2500, SX 2800, TX 2500, TX 2800	452	0.433
	GX 4500, GX 5500, SX 4500, SX 5500	580	0.567

Maximum Configuration Time Estimation

Hyper Initialization is an option that can be enabled or disabled through the setting in the Intel Quartus Prime software to initialize or reset the Intel Hyperflex™ registers to a known state at device configuration.

The maximum configuration time is estimated when the device starts configuration until CONF_DONE is asserted to high.

The maximum configuration time does not include the nCONFIG to nSTATUS time from the *General Configuration Timing Specifications for Intel Stratix 10 Devices* table.

Table 96. Maximum Configuration Time Estimation for Intel Stratix 10 Devices (JTAG and Avalon-ST)

Variant	Product Line	Maximum Configuration Time (ms) [Hyper Initialization Off/Hyper Initialization On]							
		JTAG		AVST ×8 (147)		AVST ×16 (147)		AVST ×32 (147)	
		170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)
Intel Stratix 10 GX, SX, TX, and MX	GX 400, GX 650, SX 400, SX 650	6,000/6,200	6,000/6,200	274/334	182/222	154/216	102/144	120/184	80/122
	GX 850, GX 1100, SX 850, SX 1100, MX 1100	10,600/11,200	10,600/11,200	456/1,200	304/378	246/358	164/238	190/300	126/200
	GX 1650, GX 2100, SX 1650, SX 2100, TX 1650, TX 2100, MX 1650, MX 2100	18,000/19,000	18,000/19,000	754/852	502/568	394/496	262/330	214/316	142/210
	GX 2500, GX 2800, SX 2500, SX 2800, TX 2500, TX 2800	26,600/28,000	26,600/28,000	1,102/1,240	734/826	568/708	378/472	300/442	200/294
	GX 4500, GX 5500, SX 4500, SX 5500	35,200/37,400	35,200/37,400	1,446/1,662	964/1,108	742/960	494/640	388/606	258/404

(147) The maximum configuration time does not include the time incurred from external storage and control logic, and transceiver calibration time.

Table 97. Maximum Configuration Time Estimation for Intel Stratix 10 Devices (AS and SD/MMC)

Variant	Product Line	Maximum Configuration Time (ms) [Hyper Initialization Off/Hyper Initialization On]					
		AS ×1		AS ×4		SD/MMC	
		170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)
Intel Stratix 10 GX, SX, TX, and MX	GX 400, GX 650, SX 400, SX 650	2,268/2,520	1,512/1,680	568/630	378/420	732/792	488/528
	GX 850, GX 1100, SX 850, SX 1100, MX 1100	3,600/4,044	2,400/2,696	900/1,012	600/674	1,194/1,306	796/870
	GX 1650, GX 2100, SX 1650, SX 2100, TX 1650, TX 2100, MX 1650, MX 2100	5,724/6,132	3,816/4,088	1,432/1,534	954/1,022	1,932/2,034	1,288/1,356
	GX 2500, GX 2800, SX 2500, SX 2800, TX 2500, TX 2800	8,232/8,796	5,488/5,864	2,058/2,200	1,372/1,466	2,806/2,944	1,870/1,962
	GX 4500, GX 5500, SX 4500, SX 5500	10,704/11,592	7,136/7,728	2,676/2,898	1,784/1,932	3,600/3,900	2,400/2,600

I/O Timing

I/O timing data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the timing analysis. You may generate the I/O timing report manually using the Timing Analyzer or using the automated script.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

AN 775: I/O Timing Information Generation Guidelines
Provides the techniques to generate I/O timing information using the Intel Quartus Prime software.

Programmable IOE delay

Table 98. Programmable IOE Delay for Intel Stratix 10 Devices

For the exact values for each setting, use the latest version of the Intel Quartus Prime software. The values in the table show the delay of programmable IOE delay chain with maximum offset settings after excluding the intrinsic delay (delay at minimum offset settings).

Programmable IOE delay settings are only applicable for I/O buffers and do not apply for any other delay elements in the PHY Lite for Parallel Interfaces Intel Stratix 10 FPGA IP core.

Parameter [148]	Maximum Offset	Minimum Offset [149]	Fast Model	Slow Model				Unit
			Industrial/ Extended	–E2V, –I1V	–E2V, –I2V	–E3V	–I3V	
Input Delay Chain (INPUT_DELAY_CHAIN)	63	0	1.5725	2.306	2.3485	2.6525	2.6505	ns
Output Delay Chain (OUTPUT_DELAY_CHAIN)	15	0	0.386	0.522	0.56	0.631	0.631	ns

Glossary

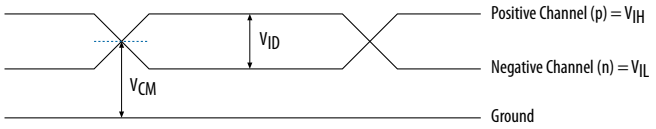
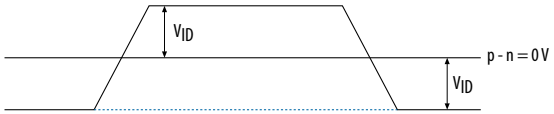
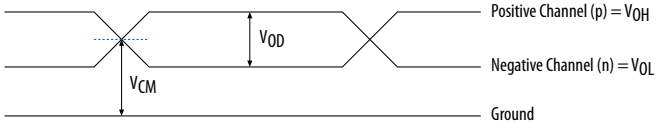
Table 99. Glossary

Term	Definition
Differential I/O Standards	Receiver Input Waveforms

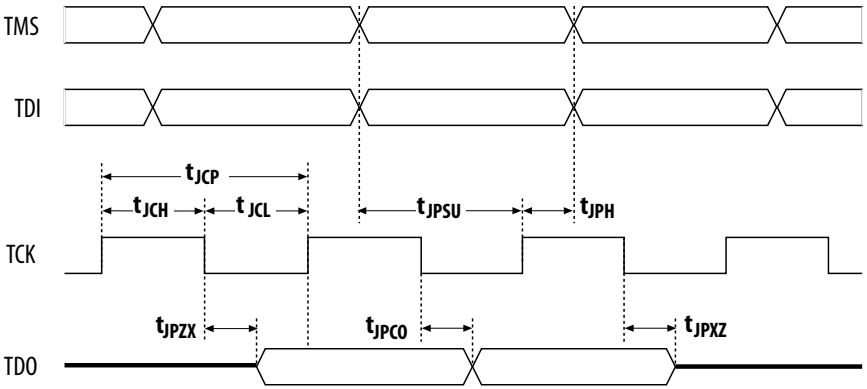
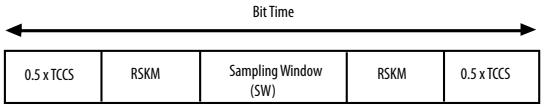
continued...

(148) You can set this value in the Intel Quartus Prime software by selecting **Input Delay Chain Setting** or **Output Delay Chain Setting** in the **Assignment Name** column.

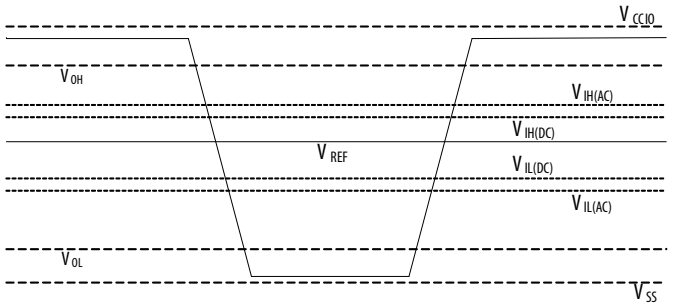
(149) Minimum offset does not include the intrinsic delay.

Term	Definition
	Single-Ended Waveform  **Differential Waveform**  Transmitter Output Waveforms **Single-Ended Waveform**  **Differential Waveform** 
f_{HSCLK}	I/O PLL input clock frequency.
f_{HSDR}	High-speed I/O block—Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
$f_{HSDRDPA}$	High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
J	High-speed I/O block—Deserialization factor (width of parallel data bus).
JTAG Timing Specifications	JTAG Timing Specifications:

continued...

Term	Definition
	
R_L	Receiver differential input discrete resistor (external to the Intel Stratix 10 device).
Sampling window (SW)	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown: 
Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing. Single-Ended Voltage Referenced I/O Standard

continued...

Term	Definition
	
t_C	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t_{DUTY}	High-speed I/O block—Duty cycle on high-speed transmitter output clock.
t_{FALL}	Signal high-to-low transition time (80–20%).
t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.
t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL.
t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL.
t_{RISE}	Signal low-to-high transition time (20–80%).
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
$V_{CM(DC)}$	DC Common mode input voltage.
V_{ICM}	Input Common mode voltage—The common mode of the differential signal at the receiver.
$V_{ICM(DC)}$	$V_{CM(DC)}$ DC Common mode input voltage.
V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.

continued...

Term	Definition
V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
$V_{IH(AC)}$	High-level AC input voltage.
$V_{IH(DC)}$	High-level DC input voltage.
V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{IL(AC)}$	Low-level AC input voltage.
$V_{IL(DC)}$	Low-level DC input voltage.
V_{OCM}	Output Common mode voltage—The common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter.
V_{SWING}	Differential input voltage.
V_{OX}	Output differential cross point voltage.
$V_{IX(AC)}$	V_{IX} Input differential cross point voltage.
W	High-speed I/O block—Clock Boost Factor.

Document Revision History for the Intel Stratix 10 Device Datasheet

Document Version	Changes
2019.02.25	• Changed the variants datasheet status from Preliminary to Final in the *Datasheet Status for Intel Stratix 10 Devices* table.
2019.02.05	• Updated the maximum specifications for V_I (for 3 V I/O) from 3.6 V to 3.8 V. • Added the LVPECL DC electrical characteristics table for the E-Tile transceiver reference clock. • Added the electrical and jitter requirements table for the E-Tile transceiver reference clock. • Merged the minimum, typical and maximum specifications for the E-Tile transmitter common mode voltage into one specification. • Updated the NRZ data rate for the E-Tile transceivers. • Added the performance specifications for the HBM2 interface in the Intel Stratix 10 MX devices. • Updated the temperature specifications for the HBM2 interface in Intel Stratix 10 devices. • Updated the Intel Quartus Prime Assignment Names in the *Programmable IOE Delay for Intel Stratix 10 Devices* table.

continued...

Document Version	Changes
2018.10.25	• Updated the description for the X suffix. • Removed the description on VREFP_ADC and VREFN_ADC I/O pins in the *Maximum Allowed Overshoot During Transitions for Intel Stratix 10 Devices (for LVDS I/O)* table. • Updated the *Recommended Operating Conditions for Intel Stratix 10 Devices* table. — Updated the V_{CC} and V_{CCP} specifications for –3X speed grade. — Removed Pulse-Width Modulation (PWM) from the note to V_{CC} and V_{CCP} for SmartVID devices. — Updated the note to V_{CCBAT}. — Removed the V_{REFP_ADC} specifications. • Changed the minimum and maximum values for $V_{CCH\_GXB[L,R]}$ in the "Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L-Tile Devices in a Non-Bonded Configuration" table. • Changed the minimum and maximum values for $V_{CCH\_GXB[L,R]}$ in the "Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L-Tile Devices in a Bonded Configuration" table. • Changed the minimum and maximum values for $V_{CCH\_GXB[L,R]}$ in the "Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX H-Tile Devices in a Bonded Configuration" table. • Changed the minimum and maximum values for $V_{CCH\_GXB[L,R]}$ in the "Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX H-Tile Devices in a Bonded Configuration" table. • Updated the footnote specifying pll_powerdown minimum assertion cycles in the "Transceiver Performance for Intel Stratix 10 GX/SX L-Tile Devices" section. • Added a noise mask specification column and updated the symbol names in the "Transceiver Power Supply Operating Conditions for Intel Stratix 10 TX/MX E-Tile Devices" table. • Added a note about TX jitter specifications for the SerialLite III protocol in the "Transceiver Performance for Intel Stratix 10 GX/SX L-Tile Devices" section. • Removed the Transmitter REFCLK Phase Jitter (100 MHz) specification from the "L-Tile Reference Clock Specifications" table. • Added a note about PCI Express reference clock phase jitter specifications to the "Transceiver Specifications for Intel Stratix 10 GX/SX L-Tile Devices" section • Changed the GXT channel specification for chip-to-chip, -3 speed grade devices in the "Intel Stratix 10 GX/SX H-Tile Transmitter and Receiver Datarate Performance" table. • Added a note about TX jitter specifications for the SerialLite III protocol in the "Transceiver Performance for Intel Stratix 10 GX/SX H-Tile Devices" section. • Removed the Transmitter REFCLK Phase Jitter (100 MHz) specification from the "H-Tile Reference Clock Specifications" table. • Added a note about PCI Express reference clock phase jitter specifications to the "Transceiver Specifications for Intel Stratix 10 GX/SX H-Tile Devices" section • Removed PWM from the note to V_{CCL_HPS} and $V_{CCPLLDIG\_HPS}$ for SmartVID devices in the *HPS Power Supply Operating Conditions for Intel Stratix 10 Devices* table. • Updated the *I/O PLL Specifications for Intel Stratix 10 Devices* table. — Updated the maximum f_{VCO} specifications for –3 speed grade. — Updated the description for $t_{CASC\_OUTPJ\_DC}$. • Added series resistance and diode ideality factor parameters for E-Tile TSD in the *External Temperature Sensing Diode Specifications for Intel Stratix 10 Devices* table.

continued...

Document Version	Changes
	• Added a note on half rate support for DDR3 SDRAM in the *Memory Standards Supported by the Hard Memory Controller for Intel Stratix 10 Devices* table. • Updated the *Memory Standards Supported by the Soft Memory Controller for Intel Stratix 10 Devices* table. — Added a note to RLDRAM 3 — Updated QDR IV SRAM specification — Added a note on full rate support for QDR II SRAM • Removed the *DQS Phase Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSERR}) for Intel Stratix 10 Devices* table. • Updated the description in the *Memory Output Clock Jitter Specifications* section. • Updated the *Maximum HPS Clock Frequencies for Intel Stratix 10 Devices* table. — Updated the MPU frequency for V_{CCL_HPS} = 0.94 V. — Added note to L3 Interconnect Frequency for V_{CCL_HPS} = 0.94 V for –E1V, –I1V, –E2L, –I2L, –E3X, and –I3X. • Updated the specifications in the *HPS Internal Oscillator Frequency for Intel Stratix 10 Devices* table. • Updated the specifications for $T_{spi\_ref\_clk}$, $T_{dssfrst}$, and T_{dsslst} in the *SPI Master Timing Requirements for Intel Stratix 10 Devices* table. • Updated the specifications for $T_{spi\_ref\_clk}$ and T_h in the *SPI Slave Timing Requirements for Intel Stratix 10 Devices* table. • Updated the *HPS Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Intel Stratix 10 Devices* table. — Updated the description for T_{sdmmc_clk}. — Removed the note to the minimum and maximum specifications for T_d. — Updated the reference clock in the note for T_d and T_{su}. • Updated T_{clk} specifications in the following tables: — *Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Intel Stratix 10 Devices* — *RGMII RX Timing Requirements for Intel Stratix 10 Devices* — *Reduced Media Independent Interface (RMII) Clock Timing Requirements for Intel Stratix 10 Devices* — *Management Data Input/Output (MDIO) Timing Requirements for Intel Stratix 10 Devices* • Updated T_d specification in the *Management Data Input/Output (MDIO) Timing Requirements for Intel Stratix 10 Devices* table. • Updated the title for the following diagrams: — *RGMII TX and RMII TX Timing Diagram* — *RGMII RX and RMII RX Timing Diagram* • Removed $t_{CF02ST0}$ specifications for Device Security Feature (Zeroization) ON in the *General Configuration Timing Specifications for Intel Stratix 10 Devices* table. • Updated t_{JCP} specification in the *JTAG Timing Parameters and Values for Intel Stratix 10 Devices* table. • Added T_{ext_skew} specifications in the *AS Timing Parameters for Intel Stratix 10 Devices* table. • Updated the *Avalon-ST Configuration Timing Diagram*.

continued...

Document Version	Changes
	• Mentioned that the SD/MMC configuration scheme will be available in a future release of the Intel Quartus Prime software.*SD/MMC Timing Parameters for Intel Stratix 10 Devices* table. • Updated the *Maximum Configuration Time Estimation* section. — Clarify the maximum configuration time. — Updated the note to AVST ×8, AVST ×16, and AVST ×32. • Removed Preliminary tags for all table. Refer to the *Data Status for Intel Stratix 10 Devices* table for the data status for each variant.
2018.07.13	Corrected the typical values for V_{CC} and V_{CCP} in the *Recommended Operating Conditions for Intel Stratix 10 Devices* table.
2018.07.12	Made the following changes: • Updated the *Absolute Maximum Ratings for Intel Stratix 10 Devices* table. — Updated the maximum values for V_{CCIO} (for LVDS I/O), V_{CCIO_HPS}, and V_{CCIO_SDM} from 2.46 V to 2.19 V. — Updated the maximum value for V_I (for LVDS I/O) from 2.5 V to 2.19 V. — Updated the I_{OUT} specifications. • Updated the *Maximum Allowed Overshoot and Undershoot Voltage* section. — Updated the overshoot and undershoot values in the description. — Updated the specifications in the *Maximum Allowed Overshoot During Transitions for Intel Stratix 10 Devices (for LVDS I/O)* and *Maximum Allowed Overshoot During Transitions for Intel Stratix 10 Devices (for LVDS I/O)* tables. — Updated the voltages in the *Intel Stratix 10 Devices Overshoot Duration* diagram. • Added a footnote to 1.03 V typical voltage in the "Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L-Tile Devices in a Non-Bonded Configuration" table. • Added a footnote to 1.03 V typical voltage in the "Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L-Tile Devices in a Bonded Configuration" table. • Added a footnote to 1.03 V typical voltage in the "Transceiver Power Supply Operating Conditions for Intel Stratix 10 H-Tile Devices in a Non-Bonded Configuration" table. • Added a footnote to 1.03 V typical voltage in the "Transceiver Power Supply Operating Conditions for Intel Stratix 10 H-Tile Devices in a Bonded Configuration" table. • Changed the minimum and maximum voltage for V_{CCT_GXB} and V_{CCR_GXB} in the "Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L-Tile Devices in a Non-Bonded Configuration" table. • Changed the minimum and maximum voltage for V_{CCT_GXB} and V_{CCR_GXB} in the "Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L-Tile Devices in a Bonded Configuration" table. • Changed the minimum and maximum voltage for V_{CCT_GXB} and V_{CCR_GXB} in the "Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX H-Tile Devices in a Non-Bonded Configuration" table. • Changed the minimum and maximum voltage for V_{CCT_GXB} and V_{CCR_GXB} in the "Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX H-Tile Devices in a Bonded Configuration" table. • Updated V_{CC}, V_{CCP}, V_{CCBAT}, V_{CCIO}, V_{CCM_WORD}, and V_I specifications in the *Recommended Operating Conditions for Intel Stratix 10 Devices* table. • Updated V_{CCL_HPS} and $V_{CCPLLDIG\_HPS}$ specifications in the *HPS Power Supply Operating Conditions for Intel Stratix 10 Devices* table. • Updated the *OCT Without Calibration Resistance Tolerance Specifications for Intel Stratix 10 Devices* table. • Removed *Equation for OCT Variation Without Recalibration*.

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Document Version	Changes
	• Added pin capacitance specifications. • Added the resistance tolerance for R_{PU} in the *Internal Weak Pull-Up Resistor Values for Intel Stratix 10 Devices* table. • Updated the V_{CCIO} specifications for POD12 in the *Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel Stratix 10 Devices* table. • Removed the V_{OL} and V_{OH} specifications for POD12 in the *Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Intel Stratix 10 Devices* table. • Updated $V_{SWING(DC)}$ specification for SSTL-12 in the *Differential SSTL I/O Standards Specifications for Intel Stratix 10 Devices* table. • Corrected $V_{X(AC)}$ to $V_{IX(AC)}$ in the *Differential SSTL I/O Standards Specifications for Intel Stratix 10 Devices* and *Glossary* tables. • Updated the minimum and maximum values for $V_{CCH\_GXB[L,R]}$ in the "Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L-Tile Devices in a Non-Bonded Configuration" table. • Updated the minimum and maximum values for $V_{CCH\_GXB[L,R]}$ in the "Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L-Tile Devices in a Bonded Configuration" table. • Updated the minimum and maximum values for $V_{CCH\_GXB[L,R]}$ in the "Transceiver Power Supply Operating Conditions for Intel Stratix 10 H-Tile Devices in a Non-Bonded Configuration" table. • Updated the minimum and maximum values for $V_{CCH\_GXB[L,R]}$ in the "Transceiver Power Supply Operating Conditions for Intel Stratix 10 H-Tile Devices in a Bonded Configuration" table. • Changed the minimum, typical, and maximum values for $V_{CCT\_GXB[L,R]}$ and $V_{CCR\_GXB[L,R]}$ for datarates > 17.4 Gbps to 28.3 Gbps in the "Transceiver Power Supply Operating Conditions for Intel Stratix 10 H-Tile Devices in a Bonded Configuration" table. • Changed the footnote for the minimum value of the Input Reference Clock Frequency (fPLL PLL) symbol in the "L-Tile Reference Clock Specifications" table. • Changed the minimum and maximum frequencies and added a Modes column to the "L-Tile Fractional PLL Performance" table. • Changed the minimum and maximum frequencies and added a Modes column to the "H-Tile Fractional PLL Performance" table. • Changed the minimum supported output frequency in the "L-Tile CMU PLL Performance" table. • Added a footnote to the Transmitter REFCLK Phase Jitter (100 MHz) specification in the "L-Tile Reference Clock Specifications" table. • Added a footnote to the Transmitter REFCLK Phase Noise (800 MHz) specification in the "H-Tile Reference Clock Specifications" table. • Removed the DC coupling description from the VICM symbol in the "L-Tile Receiver Specifications" table. • Added a footnote to the V_{OD} Setting column in the "L-Tile Typical Transmitter V_{OD} Settings" table. • Added a footnote to the GXT channels for transceiver speed grade -1 in the "Intel Stratix 10 GX/SX H-Tile Transmitter and Receiver Datarate Performance" table. • Changed the footnote for the minimum value of the Input Reference Clock Frequency (fPLL PLL) symbol in the "H-Tile Reference Clock Specifications" table. • Changed the maximum voltage for the V_{ID} (before device configuration) parameter in the "H-Tile Receiver Specifications" table. • Removed DC coupling support from the V_{ICM} parameter in the "H-Tile Receiver Specifications" table. • Added a footnote to the V_{OD} Setting column in the "H-Tile Typical Transmitter V_{OD} Settings" table. • Changed the VICM (AC Coupled) typical value in the "H-Tile Reference Clock Specifications" table. • Updated the programmable clock routing specification for –1 speed grade in the *Clock Tree Performance for Intel Stratix 10 Devices* table.

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Document Version	Changes
	• Updated the *Fractional PLL Specifications for Intel Stratix 10 Devices* table. — Updated f_{VCO} specifications. — Removed t_{PLL_PSERR} specifications. • Updated the *Memory Block Performance Specifications for Intel Stratix 10 Devices* table. — Added the specifications for the "Simple dual-port with ECC and optional pipeline registers enabled, with the read-during-write option set to **Old Data**, 512 × 32" mode in the M20K block. — Updated the specifications for eSRAM. • Updated specifications in the *External Temperature Sensing Diode Specifications for Intel Stratix 10 Devices* table. • Updated the *Internal Voltage Sensor Specifications for Intel Stratix 10 Devices* table. • Removed the note on pending silicon characterization in the *High-Speed I/O Specifications for Intel Stratix 10 Devices* table. • Added the following tables: — *Memory Standards Supported by the Hard Memory Controller for Intel Stratix 10 Devices* — *Memory Standards Supported by the Soft Memory Controller for Intel Stratix 10 Devices* — *Memory Standards Supported by the HPS Hard Memory Controller for Intel Stratix 10 Devices* • Removed the note to the DLL reference clock input specification in the *DLL Frequency Range Specifications for Intel Stratix 10 Devices* table. • Removed the *Memory Output Clock Jitter Specifications for Intel Stratix 10 Devices* table. Stated that the clock jitter is within the JEDEC specifications. • Updated T_{RS_RT} specification in the *OCT Calibration Block Specifications for Intel Stratix 10 Devices* table. • Updated the note to SDRAM interconnect frequency in the *Maximum HPS Clock Frequencies for Intel Stratix 10 Devices* table. • Added HPS Internal Oscillator Frequency specifications. • Updated the minimum specification for clock input accuracy in the *HPS PLL Input Requirements for Intel Stratix 10 Devices* table. • Updated the minimum specifications for T_d, T_{su}, and T_h in the *HPS USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) Low Pin Interface (ULPI) Timing Requirements for Intel Stratix 10 Devices* table. • Updated specifications in the *HPS Programmable I/O Delay for Intel Stratix 10 Device* table. • Removed Preliminary tags for the following tables: — *HPS PLL Input Requirements for Intel Stratix 10 Devices* — *HPS PLL Performance for Intel Stratix 10 Devices* — *HPS Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Intel Stratix 10 Devices* — *HPS USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) Low Pin Interface (ULPI) Timing Requirements for Intel Stratix 10 Devices* — *HPS I^2C Timing Requirements for Intel Stratix 10 Devices* — *HPS NAND ONFI 1.0 Timing Requirements for Intel Stratix 10 Devices* — *HPS GPIO Interface* — *HPS JTAG Timing Requirements for Intel Stratix 10 Devices* — *HPS Programmable I/O Delay for Intel Stratix 10 Device*

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Document Version	Changes
	• Removed information on NAND configuration mode. — Removed NAND mode in the *POR Delay Specification for Intel Stratix 10 Devices* table. — Removed the *NAND Configuration Timing* section. — Removed the maximum configuration time estimation for NAND mode. • Updated the note to clock input frequency in the *External Configuration Clock Source (OSC_CLK_1) Clock Input Requirements* table. • Added description in the *SD/MMC Timing Parameters for Intel Stratix 10 Devices* table. • Removed the statement stating that the maximum configuration time does not exceed 2× of the minimum configuration time in the *Maximum Configuration Time Estimation* section. • Updated the *I/O Timing* section on the I/O timing information generation guidelines. • Updated the specifications for fast and slow models in the *Programmable IOE Delay for Intel Stratix 10 Devices* table. • Finalized the data for the Intel Stratix 10 GX variant (L-Tile). • Changed the input reference clock frequency (CMU PLL) minimum specification in the "L-Tile Reference Clock Specifications" table. • Changed the input reference clock frequency (CMU PLL) minimum specification in the "H-Tile Reference Clock Specifications" table.
2018.04.06	Made the following changes: • Added notes to I_{OUT} specification in the *Absolute Maximum Ratings for Intel Stratix 10 Devices* table. • Updated the *AS Timing Parameters for Intel Stratix 10 Devices* table. — Updated the specifications for T_{clk}, T_{dcsfrs}, T_{dcslst}, and T_{do}. — Removed the T_{ext_skew} specifications. — Updated the description on trace length matching and skew tolerance. — Updated the note for T_{ext_delay}. • Removed footnote to sampling rate in the *Internal Voltage Sensor Specifications for Intel Stratix 10 Devices* table. • Updated the specifications for t_{SDCLKP}, t_{SU}, and t_H in the *SD/MMC Timing Parameters for Intel Stratix 10 Devices* table. • Updated the compressed configuration bit stream sizes in the *Configuration Bit Stream Sizes* table. • Updated the *Maximum Configuration Time Estimation for Intel Stratix 10 Devices* tables. — Changed the table title from "Minimum Configuration Time Estimation" to "Maximum Configuration Time Estimation". — Updated the specifications.
2017.12.15	Made the following changes: • Added the *Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L-Tile Devices in a Non-Bonded Configuration* table. • Added the *Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L-Tile Devices in a Bonded Configuration* table. • Added the *Transceiver Power Supply Operating Conditions for Intel Stratix 10 H-Tile Devices in a Non-Bonded Configuration* table. • Added the *Transceiver Power Supply Operating Conditions for Intel Stratix 10 H-Tile Devices in a Bonded Configuration* table. • Removed the *Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L- and H-Tile Devices* table. • Removed the *L-Tile Transmitter and Receiver Data Rate Performance, VCCR_GXB and VCCT_GXB Specifications* table. • Added the *Intel Stratix 10 GX/SX L-Tile Transmitter and Receiver Datarate Performance* table. • Added the *Intel Stratix 10 GX/SX H-Tile Transmitter and Receiver Datarate Performance* table.

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Document Version	Changes
	• Removed the *H-Tile Transmitter and Receiver Data Rate Performance, VCCR_GXB and VCCT_GXB Specifications* table • Added note to the *Maximum" column in the "Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX L- and H-Tile Devices—Preliminary* table. • Removed the Minimum differential eye opening at receiver serial input pins specification from the "L-Tile Receiver Specifications" table. • Updated *Absolute Maximum Ratings for Intel Stratix 10 Devices* table. — Updated T_{STG} minimum specifications from –65°C to –55°C. — Added V_I specifications. • Added -2 transceiver speed grade,the t_{ARESET}, and the t_{LOCK} specification to the "L-Tile ATX PLL Performance" table. • Added the t_{ARESET} and t_{LOCK} specifications to the "L-Tile Fractional PLL Performance" table. • Added the t_{ARESET} and t_{LOCK} specifications to the "L-Tile CMU PLL Performance" table. • Changed the Channel Span definition in the "L-Tile Transceiver Clock Network Maximum Data Rate Specifications" table. • Removed the VOCM (DC coupled) specification from the "L-Tile Transmitter Specifications" table. • Added the xN clock mode to the "L-Tile Transmitter Channel-to-channel Skew Specifications" table. • Added the xN clock mode to the "H-Tile Transmitter Channel-to-channel Skew Specifications" table. • Added the t_{LOCK} and t_{ARESET} specifications to the "H-Tile ATX PLL Performance" table. • Added the t_{LOCK} and t_{ARESET} specifications to the "H-Tile Fractional PLL Performance" table. • Added the t_{LOCK} and t_{ARESET} specifications to the "H-Tile CMU PLL Performance" table. • Removed the Minimum differential eye opening at receiver serial input pins specification from the "H-Tile Receiver Specifications" table. • Split LVDS I/O and 3 V I/O specifications in *Maximum Allowed Overshoot During Transitions for Intel Stratix 10 Devices* table into two separate tables. Updated the LVDS I/O specifications. • Added *Intel Stratix 10 Devices Overshoot Duration* figure and description. • Updated *Recommended Operating Conditions for Intel Stratix 10 Devices* table. — Updated V_{CCIO_UIB} specifications. — Updated note to minimum and maximum columns. — Changed the symbol from V_{CCM} to V_{CCM_WORD}. • Added specifications for V_{CCIO} = 2.5 V in the following tables: — *Bus Hold Parameters for Intel Stratix 10 Devices* — *Internal Weak Pull-Up Resistor Values for Intel Stratix 10 Devices* • Updated specifications in *OCT Calibration Accuracy Specifications for Intel Stratix 10 Devices* table. • Updated specifications in *OCT Without Calibration Resistance Tolerance Specifications for Intel Stratix 10 Devices* table. — Added specifications for V_{CCIO} = 3.0, 2.5 — Updated specifications for V_{CCIO} = 1.8, 1.5, 1.2 • Added the following specifications in *Single-Ended I/O Standards Specifications for Intel Stratix 10 Devices* table. — 2.5 V I/O standard — Schmitt trigger input • Updated SSTL-125 and SSTL-135 I/O standards in *Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel Stratix 10 Devices* table.

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Document Version	Changes
	• Added specifications for SSTL-12 I/O standard in the following tables: — *Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Intel Stratix 10 Devices* — *Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Intel Stratix 10 Devices* — *Differential SSTL I/O Standards Specifications for Intel Stratix 10 Devices* • Updated the *Fractional PLL Specifications for Intel Stratix 10 Devices* table. — Updated t_{PLL_PSERR} specifications. — Updated t_{LOCK} description. — Removed t_{ARESET} specifications. • Updated $t_{OUTDUTY}$ in the *I/O PLL Specifications for Intel Stratix 10 Devices* table. • Updated *Internal Temperature Sensing Diode Specifications for Intel Stratix 10 Devices* table. — Added note for temperature range. — Updated conversion time from < 5 ms to < 1 ms. — Removed "Resolution" and "Minimum Resolution with no Missing Codes" specifications. • Updated *High-Speed I/O Specifications for Intel Stratix 10 Devices* table. — Updated Transmitter—TCCS specifications from 150 ps to 330 ps. — Updated Sampling Window specifications from 300 ps to 330 ps. — Updated SERDES factor J = 3 maximum data rate for transmitter and receiver. • Updated from 0.35 to 0.28 for the following: — *LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Equal to 1.6 Gbps* — *LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.6 Gbps* • Updated DLL reference clock input specifications in *DLL Frequency Range Specifications for Intel Stratix 10 Devices* table. • Updated T_{do} minimum specification from 0 ns to −1 ns in *AS Timing Parameters for Intel Stratix 10 Devices* table. • Updated minimum specifications for t_H from 0 ns to −1 ns in *SD/MMC Timing Parameters for Intel Stratix 10 Devices* table. • Updated *Configuration Bit Stream Sizes for Intel Stratix 10 Devices* table. — Added IOCSR bit stream sizes. — Added specifications for Intel Stratix 10 TX and MX devices. • Updated *Minimum Configuration Time Estimation for Intel Stratix 10 Devices* tables. — Added note to AVST ×8, AVST ×16, and AVST ×32. — Updated specifications for NAND. — Added specifications for Intel Stratix 10 TX and MX devices. • Added the following tables: — *External Temperature Sensing Diode Specifications for Intel Stratix 10 Devices* — *General Configuration Timing Specifications for Intel Stratix 10 Devices* • Moved t_{ST0} specifications from *Avalon-ST Timing Parameters for ×8, ×16, and ×32 Configurations in Intel Stratix 10 Devices* table. • Moved the specifications from *Initialization Time for Intel Stratix 10 Devices* table. — *Programmable IOE Delay for Intel Stratix 10 Devices*

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Document Version	Changes
2017.08.04	Made the following changes: • Clarified DLL operating frequency range in "DLL Range Specifications" • Clarified reference clock specifications in "HPS SPI Timing Characteristics"
2017.05.08	Made the following changes: • Updated description for V_{CCERAM} in Absolute Maximum Ratings for Intel Stratix 10 Devices table. • Added Maximum Allowed Overshoot During Transitions for Intel Stratix 10 Devices table. • Updated Recommended Operating Conditions for Intel Stratix 10 Devices table. — Updated V_{CC}, V_{CCIO}, and V_{CCBAT} specifications. — Updated symbol from $V_{CCPFUSE\_SDM}$ to $V_{CCFUSEWR\_SDM}$. — Updated description for V_{CCERAM} and V_{CCIO_UIB} . — Added V_{CCM} specifications. — Added footnotes to t_{RAMP} and V suffix speed grades. • Removed table: Temperature Compensation for SmartVID for Intel Stratix 10 Devices. Moved the table to the Intel Stratix 10 Power Management User Guide. • Updated the note in the "Transceiver Power Supply Operating Conditions" section. • Updated HPS Power Supply Operating Conditions for Intel Stratix 10 Devices table. — Updated V_{CCL_HPS} and $V_{CCPLLDIG\_HPS}$ specifications. — Added footnote for SmartVID. • Updated footnote to I_{OL} and I_{OH} in Single-Ended I/O Standards Specifications for Intel Stratix 10 Devices table. • Updated Differential I/O Standards Specifications for Intel Stratix 10 Devices table. — Changed D_{MAX} to data rate. — Added a note to V_{OD}. • Updated t_{OUTPJ_DC} and t_{OUTCCJ_DC} specifications in I/O PLL Specifications for Intel Stratix 10 Devices. • Changed the units of measure for the minimum frequency in the "L-Tile CMU PLL Performance" table. • Changed the units of measure for the minimum frequency in the "H-Tile CMU PLL Performance" table. • Updated t_{INCCJ} specification for F_{REF} < 100 MHz in the following tables: — Fractional PLL Specifications for Intel Stratix 10 Devices — I/O PLL Specifications for Intel Stratix 10 Devices • Added footnote to the following modes in DSP Block Performance Specifications for Intel Stratix 10 Devices table: — Fixed-point 27 × 27 multiplication mode — Fixed-point 18 × 18 multiplier adder mode — Fixed-point 18 × 18 multiplier adder summed with 36-bit input mode • Updated soft CDR mode specifications in High-Speed I/O Specifications for Intel Stratix 10 Devices table. • Added POR specifications. • Updated T_{do} maximum specification in AS Timing Parameters for Intel Stratix 10 Devices table. • Updated notes in Avalon-ST Configuration Timing Diagram.

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Document Version	Changes
	• Added description in NAND ONFI 1.0 Mode 0-5 Timing Requirements for Intel Stratix 10 Devices table. • Updated t_{SU}, t_H, and t_d specifications in SD/MMC Timing Parameters for Intel Stratix 10 Devices table. • Updated table title from "Initialization Clock Source Option and the Maximum Frequency for Intel Stratix 10 Devices" to "Initialization Time for Intel Stratix 10 Devices". • Updated description in Configuration Bit Stream Sizes for Intel Stratix 10 Devices to mention that the actual sizes may be equal or smaller than the bit stream sizes in this table. • Updated description in Minimum Configuration Time Estimation section. • Removed AS ×1 specifications in Minimum Configuration Time Estimation for Intel Stratix 10 Devices (AS, NAND, and SD/MMC) table. • Added Glossary. • Removed PowerPlay text from tool name.
2017.02.17	Made the following changes: • Added the "Transceiver Power Supply Operating Conditions for Intel Stratix 10 GX/SX E-Tile Devices" table. • Added the "E-Tile Transceiver Performance Specifications" section. • Added the "Transceiver Performance forIntel Stratix 10 E-Tile Devices" section. • Added the "Transceiver Reference Clock Specifications" section. • Added the "Transmitter Specifications for Intel Stratix 10 E-Tile Devices" section. • Added the "Receiver Specifications for Intel Stratix 10 E-Tile Devices" section. • Updated the "AS Timing Parameters for Intel Stratix 10 Devices" table. — Updated T_{dcsfrs} and T_{dcslst}. — Added T_{ext_delay} and T_{ext_skew}. — Removed T_{su} and T_h. • Updated AS Configuration Serial Input Timing Diagram.
2016.12.09	Made the following changes: • Changed the max t_{LTR} value and unit of measure in the "L-Tile Receiver Specifications" table. • Made the following changes to the "Transceiver Clocks Specifications for Stratix 10 GX/SX L-Tile Devices" table: — Changed the value of the `reconfig_clk` signal — Added a new footnote to the GX channel — Changed the minimum values for the GXT channel • Changed the max t_{LTR} value and unit of measure in the "H-Tile Receiver Specifications" table. • Removed the QPI footnote from the "H-Tile Transmitter Specifications" table. • Changed the value of the `reconfig_clk` signal in the "Transceiver Clocks Specifications for Stratix 10 GX/SX H-Tile Devices" table. • Changed the minimum value of f_{INPFD} in the "Fractional PLL Specifications for Stratix 10 Devices" table.
2016.10.31	Initial release.