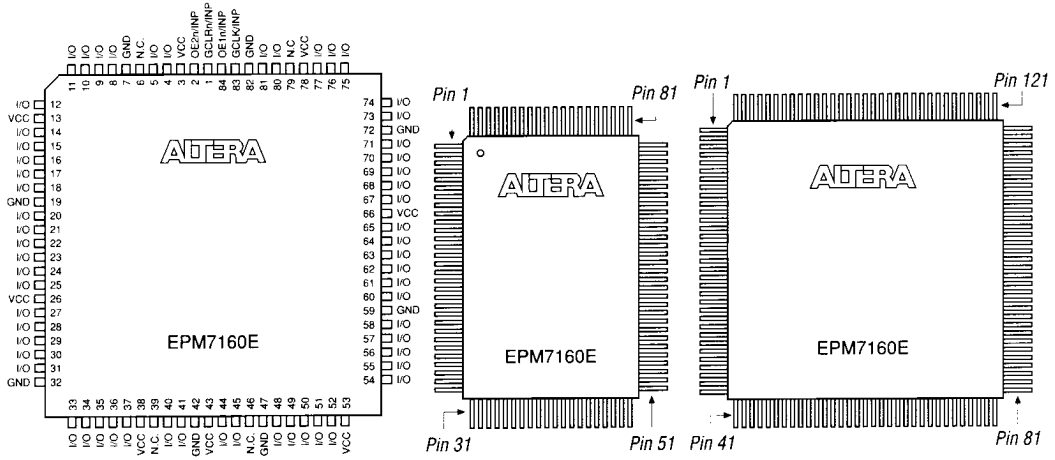
Features

- High-density, erasable CMOS EPLD based on second-generation MAX architecture
  - 3,200 usable gates
  - Combinatorial speeds with t_{PD} = 12 ns
  - Counter frequencies up to 90.9 MHz
- Advanced 0.8-micron CMOS EEPROM technology
- Programmable I/O architecture with up to 104 inputs or 100 outputs
- 160 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing up to 32 product terms in a single macrocell
- Available in plastic packages (see Figure 26):
  - 84-pin plastic J-lead chip carrier (PLCC)
  - 100- and 160-pin plastic quad flat pack (PQFP)

Figure 26. EPM7160 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 9 and 10 in this data sheet for pin-out information.



84-Pin J-Lead 100-Pin QFP 160-Pin QFP

General Description

The Altera EPM7160 is a high-density, high-performance CMOS device based on Altera's second-generation MAX architecture. See Figure 27. Fabricated on a 0.8-micron EEPROM technology, the EPM7160 provides 3,200 usable gates, counter speeds of 90.9 MHz, and propagation delays of 12 ns. The EPM7160 architecture supports 100% TTL emulation and allows high integration of SSI, MSI, and LSI logic functions. With 160 macrocells, the EPM7160 implements complete system-level designs. It easily integrates multiple programmable logic devices such as PALs, GALs, and 22V10s. With its high performance and density, the EPM7160 provides FPGA

density with PAL performance. The high density and high I/O pin count also make the EPM7160 appropriate for prototyping gate arrays. The EPM7160 can accommodate both logic- and I/O-intensive designs.

Figure 27. EPM7160 Block Diagram

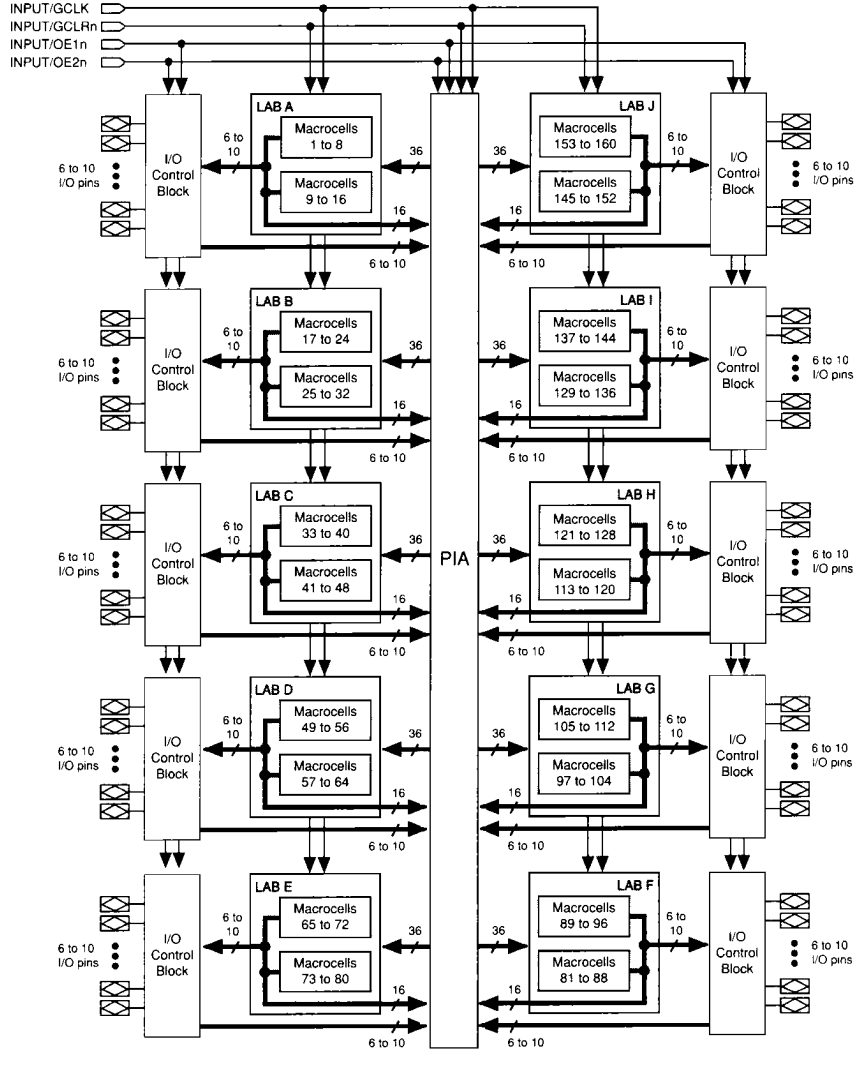


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Figure 28 shows the output drive characteristics of EPM7160 I/O pins.

Figure 28. EPM7160 Output Drive Characteristics

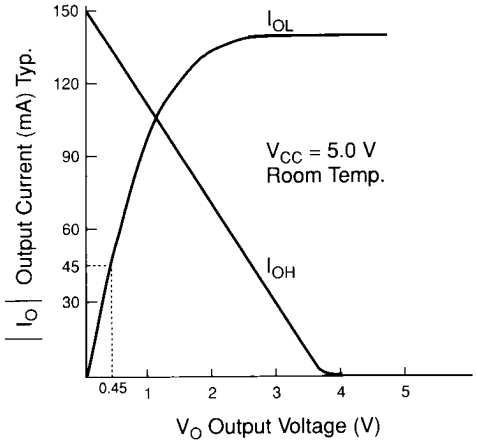


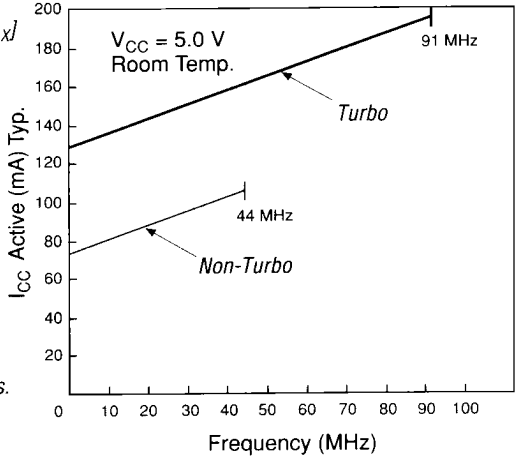
Figure 29 shows typical supply current versus frequency for the EPM7160.

Figure 29. EPM7160 I_{CC} vs. Frequency

I_{CC} is calculated with the following equation:
$I_{CC} = (0.82 \times MC_{TON}) + (0.43 \times MC_{TOFF}) + [(0.0046 \times MC) \times f_{MAX}]$

The parameters for this equation are:
MC_{TON} = number of macrocells used with Turbo Bit on
MC_{TOFF} = number of macrocells used with Turbo Bit off
MC = total number of macrocells used in the design ($MC_{TON} + MC_{TOFF}$)
f_{MAX} = highest Clock frequency to the device

This measurement provides an I_{CC} estimate based on typical conditions (V_{CC} = 5.0 V, room temperature) using a typical pattern of a 16-bit loadable, enabled, up/down counter in each LAB with an output load. Actual I_{CC} should be verified during operation since this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.



Absolute Maximum Ratings See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			800	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			4000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (low-power mode, standby)	V_I = GND, No load *Note (4)*		110		mA
I_{CC2}	V_{CC} supply current (low-power mode, active)	V_I = GND, No load, f = 1.0 MHz, *Note (4)*		115		mA

Capacitance *Note (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF

AC Operating Conditions *Note (2)*

External Timing Parameters			EPM7160-12		EPM7160-15		EPM7160-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		12		15		20	ns
t_{PD2}	I/O input to non-registered output			12		15		20	ns
t_{SU}	Global clock setup time		10		11		12		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		6		9		12	ns
t_{CH}	Global clock high time		4		5		6		ns
t_{CL}	Global clock low time		4		5		6		ns
t_{ASU}	Array clock setup time		4		5		5		ns
t_{AH}	Array clock hold time		4		5		5		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		12		15		20	ns
t_{ACH}	Array clock high time		5		6		8		ns
t_{ACL}	Array clock low time		5		6		8		ns
t_{CNT}	Minimum global clock period			11		13		16	ns
f_{CNT}	Max. internal global clock frequency	*Note (4)*	90.9		76.9		62.5		MHz
t_{ACNT}	Minimum array clock period			11		13		16	ns
f_{ACNT}	Max. internal array clock frequency	*Note (4)*	90.9		76.9		62.5		MHz
f_{MAX}	Maximum clock frequency	*Note (6)*	125		100		83.3		MHz

Internal Timing Parameters			EPM7160-12		EPM7160-15		EPM7160-20		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			2		3		3	ns
t_{IO}	I/O input pad and buffer delay			2		3		3	ns
t_{SEXP}	Shared expander delay			7		8		9	ns
t_{PEXP}	Parallel expander delay			1		2		2	ns
t_{LAD}	Logic array delay			5		5		8	ns
t_{LAC}	Logic control array delay			5		5		8	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3		4		5	ns
t_{ZX}	Output buffer enable delay			6		6		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6		6		9	ns
t_{SU}	Register setup time		4		5		4		ns
t_{H}	Register hold time		4		5		5		ns
t_{RD}	Register delay			1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1	ns
t_{IC}	Array clock delay			5		5		8	ns
t_{EN}	Register enable time			5		5		8	ns
t_{GLOB}	Global control delay			0		1		3	ns
t_{PRE}	Register preset time			3		4		4	ns
t_{CLR}	Register clear time			3		4		4	ns
t_{PIA}	Prog. Interconnect Array delay			1		2		3	ns
t_{LPA}	Low power adder	*Note (7)*		12		13		15	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(3) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5.0 V ± 10%, T_C = –55° C to 125° C for military use.
(4) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} measured at 0° C.
(5) Capacitance measured at 25° C. Sample tested only. `OE1n` (high-voltage pin during programming) has a capacitance of 25 pF.
(6) The f_{MAX} values represent the highest frequency for pipelined data.
(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{EN}, t_{SEXP}, and t_{ACL} parameters for macrocells running in low-power mode.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPM7160-12, EPM7160-15, EPM7160-20
Industrial Temp.	(–40° C to 85° C)	EPM7160-20
Military Temp.	(–55° C to 125° C)	Consult factory

New Speed-Grade Ordering Codes

Speed-grade codes for EPM7128 devices have changed. The following table provides the new codes, which indicate the actual propagation delay times.

Old Speed Grade	New Speed Grade
EPM7160-1	EPM7160-12
EPM7160-2	EPM7160-15
EPM7160-3	EPM7160-20

Pin-Out Information

Tables 9 and 10 provide pin-out information for the EPM7160 packages.

Table 9. EPM7160 Dedicated Pin-Outs

Dedicated Pin	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
GCLK	83	89	139
GCLRn	1	91	141
OE1n	84	90	140
OE2n	2	92	142
GND	7, 19, 32, 42, 47, 59, 72, 82	13, 28, 40, 45, 61, 76, 88, 97	17, 42, 60, 66, 95, 113, 138, 148
VCC	3, 13, 26, 38, 43, 53, 66, 78	5, 20, 36, 41, 53, 68, 84, 93	8, 26, 55, 61, 79, 104, 133, 143
No Connect (N.C.)	6, 39, 46, 79	–	1, 2, 3, 4, 5, 6, 34, 35, 36, 37, 38, 39, 40, 45, 46, 47, 74, 75, 76, 81, 82, 83, 84, 85, 86, 87, 115, 116, 117, 118, 119, 120, 124, 125, 126, 127, 154, 155, 156, 157

Table 10. EPM7160 I/O Pin-Outs (Part 1 of 3)

MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
1	A	11	2	158	17	B	18	11	15
2	A	–	–	–	18	B	–	–	–
3	A	10	1	153	19	B	17	10	14
4	A	–	–	–	20	B	–	–	–
5	A	–	–	152	21	B	–	–	13
6	A	–	100	151	22	B	–	9	12
7	A	–	–	–	23	B	–	–	–
8	A	9	99	150	24	B	16	8	11
9	A	8	98	149	25	B	15	7	10
10	A	–	–	–	26	B	–	–	–
11	A	5	96	147	27	B	14	6	9
12	A	–	–	–	28	B	–	–	–
13	A	–	–	146	29	B	–	–	7
14	A	–	95	145	30	B	–	4	160
15	A	–	–	–	31	B	–	–	–
16	A	4	94	144	32	B	12	3	159
33	C	–	21	27	49	D	–	–	48
34	C	–	–	–	50	D	–	–	–
35	C	25	19	25	51	D	33	30	44
36	C	–	–	–	52	D	–	–	–
37	C	–	–	24	53	D	–	29	43
38	C	24	18	23	54	D	31	27	41
39	C	–	–	–	55	D	–	–	–
40	C	23	17	22	56	D	30	26	33
41	C	–	12	16	57	D	–	–	32
42	C	–	–	–	58	D	–	–	–
43	C	20	14	18	59	D	29	25	31
44	C	–	–	–	60	D	–	–	–
45	C	–	–	19	61	D	–	24	30
46	C	21	15	20	62	D	28	23	29
47	C	–	–	–	63	D	–	–	–
48	C	22	16	21	64	D	27	22	28

Table 10. EPM7160 I/O Pin-Outs (Part 2 of 3)

MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
65	E	–	–	59	81	F	–	–	62
66	E	–	–	–	82	F	–	–	–
67	E	41	39	58	83	F	44	42	63
68	E	–	–	–	84	F	–	–	–
69	E	–	38	57	85	F	–	43	64
70	E	40	37	56	86	F	45	44	65
71	E	–	–	–	87	F	–	–	–
72	E	37	35	54	88	F	48	46	67
73	E	–	–	53	89	F	–	–	68
74	E	–	–	–	90	F	–	–	–
75	E	36	34	52	91	F	49	47	69
76	E	–	–	–	92	F	–	–	–
77	E	–	33	51	93	F	–	48	70
78	E	35	32	50	94	F	50	49	71
79	E	–	–	–	95	F	–	–	–
80	E	34	31	49	96	F	51	50	72
97	G	–	–	73	113	H	–	60	94
98	G	–	–	–	114	H	–	–	–
99	G	52	51	77	115	H	60	62	96
100	G	–	–	–	116	H	–	–	–
101	G	–	52	78	117	H	–	–	97
102	G	54	54	80	118	H	61	63	98
103	G	–	–	–	119	H	–	–	–
104	G	55	55	88	120	H	62	64	99
105	G	–	–	89	121	H	–	69	105
106	G	–	–	–	122	H	–	–	–
107	G	56	56	90	123	H	65	67	103
108	G	–	–	–	124	H	–	–	–
109	G	–	57	91	125	H	–	–	102
110	G	57	58	92	126	H	64	66	101
111	G	–	–	–	127	H	–	–	–
112	G	58	59	93	128	H	63	65	100

Table 10. EPM7160 I/O Pin-Outs (Part 3 of 3)

MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP	MC	LAB	84-Pin J-Lead	100-Pin QFP	160-Pin QFP
129	I	67	70	106	145	J	74	79	123
130	I	–	–	–	146	J	–	–	–
131	I	68	71	107	147	J	75	80	128
132	I	–	–	–	148	J	–	–	–
133	I	–	–	108	149	J	–	–	129
134	I	–	72	109	150	J	–	81	130
135	I	–	–	–	151	J	–	–	–
136	I	69	73	110	152	J	76	82	131
137	I	70	74	111	153	J	77	83	132
138	I	–	–	–	154	J	–	–	–
139	I	71	75	112	155	J	80	85	134
140	I	–	–	–	156	J	–	–	–
141	I	–	–	114	157	J	–	–	135
142	I	–	77	121	158	J	–	86	136
143	I	–	–	–	159	J	–	–	–
144	I	73	78	122	160	J	81	87	137