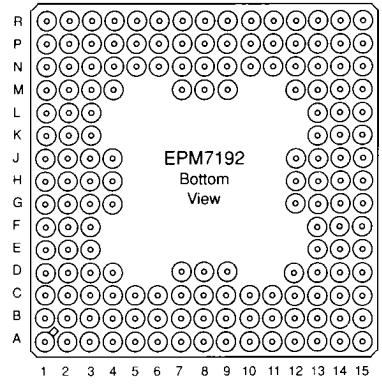
## Features

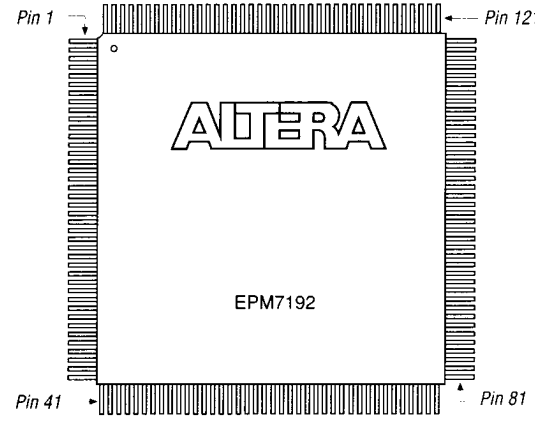
- High-density, erasable CMOS EPLD based on second-generation MAX architecture
  - 3,750 usable gates
  - Combinatorial speeds with $t_{PD}$ = 12 ns
  - Counter frequencies up to 90.9 MHz
- Advanced 0.8-micron CMOS EEPROM technology
- Programmable I/O architecture providing up to 124 inputs or 120 outputs
- 192 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing up to 32 product terms in a single macrocell
- Available in 160-pin packages (see Figure 30):
  - Pin-grid array (PGA)
  - Plastic quad flat pack (PQFP)

***Figure 30. EPM7192 Package Pin-Out Diagrams***

*Package outlines not drawn to scale. See Tables 11 and 12 in this data sheet for pin-out information.*




160-Pin PGA




160-Pin QFP

## General Description

The Altera EPM7192 is a high-density, high-performance CMOS EPLD based on Altera's second-generation MAX architecture. See Figure 31. Fabricated on a 0.8-micron EEPROM technology, the EPM7192 provides 3,750 usable gates, counter speeds of 90.9 MHz and propagation delays of 12 ns. The EPM7192 architecture supports 100% TTL emulation and allows high integration of SSI, MSI, and LSI logic functions. With 192 macrocells, the EPM7192 implements complete system-level designs. It easily integrates multiple programmable logic devices such as PALs, GALs, and 22V10s.

The high density and high I/O pin count make the EPM7192 appropriate for prototyping gate arrays. The EPM7192 can accommodate both logic- and I/O-intensive designs.

*Figure 31. EPM7192 Block Diagram*

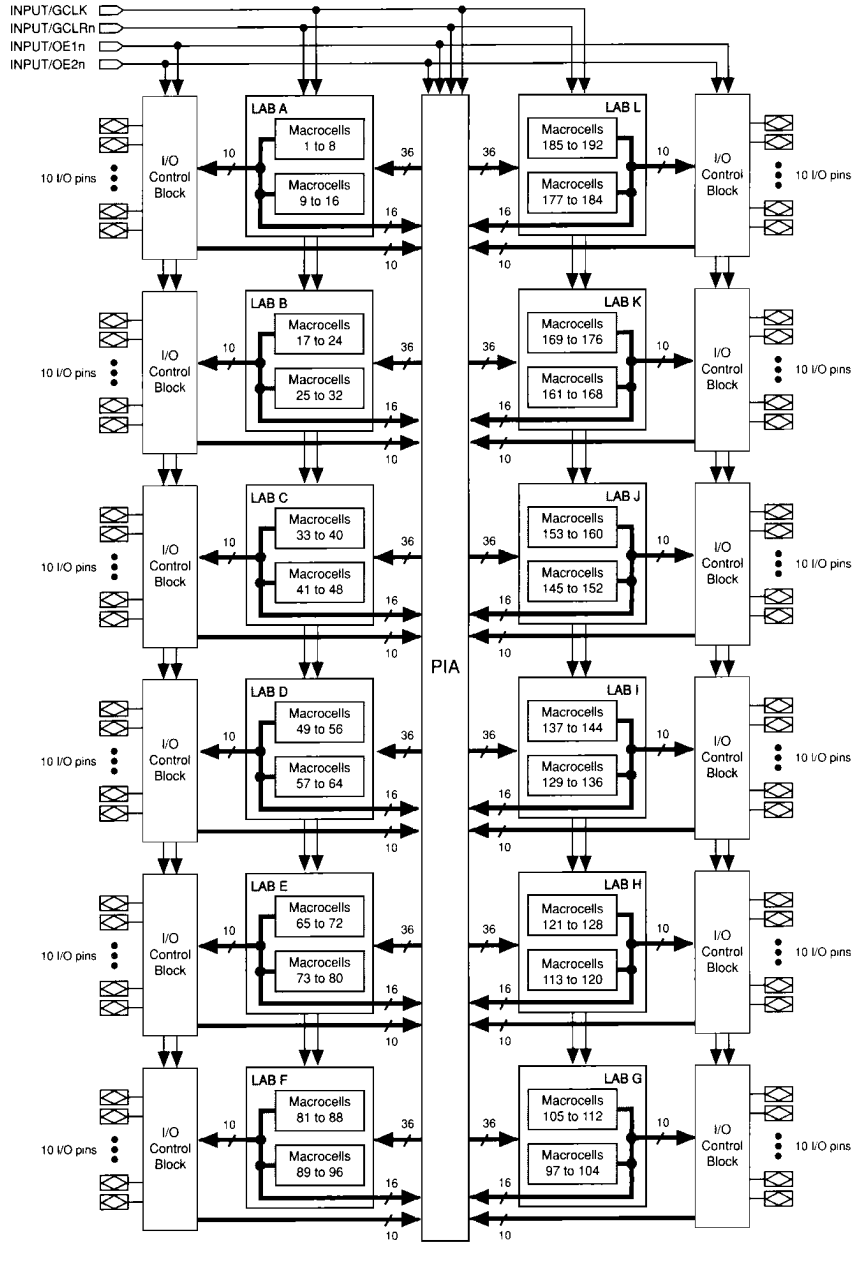


Figure 32 shows the output drive characteristics of EPM7192 I/O pins.

***Figure 32. EPM7192 Output Drive Characteristics***

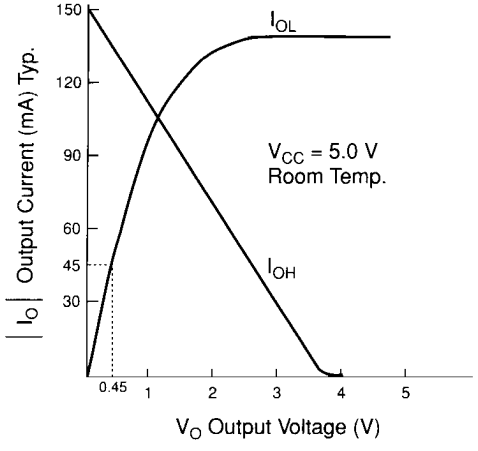



Figure 33 shows typical supply current versus frequency for the EPM7192.

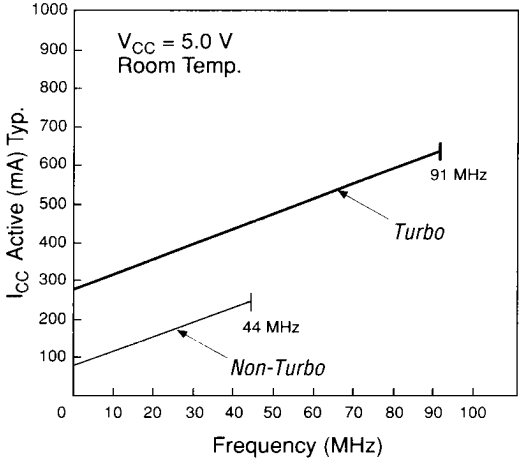
***Figure 33. EPM7192 $I_{CC}$ vs. Frequency***

*$I_{CC}$ is calculated with the following equation:*
*$I_{CC} = (1.5 \times MC_{TON}) + (0.48 \times MC_{TOFF}) + [(0.0088 \times MC) \times f_{MAX}]$*

*The parameters for this equation are:*

$MC_{TON}$ = *number of macrocells used with Turbo Bit on*
$MC_{TOFF}$ = *number of macrocells used with Turbo Bit off*
$MC$ = *total number of macrocells used in the design ($MC_{TON} + MC_{TOFF}$)*
$f_{MAX}$ = *highest Clock frequency to the device*

*This measurement provides an $I_{CC}$ estimate based on typical conditions ($V_{CC}$ = 5.0 V, room temperature) using a typical pattern of a 16-bit loadable, enabled, up/down counter in each LAB with no output load. Actual $I_{CC}$ should be verified during operation since this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.*







### *Absolute Maximum Ratings*

See *Operating Requirements for Altera Devices* in this data book.

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to GND | –2.0 | 7.0 | V |
| $V_I$ | DC input voltage | *Note (1)* | –2.0 | 7.0 | V |
| $I_{MAX}$ | DC $V_{CC}$ or GND current | | | 800 | mA |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $P_D$ | Power dissipation | | | 4000 | mW |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | Under bias | | 150 | ° C |

### *Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.75 | 5.25 | V |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating temperature | For commercial use | 0 | 70 | ° C |
| $T_A$ | Operating temperature | For industrial use | –40 | 85 | ° C |
| $T_C$ | Case temperature | For military use | –55 | 125 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

### *DC Operating Conditions* *Notes (2), (3)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2.0 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | 0.8 | V |
| $V_{OH}$ | High-level TTL output voltage | $I_{OH}$ = –4 mA DC | 2.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 8 mA DC | | | 0.45 | V |
| $I_I$ | Input leakage current | $V_I = V_{CC}$ or GND | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-state output off-state current | $V_O = V_{CC}$ or GND | –40 | | 40 | µA |
| $I_{CC1}$ | $V_{CC}$ supply current (low-power mode, standby) | $V_I$ = GND, No load *Note (4)* | | 130 | | mA |
| $I_{CC2}$ | $V_{CC}$ supply current (low-power mode, active) | $V_I$ = GND, No load, f = 1.0 MHz, *Note (4)* | | 135 | | mA |

### *Capacitance* *Note (5)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 15 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 15 | pF |

### *AC Operating Conditions* *Note (3)*

| *External Timing Parameters* | | | EPM7192-12 | | EPM7192-15 | | EPM7192-20 | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{PD1}$ | Input to non-registered output | C1 = 35 pF | | 12 | | 15 | | 20 | ns |
| $t_{PD2}$ | I/O input to non-registered output | | | 12 | | 15 | | 20 | ns |
| $t_{SU}$ | Global clock setup time | | 10 | | 11 | | 12 | | ns |
| $t_{H}$ | Global clock hold time | | 0 | | 0 | | 0 | | ns |
| $t_{CO1}$ | Global clock to output delay | C1 = 35 pF | | 6 | | 9 | | 12 | ns |
| $t_{CH}$ | Global clock high time | | 4 | | 5 | | 6 | | ns |
| $t_{CL}$ | Global clock low time | | 4 | | 5 | | 6 | | ns |
| $t_{ASU}$ | Array clock setup time | | 4 | | 5 | | 5 | | ns |
| $t_{AH}$ | Array clock hold time | | 4 | | 5 | | 5 | | ns |
| $t_{ACO1}$ | Array clock to output delay | C1 = 35 pF | | 12 | | 15 | | 20 | ns |
| $t_{ACH}$ | Array clock high time | | 5 | | 6 | | 8 | | ns |
| $t_{ACL}$ | Array clock low time | | 5 | | 6 | | 8 | | ns |
| $t_{CNT}$ | Minimum global clock period | | | 11 | | 13 | | 16 | ns |
| $f_{CNT}$ | Max. internal global clock frequency | *Note (4)* | 90.9 | | 76.9 | | 62.5 | | MHz |
| $t_{ACNT}$ | Minimum array clock period | | | 11 | | 13 | | 16 | ns |
| $f_{ACNT}$ | Max. internal array clock frequency | *Note (4)* | 90.9 | | 76.9 | | 62.5 | | MHz |
| $f_{MAX}$ | Maximum clock frequency | *Note (6)* | 125 | | 100 | | 83.3 | | MHz |

| *Internal Timing Parameters* | | | EPM7192-12 | | EPM7192-15 | | EPM7192-20 | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{IN}$ | Input pad and buffer delay | | | 2 | | 3 | | 3 | ns |
| $t_{IO}$ | I/O input pad and buffer delay | | | 2 | | 3 | | 3 | ns |
| $t_{SEXP}$ | Shared expander delay | | | 7 | | 8 | | 9 | ns |
| $t_{PEXP}$ | Parallel expander delay | | | 1 | | 2 | | 2 | ns |
| $t_{LAD}$ | Logic array delay | | | 5 | | 5 | | 8 | ns |
| $t_{LAC}$ | Logic control array delay | | | 5 | | 5 | | 8 | ns |
| $t_{OD}$ | Output buffer and pad delay | C1 = 35 pF | | 3 | | 4 | | 5 | ns |
| $t_{ZX}$ | Output buffer enable delay | | | 6 | | 6 | | 9 | ns |
| $t_{XZ}$ | Output buffer disable delay | C1 = 5 pF | | 6 | | 6 | | 9 | ns |
| $t_{SU}$ | Register setup time | | 4 | | 5 | | 4 | | ns |
| $t_{H}$ | Register hold time | | 4 | | 5 | | 5 | | ns |
| $t_{RD}$ | Register delay | | | 1 | | 1 | | 1 | ns |
| $t_{COMB}$ | Combinatorial delay | | | 1 | | 1 | | 1 | ns |
| $t_{IC}$ | Array clock delay | | | 5 | | 5 | | 8 | ns |
| $t_{EN}$ | Register enable time | | | 5 | | 5 | | 8 | ns |
| $t_{GLOB}$ | Global control delay | | | 0 | | 1 | | 3 | ns |
| $t_{PRE}$ | Register preset time | | | 3 | | 4 | | 4 | ns |
| $t_{CLR}$ | Register clear time | | | 3 | | 4 | | 4 | ns |
| $t_{PIA}$ | Prog. Interconnect Array delay | | | 1 | | 2 | | 3 | ns |
| $t_{LPA}$ | Low power adder | *Note (7)* | | 12 | | 13 | | 15 | ns |

*Notes to tables:*

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Typical values are for $T_A$ = 25° C and $V_{CC}$ = 5.0 V.
(3) Operating conditions: $V_{CC}$ = 5.0 V ± 5%, $T_A$ = 0° C to 70° C for commercial use.
$V_{CC}$ = 5.0 V ± 10%, $T_A$ = –40° C to 85° C for industrial use.
$V_{CC}$ = 5.0 V ± 10%, $T_C$ = –55° C to 125° C for military use.
(4) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. $I_{CC}$ measured at 0° C.
(5) Capacitance measured at 25° C. Sample-tested only. The OE1n pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.
(6) The $f_{MAX}$ values represent the highest frequency for pipelined data.
(7) The $t_{LPA}$ parameter must be added to the $t_{LAD}$, $t_{LAC}$, $t_{IC}$, $t_{ACL}$, $t_{EN}$, and $t_{SEXP}$ parameters for macrocells running in low-power mode.

## Product Availability

| Product Grade | | Availability |
|---|---|---|
| Commercial Temp. | (0° C to 70° C) | EPM7192-12, EPM7192-15, EPM7192-20 |
| Industrial Temp. | (–40° C to 85° C) | EPM7192-20 |
| Military Temp. | (–55° C to 125° C) | Consult factory |
| MIL-STD-883-Compliant | *Note (1)* | See *Military Products* in this data book. |

*Note:*

(1) MIL-STD-883-compliant product specifications are provided in this data book and in Military Product Drawings (MPDs). However, only MPDs should be used to prepare Source Control Drawings (SCDs). MPDs are available from Altera Marketing at (408) 894-7000.

## New Speed-Grade Ordering Codes

Speed-grade codes for EPM7192 devices have changed. The following table provides the new codes, which indicate the actual propagation delay times.

| Old Speed Grade | New Speed Grade |
|---|---|
| EPM7192-1 | EPM7192-12 |
| EPM7192-2 | EPM7192-15 |
| EPM7192-3 | EPM7192-20 |

## Pin-Out Information

Tables 11 and 12 provide pin-out information for the EPM7192 packages.

*Table 11. EPM7192 Dedicated Pin-Outs*

| Dedicated Pin | 160-Pin PGA | 160-Pin QFP |
|---|---|---|
| GCLK | M8 | 139 |
| GCLRn | N8 | 141 |
| OE1n | P8 | 140 |
| OE2n | R8 | 142 |
| GND | C4, C6, C11, D7, D9, D13, G4, H12, J4, M7, M9, M13, N4, N11 | 3, 18, 32, 47, 57, 64, 66, 81, 96, 111, 126, 138, 143, 148 |
| VCC | C5, C7, C9, C10, C12, D3, G12, H4, J12, M3, N5, N7, N9, N12 | 10, 25,40,55, 56, 65, 74, 89, 103, 118, 133, 137, 144, 155 |
| No Connect (N.C.) | A1, A2, A14, A15, R1, R2, R14, R15 | 1, 11, 39,54, 67, 82, 110, 120 |

*Table 12. EPM7192 I/O Pin-Outs (Part 1 of 2)*

| MC | LAB | 160-Pin PGA | 160-Pin QFP | MC | LAB | 160-Pin PGA | 160-Pin QFP | MC | LAB | 160-Pin PGA | 160-Pin QFP |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | A | M12 | 156 | 17 | B | L14 | 8 | 33 | C | H14 | 21 |
| 2 | A | – | – | 18 | B | – | – | 34 | C | – | – |
| 3 | A | P11 | 154 | 19 | B | M14 | 7 | 35 | C | J13 | 20 |
| 4 | A | – | – | 20 | B | – | – | 36 | C | – | – |
| 5 | A | P12 | 153 | 21 | B | M15 | 6 | 37 | C | H15 | 19 |
| 6 | A | P10 | 152 | 22 | B | N14 | 5 | 38 | C | J15 | 17 |
| 7 | A | – | – | 23 | B | – | – | 39 | C | – | – |
| 8 | A | R12 | 151 | 24 | B | N15 | 4 | 40 | C | J14 | 16 |
| 9 | A | N10 | 150 | 25 | B | P15 | 2 | 41 | C | K15 | 15 |
| 10 | A | – | – | 26 | B | – | – | 42 | C | – | – |
| 11 | A | R11 | 149 | 27 | B | N13 | 160 | 43 | C | K13 | 14 |
| 12 | A | – | – | 28 | B | – | – | 44 | C | – | – |
| 13 | A | R10 | 147 | 29 | B | P14 | 159 | 45 | C | L15 | 13 |
| 14 | A | P9 | 146 | 30 | B | P13 | 158 | 46 | C | K14 | 12 |
| 15 | A | – | – | 31 | B | – | – | 47 | C | – | – |
| 16 | A | R9 | 145 | 32 | B | R13 | 157 | 48 | C | L13 | 9 |
| 49 | D | D15 | 33 | 65 | E | B12 | 45 | 81 | F | D8 | 60 |
| 50 | D | – | – | 66 | E | – | – | 82 | F | – | – |
| 51 | D | E15 | 31 | 67 | E | B13 | 44 | 83 | F | A9 | 59 |
| 52 | D | – | – | 68 | E | – | – | 84 | F | – | – |
| 53 | D | E14 | 30 | 69 | E | C13 | 43 | 85 | F | C8 | 58 |
| 54 | D | F15 | 29 | 70 | E | B14 | 42 | 86 | F | B9 | 53 |
| 55 | D | – | – | 71 | E | – | – | 87 | F | – | – |
| 56 | D | F13 | 28 | 72 | E | C14 | 41 | 88 | F | A10 | 52 |
| 57 | D | G14 | 27 | 73 | E | D12 | 38 | 89 | F | B10 | 51 |
| 58 | D | – | – | 74 | E | – | – | 90 | F | – | – |
| 59 | D | F14 | 26 | 75 | E | B15 | 37 | 91 | F | A11 | 50 |
| 60 | D | – | – | 76 | E | – | – | 92 | F | – | – |
| 61 | D | G13 | 24 | 77 | E | D14 | 36 | 93 | F | B11 | 49 |
| 62 | D | G15 | 23 | 78 | E | C15 | 35 | 94 | F | A12 | 48 |
| 63 | D | – | – | 79 | E | – | – | 95 | F | – | – |
| 64 | D | H13 | 22 | 80 | E | E13 | 34 | 96 | F | A13 | 46 |

*Table 12. EPM7192 I/O Pin-Outs (Part 2 of 2)*

| MC | LAB | 160-Pin PGA | 160-Pin QFP | MC | LAB | 160-Pin PGA | 160-Pin QFP | MC | LAB | 160-Pin PGA | 160-Pin QFP |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 97 | G | A8 | 61 | 113 | H | A3 | 76 | 129 | I | E3 | 88 |
| 98 | G | – | – | 114 | H | – | – | 130 | I | – | – |
| 99 | G | B8 | 62 | 115 | H | B4 | 77 | 131 | I | F3 | 90 |
| 100 | G | – | – | 116 | H | – | – | 132 | I | – | – |
| 101 | G | A7 | 63 | 117 | H | B3 | 78 | 133 | I | E2 | 91 |
| 102 | G | A6 | 68 | 118 | H | C3 | 79 | 134 | I | F2 | 92 |
| 103 | G | – | – | 119 | H | – | – | 135 | I | – | – |
| 104 | G | B7 | 69 | 120 | H | B2 | 80 | 136 | I | E1 | 93 |
| 105 | G | A5 | 70 | 121 | H | B1 | 83 | 137 | I | G3 | 94 |
| 106 | G | – | – | 122 | H | – | – | 138 | I | – | – |
| 107 | G | B6 | 71 | 123 | H | C2 | 84 | 139 | I | F1 | 95 |
| 108 | G | – | – | 124 | H | – | – | 140 | I | – | – |
| 109 | G | A4 | 72 | 125 | H | C1 | 85 | 141 | I | G1 | 97 |
| 110 | G | B5 | 73 | 126 | H | D2 | 86 | 142 | I | G2 | 98 |
| 111 | G | – | – | 127 | H | – | – | 143 | I | – | – |
| 112 | G | D4 | 75 | 128 | H | D1 | 87 | 144 | I | H1 | 99 |
| 145 | J | H2 | 100 | 161 | K | L2 | 113 | 177 | L | R3 | 125 |
| 146 | J | – | – | 162 | K | – | – | 178 | L | – | – |
| 147 | J | J1 | 101 | 163 | K | N1 | 114 | 179 | L | R4 | 127 |
| 148 | J | – | – | 164 | K | – | – | 180 | L | – | – |
| 149 | J | H3 | 102 | 165 | K | L3 | 115 | 181 | L | M4 | 128 |
| 150 | J | J3 | 104 | 166 | K | P1 | 116 | 182 | L | R5 | 129 |
| 151 | J | – | – | 167 | K | – | – | 183 | L | – | – |
| 152 | J | K1 | 105 | 168 | K | M2 | 117 | 184 | L | P5 | 130 |
| 153 | J | J2 | 106 | 169 | K | N2 | 119 | 185 | L | R6 | 131 |
| 154 | J | – | – | 170 | K | – | – | 186 | L | – | – |
| 155 | J | K2 | 107 | 171 | K | P2 | 121 | 187 | L | P6 | 132 |
| 156 | J | – | – | 172 | K | – | – | 188 | L | – | – |
| 157 | J | K3 | 108 | 173 | K | N3 | 122 | 189 | L | N6 | 134 |
| 158 | J | L1 | 109 | 174 | K | P3 | 123 | 190 | L | R7 | 135 |
| 159 | J | – | – | 175 | K | – | – | 191 | L | – | – |
| 160 | J | M1 | 112 | 176 | K | P4 | 124 | 192 | L | P7 | 136 |