Enpirion® Power Datasheet

EN23F2QI 15A PowerSoC Voltage Mode Synchronous Buck With Integrated Inductor

Description

The EN23F2QI is a Power System on a Chip (PowerSoC) DC-DC converter. It integrates MOSFET switches, small-signal control circuits, compensation and an integrated inductor in an advanced 12x13x3mm QFN module. It offers high efficiency, excellent line and load regulation. The EN23F2QI operates over a wide input voltage range and is specifically designed to meet the precise voltage and fast transient requirements of high-performance products. The EN23F2QI features frequency synchronization to an external clock, power OK output voltage monitor, programmable soft-start along with thermal shutdown, current limit and over current protection. The device's advanced circuit design, ultra high switching frequency and proprietary integrated inductor technology delivers high-quality, ultra compact, non-isolated DC-DC conversion.

The Altera Enpirion solution significantly helps in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, overall system level reliability is improved given the small number of components required with the Altera Enpirion solution.

All Altera Enpirion products are RoHS compliant, halogen free and are compatible with lead-free manufacturing environments.

Features

- Integrated Inductor, MOSFETs, Controller
- Total Solution Size Estimate 308mm^2
- Wide Input Voltage Range: 4.5V – 13.2V
- 1% Initial Output Voltage Accuracy
- Master/Slave Parallel Operation (up to 4 devices)
- Frequency Synchronization (External Clock)
- Output Enable Pin and Power OK Signal
- Programmable Soft-Start Time
- Pin Compatible with the EN23F0QI
- Under Voltage Lockout Protection (UVLO)
- Over Current and Short Circuit Protection
- Pre-Bias Startup Protection
- Thermal Soft-Shutdown Protection
- RoHS compliant, MSL level 3, 260°C reflow

Applications

- Space Constrained Applications
- Distributed Power Architectures
- Output Voltage Ripple Sensitive Applications
- Beat Frequency Sensitive Applications
- Servers, Embedded Computing Systems, LAN/SAN Adapter Cards, RAID Storage Systems, Industrial Automation, Test and Measurement, and Telecommunications

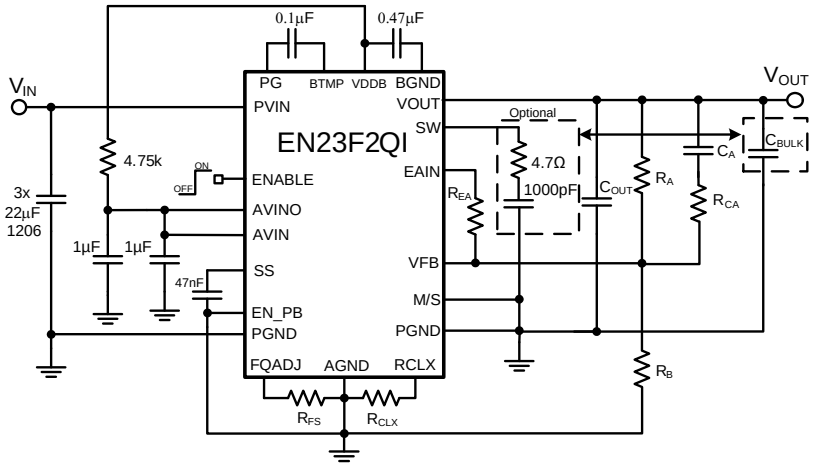


Figure 1. Simplified Application Circuit

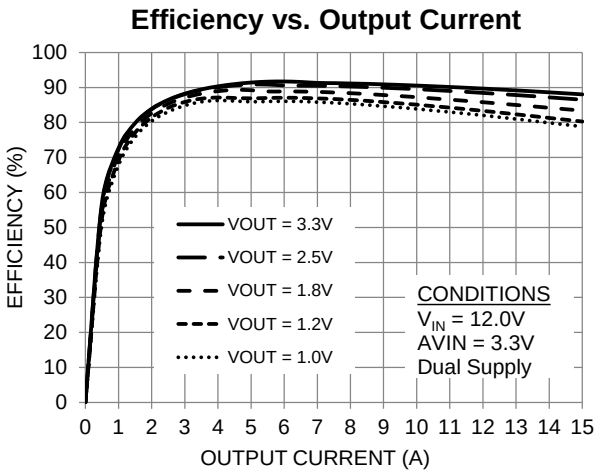


Figure 2. Highest Efficiency in Smallest Solution Size

Ordering Information

Part Number	Package Markings	$T_{AMBIENT}$ Rating (°C)	Package Description
EN23F2QI	EN23F2QI	-40 to +85	92-pin (12mm x 13mm x 3mm) QFN T&R
EVB-EN23F2QI	EN23F2QI	QFN Evaluation Board	

Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

Pin Assignments (Top View)

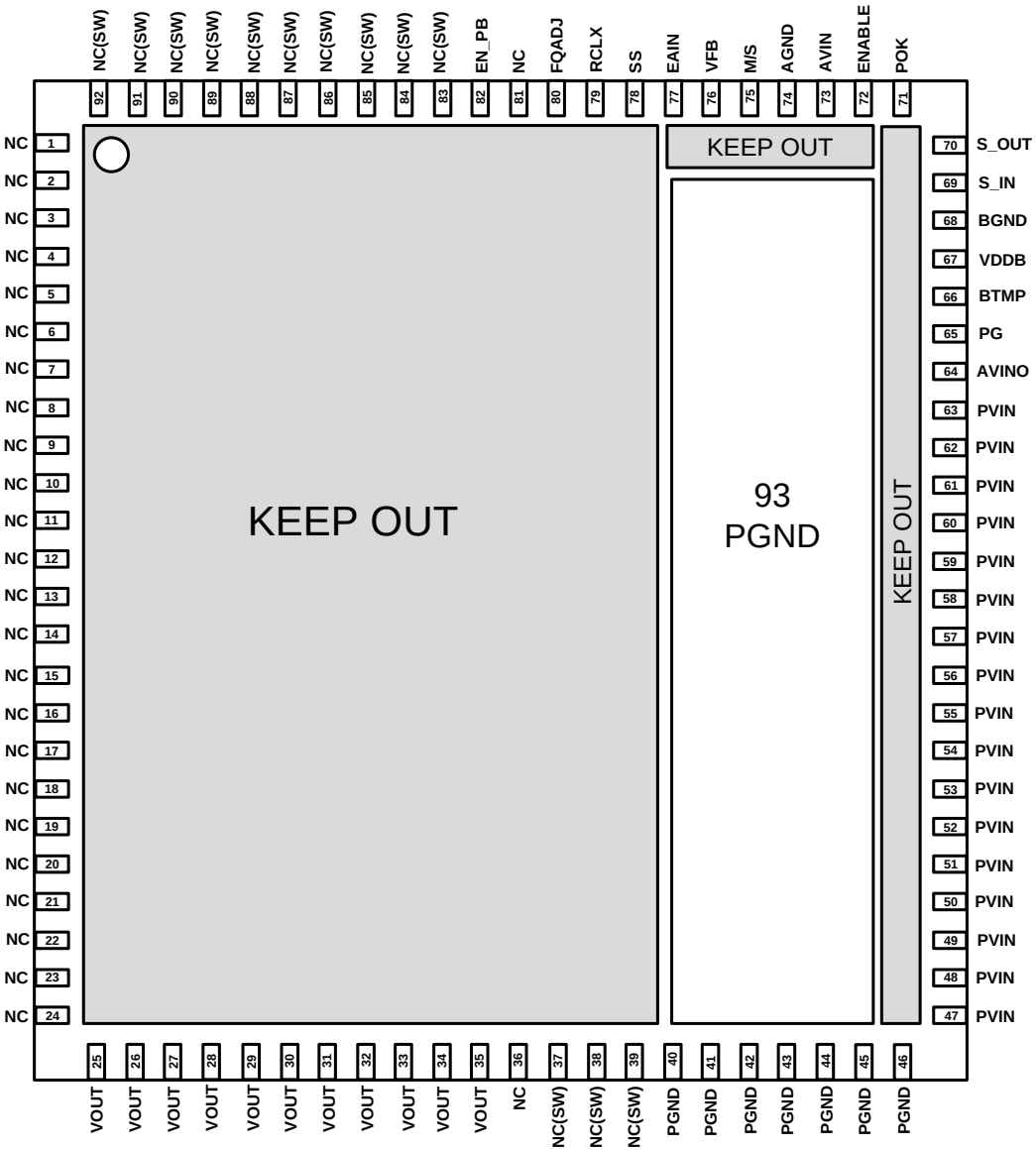


Figure 3: Pin Out Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. All pins including NC pins must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: Shaded area highlights exposed metal below the package that is not to be mechanically or electrically connected to the PCB. Refer to Figure 15 for details.

NOTE C: White 'dot' on top left is pin 1 indicator on top of the device package.

Pin Description

I/O Legend: P=Power G=Ground NC=No Connect I=Input O=Output I/O=Input/Output

PIN	NAME	I/O	FUNCTION
1-24, 36, 81	NC	NC	NO CONNECT – These pins may be internally connected. Do not connect them to each other or to any other electrical signal. Failure to follow this guideline may result in device damage.
25-35	VOUT	O	Regulated converter output. Connect these pins to the load and place output capacitors between these pins and PGND pins 40-43.
37-39, 83-92	NC(SW)	NC	Switching node – These pins are internally connected to the common switching node of the internal MOSFETs. In applications where the total output capacitance exceeds 50% of the maximum allowed, a "snubber" circuit consisting of a series 4.7Ω resistor and a 680pF capacitor should be connected from the NC(SW) pin to the PGND. See Output Capacitor Selection for details.
40-46	PGND	G	Input/output power ground. Connect these pins to the ground electrode of the input and output filter capacitors. See VOUT and PVIN pin descriptions for more details.
47-63	PVIN	P	Input power supply. Connect to input power supply. Decouple with input capacitor to PGND pins 44-46.
64	AVINO	O	Internal 3.4V linear regulator output. Connect this pin to AVIN for applications where operation from a single input voltage (PVIN) is required. If AVINO is being used, place a 1µF, X5R/X7R, capacitor between AVINO and AGND as close as possible to AVINO.
65	PG	I/O	PMOS Gate. Place a 0.1µF, X7R, capacitor between this pin and BTMP.
66	BTMP	I/O	See pin 65 description.
67	VDDB	O	Internal regulated voltage used for the internal control circuitry. Place a 0.47µF, X5R/X7R, capacitor between this pin and BGND.
68	BGND	G	Ground for VDDB. Do not connect BGND to any other ground. See pin 67 description.
69	S_IN	I	Digital synchronization input. This pin accepts either an input clock to phase lock the internal switching frequency or a S_OUT signal from another EN23F2QI. Leave this pin floating if not used.
70	S_OUT	O	Digital synchronization output. PWM signal is output on this pin. Leave this pin floating if not used.
71	POK	O	Power OK is an open drain transistor (pulled up to AVIN or similar voltage) used for power system state indication. POK is logic high when VOUT is within -10% of VOUT nominal. Leave this pin floating if not used.
72	ENABLE	I	Output enable. Applying a logic high to this pin enables the output and initiates a soft-start. Applying a logic low disables the output. ENABLE logic cannot be higher than AVIN (refer to Absolute Maximum Ratings). Do not leave floating. See Power Up/Down Sequencing section for details.
73	AVIN	P	3.4V Input power supply for the controller. Place a 1µF, X5R/X7R, capacitor between AVIN and AGND.
74	AGND	G	Analog ground. This is the ground return for the controller. All AGND pins need to be connected to a quiet ground.
75	M/S	I	A logic level low configures the device as Master and a logic level high configures the device as a Slave. Connect to ground in standalone mode.
76	VFB	I/O	External feedback input. The feedback loop is closed through this pin. A voltage divider at VOUT is used to set the output voltage. The mid-point of the divider is connected to VFB. A phase lead network from this pin to VOUT is also required to stabilize the loop.
77	EAIN	I	Optional error amplifier input. Allows for customization of the control loop for performance optimization. Leave this pin floating if not used.
78	SS	I/O	Soft-start node. The soft-start capacitor is connected between this pin and AGND. The value of this capacitor determines the startup time. See Soft-Start Operation in the Functional Description section for details.
79	RCLX	I/O	Over-current protection setting. Placement of a resistor on this pin will adjust the over-current protection threshold. See Table 2 for the recommended RCLX Value to set OCP at the nominal value specified in the Electrical Characteristics table.
80	FQADJ	I/O	Adding a resistor (R_{FS}) to this pin will adjust the switching frequency of the EN23F2QI. See Table 1 for suggested resistor values on R_{FS} for various PVIN/VOUT combinations to maximize efficiency. Do not leave this pin floating.

PIN	NAME	I/O	FUNCTION
82	EN_PB	I	Enable pre-bias protection. Connect EN_PB directly to AVIN to enable the Pre-Bias Protection feature. Pull EN_PB directly to ground to disable the feature. Do not leave this pin floating. See Pre-Bias Operation for details.
93	PGND	G	Not a perimeter pin. Device thermal pad to be connected to the system GND plane for heat-sinking purposes. See Layout Recommendations

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Pin Voltages – PVIN, VOUT, PG		-0.5	15	V
Pin Voltages – ENABLE, S_IN, M/S, POK, EN_PB		-0.5	AV_{IN} + 0.3	V
Pin Voltages – AVINO, AVIN, ENABLE, S_IN, S_OUT, M/S		-0.5	6.0	V
Pin Voltages – VFB, SS, EAIN, RCLX, FQADJ, VDDB, BTMP		-0.5	2.75	V
Dual Supply PVIN Rising and Falling Slew Rate (Note 1)			25	V/ms
Single Supply PVIN Rising and Falling Slew Rate (Note 1, 2)			10	V/ms
Storage Temperature Range	T_{STG}	-65	150	°C
Maximum Operating Junction Temperature	$T_{J\text{-}ABS\ Max}$		150	°C
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A			260	°C
ESD Rating (based on Human Body Model)			2000	V
ESD Rating (based on CDM)			500	V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	PVIN	4.5	13.2	V
AVIN: Controller Supply Voltage	AVIN	2.5	5.5	V
Output Voltage Range (Note 3)	V_{OUT}	0.75	3.3	V
Output Current (Note 4)	I_{OUT}	0	15	A
Operating Ambient Temperature	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNITS
Thermal Shutdown	T_{SD}	150	°C
Thermal Shutdown Hysteresis	T_{SDH}	35	°C
Thermal Resistance: Junction to Ambient (0 LFM) (Note 4)	θ_{JA}	13	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	1	°C/W

Note 1: PVIN rising and falling slew rates cannot be outside of specification. PVIN should rise monotonically into regulation. Filter PVIN with proper input bulk capacitance so that the input AC ripple in regulation is less than ±1V of the regulation voltage. See Input Capacitor Selection for details.

Note 2: For accurate power up sequencing, use a fast ENABLE logic (>3V/100µs) after both AVIN and PVIN are high. Tying ENABLE to AVIN may result in a startup delay due to a slow ENABLE logic.

Note 3: Dropout: Maximum $V_{OUT} \leq V_{IN}$ - 2.5V

Note 4: Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

Electrical Characteristics

NOTE: V_{IN}=12V, Minimum and Maximum values are over operating ambient temperature range unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	PVIN		4.5		13.2	V
Controller Input Voltage	AVIN		3		5.5	V
AVIN Under Voltage Lock-out rising	$AVIN_{UVLOR}$	Voltage above which UVLO is not asserted	2.5	2.75	3	V
AVIN Under Voltage Lock-out falling	$AVIN_{OVLOF}$	Voltage below which UVLO is asserted	2.1	2.35	2.6	V
AVIN UVLO Hysteresis	$AVIN_{HYS}$			400		mV
AVIN Pin Input Current	I_{AVIN}			14		mA
Internal LDO Output	AVINO			3.4		V
Shut-Down Supply Current	$IPVIN_S$	PVIN=12V, AVIN=3.4V, ENABLE=0V		1		mA
	$IAVIN_S$	PVIN=12V, AVIN=3.4V, ENABLE=0V		75		µA
Feedback Pin Voltage	V_{FB}	Feedback node voltage at: PVIN = 12V, ILOAD = 0, T_A = 25°C	0.594	0.60	0.606	V
Feedback Pin Voltage	V_{FB}	Feedback node voltage at: 4.5V ≤ PVIN ≤ 13.2V 0A ≤ I_{LOAD} ≤ 15A, T_A = -40 to 85°C	0.588	0.60	0.612	V
Feedback Pin Input Leakage Current	I_{FB}	VFB pin input leakage current (Note 5)	-5		5	nA
V_{OUT} Rise Time	t_{RISE}	C_{SS} = 47nF (Note 5, Note 6 and Note 7)	1.96	2.8	3.64	ms
Soft Start Capacitor Range	C_{SS_RANGE}	Note 5	10	47	68	nF
Output Capacitance Range	C_{OUT}	V_{IN} = 12V V_{OUT} = 3.3V; R_{FS} = 22kΩ See Table 3 for other output voltages (Note 5)	80	200	800	µF
		V_{IN} = 12V V_{OUT} ≤ 1.0V; R_{FS} = 3.01kΩ See Table 3 for other output voltages (Note 5)	80	200	2200	µF
Continuous Output Current	$I_{OUT\_MAX\_CONT}$	Subject to thermal derating	0		15	A
OCP Trip Point	I_{OCP}	V_{IN} = 12V	15.2	20		A
Short Circuit Average Input Current	I_{IN_OCP}	Short = 10mΩ (Note 8)		100		mA
ENABLE Logic High	V_{ENABLE_HIGH}	4.5V ≤ V_{IN} ≤ 13.2V;	1.25		AV_{IN}	V
ENABLE Logic Low	V_{ENABLE_LOW}	4.5V ≤ V_{IN} ≤ 13.2V;	0		0.95	V
ENABLE Hysteresis	EN_{HYS}			200		mV
ENABLE Lockout Time	$T_{ENLOCKOUT}$	fsw = 1MHz (Note 5)		8		ms
ENABLE Pin Input Current	I_{ENABLE}	AVIN = 5.5V ENABLE = 1.8V; ENABLE = 3.4V; ENABLE = 5.5V;		5 11 23	8 18 32	µA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Switching Frequency	F_{SW}	R_{FS} =3.01kΩ		1.0		MHz
External SYNC Clock Frequency Lock Range	F_{PLL_LOCK}	Range of SYNC clock frequency (See Table 1)	0.9		1.8	MHz
S_IN Threshold – Low	$V_{S\_IN\_LO}$	S_IN Clock Logic Low Level (Note 5)			0.8	V
S_IN Threshold – High	$V_{S\_IN\_HI}$	S_IN Clock Logic High Level (Note 5)	1.8		2.5	V
S_OUT Threshold – Low	$V_{S\_OUT\_LO}$	S_OUT Clock Logic Low Level (Note 5)			0.8	V
S_OUT Threshold – High	$V_{S\_OUT\_HI}$	S_OUT Clock Logic High Level (Note 5)	1.8		2.5	V
POK Lower Threshold	POK_{LT}	Percentage of Nominal Output Voltage for POK to be Low		90		%
POK Output Low Voltage	V_{POKL}	With 4mA Current Sink into POK			0.4	V
POK Output Hi Voltage	V_{POKH}	PVIN range: 4.5V ≤ PVIN ≤ 15V			AVIN	V
POK pin V_{OH} leakage current	I_{POKL}	POK High (Note 5)			1	µA
M/S Pin Logic Low	V_{T-LOW}	Tie Pin to GND (Master Mode)			0.8	V
M/S Pin Logic High	V_{T-HIGH}	Pull up to AVIN Through an External Resistor REXT (Slave Mode)	1.8			V
M/S Pin Input Current	$I_{M/S}$	REXT = 15kΩ; AVIN = 3.4V; AVIN = 5.5V;		65 175		µA

Note 5: Parameter not production tested but is guaranteed by design.

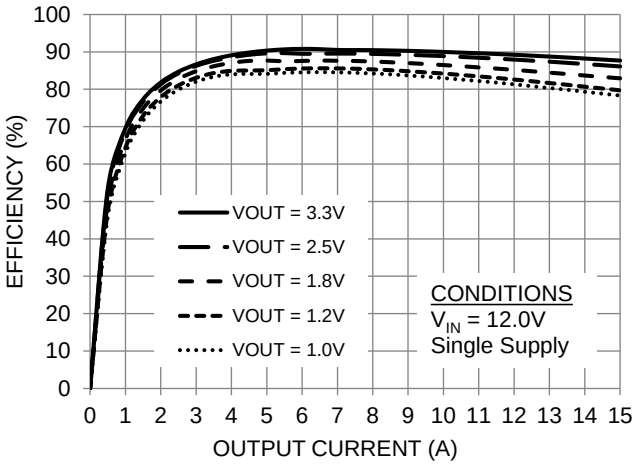
Note 6: Rise time calculation begins when AVIN > V_{UVLO} and ENABLE = HIGH.

Note 7: V_{OUT} Rise Time Accuracy does not include soft-start capacitor tolerance.

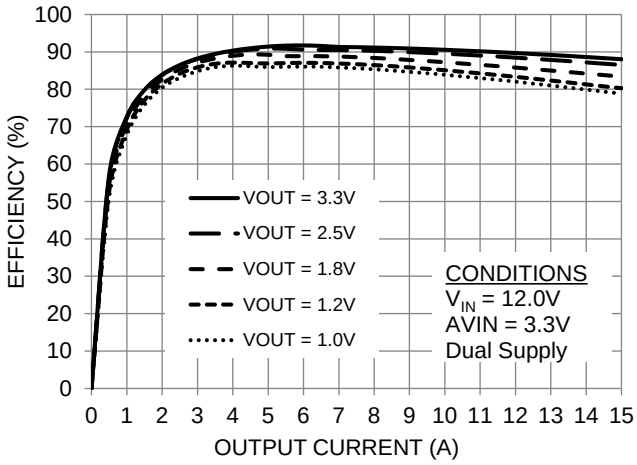
Note 8: Output short circuit condition was performed with load impedance that is greater than or equal to 10mΩ.

Typical Performance Curves

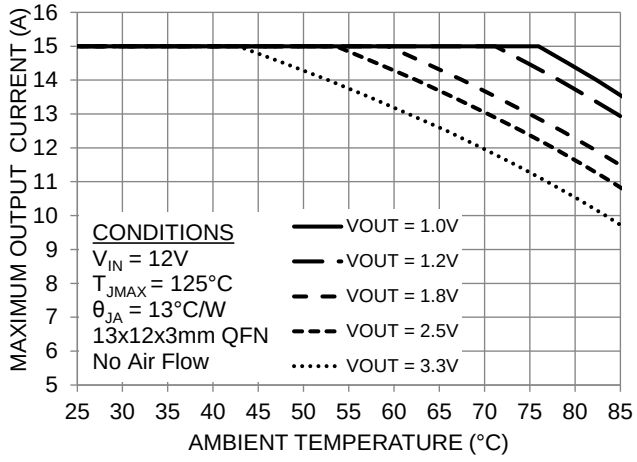
Efficiency vs. Output Current



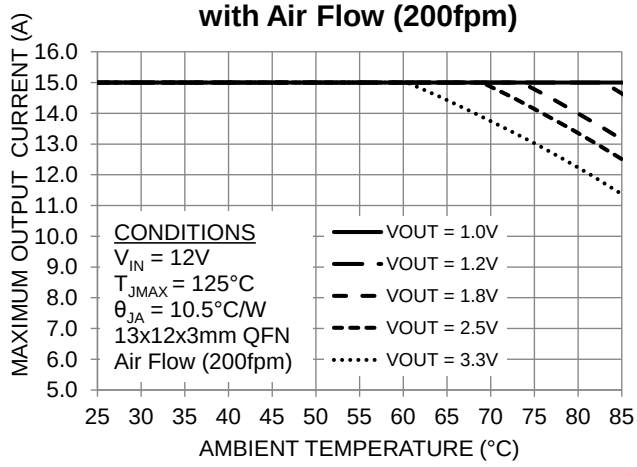
Efficiency vs. Output Current



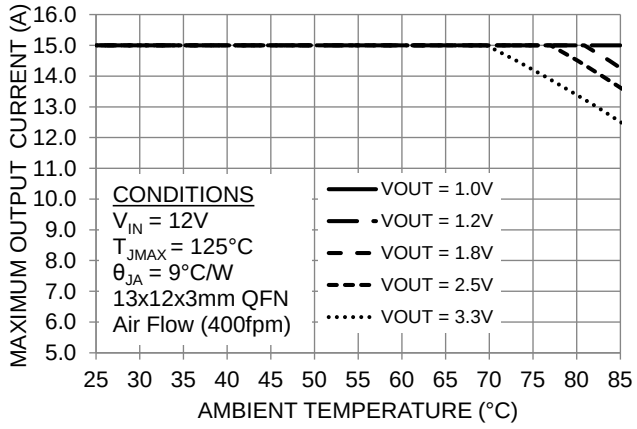
Output Current De-rating



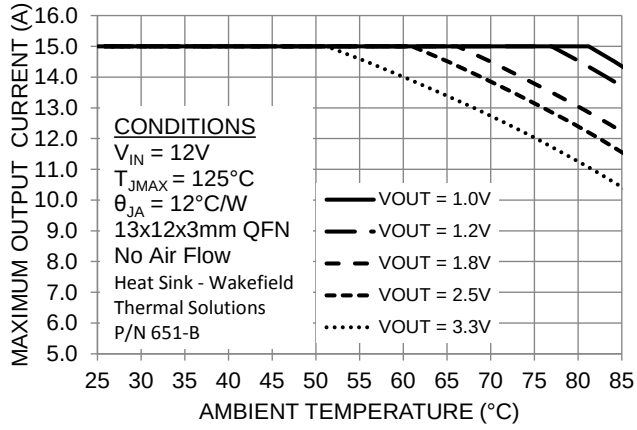
Output Current De-rating with Air Flow (200fpm)



Output Current De-rating with Air Flow (400fpm)

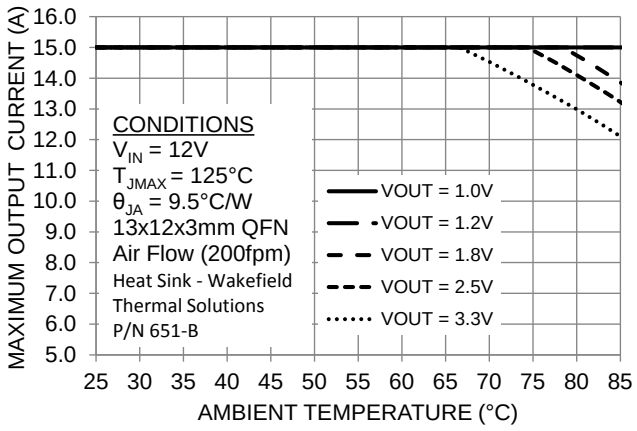


Output Current De-rating with Heat Sink

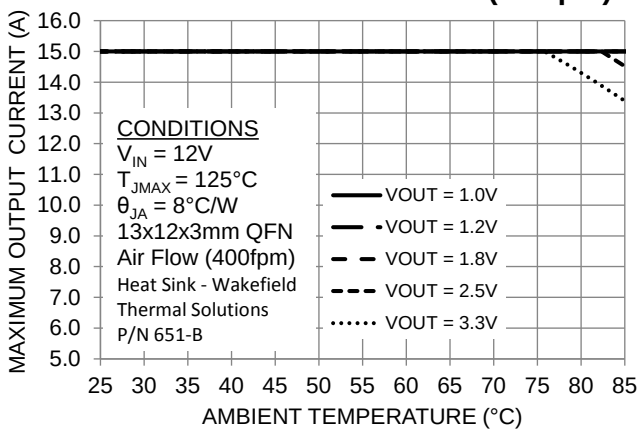


Typical Performance Curves

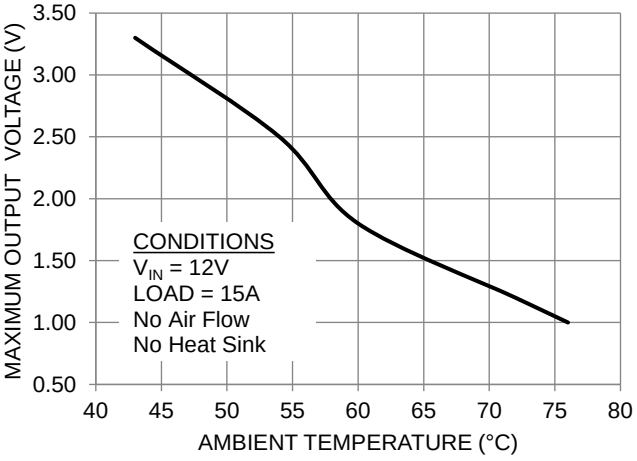
Output Current De-rating w/ Heat Sink and Air Flow (200fpm)



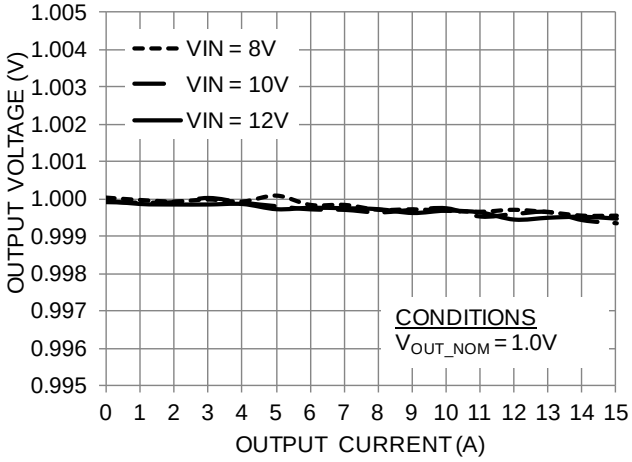
Output Current De-rating w/ Heat Sink and Air Flow (400fpm)



Max V_{OUT} at 15A vs. Temperature



Output Voltage vs. Output Current



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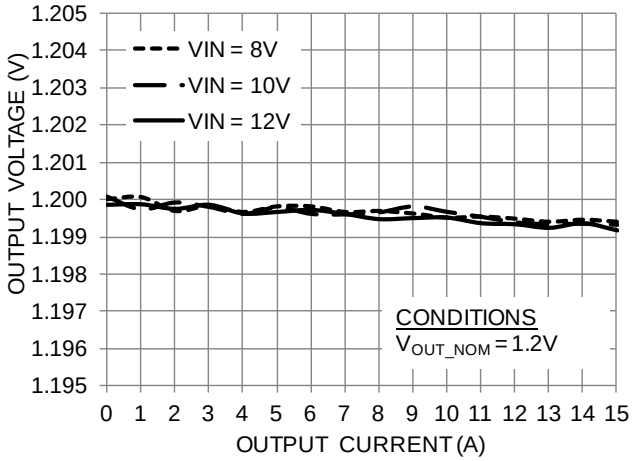

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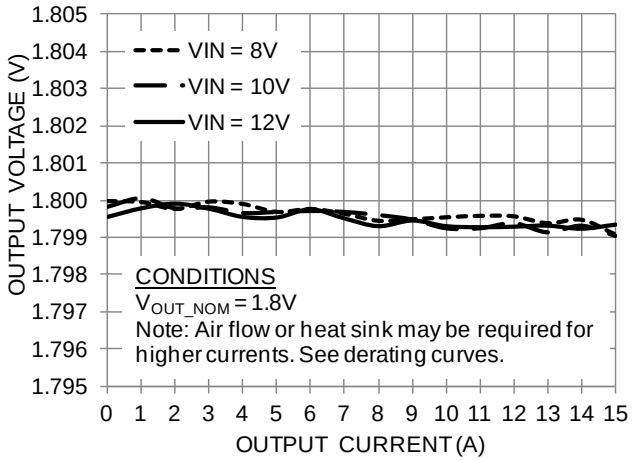
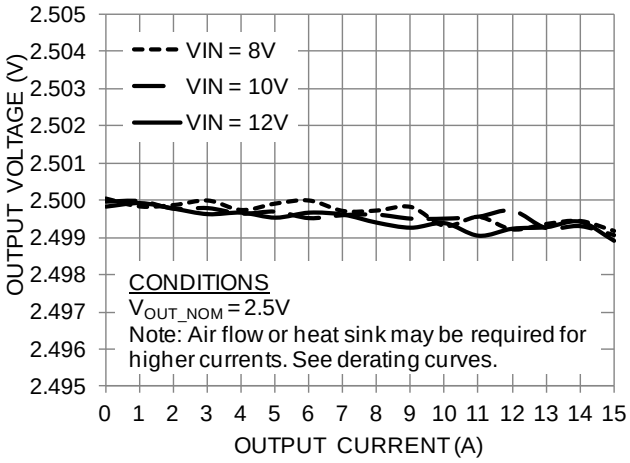
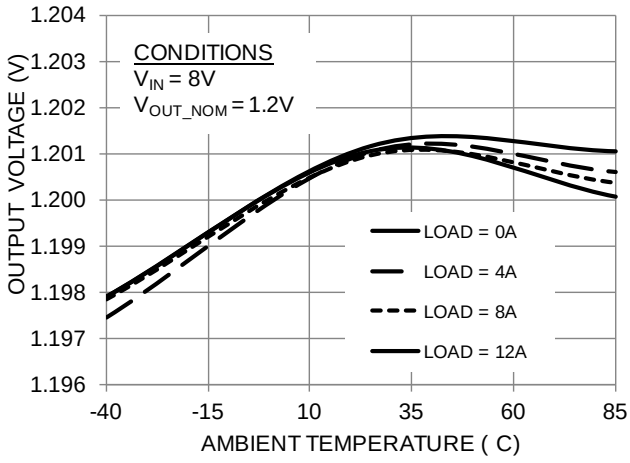


Typical Performance Curves

Output Voltage vs. Output Current



Output Voltage vs. Temperature



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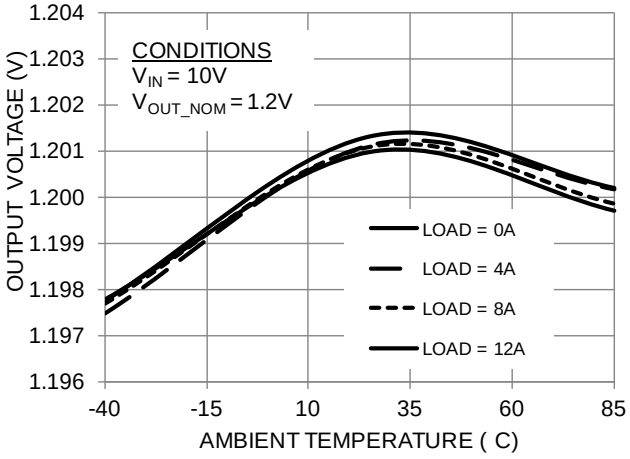

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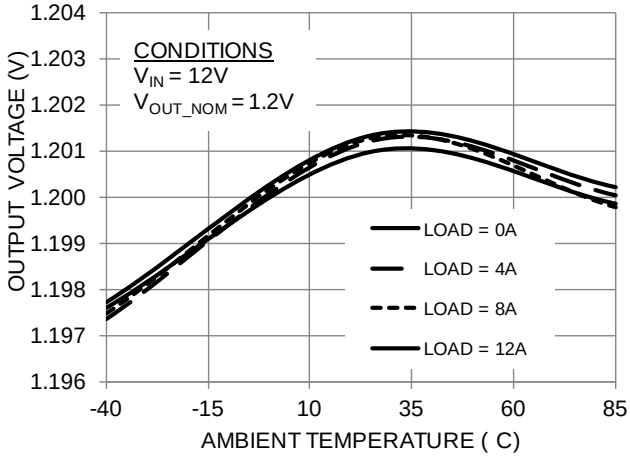
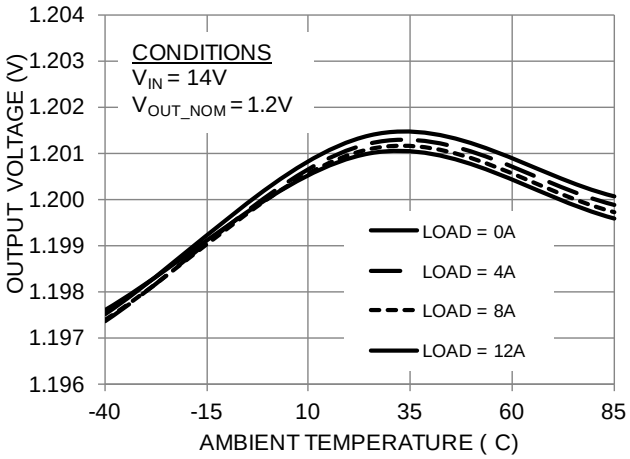
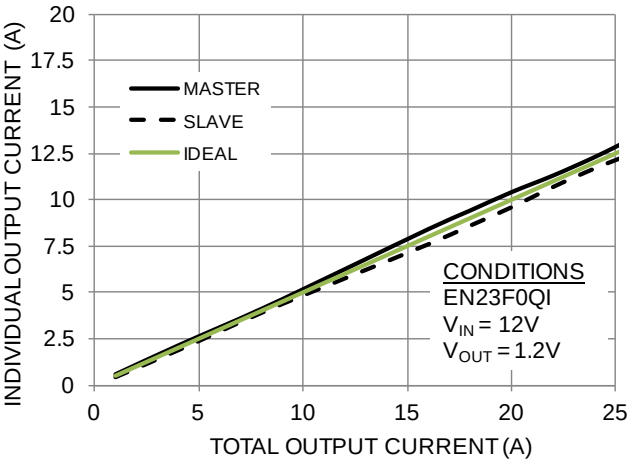


Output Voltage vs. Temperature

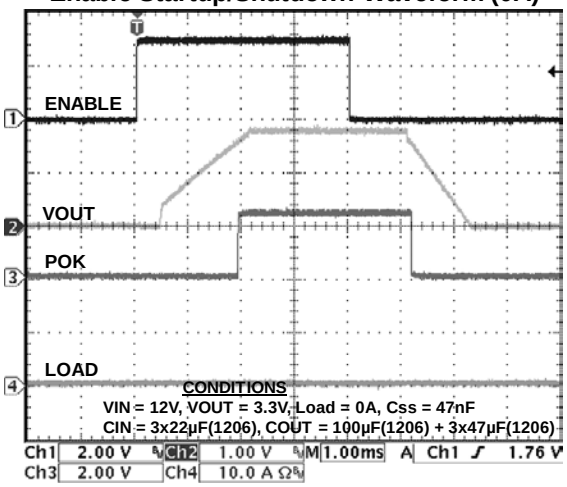


Parallel Current Share Breakdown

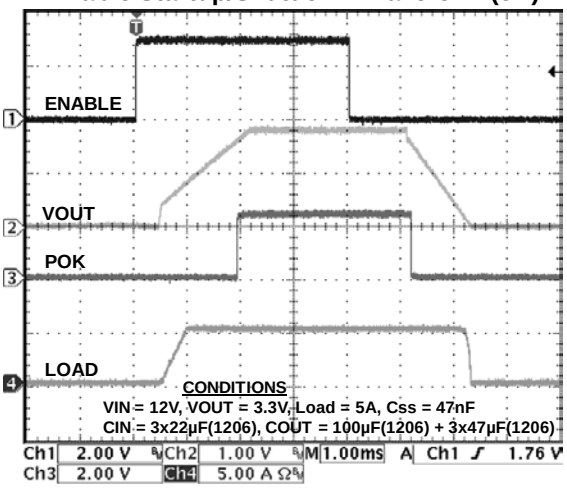


Typical Performance Characteristics

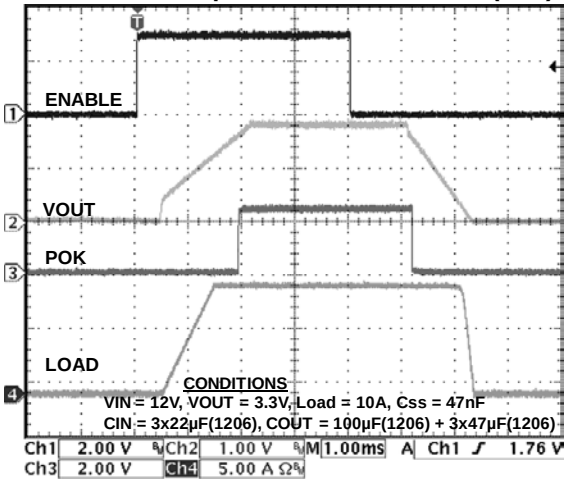
Enable Startup/Shutdown Waveform (0A)



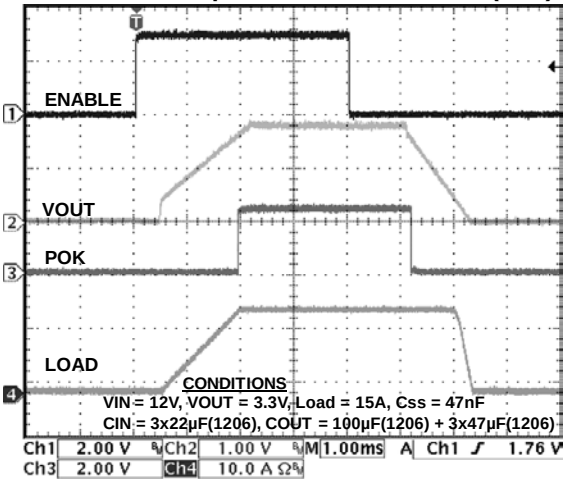
Enable Startup/Shutdown Waveform (5A)



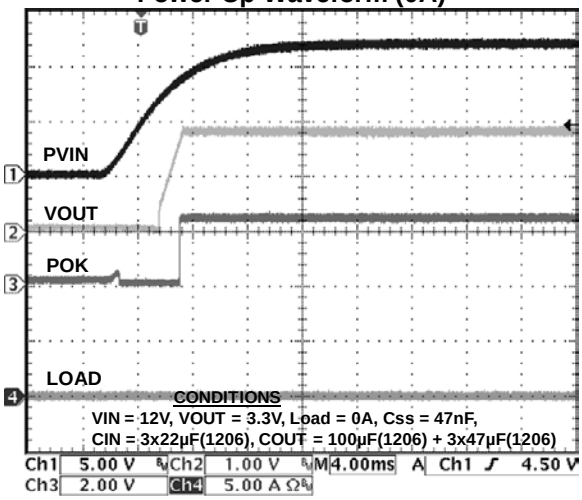
Enable Startup/Shutdown Waveform (10A)



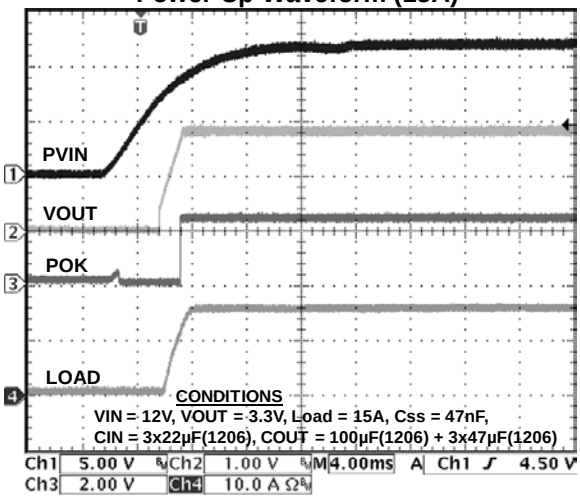
Enable Startup/Shutdown Waveform (15A)



Power Up Waveform (0A)

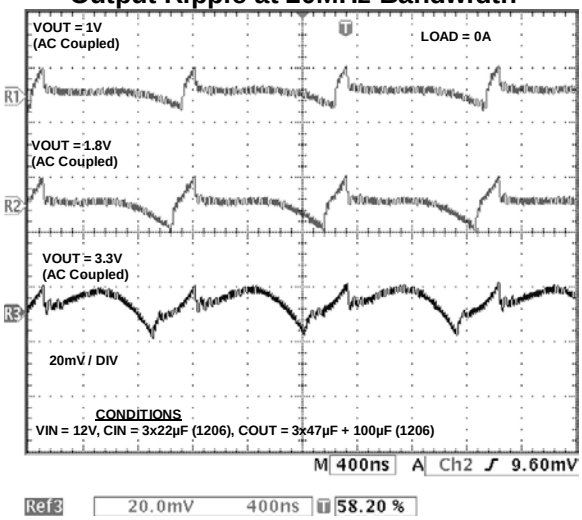


Power Up Waveform (15A)

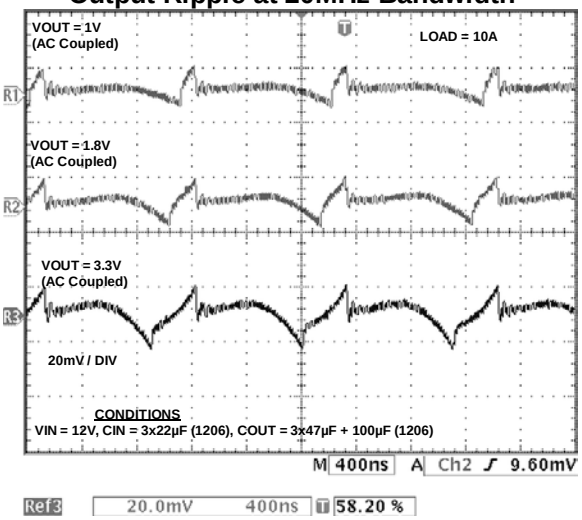


Typical Performance Characteristics

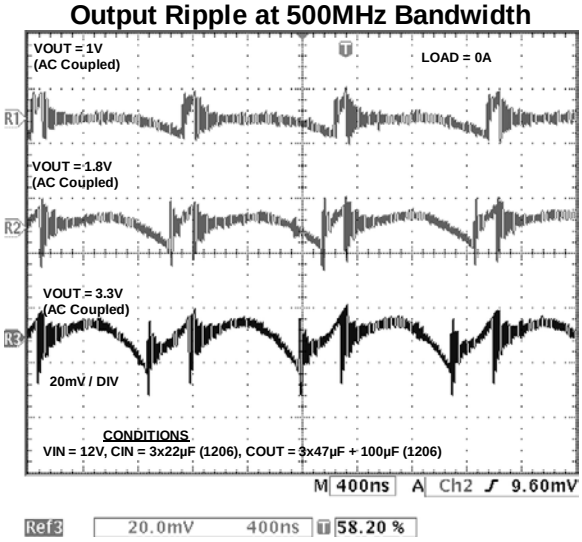
Output Ripple at 20MHz Bandwidth



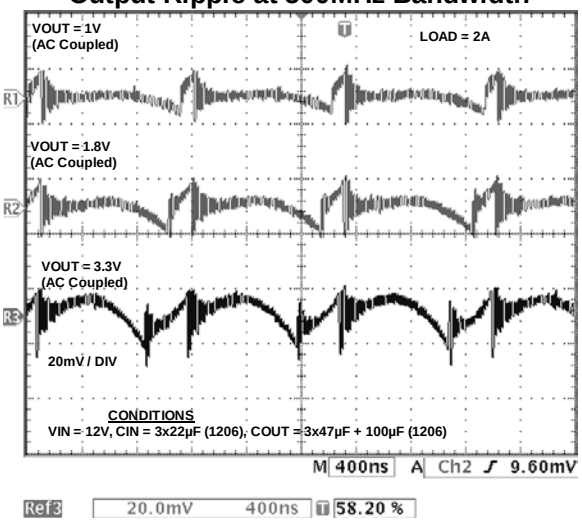
Output Ripple at 20MHz Bandwidth



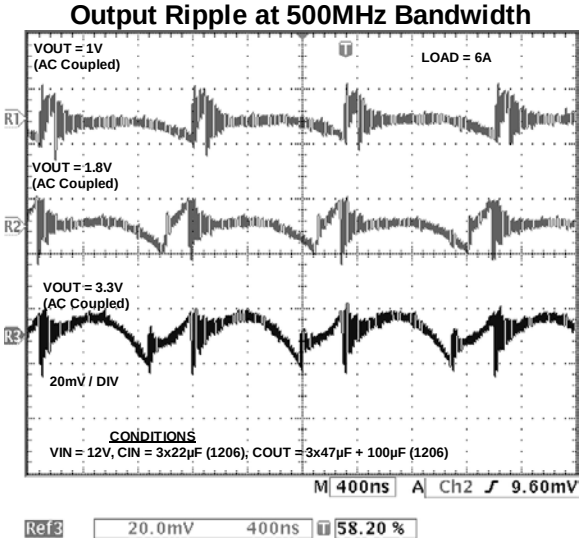
Output Ripple at 500MHz Bandwidth



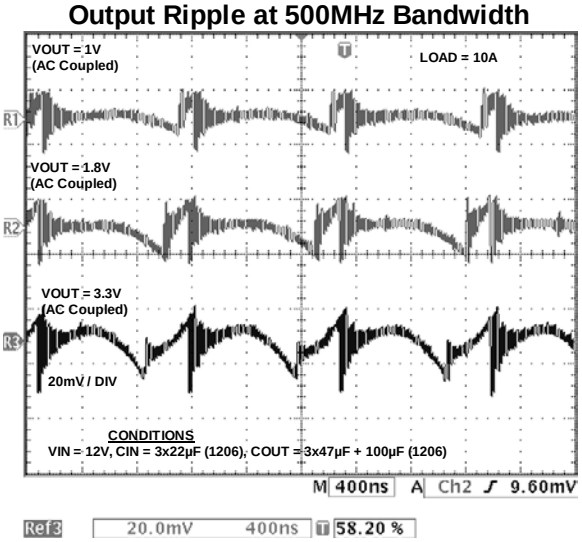
Output Ripple at 500MHz Bandwidth



Output Ripple at 500MHz Bandwidth

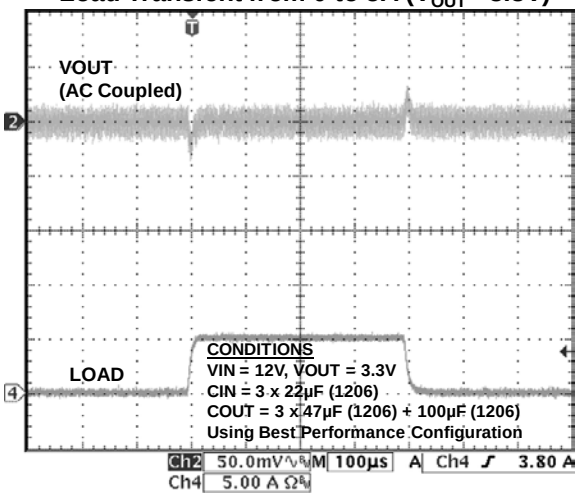


Output Ripple at 500MHz Bandwidth

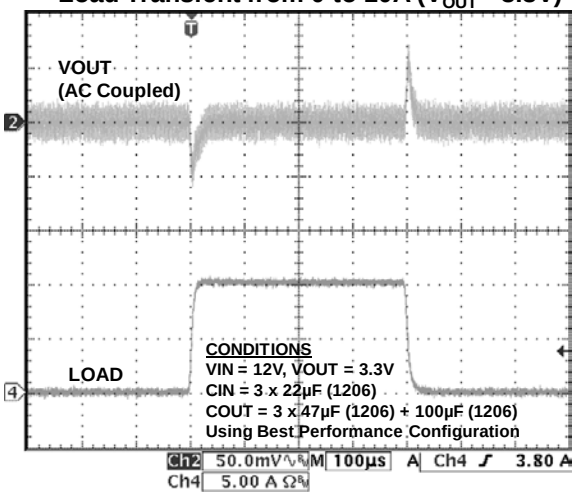


Typical Performance Characteristics

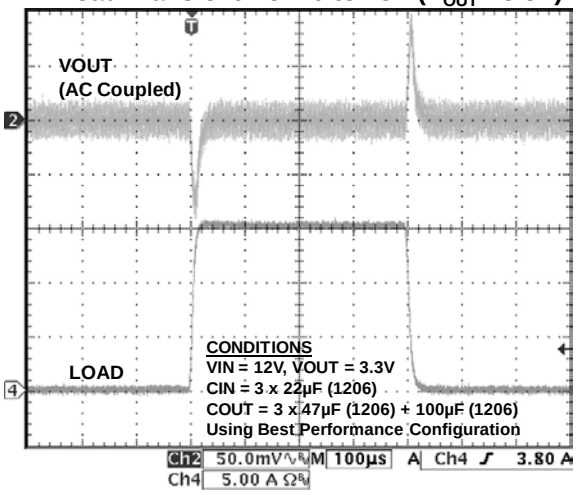
Load Transient from 0 to 5A (V_{OUT} =3.3V)



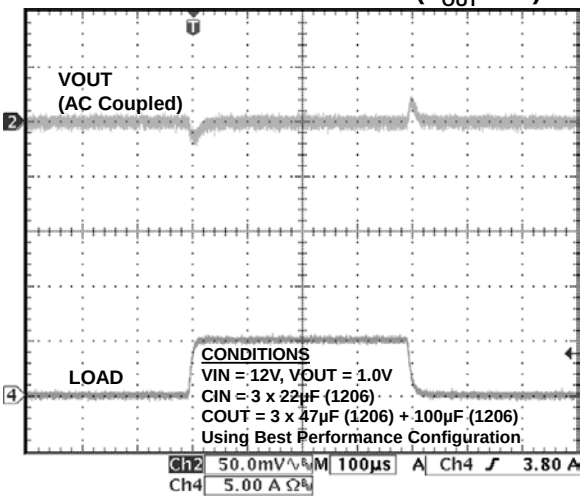
Load Transient from 0 to 10A (V_{OUT} =3.3V)



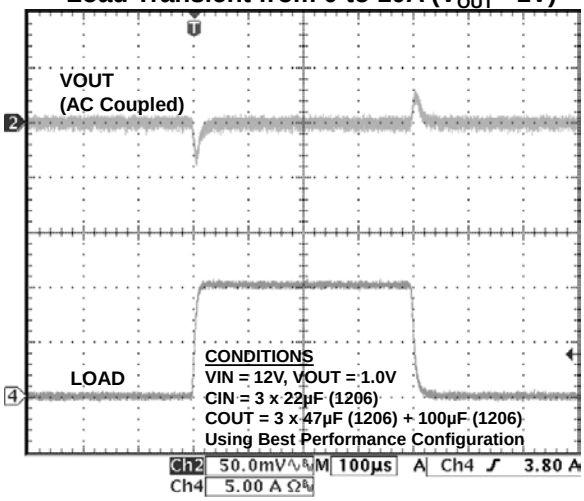
Load Transient from 0 to 15A (V_{OUT} =3.3V)



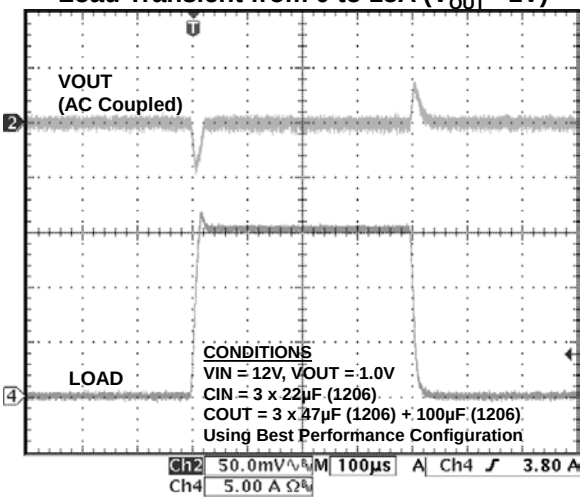
Load Transient from 0 to 5A (V_{OUT} =1V)



Load Transient from 0 to 10A (V_{OUT} =1V)

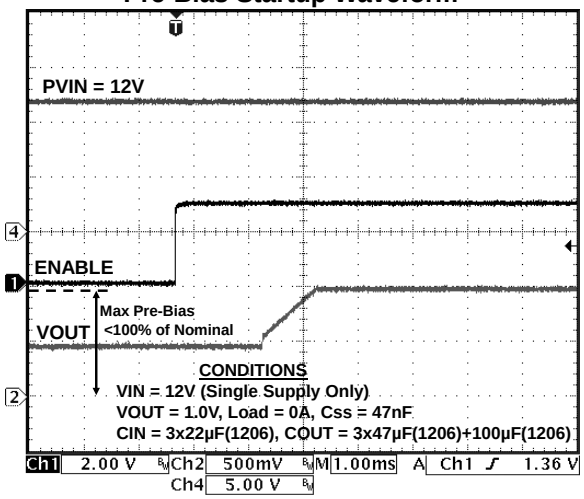


Load Transient from 0 to 15A (V_{OUT} =1V)

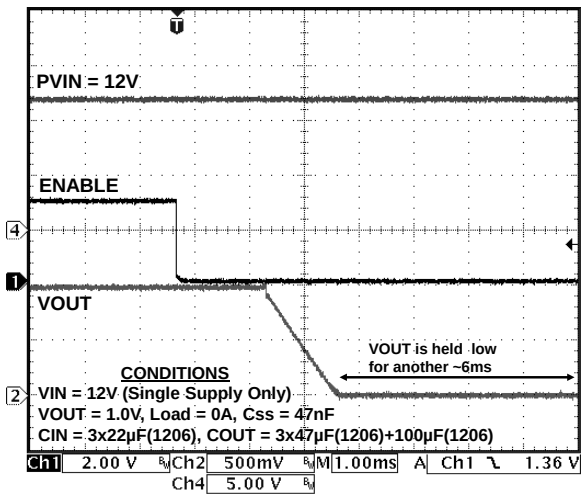


Typical Performance Characteristics

Pre-Bias Startup Waveform



Pre-Bias Shutdown Waveform



Functional Block Diagram

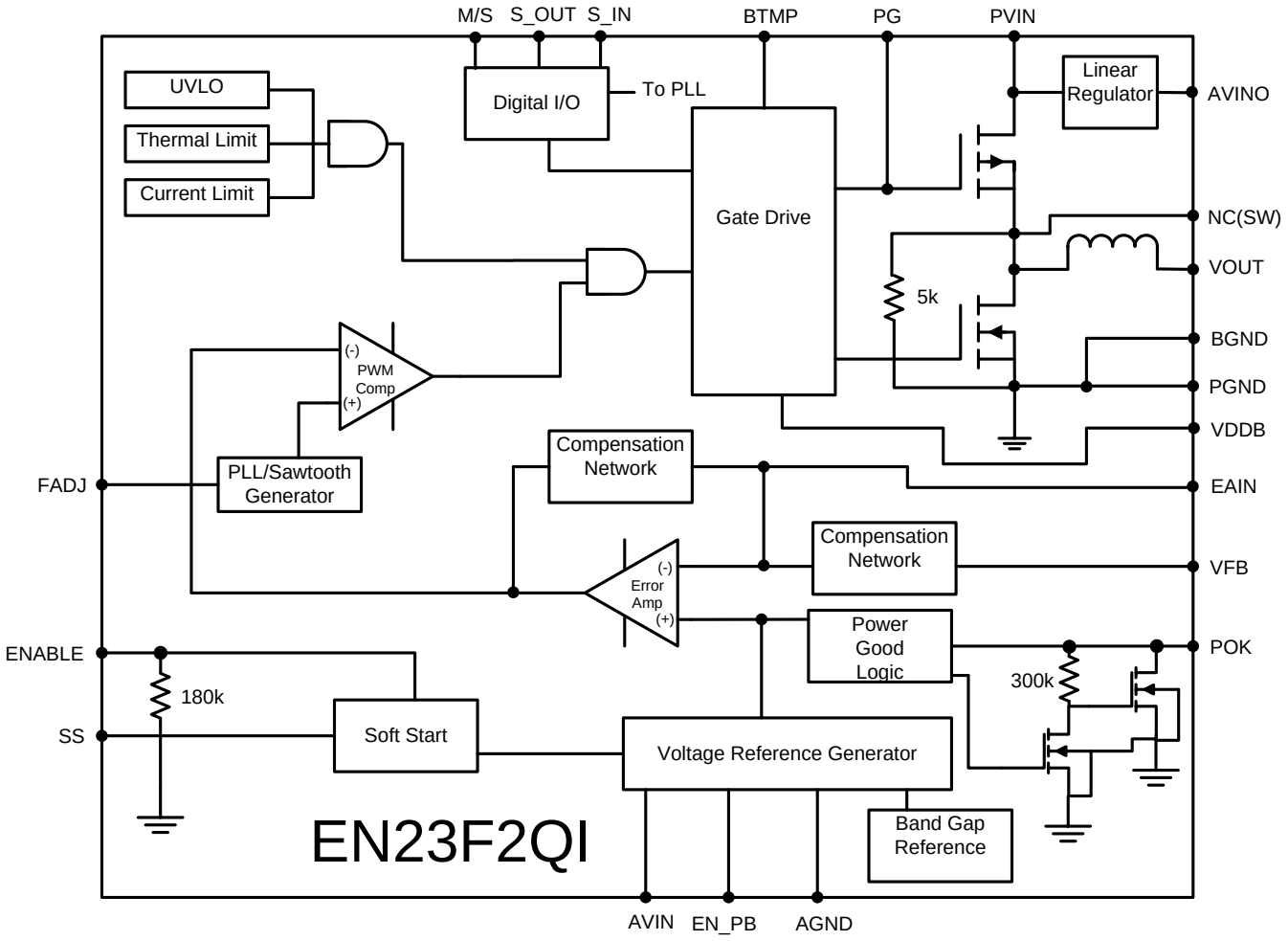


Figure 4: Functional Block Diagram

Functional Description

Synchronous Buck Converter

The EN23F2QI is a highly integrated synchronous, buck converter with integrated controller, power MOSFET switches and integrated inductor. The nominal input voltage (PVIN) range is 4.5V to 13.2V and can support up to 15A of continuous output current. The output voltage is programmed using an external resistor divider network. The control loop utilizes a Type IV Voltage-Mode compensation network and maximizes on a low-noise PWM topology. Much of the compensation circuitry is internal to the device. However, a phase lead capacitor is required along with the output voltage feedback resistor divider to complete the Type IV compensation network. The high switching frequency of the EN23F2QI enables the use of small size input and output filter capacitors, as well as a wide loop bandwidth within a small foot print.

Protection Features:

The power supply has the following protection features:

- Over Current and Short Circuit Protection
- Thermal Soft-Shutdown with Hysteresis
- Under-Voltage Lockout Protection
- Pre-Bias Protection

Additional Features:

- Switching Frequency Synchronization
- Programmable Soft-Start
- Power OK Output Monitoring

Modes of Operation

The EN23F2QI is designed to be powered by either a single input supply (PVIN) or two separate supplies: one for PVIN and the other for AVIN. The EN23F2QI is not "hot pluggable." Refer to the PVIN Slew Rate specification on page 4.

Single Input Supply Application (PVIN Only):

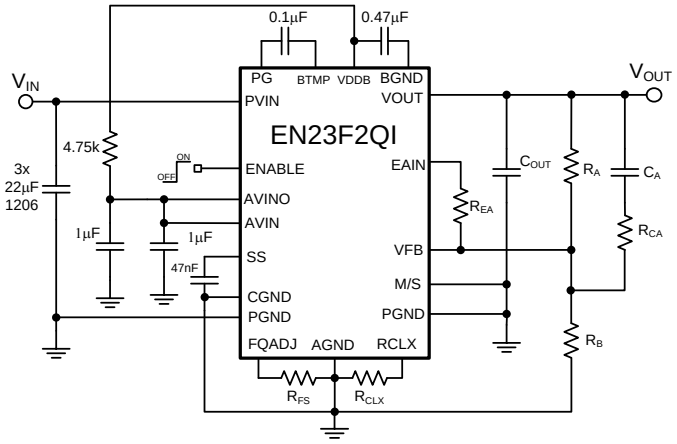


Figure 5: Single Input Supply Schematic

In single input supply mode, the EN23F2QI only requires one input voltage rail (typically 12V). The EN23F2QI has an internal linear regulator that converts PVIN to 3.4V. The output of the linear regulator is provided on the AVINO pin once the device is enabled. AVINO should be connected to AVIN. Also, in this single supply application, place a resistor (R_{VB}) between VDDB and AVIN, as shown in Figure 5. Altera recommends R_{VB}=4.75kΩ.

Dual Input Supply Application (PVIN and AVIN):

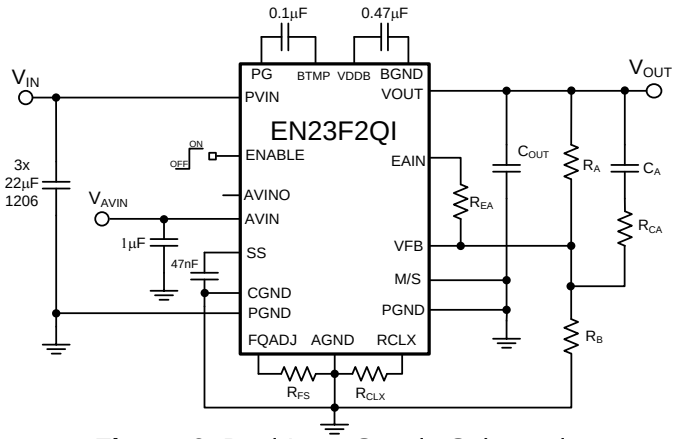


Figure 6: Dual Input Supply Schematic

In dual input supply mode, two input voltage rails are required (typically 12V for PVIN and 3.4V for AVIN). Refer to Figure 6 for the recommended schematic for a dual input supply application. Since AVINO is not used, it can be left open.

ENABLE Operation

The ENABLE pin provides a means to enable normal operation or to shut down the device. A logic high will enable the converter into normal operation. When the ENABLE pin is asserted (high) the device will undergo a normal soft-start. A logic low will disable the converter. A logic low will power down the device in a controlled manner and the device is subsequently shut down. The ENABLE signal has to be low for at least the ENABLE Lockout Time (8ms) in order for the device to be re-enabled. To ensure accurate startup sequencing the ENABLE/DISABLE signal should be faster than 3V/100µs. A slower ENABLE/DISABLE signal may result in a delayed startup and shutdown response. Do not leave ENABLE floating.

Pre-Bias Operation

The EN23F2QI has a Pre-Bias feature which will allow the regulator to startup into a pre-charged output. The pre-biased output voltage must be below the nominal regulation voltage; otherwise, damage may occur during startup and shutdown. To use this feature, the EN23F2QI must be configured to Single Supply mode, set to standalone operation (no parallel operation) and follow the instructions below:

- The EN_PB pin must be pulled high to AVIN
- A resistor divider must be connected from PVIN to ENABLE to Ground (10k on top, 2.26k on the bottom) to ensure proper shutdown. The resistor divider will disable the device when PVIN falls below approximately 6.8V. The resistor divider values may be adjusted accordingly to meet PVIN requirements. See Figure X.
- PVIN rail should be in regulation (>4.5V) prior to being enabled.
- Since the ENABLE pin is tied to the resistor divider to PVIN, an open drain (such as the POK signal of another regulator or Sequencer) should be tied to ENABLE in order to keep the device disabled while the PVIN rail rises into regulation.
- Once the PVIN rail is in regulation, the ENABLE may be pulled high through the resistor divider.
- The ENABLE rise time must be faster than 3V/100us.

The output will start up from the Pre-Bias voltage into regulation monotonically if the instructions are followed; otherwise, the Pre-Bias Protection feature may not function properly and the device will startup into a Pre-Bias output voltage. Starting up into a Pre-Bias voltage without the Pre-Bias Protection feature enabled can lead to device

damage. When using the Pre-Bias feature, the device must be disabled using the ENABLE pin prior to PVIN falling out of regulation (<4.5V), otherwise damage may occur during shutdown. To disable the Pre-Bias feature pull the EN_PB pin directly to ground. Do not leave the EN_PB pin floating. See Typical Performance Characteristics for an example of Pre-Bias Protection. See Figure X for a typical schematic with Pre-Bias Protection enabled.

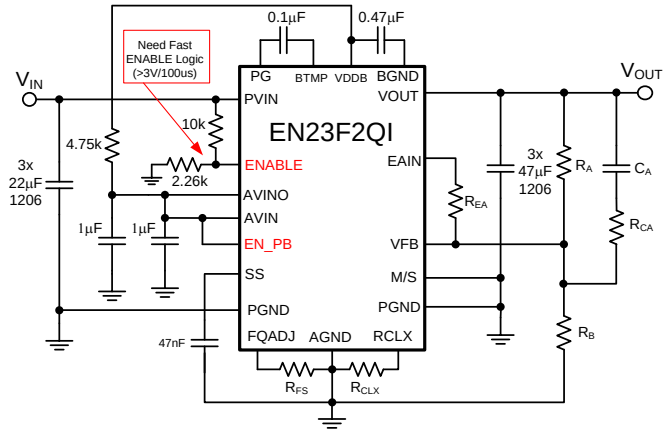


Figure X. Pre-Bias Application Circuit

Frequency Synchronization

The switching frequency of the EN23F2QI can be phase-locked to an external clock source to move unwanted beat frequencies out of band. The internal switching clock of the EN23F2QI can be phase locked to a clock signal applied to the S_IN pin. An activity detector recognizes the presence of an external clock signal and automatically phase-locks the internal oscillator to this external clock. Phase-lock will occur as long as the input clock frequency is in the range of 0.9MHz to 1.8MHz. The external clock frequency must be within ±10% of the nominal switching frequency set by the R_{FS} resistor. It is recommended to use a synchronized clock frequency close to the typical frequency recommendations in Table 1. A 3.01kΩ resistor from FQADJ to ground is recommended for clock frequencies within ±10% of 1MHz. When no clock is present, the device reverts to the free running frequency of the internal oscillator set by the R_{FS} resistor.

The efficiency performance of the EN23F2QI for various PVIN/VOUT combinations can be optimized by adjusting the switching frequency. Table 1 shows recommended R_{FS} values for various PVIN/VOUT combinations in order to optimize performance of the EN23F2QI. Using higher R_{FS} resistor values are allowed. Do not use lower R_{FS} values than recommendations as that may set the frequency too low and cause inductor saturation. When synchronizing multiple devices, use the highest recommended switching frequency of the devices.

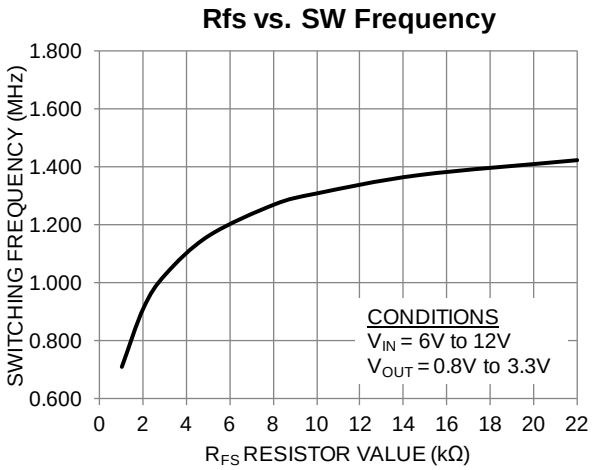


Figure 7. R_{FS} versus Switching Frequency

PVIN	VOUT	R_{FS}	Typical fsw
12V	3.3V	22k	1.42 MHz
	2.5V	10k	1.3 MHz
	1.8V	4.87k	1.15 MHz
	1.5V	3.01k	1.0 MHz
	1.2V	3.01k	1.0 MHz
	<1.0V	3.01k	1.0 MHz

Table 1: Recommended R_{FS} Values

Soft-Start Operation

Soft start is a means to ramp the output voltage gradually upon start-up. The output voltage rise time is controlled by the choice of soft-start capacitor, which is placed between the SS pin and the AGND pin. During start-up of the converter, the reference voltage to the error amplifier is linearly increased to its final level by an internal current source of approximately 10µA. The soft-start time is measured from when $V_{IN} > V_{UVLOR}$ and ENABLE pin voltage crosses its logic high threshold to when V_{OUT} reaches its programmed value. The total soft-start time can be calculated by:

Soft Start Time (ms): $T_{SS} \approx C_{ss}$ [nF] x 0.06

Typical soft-start time is approximately 2.8ms with SS capacitor value of 47nF.

POK Operation

The POK signal is an open drain signal (requires a pull up resistor to AVIN or similar voltage) from the converter indicating the output voltage is within the specified range. Typically, a 100kΩ or lower resistance is used as the pull-up resistor. The POK signal will be logic high (AVIN) when the output voltage is above 90% of the programmed voltage level. If the output voltage is below this point, the POK signal will be a logic low. The POK signal can be used to sequence down-stream converters by tying to their enable pins.

Over Current Protection

The current limit function is achieved by sensing the current flowing through a high-side sense PFET. If the current exceeds the OCP threshold, the switching cycle is terminated and an OCP counter is incremented. If the counter value reaches 32 OCP cycles, the device will shut down as described below. If there are 8 consecutive cycles that do not exceed the OCP threshold, the counter will reset. Once the OCP counter has reached 32 cycles, the MOSFET switches will tri-state and the soft start capacitor will be discharged. After approximately 32ms the device will attempt a restart. If the OCP condition persists, the device will enter a hiccup mode until the OCP condition is removed. The OCP trip point depends on PVIN, VOUT, RCLX, RFS and is meant to protect the device from damage. OCP is not an adjustable threshold. Follow Table 2 for recommended RCLX and RFS values to set the current limit above 9A under normal operating conditions. Not following Table 2 may result in current limit being too low or too high.

Note: Do not leave RCLX pin floating.

PVIN	V_{OUT}	R_{CLX}	R_{FS}
4.5V to 13.2V	3.3V	32.4k	22k
	2.5V	35.7k	10k
	1.8V	43.2k	4.87k
	1.5V	41.2k	3.01k
	1.2V	46.4k	3.01k
	≤1.0V	54.9k	3.01k

Table 2: Recommended R_{CLX} Values

Thermal Overload Protection

Thermal shutdown circuit will disable device operation when the junction temperature exceeds approximately 150°C. The device will go through a soft-shutdown and allow the output to discharge in a controlled manner. This prevents excessive output ringing in the event of a thermal fault condition. After a thermal shutdown event, when the junction temperature drops by approximately 35°C, the converter will re-start with a normal soft-start.

AVIN Under-Voltage Lock-Out (UVLO)

Internal circuits ensure that the converter will not start switching until the AVIN input voltage is above the specified minimum voltage. Hysteresis, input de-glitch and output leading edge blanking ensures high noise immunity and prevents false UVLO triggers.

Master / Slave (Parallel) Operation:

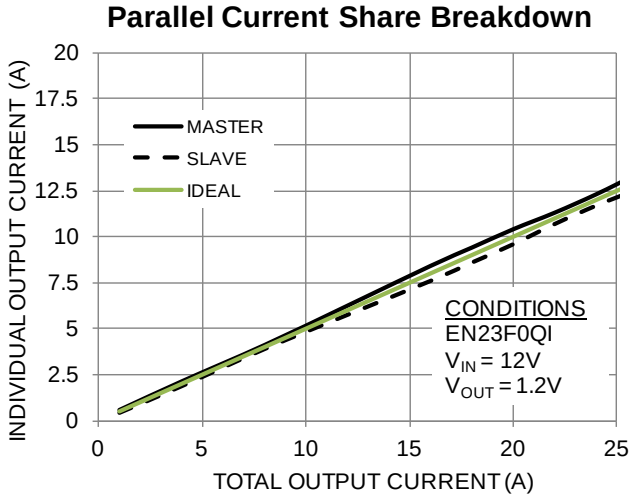


Figure 8. Parallel Current Matching

Up to four EN23F2QI devices may be connected in a Master/Slave configuration to handle larger load currents. The maximum output current for each parallel device will need to be de-rated by 20 percent so that no devices will over current due to current mis-match. The Master device's switching clock may be phase-locked to an external clock source via the S_IN pin or left open and use its default switching frequency. The device is placed in Master mode by pulling the M/S pin low or in Slave mode by pulling M/S pin high. Note that the M/S pin is also pulled low for standalone mode. In Master mode, the internal PWM signal is output on the S_OUT pin. This PWM signal from the Master is fed to the Slave device at its S_IN input. The Slave device acts like an extension of the power FETs in the Master. The inductor in the Slave prevents crow-bar currents from Master to Slave due to timing delays. Parallel operation in dual supply mode is shown in Figure 9. Single supply mode operation may also be implemented. Note that only critical components are shown. The red text and

red lines indicate the important parallel operation connections and care should be taken in layout to ensure low impedance between those paths. The parallel current matching is illustrated in Figure 8.

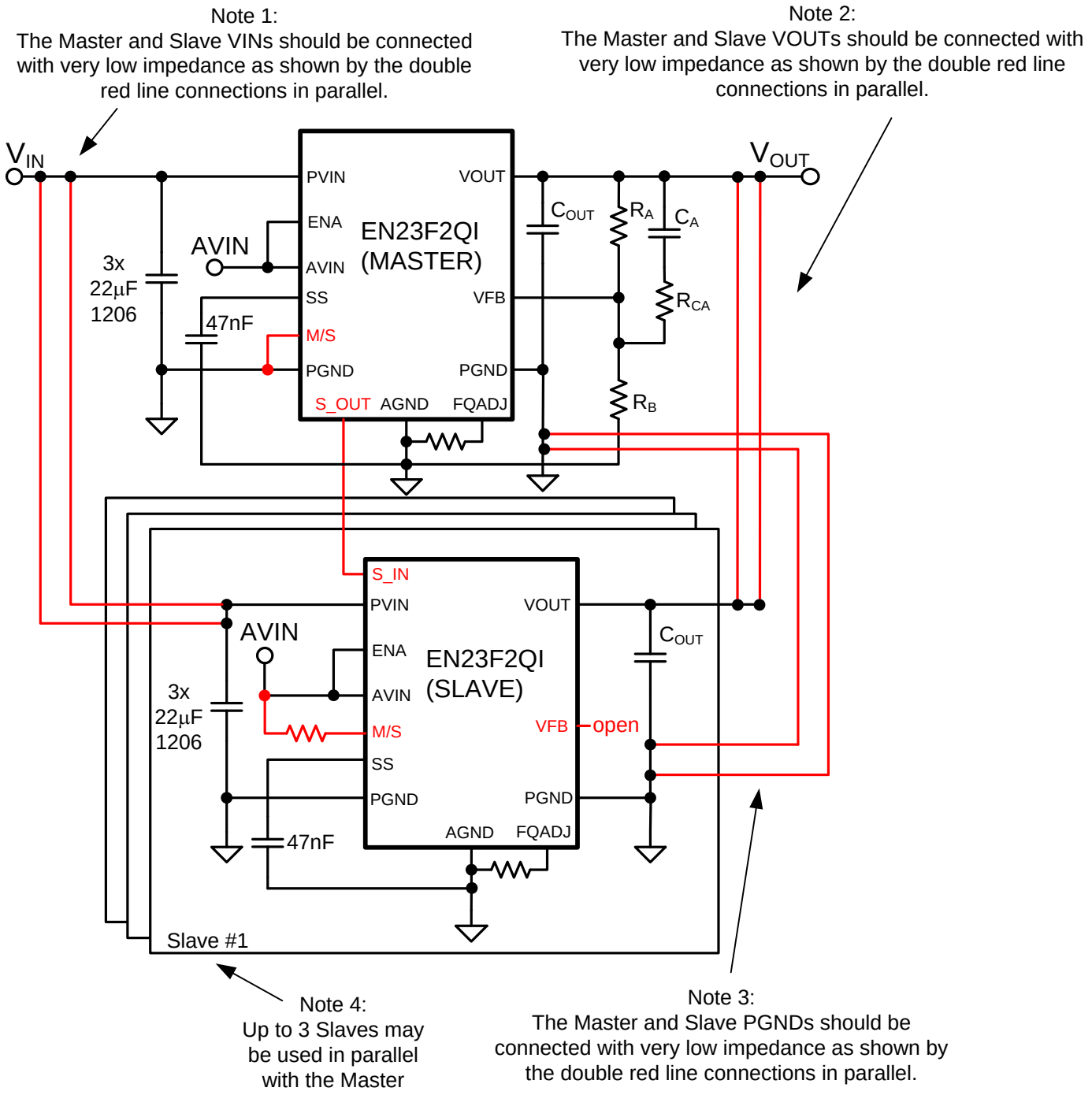


Figure 9. Parallel Operation Illustration

Application Information

Output Voltage Programming and Loop Compensation

The EN23F2QI uses a Type IV Voltage Mode compensation network. Type IV Voltage Mode control is a proprietary Altera Enpirion control scheme that maximizes control loop bandwidth to deliver excellent load transient responses and maintain output regulation with pin point accuracy. For ease of use, most of this network has been customized and is integrated within the device package.

The EN23F2QI output voltage is programmed using a simple resistor divider network (R_A and R_B). The feedback voltage at VFB is nominally 0.6V. R_A is predetermined based on Table 4 and R_B can be calculated based on Figure 10. The values recommended for C_{OUT}, C_A, R_{CA} and R_{EA} make up the external compensation of the EN23F2QI. It will vary with each PVIN and VOUT combination to optimize on performance. The EN23F2QI solution can be optimized for either smallest size or highest performance. Please see Table 4 for a list of recommended R_A, C_A, R_{CA}, R_{EA} and C_{OUT} values for each solution. Since VFB is a sensitive node, do not touch the VFB node while the device is in operation as doing so may introduce parasitic capacitance into the control loop that causes the device to behave abnormally and damage may occur.

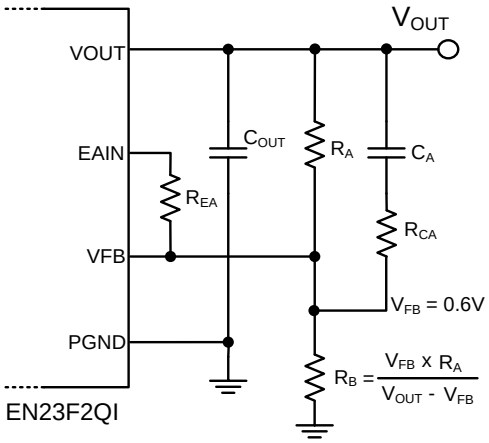


Figure 10: V_{OUT} Resistor Divider & Compensation Components. See Table 4 for details.

Input Capacitor Selection

The EN23F2QI requires three 22µF/1206 input capacitor. Low-cost, low-ESR ceramic capacitors should be used as input capacitors for this converter. The dielectric must be X5R or X7R rated. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. In some applications, lower value capacitors are needed in parallel with the larger, capacitors in order to provide high frequency decoupling. Distance from the input power source to the input of the device creates parasitic inductance which can increase input ripple during startup or in steady state operation. Be sure the input is properly filtered with additional bulk capacitance so that the input AC ripple on PVIN is less than 1V peak-to-peak. Placing capacitors in parallel reduces the impedance and will result in lower ripple voltage. Table 2 contains a list of recommended input capacitors.

Recommended Input Capacitors

Description	MFG	P/N
22µF, 16V, X5R, 10%, 1206	Murata	GRM31CR61C226ME15
22µF, 16V, X5R, 20%, 1206	Taiyo Yuden	EMK316ABJ226ML-T
22µF, 25V, X5R, 10%, 1210	Murata	GRM32ER61E226KE15L
22µF, 25V, X5R, 20%, 1210	Taiyo Yuden	TMK325BJ226MM-T

Table 2: Recommended Input Capacitors

Output Capacitor Selection

As seen from Table 4, the EN23F2QI has been optimized for use with one 100µF/1206 plus three 47µF/1206 output capacitors for best performance. For smallest solution size, various combinations of output capacitance may be used. See Table 4 for details. Low ESR ceramic capacitors are required with X5R or X7R rated dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these lose too much capacitance with frequency, temperature and bias voltage. Table 3 contains a list of recommended output capacitors. Extra bulk capacitors may be used to improve load transient response at the load. The maximum output capacitance allowed on the EN23F2QI depends on the output voltage. Table 3 shows the maximum output capacitance based on output voltage. The maximum output capacitance includes all capacitors connected from the output power plain to ground.

VOUT	R_{FS}	COUT_MAX	Snubber
3.3V	22k	800µF	4.7Ω + 1000pF
2.5V	10k	1200µF	4.7Ω + 1000pF
1.8V	4.87k	1600µF	4.7Ω + 1000pF
1.5V	3.01k	1800µF	4.7Ω + 1000pF
1.2V	3.01k	2000µF	4.7Ω + 1000pF
≤1.0V	3.01k	2200µF	4.7Ω + 1000pF

Table 3: Maximum Output Capacitance

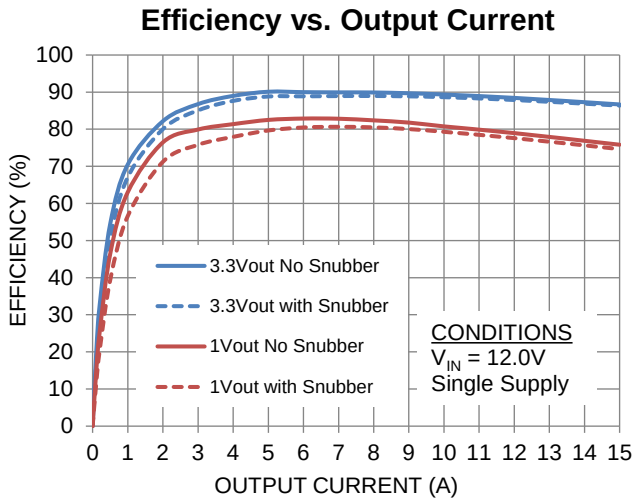


Figure 11: Efficiency with/without Snubber

If the maximum output capacitance in the application exceeds 50% of the COUT_MAX value in Table 3, then a "snubber" circuit is required (See Figure 1). The "snubber" circuit is a series resistor and capacitor from the NC(SW) pin to PGND. The "snubber" values are optimized for the EN23F2QI and should be followed to within 10% of the recommendations. Due to the added power dissipation, using the "snubber" will decrease the converter efficiency as shown in Figure 11. It is recommended to use at least a ¼W resistor at 1206 case size or greater due to power dissipation. The capacitor should be at least 0603 case size.

Since additional bulk capacitance changes the LC double pole of the Voltage Mode Control architecture, be sure to have at least 4mΩ of separation between the feedback sense point and the additional bulk capacitors. Be sure to follow the Best Performance external compensation recommendations in Table 5.

The output capacitance can also influence the output ripple. Output ripple voltage is determined by the aggregate output capacitor impedance. Capacitor impedance, denoted as Z, is comprised of capacitive reactance, effective series resistance, ESR, and effective series inductance, ESL reactance.

Placing output capacitors in parallel reduces the impedance and will hence result in lower ripple voltage.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \ldots + \frac{1}{Z_n}$$

Recommended Output Capacitors

Description	MFG	P/N
47µF, 6.3V, X5R, 20%, 1206	Murata	GRM31CR60J476ME19L
47µF, 10V, X5R, 20%, 1206	Taiyo Yuden	LMK316BJ476ML-T
22µF, 10V, X5R, 20%, 0805	Taiyo Yuden	LMK212BJ226MG-T
100µF, 6.3V, X5R, 20%, 1206	Murata	GRM31CR60J107ME39L
	Taiyo Yuden	JMK316BJ107ML-T

Table 4: Recommended Output Capacitors

Best Performance							Smallest Solution Size						
C_{IN} = 3 x 22µF/1206							C_{IN} = 3 x 22µF/1206						
C_{OUT} = 3x47µF (1206) + 100µF(1206)							$V_{OUT} \leq 1.8V$, C_{OUT} = 22µF/0805 + 2x47µF/0805 $3.3V > V_{OUT} > 1.8V$, C_{OUT} = 3x47µF/1206						
R_A = 200 kΩ							R_A = 100 kΩ						
PVIN (V)	VOUT (V)	C_A (pF)	R_{CA} (kΩ)	R_{EA} (kΩ)	Ripple (mV)	Deviation (mV)	PVIN (V)	VOUT (V)	C_A (pF)	R_{CA} (kΩ)	R_{EA} (kΩ)	Ripple (mV)	Deviation (mV)
13.2V	1.0V	27	15	200	25.6	40	13.2V	1.0V	12	36	Open	15	78
	1.2V	27	15	200	24	42		1.2V	12	36	Open	18	93
	1.5V	27	15	200	26.4	60		1.5V	12	36	Open	22	104
	1.8V	15	15	86	28.4	70		1.8V	12	36	Open	25	130
	2.5V	15	15	86	31.6	86		2.5V	15	27	Open	32	162
	3.3V	15	15	86	37.3	96		3.3V	10	27	Open	46	200
12V	1.0V	27	15	200	21.6	42	12V	1.0V	22	27	Open	15	84
	1.2V	27	15	200	22.7	48		1.2V	22	27	Open	18	97
	1.5V	27	15	200	25.2	70		1.5V	18	27	Open	21	118
	1.8V	15	15	86	25.8	72		1.8V	18	27	Open	24	130
	2.5V	15	15	86	30	82		2.5V	22	27	Open	30	172
	3.3V	15	15	86	30.8	110		3.3V	15	27	Open	43	213
10V	1.0V	27	5	86	18.8	46	10V	1.0V	56	20	Open	15	85
	1.2V	27	5	86	20.4	54		1.2V	47	20	Open	17	100
	1.5V	27	5	86	22	60		1.5V	39	20	Open	20	120
	1.8V	15	15	86	23.6	78		1.8V	33	20	Open	22	140
	2.5V	15	15	86	26.5	92		2.5V	33	20	Open	29	177
	3.3V	15	15	86	28.9	132		3.3V	22	20	Open	41	230
8V	1.0V	27	5	86	17.2	64	8V	1.0V	200	10	Open	14	83
	1.2V	27	5	86	18.7	64		1.2V	200	10	Open	16	90
	1.5V	27	5	86	20.1	70		1.5V	150	10	Open	19	107
	1.8V	15	5	86	20.9	100		1.8V	82	10	Open	20	138
	2.5V	15	5	86	23.6	120		2.5V	68	10	Open	27	178
	3.3V	15	5	86	22.8	156		3.3V	39	10	Open	36	239
6.6V	1.0V	27	1	86	13.8	74	6.6V	1.0V	200	10	Open	13	99
	1.2V	27	1	86	15.2	76		1.2V	200	10	Open	15	105
	1.5V	27	1	86	16.4	88		1.5V	200	10	Open	17	118
	1.8V	15	5	86	19.6	116		1.8V	150	10	Open	19	138
	2.5V	15	5	86	20.4	148		2.5V	100	10	Open	24	183
	3.3V	15	5	86	21.1	204		3.3V	56	10	Open	32	250
5V	1.0V	27	1	86	12.4	92	5V	1.0V	200	10	Open	12	123
	1.2V	27	1	86	13.4	100		1.2V	200	10	Open	13	132
	1.5V	27	1	86	14.3	120		1.5V	200	10	Open	16	145
	1.8V	15	5	86	15.4	160		1.8V	200	10	Open	17	156
	2.5V	15	5	86	15.5	204		2.5V	100	10	Open	20	216
	3.3V	15	5	86	12.9	300		3.3V	100	10	Open	21	253

Table 4: R_A, C_A, R_{CA} and R_{EA} Values for Various PVIN/VOUT Combinations: Best Performance vs. Smallest Solution Size. Use the equations in Figure 10 to calculate R_B. Output ripple is measured at no load and nominal deviation is for a 15A load transient step. For compensation values of output voltage in between the specified output voltages, choose compensation values of the lower output voltage setting.

Thermal Considerations

Thermal considerations are important power supply design facts that cannot be avoided in the real world. Whenever there are power losses in a system, the heat that is generated by the power dissipation needs to be accounted for. The Altera Enpirion PowerSoC helps alleviate some of those concerns.

The Altera Enpirion EN23F2QI DC-DC converter is packaged in a 13x12x3mm 92-pin QFN package. The QFN package is constructed with copper lead frames that have an exposed thermal pad. The exposed thermal pad on the package should be soldered directly on to a copper ground pad on the printed circuit board (PCB) to act as a heat sink. The recommended maximum junction temperature for continuous operation is 125°C. Continuous operation above 125°C may reduce long-term reliability. The device has a thermal overload protection circuit designed to turn off the device at an approximate junction temperature value of 150°C.

The following example and calculations illustrate the thermal performance of the EN23F2QI.

Example:

V_{IN} = 12V

V_{OUT} = 1.2V

I_{OUT} = 15A

First calculate the output power.

P_{OUT} = 1.2V x 15A = 18W

Next, determine the input power based on the efficiency (η) shown in Figure 12.

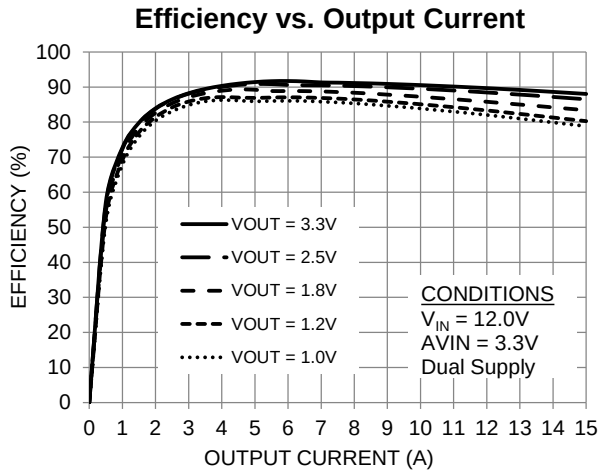


Figure 12: Efficiency vs. Output Current

For V_{IN} = 12V, V_{OUT} = 1.2V at 15A, η ≈ 80%

$\eta = P_{OUT} / P_{IN} = 80\% = 0.8$

$P_{IN} = P_{OUT} / \eta$

$P_{IN} \approx 18W / 0.8 \approx 22.5W$

The power dissipation (P_D) is the power loss in the system and can be calculated by subtracting the output power from the input power.

$P_D = P_{IN} - P_{OUT}$

$\approx 22.5W - 18W \approx 4.5W$

With the power dissipation known, the temperature rise in the device may be estimated based on the theta JA value (θ_{JA}). The θ_{JA} parameter estimates how much the temperature will rise in the device for every watt of power dissipation. The EN23F2QI has a θ_{JA} value of 13 ºC/W without airflow.

Determine the change in temperature (ΔT) based on P_D and θ_{JA}.

$\Delta T = P_D \times \theta_{JA}$

$\Delta T \approx 4.5W \times 13°C/W = 58.5°C \approx 59°C$

The junction temperature (T_J) of the device is approximately the ambient temperature (T_A) plus the change in temperature. We assume the initial ambient temperature to be 25°C.

$T_J = T_A + \Delta T$

$T_J \approx 25°C + 59°C \approx 84°C$

The maximum operating junction temperature (T_{JMAX}) of the device is 125°C, so the device can operate at a higher ambient temperature. The maximum ambient temperature (T_{AMAX}) allowed can be calculated.

$T_{AMAX} = T_{JMAX} - P_D \times \theta_{JA}$

$\approx 125°C - 59°C \approx 66°C$

The maximum ambient temperature the device can reach is 66°C given the input and output conditions. Note that the efficiency will be slightly lower at higher temperatures and this calculation is an estimate. Check De-rating Curves for guaranteed maximum output current over temperature.

Engineering Schematic

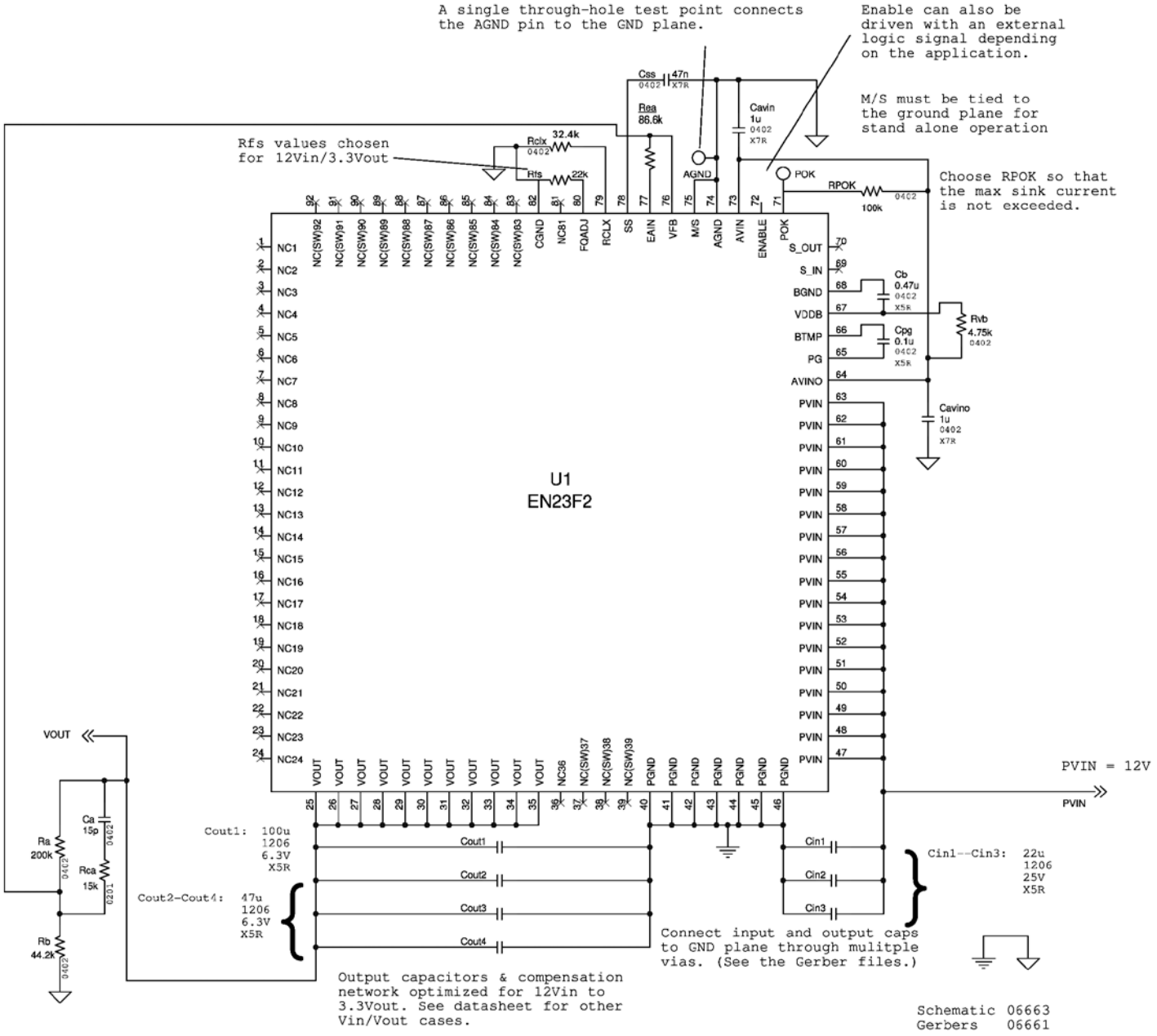


Figure 13: Engineering Schematic

Layout Recommendation

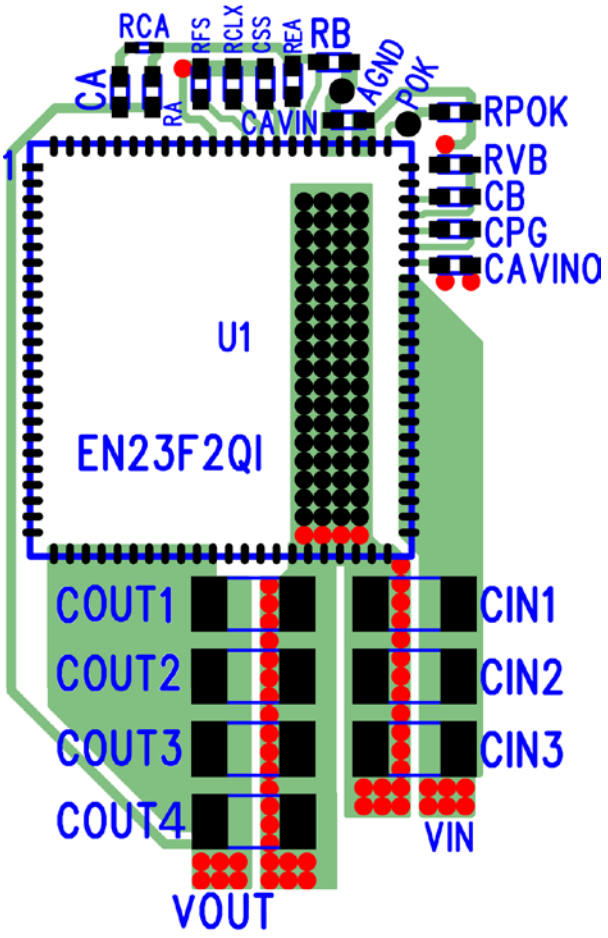


Figure 14: Top Layer Layout with Critical Components (Top View). See Figure 13 for corresponding schematic.

This layout only shows the critical components and top layer traces for minimum footprint in single-supply mode. Alternate circuit configurations & other low-power pins need to be connected and routed according to customer application. Please see the Gerber files at www.altera.com/enpirion for details on all layers.

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EN23F2QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EN23F2QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: The PGND connections for the input and output capacitors on layer 1 need to have a slit between them in order to provide some separation between input and output current loops.

Recommendation 3: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors.

Recommendation 4: The thermal pad underneath the component must be connected to the system ground plane through as many vias as possible. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. This connection provides the path for heat dissipation from the converter.

Recommendation 5: Multiple small vias (the same size as the thermal vias discussed in recommendation 4) should be used to connect ground terminal of the input capacitor and output capacitors to the system ground plane. It is preferred to put these vias along the edge of the GND copper closest to the +V copper. These vias connect the input/output filter capacitors to the GND plane, and help reduce parasitic inductances in the input and output current loops. If vias cannot be placed under the capacitors, then place them on both sides of the slit in the top layer PGND copper.

Recommendation 6: AVIN is the power supply for the small-signal control circuits. AVINO powers AVIN in single supply mode. AVIN and AVINO should have a decoupling capacitor close to each of their pins. Refer to Figure 14.

Recommendation 7: The layer 1 metal under the device must not be more than shown in Figure 14. Refer to the section regarding Exposed Metal on Bottom of Package. As with any switch-mode DC/DC converter, try not to run sensitive signal or control lines underneath the converter package on other layers.

Recommendation 8: The V_{OUT} sense point should be just after the last output filter capacitor. Keep the sense trace short in order to avoid noise coupling into the node. Contact Altera MySupport for any remote sensing applications.

Recommendation 9: Keep R_A, C_A, R_B, and R_{CA} close to the VFB pin (Refer to Figure 14). The VFB pin is a high-impedance, sensitive node. Keep the trace to this pin as short as possible. Whenever possible, connect R_B directly to the AGND instead of going through the GND plane.

Recommendation 10: Follow all the layout recommendations as close as possible to optimize performance. Altera provides schematic and layout reviews for all customer designs. Contact Altera MySupport for detailed support (www.altera.com/mysupport).

Design Considerations for Lead-Frame Based Modules

Exposed Metal on Bottom of Package

Lead-frames offer many advantages in thermal performance, in reduced electrical lead resistance, and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package, as shown in Figure 15.

Only the thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EN23F2QI should be clear of any metal (copper pours, traces, or vias) except for the thermal pad. The “shaded-out” area in Figure 15 represents the area that should be clear of any metal on the top layer of the PCB. Any layer 1 metal under the shaded-out area runs the risk of undesirable shorted connections even if it is covered by soldermask.

The solder stencil aperture should be smaller than the PCB ground pad. This will prevent excess solder from causing bridging between adjacent pins or other exposed metal under the package. Please consult the Enpirion Manufacturing Application Note for more details and recommendations.

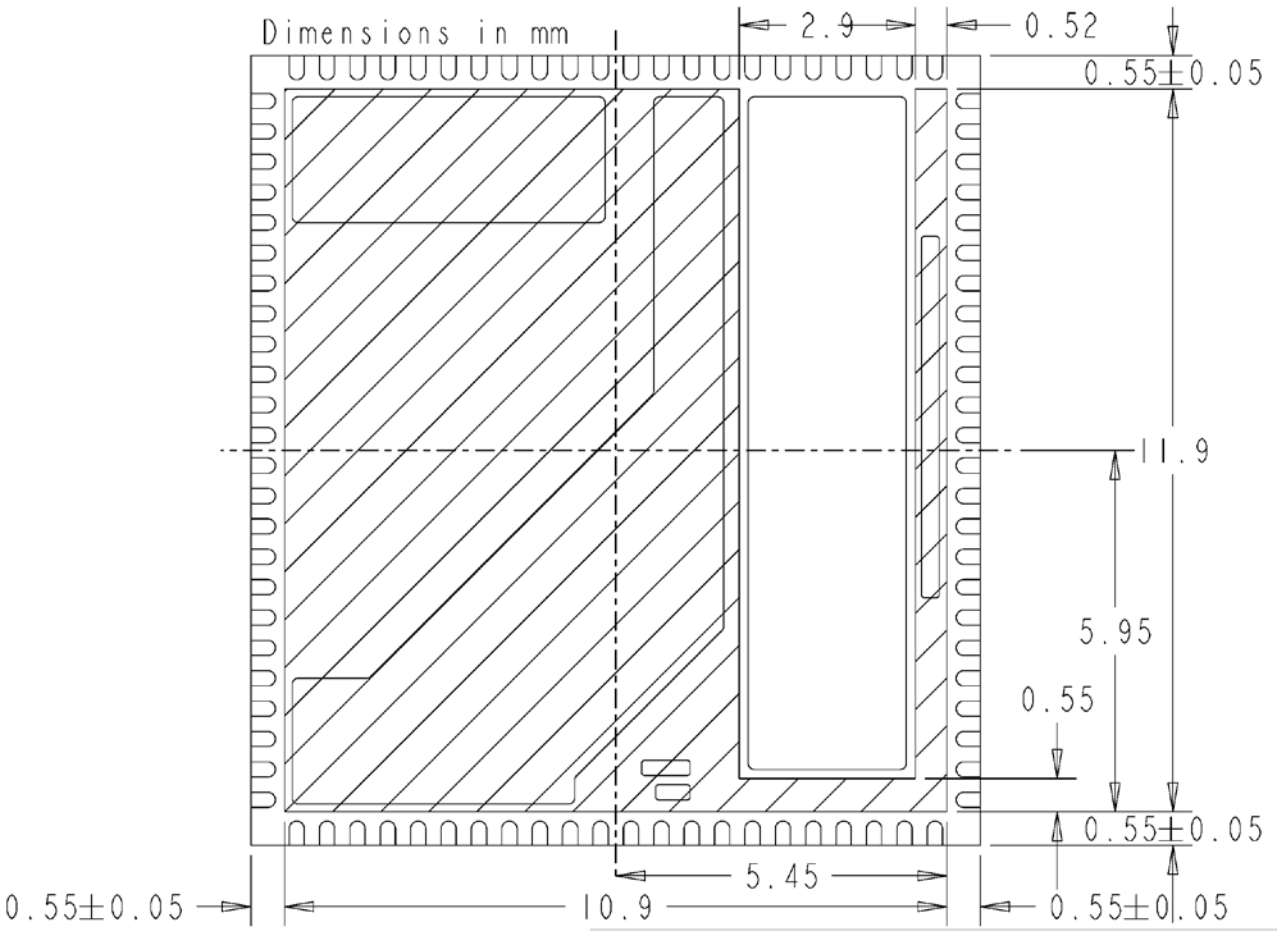


Figure 15: Lead-Frame exposed metal (Bottom View)

Shaded area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.

Recommended PCB Footprint

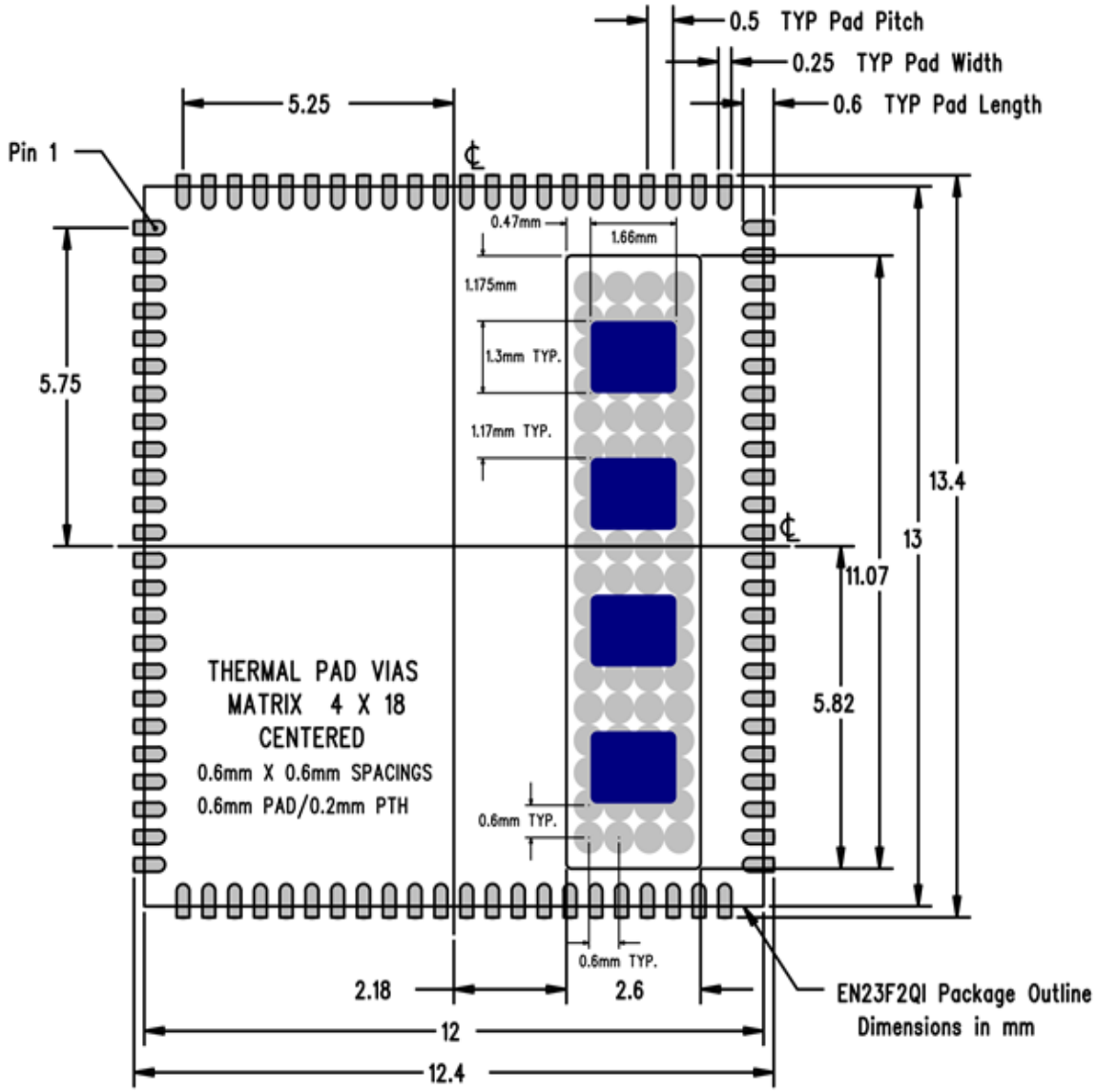


Figure 16: EN23F2QI PCB Footprint (Top View)

The solder stencil aperture for the thermal pad (shown in blue) is based on Altera's manufacturing recommendations.

Package and Mechanical

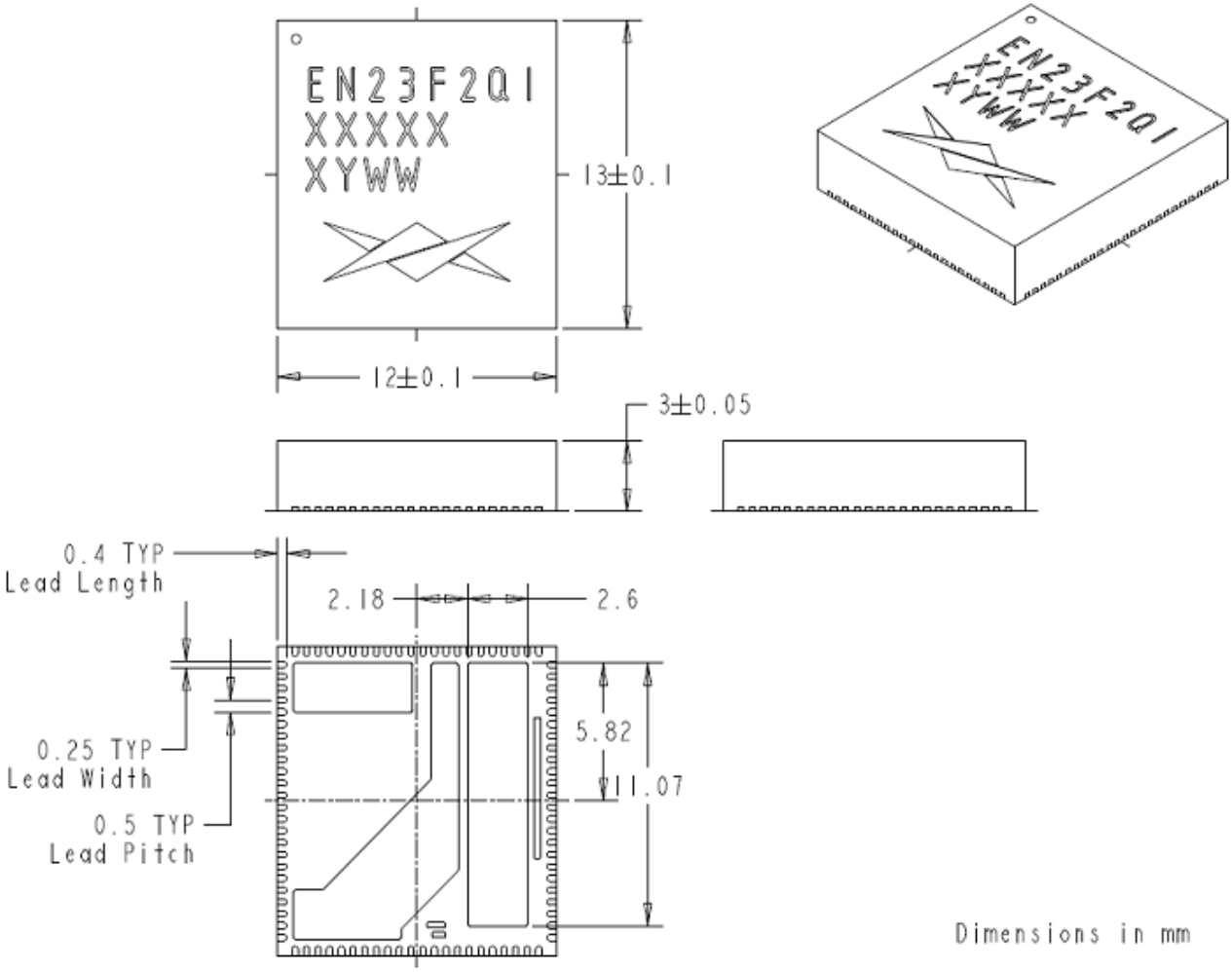


Figure 17: EN23F2QI Package Dimensions (Bottom View)

Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

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