Enpirion® Power Datasheet

ED8106 True Digital Single-Phase Single-Rail PWM controller

Description

The ED8106 is true-digital single-phase PWM controllers optimally configured for use with the Altera ET4040 40A Power Train.

The ED8106 integrates a digital control loop that is optimized for maximum flexibility and stability as well as load step and steady-state performance. In addition, a rich set of protection functions is provided.

To simplify the system design, a set of optimized configuration options have been pre-programmed in the devices. These configurations can be selected by setting the values of two external resistors.

Reference solutions are available complete with layout recommendations, example circuit board layouts, complete bill of materials and more.

Features

- Programmable digital control loop.
- Advanced, digital control techniques
- Improved transient response and noise immunity
- Protection features
  - Over-current protection
  - Over-voltage protection (VIN, VOUT)
  - Under-voltage protection (VIN, VOUT)
  - Overloaded startup
  - Continuous retry (“hiccup”) mode for fault conditions
- Pre-programmed for optimized use with Altera ET4040 40A Power Train.
- 2-pin configuration for loop compensation, output voltage, and slew rate.
- Fuse-based one-time programmable (OTP) nonvolatile memory for improved reliability
- Operation from a single 5V or 3.3V supply.

Physical Characteristics

- Operation temperature: -40°C to +85°C
- V_{OUT} max: 5V
- Lead free (RoHS compliant) 24-pin QFN package (4mm x 4mm)

Benefits

- Fast time-to-market using an off-the-shelf, optimally configured controller and power train.
- Fast configuration and design flexibility.
- FPGA designer-friendly solution.
- Highest power density with smallest footprint.
- PWM controller enabling point-of-load platform designs without digital communication.
- Higher energy efficiency across all output loading conditions.

Applications

- FPGA Designs
- Single-Rail/Single-Phase supplies for FPGA’s, Processors, ASIC’s, DSP’s, etc.
- Servers and Storage
- Base Stations
- Network Routers
- Industrial Applications
- Telecommunications

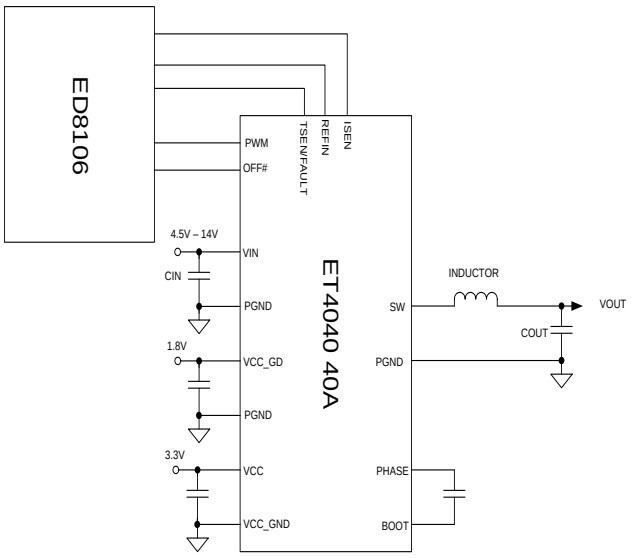

Figure 1: Simplified Applications Circuit

Ordering Information

Part Number	Package Markings	$T_{AMBIENT}$ Rating (°C)	Package Description
ED8106N00QI	81060	-40°C to +85°C	24-pin (4mm x 4mm x 0.95mm) QFN T&R
ED8106N01QI	81061	-40°C to +85°C	24-pin (4mm x 4mm x 0.95mm) QFN T&R
ED8106N02QI	81062	-40°C to +85°C	24-pin (4mm x 4mm x 0.95mm) QFN T&R
EVB-ED8106N02QI	Evaluation Board with computer communication interface and design GUI		

Note: ED8106N00QI is a blank part without any pre-configuration. ED8106N01QI is the part per-configured particularly for Statix V FPGA Development Kit Board. ED8106N02QI is pre-configured for Evaluation Board only.

Packing and Marking Information: www.altera.com/support/reliability/packing/rel-packing-and-marking.html

Pin Assignments (Top View)

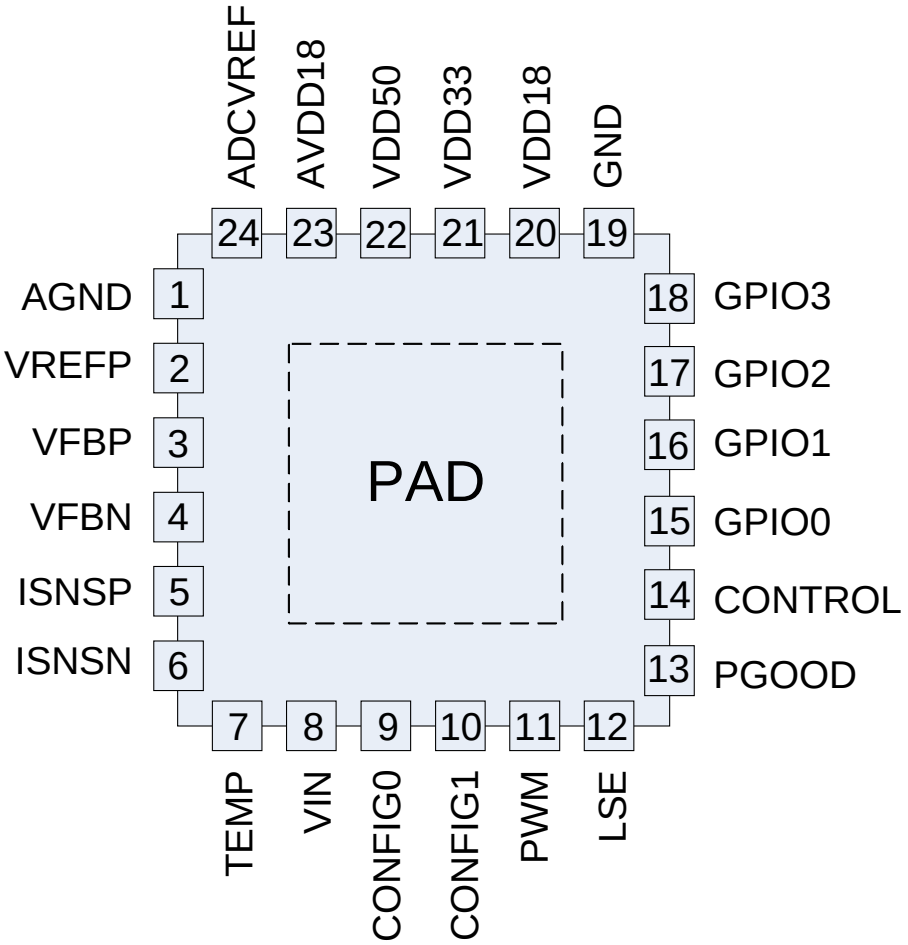

Figure 2: Pin Out Diagram (Top View)

Pin Description

Pin	Name	Direction	Type	Description
1	AGND	Input	Supply	Analog Ground
2	VREFP	Output	Supply	Reference Terminal
3	VFBP	Input	Analog	Positive Input of Differential Feedback Voltage Sensing
4	VFBN	Input	Analog	Negative Input of Differential Feedback Voltage Sensing
5	ISNSP	Input	Analog	Positive Input of Differential Current Sensing
6	ISNSN	Input	Analog	Negative Input of Differential Current Sensing
7	TEMP	Input	Analog	Connection to External Temperature Sensing Element
8	VIN	Input	Analog	Power Supply Input Voltage Sensing
9	CONFIG0	Input	Analog	Configuration Selection 0
10	CONFIG1	Input	Analog	Configuration Selection 1
11	PWM	Output	Digital	High-Side FET Control Signal
12	LSE	Output	Digital	Low-Side FET Control Signal
13	PGOOD	Output	Digital	PGOOD Output (Internal Pull-Down)
14	CONTROL	Input	Digital	Control Input – Active High
15	GPIO0	Input/Output	Digital	General Purpose Input/Output Pin
16	GPIO1	Input/Output	Digital	General Purpose Input/Output Pin
17	GPIO2	Input/Output	Digital	General Purpose Input/Output Pin
18	GPIO3	Input/Output	Digital	General Purpose Input/Output Pin
19	GND	Input	Supply	Digital Ground
20	VDD18	Output	Supply	Internal 1.8 V Digital Supply Terminal
21	VDD33	Input/Output	Supply	3.3 V Supply Voltage Terminal
22	VDD50	Input	Supply	5.0 V Supply Voltage Terminal
23	AVDD18	Output	Supply	Internal 1.8 V Analog Supply Terminal
24	ADCVREF	Input	Analog	Analog-to-Digital Converter (ADC) Reference Terminal
PAD	PAD	Input	Analog	Exposed Pad, Digital Ground

IC Characteristics

Note: The absolute maximum ratings are stress ratings only. The ED8106 might not function or be operable above the recommended operating conditions. Stresses exceeding the absolute maximum ratings might also damage the device. In addition, extended exposure to stresses above the recommended operating conditions might affect device reliability. Altera does not recommend designing to the “Absolute Maximum Ratings.”

Absolute Maximum Ratings

PARAMETER	PINS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltages						
5 V supply voltage	VDD50	dV/dt < 0.15V/µs	-0.3		5.5	V
Maximum slew rate					0.15	V/µs
3.3 V supply voltage	VDD33		-0.3		3.6	V
1.8 V supply voltage	VDD18 AVDD18		-0.3		2.0	V
Digital pins						
Digital I/O pins	GPIOx CONTROL PGOOD LSE PWM		-0.3		5.5	V
Analog pins						
Current sensing	ISNSP ISNSN		-0.3		5.5	V
Voltage feedback	VFBP VFBN		-0.3		2.0	V
All other analog pins	ADCVREF VREFP TEMP VIN CONFIGx		-0.3		2.0	V
Ambient conditions						
Storage temperature			-40		150	°C
Electrostatic discharge – Human Body Model [1)]					+/-2k	V
Electrostatic discharge – Charge Device Model [1)]					+/- 500	V
Note 1: ESD testing is performed according to the respective JESD22 JEDEC standard.						

Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Ambient conditions						
Operation temperature	T_{AMB}		-40		85	°C
Thermal resistance junction to ambient	θ_{JA}			40		K/W

Electrical Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply voltages						
5 V supply voltage (VDD50 pin)	V_{VDD50}		4.75	5.0	5.25	V
5 V supply current	I_{VDD50}	VDD50=5.0 V		23		mA
3.3 V supply voltage	V_{VDD33}	Supply for both the VDD33 and VDD50 pins if the internal 3.3V regulator is not used.	3.0	3.3	3.6	V
3.3 V supply current	I_{VDD33}	VDD50=VDD33=3.3 V		23		mA
Internally generated supply voltages						
3.3 V supply voltage (VDD33 pin)	V_{VDD33}	VDD50=5.0 V	3.0	3.3	3.6	V
3.3 V output current	I_{VDD33}	VDD50=5.0 V			2.0	mA
1.8 V supply voltages (AVDD18 and VDD18 pins)	V_{AVDD18} V_{VDD18}	VDD50=5.0 V	1.72	1.80	1.98	V
1.8 V output current					0	mA
Power-on reset threshold for VDD33 pin – on	$V_{TH\_POR\_ON}$			2.8		V
Power-on reset threshold for VDD33 pin – off	$V_{TH\_POR\_OFF}$			2.6		V
Digital IO pins (GPIOx, CONTROL, PGOOD)						
Input high voltage		VDD33=3.3 V	2.0			V
Input low voltage		VDD33=3.3 V			0.8	V
Output high voltage		VDD33=3.3 V	2.4		VDD33	V
Output low voltage					0.5	V
Input leakage current					±1	µA
Output current - high					2.0	mA
Output current - low					2.0	mA
Digital IO pins with tri-state capability (LSE, PWM)						
Output high voltage		VDD33=3.3 V	2.4		VDD33	V
Output low voltage					0.5	V
Output current - high					2.0	mA
Output current - low					2.0	mA
Tri-state leakage current					±1.0	µA
Output voltage (without external feedback divider; see section 0)						
Set-point voltage			0		1.4	V
Set-point resolution				1.4		mV
Set-point accuracy		VOUT=1.2 V		1		%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Inductor current measurement						
Common mode voltage - ISNSP and ISNSN pins to AGND			0		5.0	V
Differential voltage range across ISNSP and ISNSN pins					±100	mV
Accuracy				5		%
Digital pulse width modulator						
Switching frequency	f_{SW}		500		1000	kHz
Resolution				163		ps
Frequency accuracy				2.0		%
Duty Cycle			2.5		100	%
Over-voltage protection						
Reference DAC						
Set-point voltage			0		1.58	V
Resolution				25		mV
Set point accuracy				2		%
Comparator						
Hysteresis				35		mV
Housekeeping analog-to-digital converter (HKADC) input pins						
Input voltage (TEMP, VIN, CONFIG0, and CONFIG1 pins)			0		1.44	V
Source impedance Vin sensing					3	kΩ
ADC resolution				0.7		mV
External temperature measurement (PN-junction, voltage input with positive/negative temperature coefficient sense elements are supported)						
Bias currents for external temperature sensing (TEMP pin)		Use PN-junction		60		µA
Bias currents for external temperature sensing (TEMP pin)		Use voltage input		0		µA
Resolution (TEMP pin)				0.32		K
Accuracy of measurement (TEMP pin)				±5.0		K
Internal temperature measurement						
Resolution				0.22		K
Accuracy of measurement				±5.0		K

Functional Block Diagram

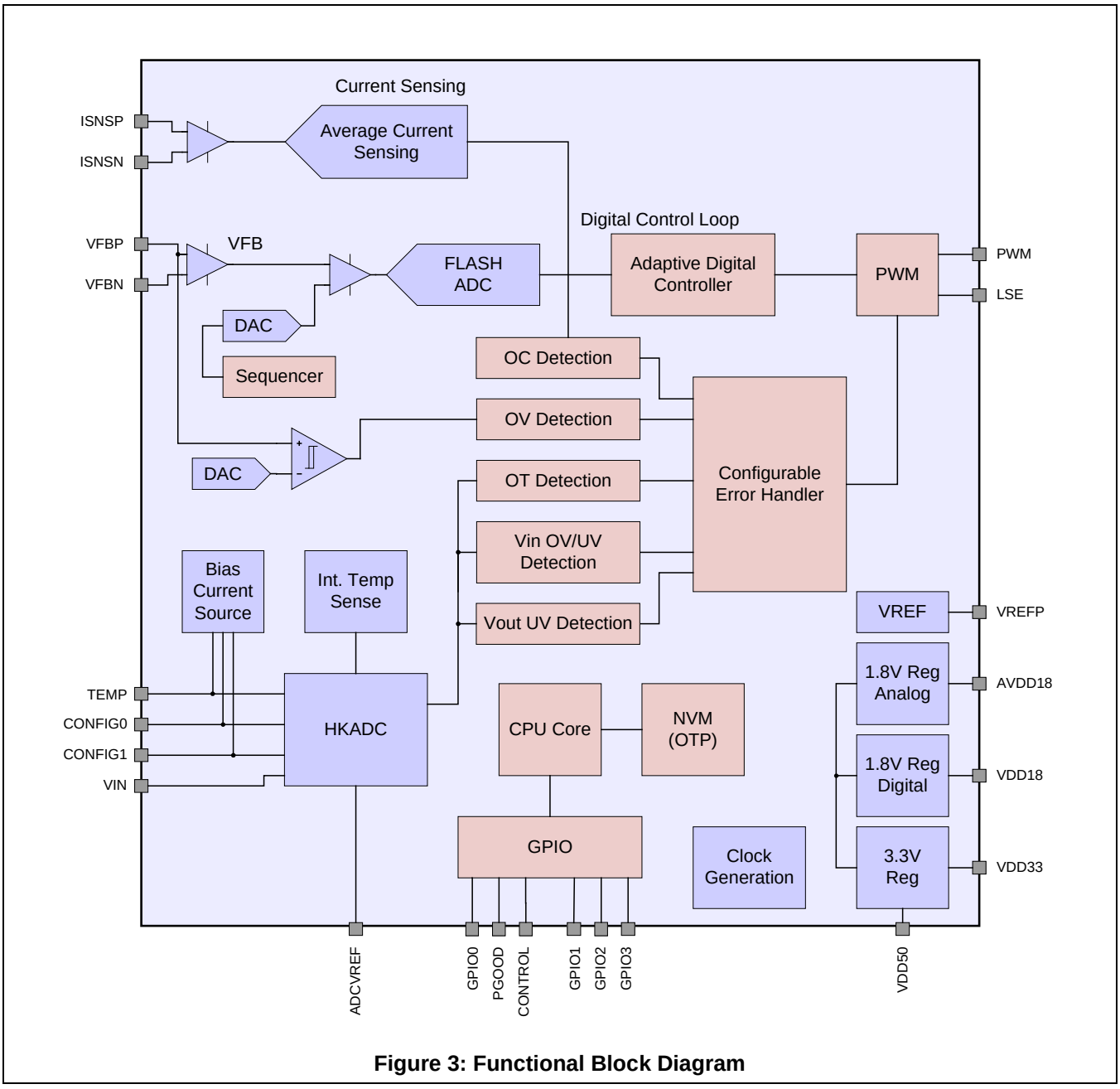

Figure 3: Functional Block Diagram

Functional Description

Overview

The ED8106 is true-digital single-phase PWM controller optimally configured for use with the Altera Power Solutions 40A Power Train ET4040. The ED8106 has a digital power control loop incorporating output voltage sensing, average inductor current sensing, and extensive fault monitoring and handling features. Several different functional units are integrated in the device. A dedicated digital control loop is used to provide fast loop response and optimal output voltage regulation. This includes output voltage sensing, average inductor current sensing, a digital control law, and a digital pulse-width modulator (DPWM). In parallel, a dedicated error handler allows fast and flexible detection of error signals and their appropriate handling. A housekeeping analog-to-digital converter (HKADC) ensures the reliable and efficient measurement of environmental signals, such as input voltage and temperature.

An application-specific, low-energy integrated microcontroller is used to control the overall system. It manages configuration of the various logic units according to the preprogrammed configuration look-up tables and the external configuration resistors connected to the CONFIG0 and CONFIG1 pins. These pin-strapping resistors expedite configuration of output voltage, compensation, and rise time without requiring digital communication. Altera's ED81xx Power Designer graphical user interface (GUI) allows the user to monitor the controller's measurements of the environmental signals and the status of the error handler via the GPIO2 and GPIO3 pins.

A high-reliability, high-temperature one-time programmable memory (OTP) is used to store configuration parameters. All required bias and reference voltages are internally derived from the external supply voltage.

Power Supply Circuitry, Reference Decoupling, and Grounding

The ED8106 incorporates several internal power regulators in order to derive all required supply and bias voltages from a single external supply voltage. This supply voltage can be either 5V or 3.3V depending on whether the internal 3.3V regulator should be used. If the internal 3.3V regulator is not used, 3.3V must be supplied to the 3.3V and 5V supply pins. Decoupling capacitors are required at the VDD33, VDD18, and AVDD18 pins (1.0µF minimum; 4.7µF recommended). If the 5.0V supply voltage is used, i.e., the internal 3.3V regulator is used, a small load current can be drawn from the VDD33 pin. This can be used to supply pull-up resistors, for example.

The reference voltages required for the analog-to-digital converters are generated within the ED8106. External decoupling must be provided between the VREFP and ADCVREF pins. Therefore, a 4.7µF capacitor is required at the VREFP pin, and a 100nF capacitor is required at the ADCVREF pin. The two pins should be connected with approximately 50Ω resistance in order to provide sufficient decoupling between the pins.

Three different ground connections (the pad, AGND pin, and GND pin) are available on the outside of the package. These should be connected together to a single ground tie. A differentiation between analog and digital ground is not required.

Reset/Start-up Behavior

The ED8106 employs an internal power-on-reset (POR) circuit to ensure proper start up and shut down with a changing supply voltage. Once the supply voltage increases above the POR threshold voltage (see section 0), the ED8106 begins the internal start-up process. Upon its completion, the device is ready for operation.

Digital Power Control

Overview

The digital power control loop consists of the integral parts required for the control functionality of the ED8106. A high-speed analog front-end is used to digitize the output voltage. A digital control core uses the acquired information to provide duty-cycle information to the PWM that controls the drive signals to the power stage.

Switching Frequency

The ED8106 supports the switching frequencies listed in Table 1.

Table1: Supported Switching Frequencies

1000 kHz	666.6 kHz
888 kHz	571.4 kHz
800 kHz	500.0 kHz

Output Voltage Feedback

The voltage feedback signal is sampled with a high-speed analog front-end. The feedback voltage is differentially measured and subtracted from the voltage reference provided by a reference digital-to-analog converter (DAC) using an error amplifier. A flash ADC is then used to convert the voltage into its digital equivalent. This is followed by internal digital filtering to improve the system's noise rejection.

Although the reference DAC generates a voltage up to 1.44V, keeping the voltage on the feedback pin (VFBP) at approximately 1.20V is recommended to guarantee sufficient headroom.

Digital Compensator

The sampled output voltage is processed by a digital control loop in order to modulate the DPWM output signals controlling the power stage. This digital control loop works as a voltage-mode controller using PID-type compensation. The basic structure of the controller is shown in Figure 4. The controller features two parallel compensators, steady-state operation, and fast transient operation. The ED8106 implements fast, reliable switching between the different compensation modes in order to ensure good transient performance and quiet steady state. This has been utilized to tune the compensators individually for the respective needs; i.e. quiet steady-state and fast transient performance.

Three different techniques are used to improve transient performance further:

- Phase-lag reducing sampling technology is used to acquire fast, accurate, and continuous information about the output voltage so that the device can react quickly to any change in output voltage.
- The technique to drive the DPWM asynchronously during load transients, allows limiting the maximum deviation of the output voltage and recharging the output capacitors faster.
- A nonlinear gain adjustment is used during large load transients to boost the loop gain and reduce the settling time.

Power Sequencing and the CONTROL Pin

The ED8106 supports power-sequencing features such as programmable ramp up/down and delays. The typical sequence of events is shown in Figure 5. The individual values for the delay, ramp time, and post ramp time can be configured. Note that the device is slew-rate controlled for ramping. Hence, when pin-strapping options for the output voltage are used, the ramp time can change based on the configured slew-rate and the actual selected output voltage. The slew rate can be selected in the application circuit using the pin-strap options as explained in section of *Application Information Section*. The CONTROL pin is configured for active high operation.

The ED8106 features a power good (PGOOD) output, which can be used to indicate the state of the power rail. If the output voltage level is above the power good ON threshold, the pin is set to active, indicating a stable output voltage on the rail. Different levels for turn-on and turn-off are used to enable the use of a hysteresis if desired. Note that the power good thresholds are stored in the device as factors relative to the nominal output voltage. Hence, using the strapping options to change the output voltage level also changes the PGOOD thresholds.

Pre-biased Start-up and Soft-Off

Dedicated pre-biased start-up logic ensures proper start-up of the power converter when the output capacitors are pre-charged to a non-zero output voltage. Closed-loop stability is ensured during this phase.

When the DC/DC converter output is disabled, i.e. when the CONTROL pin is set low, the ED8106 will execute the soft-off sequence. The soft-off sequence will ramp down the output voltage to 0V and set the PWM output in a tri-state condition.

Current Sensing

The ED8106 offers cycle-by-cycle average current sensing and over-current protection. A dedicated ADC is used to provide fast and accurate current information over the switching period. The acquired information is compared with the pre-configured over-current threshold to trigger an over-current fault event. DCR current sensing across the inductor is supported. This part works the best with ET4040 which provides a voltage based replica of the dynamic inductor current waveform (ISEN). Additionally, this ISEN signal is internally temperature compensated, allowing the ISEN indication to correctly track output current even as internal junction temperature changes due to self-heating and due to changes in ambient temperature. Figure 6 shows the current sensing circuit with ET4040.

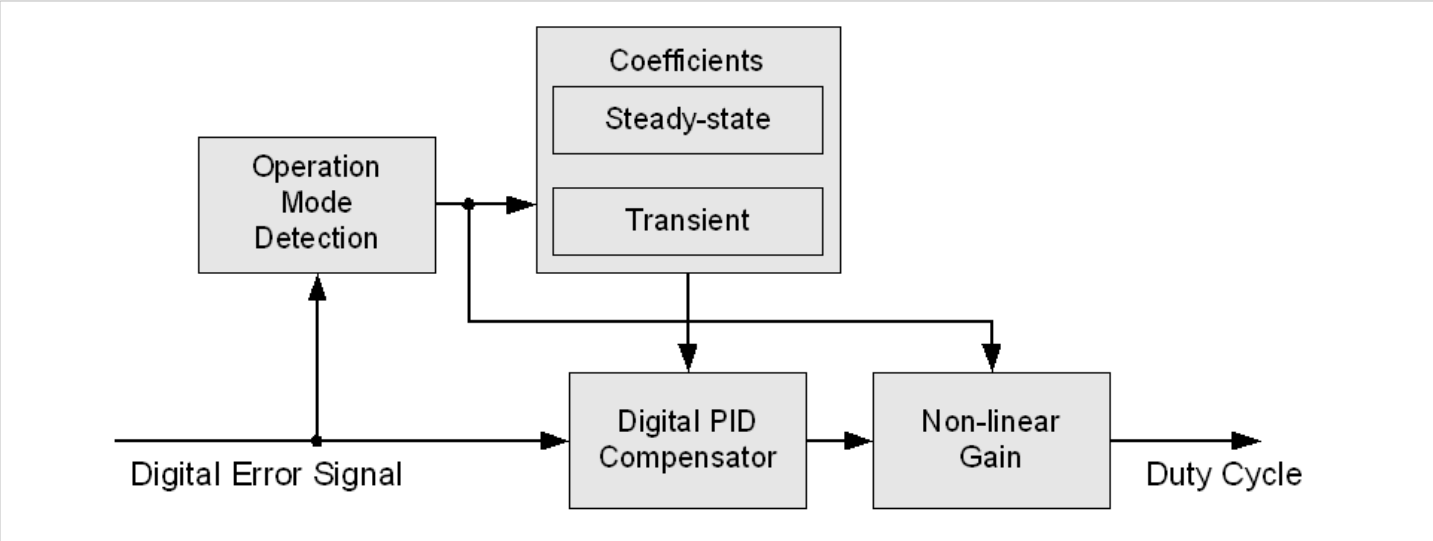

Figure 4: Simplified Block Diagram for the Digital Compensation

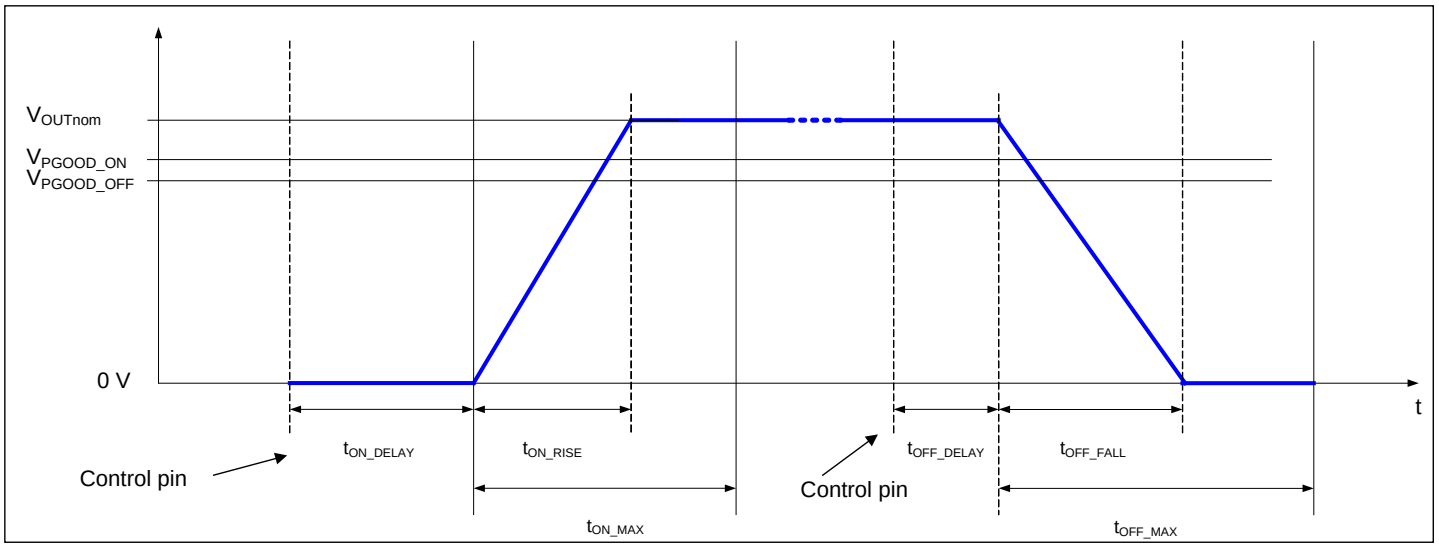

Figure 5: Power Sequencing

Temperature Measurement

The ED8106 features two independent temperature measurement units. The internal temperature sensing measures the temperature inside the IC; the external temperature sensing measures the voltage on the TEMP pin, which is coming from the TSEN temperature monitoring signal of Altera power train ET4040. This signal provides a thermal monitor that indicates the internal junction temperature of the ET4040.

Fault Monitoring and Response Generation

The ED8106 monitors various signals for possible fault conditions during operation. The fault thresholds of the ED8106 controllers are given in Table 2.

The controller fault handling will infinitely try to restart the converter on some of the fault conditions. In analog controllers, this infinite re-try feature is also known as “hiccup mode.”

Output Over/Under Voltage

To prevent damage to the load, the ED8106 utilizes an output over-voltage protection circuit. The voltage at VFBP is continuously compared with a configurable threshold using a high-speed analog comparator. If the voltage exceeds the configured threshold, the fault response is generated and the PWM output is set to low.

The ED8106 also monitors the output voltage with

a lower threshold. If the output voltage falls below the under-voltage fault level, a fault event is generated and the PWM output is set to tri-state condition.

Note that the fault thresholds are stored in the ED8106 as factors relative to the nominal output voltage. Hence, using the strapping options to change the output voltage level, also changes the fault thresholds.

Table 2: Fault Configuration Overview

Fault	Retries	Response
Output Over-Voltage	None	Low
Output Under-Voltage	Infinity	High-Z
Input Over-Voltage	Infinity	High-Z
Input Under-Voltage	Infinity	High-Z
Over-Current	Infinity	High-Z
External Over-Temperature	Infinity	Soft-off
Internal Over-Temperature	Infinity	Soft-off

Output Current Protection

The ED8106 continuously monitors the average inductor current and utilizes this information to protect the power supply against excessive output current.

Over-Temperature Protection

The ED8106 monitors internal and external temperature. For the temperature fault conditions a soft-off sequence is started. The soft-off sequence will ramp down the output voltage to 0V and set the PWM output in a tri-state condition.

Configuration and Engineering Mode

The ED8106 incorporates several different configuration parameters. These configuration parameters can be reconfigured during design time and then stored in the OTP. They cannot be changed during run-time.

In order to evaluate the device and its configuration on the bench, a special engineering mode is supported by the device and the ED81xx Power Designer GUI. In this mode, the device can be reconfigured multiple times without writing the configuration into the OTP. During this “engineering mode”, the device starts up after power-on reset in an unfigured state or a configured state if the OTP has already been configured. The ED81xx Power Designer then provides the configuration to the ED8106 enabling full operation which overwrites any configuration in the OTP if there is any. The user can use this mode to evaluate the configuration on the bench. However, the configuration will be lost upon power-on-reset.

After the user has determined the final configuration options, a configuration file or OTP image can be created that is then written into the blank un-configured ED8106. This can be either on the bench using the ED81xx Power Designer or in end-of-line testing during mass production.

The ED81xx Power Designer GUI communicates with the ED8106 via an I^2C interface in which the SCL signal is connected to the GPIO3 pin and the SDA signal is connected to the GPIO2 pin.

Application Information

The ED8106 controllers have been designed operate with the Altera ET4040 Power Train, which is a complete point-of-load solution for 40A output currents. This section includes information about the typical application circuits and recommended component values.

The pin-strap configuration options for the ED8106 are also documented in this section.

Typical Application Circuit

The schematic for the typical application circuits for the ED8106 is shown in Figure 6. A list of recommended component values for the passive components can be found in Table 3.

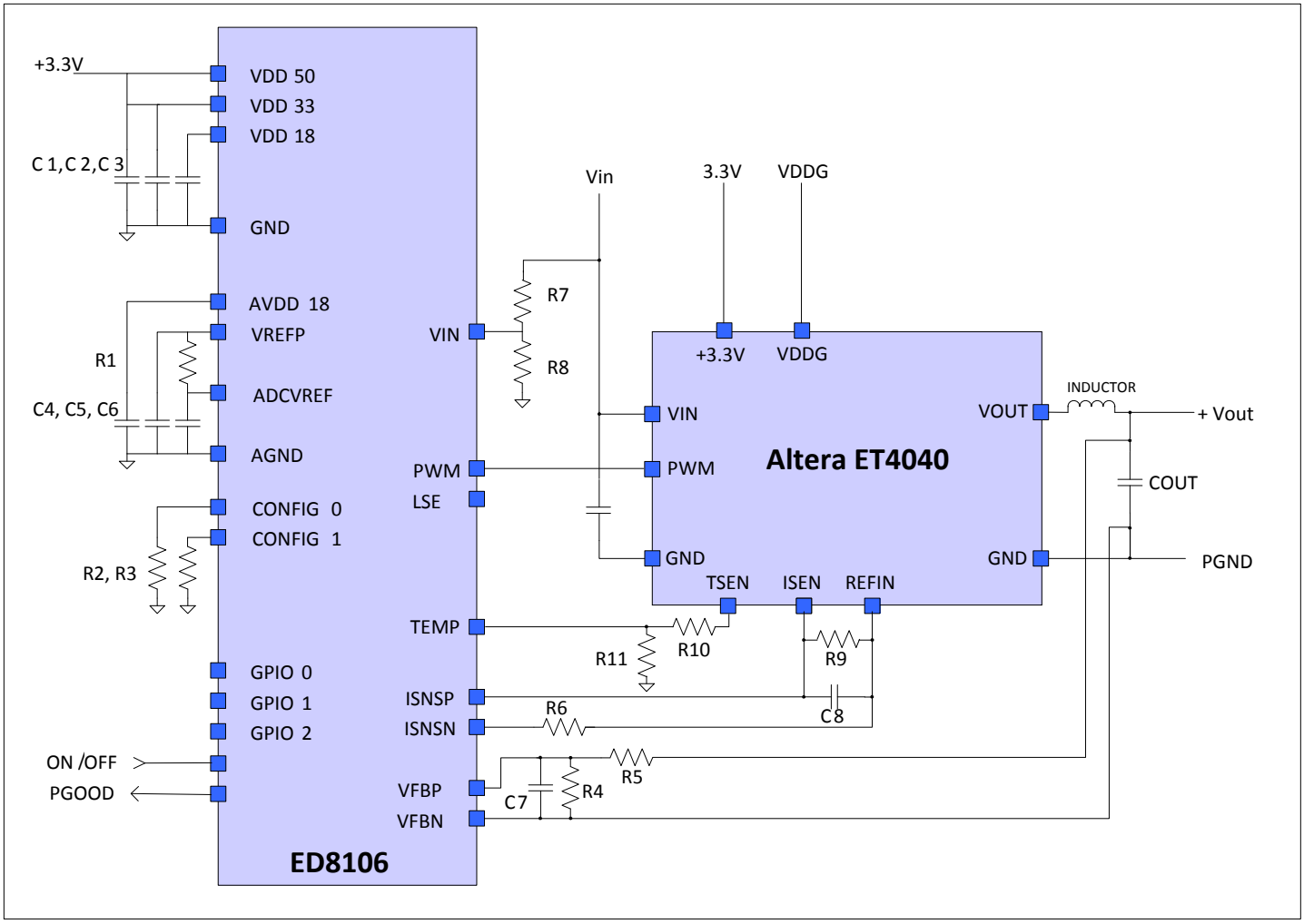

Figure 6: Application Circuit with a 3.3V Supply Voltage

Table 3: Passive Component Values for the Application Circuits

Reference Designator	Component value	Description
C1	1.0µF	Ceramic capacitor.
C2	4.7µF	Ceramic capacitor. Recommended 4.7µF; minimum 1.0µF.
C3	4.7µF	Ceramic capacitor. Recommended 4.7µF; minimum 1.0µF.
C4	4.7µF	Ceramic capacitor. Recommended 4.7µF; minimum 1.0µF.
C5	4.7µF	Ceramic capacitor. Recommended 4.7µF; minimum 1.0µF.
C6	100nF	

Reference Designator	Component value	Description
C7	22pF	Output voltage sense filtering capacitor. Recommended 22pF; maximum 1nF.
C8	0.1 µF	Current-sense filter capacitor.
CIN		Input filters capacitors. Can be a combination of ceramic and electrolytic capacitors.
COUT		Output filter capacitors
R1	51Ω	
R2, R3		Pin-strap configuration resistors.
R4	1.0kΩ	Output voltage feedback divider bottom resistor. Connect between the VFBP and VFBN pins.
R5	1.69kΩ	Output voltage feedback divider top resistor. Connect between the output terminal and the VFBP pin.
R6	1.5kΩ	Current sense resistor.
R7	9.1kΩ	Input voltage divider top resistor. Connect between the main power input and the VIN pin of the ED8106.
R8	1.0kΩ	Input voltage divider bottom resistor. Connect between the VIN and AGND pins of the ED8106.
R9	1.5kΩ	Current sense resistor.
R10	10kΩ	
R11	20kΩ	

Pin Strap Options of the ED8106

The ED8106 supports multiple sets of configuration options that allow the user to employ two simple resistors to select various options from user-configured look-up tables that are stored in the nonvolatile memory (NVM).

The ED81xx Power Designer GUI is used to define the tables and store them in NVM. For the end user, the configuration is dramatically simplified by using the pin strap features to select the following parameters:

- Output Voltage
- Compensation
- Over-Current Protection Threshold
- Ramp-up Time

The CONFIG0 pin is recommended to be used to select the nominal output voltage and the compensation loop parameters of the non-isolated DC/DC converter. The capacitance value of ceramic capacitor may change with applied voltage. It might need different compensation parameters at different output voltage. The CONFIG1 is recommended to be used to select the OCP threshold in combination with the turn-on rise time for the output voltage during the power-up sequence.

The CONFIG0 and CONFIG1 pins are used to determine the index of the selected values using the resistor values listed in Table 4. Each pin provides 8 configuration indexes based on resistor values. A resistor variation of ~2% is taken into account for initial tolerance and temperature dependency. The values are read during the initialization phase and then used to look up the selected values from the user-configured look-up tables. The user can freely correlate the two configuration pins with the four parameters to choose the optimal configuration options for the desired application. A total of four compensation settings and 8 values for each of the other parameters are available.

Table 4: Pin Strap Resistor Values

Index	Resistor Value
0	0Ω
1	1.5 kΩ
2	3.3 kΩ
3	5.6 kΩ
4	8.2 kΩ
5	12 kΩ
6	15 kΩ
7	22 kΩ

Mechanical Specifications

Based on JEDEC MO-220, all dimensions are in millimeters.

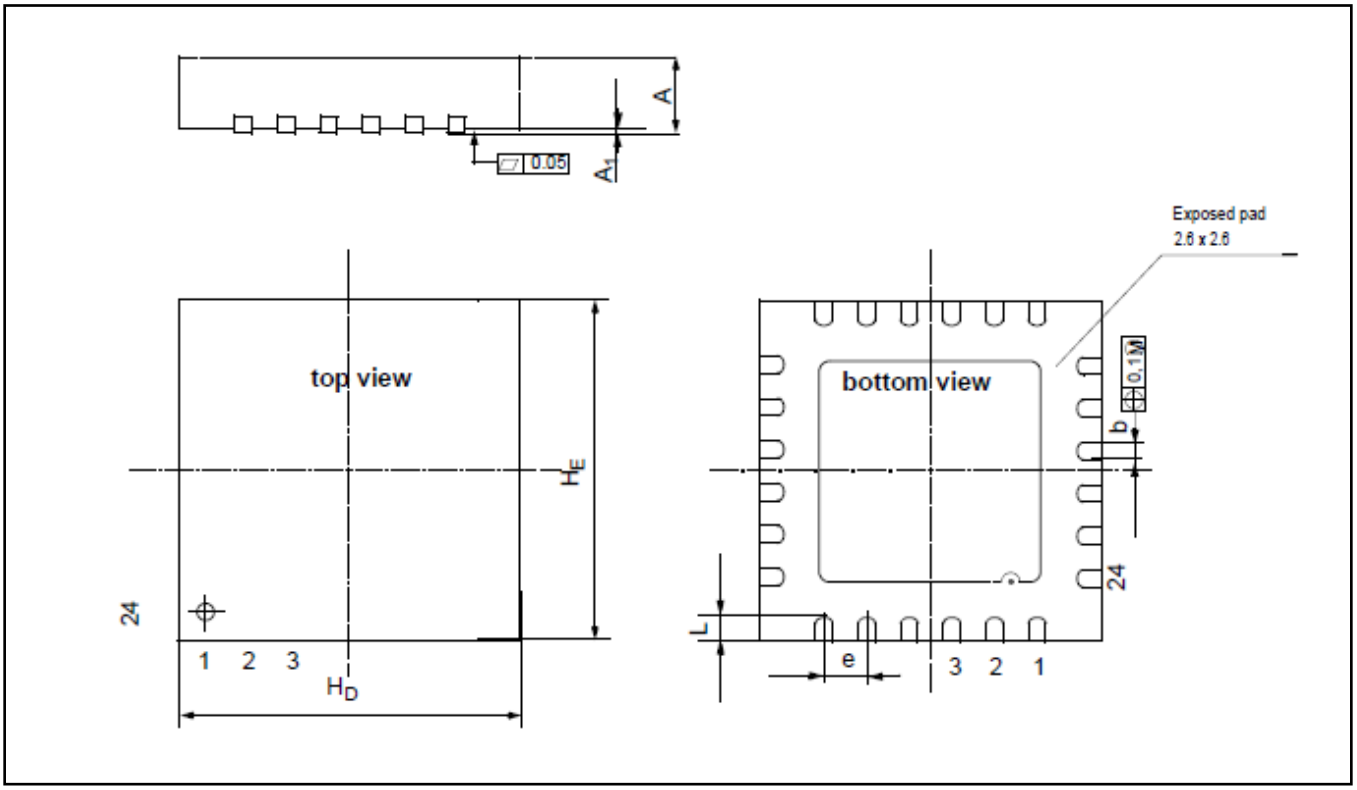

Figure 7: 24-pin QFN Package Drawing

Dimension	Min (mm)	Max (mm)
A	0.8	0.90
A_1	0.00	0.05
b	0.18	0.30
e	0.5 nominal	
H_D	3.90	4.1
H_E	3.90	4.1
L	0.35	0.45

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