MAX 7000B

Programmable Logic Device Family

February 2000, ver. 2.0 Data Sheet

Features...

Preliminary Information

- High-performance 2.5-V CMOS EEPROM-based programmable logic devices (PLDs) built on second-generation Multiple Array MatriX (MAX®) architecture (see Table 1)
  - Pin-compatible with the popular 5.0-V MAX 7000S and 3.3-V MAX 7000A device families
  - High-density PLDs ranging from 600 to 10,000 usable gates
  - 3.5-ns pin-to-pin logic delays with counter frequencies in excess of 285.7 MHz
- Advanced 2.5-V in-system programmability (ISP)
  - Programs through the built-in IEEE Std. 1149.1 Joint Test Action Group (JTAG) interface with advanced pin-locking capability
  - Enhanced ISP algorithm for faster programming
  - ISP_Done bit to ensure complete programming
  - Pull-up resistor on I/O pins during in-system programming

For information on in-system programmable 5.0-V MAX 7000S or 3.3-V MAX 7000A devices, see the *MAX 7000 Programmable Logic Device Family Data Sheet* or the *MAX 7000A Programmable Logic Device Family Data Sheet*.

Table 1. MAX 7000B Device Features *Note (1)*

Feature	EPM7032B	EPM7064B	EPM7128B	EPM7256B	EPM7512B
Usable gates	600	1,250	2,500	5,000	10,000
Macrocells	32	64	128	256	512
Logic array blocks	2	4	8	16	32
Maximum user I/O pins	36	68	100	164	212
t_{PD} (ns)	3.5	3.5	4.5	5.0	6.0
t_{SU} (ns)	2.8	2.7	3.5	3.8	4.3
t_{FSU} (ns)	1.0	1.0	1.0	1.0	2.0
t_{CO1} (ns)	1.9	2.0	2.5	2.9	3.9
f_{CNT} (MHz)	285.7	277.8	212.8	188.7	147.1

Note:
(1) Contact Altera for up-to-date information on timing information.

A-DS-MAX7000B-01.1

…and More Features

- System-level features
  - MultiVolt™ I/O interface enabling device core to run at 2.5 V, while I/O pins are compatible with 3.3-V, 2.5-V, and 1.8-V logic levels
  - Programmable power-saving mode for 50% or greater power reduction in each macrocell
  - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
  - Support for advanced I/O standards, including stub-series terminated logic (SSTL-2 and SSTL-3) and Gunning transceiver logic (GTL+)
  - Bus-hold option on I/O pins
  - Peripheral component interconnect (PCI) compatible
  - Bus friendly architecture including programmable slew-rate control
  - Open-drain output option
  - Programmable security bit for protection of proprietary designs
  - Built-in boundary-scan test circuitry compliant with IEEE Std. 1149.1
  - Supports hot-socketing operation
  - Programmable ground pins
- Advanced architecture features
  - Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
  - Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
  - Programmable macrocell registers with individual clear, preset, clock, and clock enable controls
  - Two global clock signals with optional inversion
  - Programmable power-up states for macrocell registers
  - 6 to 10 pin- or logic-driven output enable signals
- Advanced package options
  - Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), ball-grid array (BGA), space-saving FineLine BGA™, 0.8-mm Ultra FineLine BGA, and plastic J-lead chip carrier (PLCC) packages
  - Pin-compatibility with other MAX 7000B devices in the same package
- Advanced software support
  - Software design support and automatic place-and-route provided by Altera's Quartus™ development system for Windows-based PCs and Sun SPARCstation and HP 9000 Series 700/800 workstations, and the MAX+PLUS® II development system for Windows-based PCs and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations

- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPMs), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), MasterBlaster™ serial / universal serial bus (USB) communications cable, and ByteBlasterMV™ parallel port download cable, as well as programming hardware from third-party manufacturers and any Jam™ STAPL File (**.jam**), Jam Byte-Code File (**.jbc**), or Serial Vector Format File (**.svf**)-capable in-circuit tester

General Description

MAX 7000B devices are high-density, high-performance devices based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000B devices operate with a 2.5-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 3.5 ns, and counter speeds up to 285.7 MHz. All MAX 7000B device speed grades are compatible with the timing requirements of the PCI Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2***. See Table 2.

Table 2. MAX 7000B Speed Grades *Notes (1), (2)*

Device	Speed Grade					
	-3	-4	-5	-6	-7	-10
EPM7032B	✓		✓		✓	
EPM7064B	✓		✓		✓	
EPM7128B		✓			✓	✓
EPM7256B			✓		✓	✓
EPM7512B				✓	✓	✓

Notes:
(1) Contact Altera Marketing for up-to-date information on available device speed grades.
(2) Timing parameters are preliminary.

The MAX 7000B architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000B devices are available in a wide range of packages, including PLCC, BGA, FineLine BGA, 0.8-mm Ultra FineLine BGA, PQFP, TQFP, and VTQFP packages. See Table 3.

Table 3. MAX 7000B Maximum User I/O Pins *Notes (1), (2)*

Device	44-Pin PLCC	44-Pin TQFP	48-Pin VTQFP	49-Pin 0.8-mm Ultra FineLine BGA *(3)*	100-Pin TQFP	100-Pin FineLine BGA *(4)*	144-Pin TQFP	169-Pin 0.8-mm Ultra FineLine BGA *(3)*	208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA *(4)*
EPM7032B	36	36	36								
EPM7064B	36	36	36	✓ *(1)*	68	68		✓ *(1)*			68
EPM7128B			40	✓ *(1)*	84	84	100	✓ *(1)*			100
EPM7256B					84	84	120	✓ *(1)*	164		164
EPM7512B					84		120		176	212	212

Notes:

(1) Contact Altera for up-to-date information on available device package options.

(2) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.

(3) All 0.8-mm BGA packages are footprint-compatible via the SameFrame™ pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 14 for more details.

(4) All FineLine BGA packages are footprint-compatible via the SameFrame pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 14 for more details.

MAX 7000B devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000B architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000B devices contain 32 to 512 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

MAX 7000B devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000B devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000B devices can be set for 3.3 V, 2.5 V, or 1.8 V and all input pins are 3.3-V, 2.5-V, and 1.8-V tolerant, allowing MAX 7000B devices to be used in mixed-voltage systems.

MAX 7000B devices are supported by the Quartus and MAX+PLUS II development systems, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The Quartus and MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The Quartus software runs on Windows-based PCs, as well as Sun SPARCstation and HP 9000 Series 700/800 workstations. The MAX+PLUS II software runs on Windows-based PCs, as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations.

For more information on development tools, see the *Quartus Programmable Logic Development System & Software Data Sheet* and the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*.

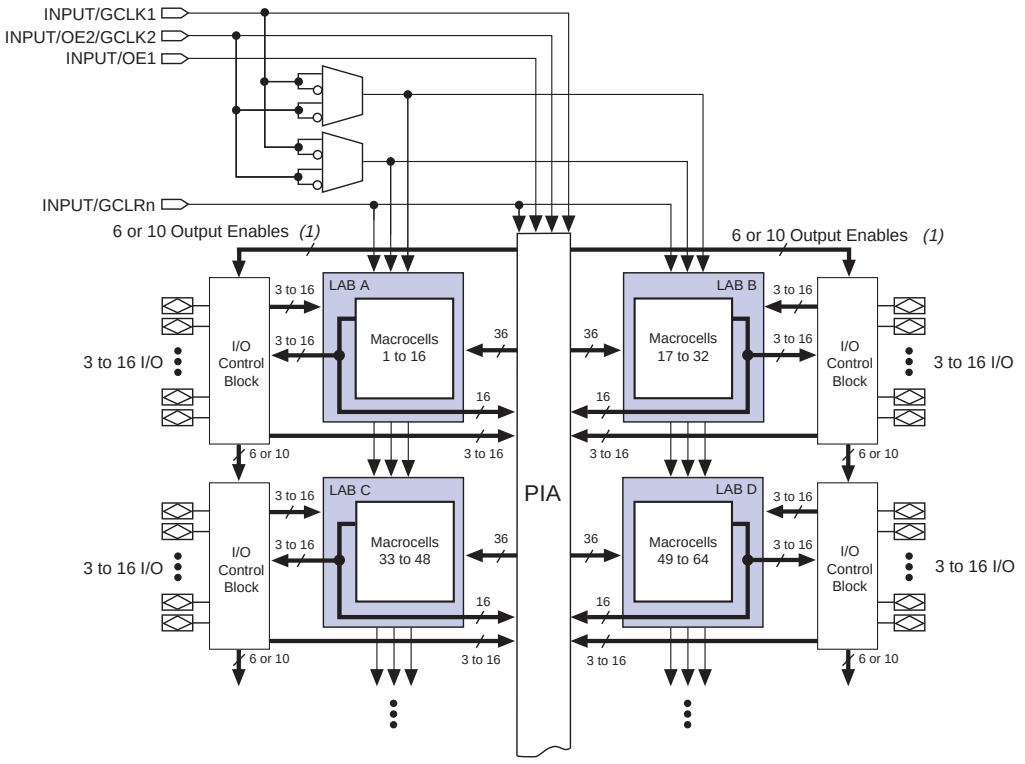
Functional Description

The MAX 7000B architecture includes the following elements:

- LABs
- Macrocells
- Expander product terms (shareable and parallel)
- PIA
- I/O control blocks

The MAX 7000B architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of MAX 7000B devices.

Figure 1. MAX 7000B Device Block Diagram



Note:

(1) EPM7032B, EPM7064B, EPM7128B, and EPM7256B devices have six output enables. EPM7512B devices have ten output enables.

Logic Array Blocks

The MAX 7000B device architecture is based on the linking of high-performance LABs. LABs consist of 16 macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

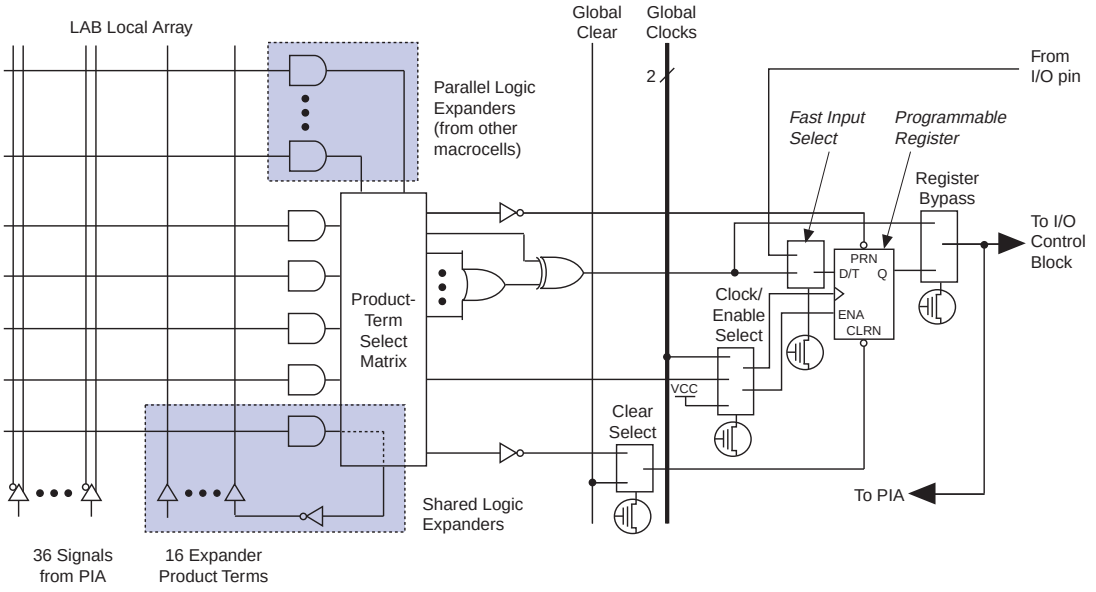
Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

Macrocells

The MAX 7000B macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. Figure 2 shows the MAX 7000B macrocell.

Figure 2. MAX 7000B Macrocell



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The MAX+PLUS II development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the MAX+PLUS II software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- Global clock signal. This mode achieves the fastest clock-to-output performance.
- Global clock signal enabled by an active-high clock enable. A clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- Array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available in MAX 7000B devices. As shown in Figure 1, these global clock signals can be the true or the complement of either of the global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in Figure 2, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear from the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn). Upon power-up, each register in a MAX 7000B device may be set to either a high or low state. This power-up state is specified at design entry.

All MAX 7000B I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be clocked to an input D flipflop with an extremely fast input setup time. The input path from the I/O pin to the register has a programmable delay element that can be selected to either guarantee zero hold time or to get the fastest possible set-up time (as fast as 1.0 ns).

Expander Product Terms

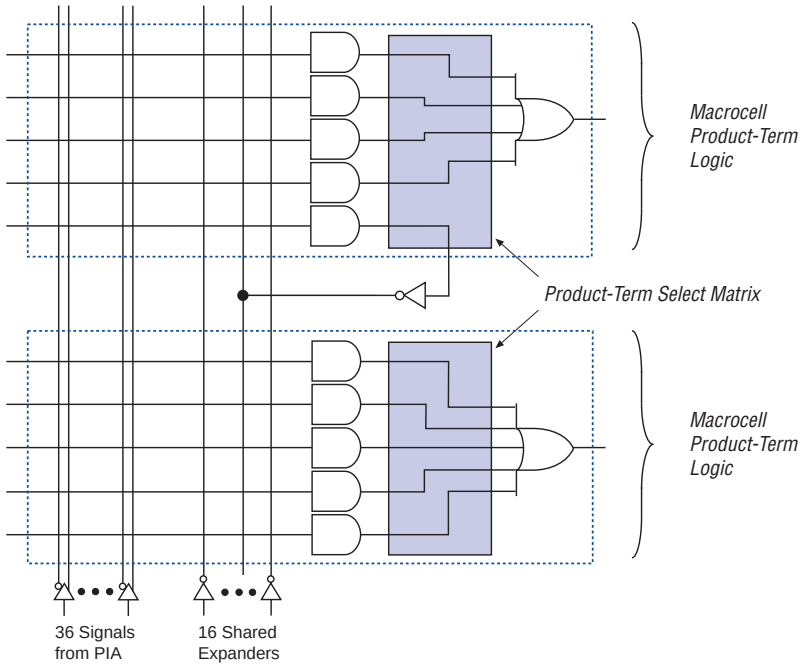
Although most logic functions can be implemented with the five product terms available in each macrocell, more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources. However, the MAX 7000B architecture also offers both shareable and parallel expander product terms (“expanders”) that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay (t_{SEXP}) is incurred when shareable expanders are used. Figure 3 shows how shareable expanders can feed multiple macrocells.

Figure 3. MAX 7000B Shareable Expanders

Shareable expanders can be shared by any or all macrocells in an LAB.



Parallel Expanders

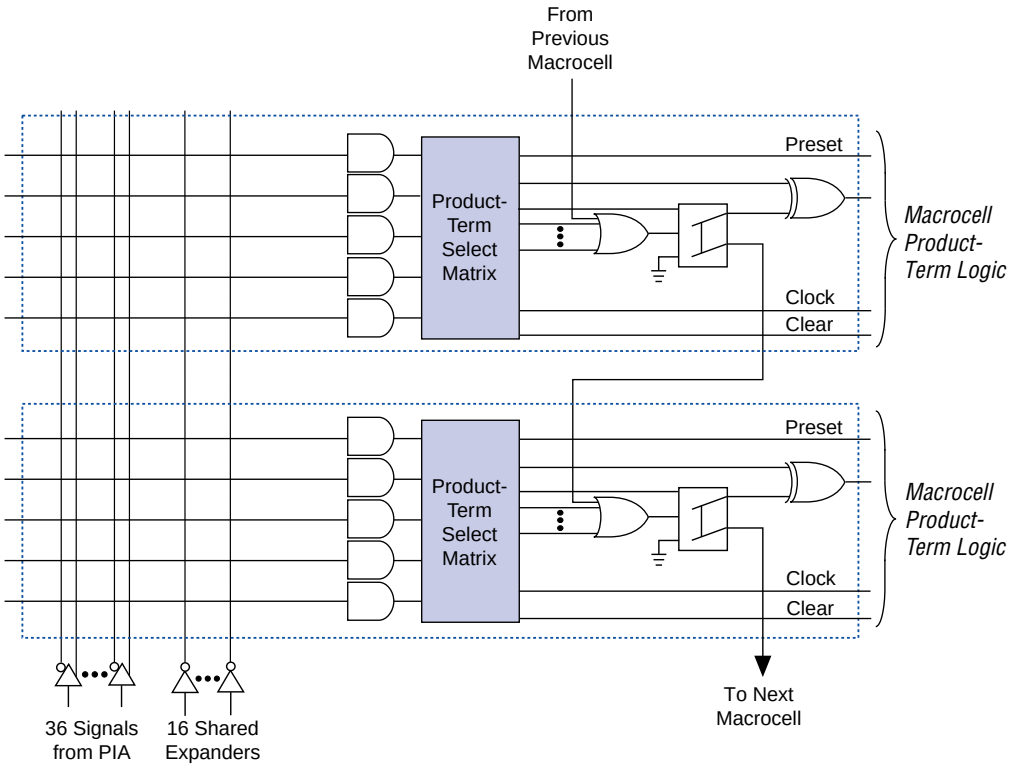
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The MAX+PLUS II Compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8, and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 4. MAX 7000B Parallel Expanders

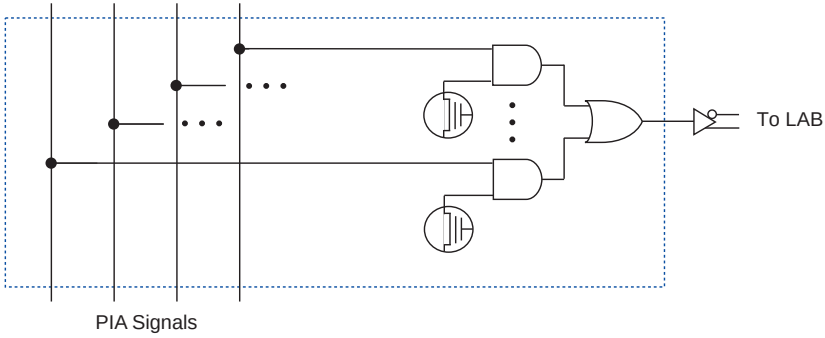
Unused product terms in a macrocell can be allocated to a neighboring macrocell.



Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000B dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a two-input AND gate, which selects a PIA signal to drive into the LAB.

Figure 5. MAX 7000B PIA Routing

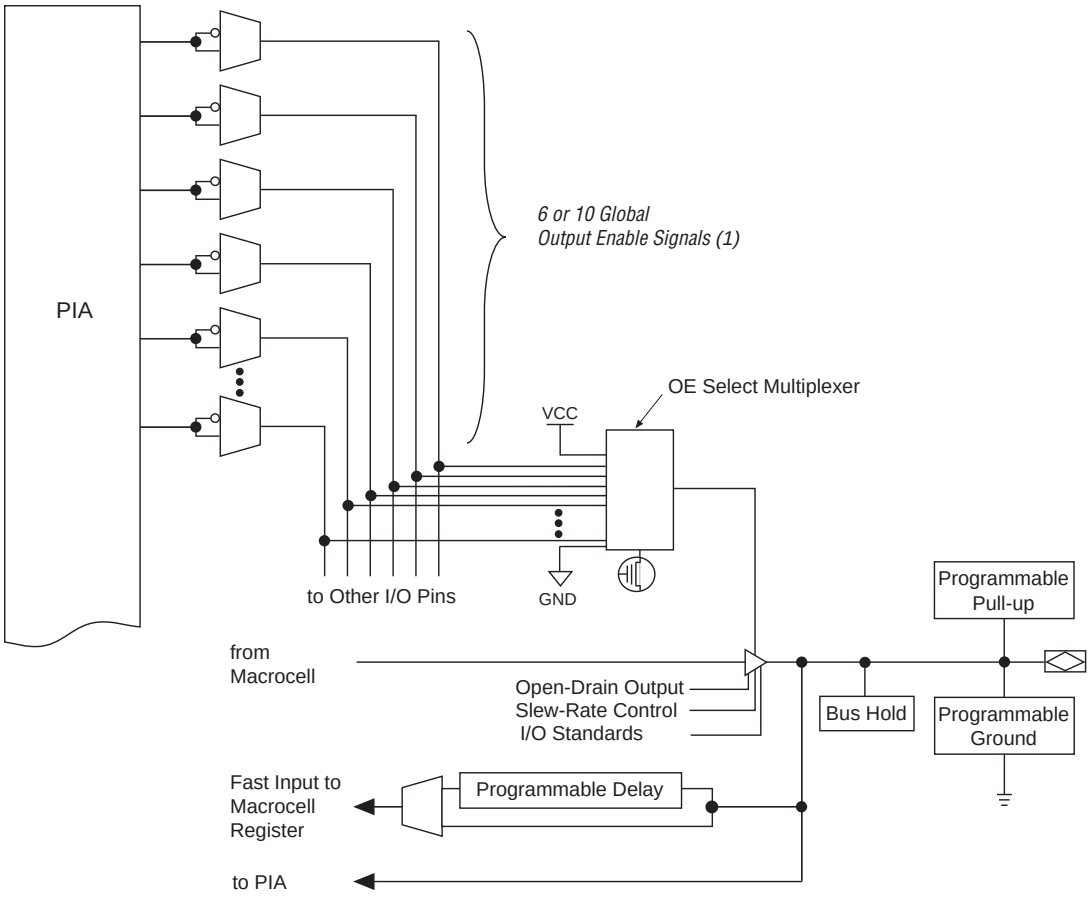


While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 7000B PIA has a predictable delay. The PIA makes a design's timing performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC}. Figure 6 shows the I/O control block for MAX 7000B devices. The I/O control block has six or ten global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

Figure 6. I/O Control Block of MAX 7000B Devices



Note:

(1) EPM7032B, EPM7064B, EPM7128B, and EPM7256B devices have six output enable signals. EPM7512B devices have ten output enable signals.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to V_{CC}, the output is enabled.

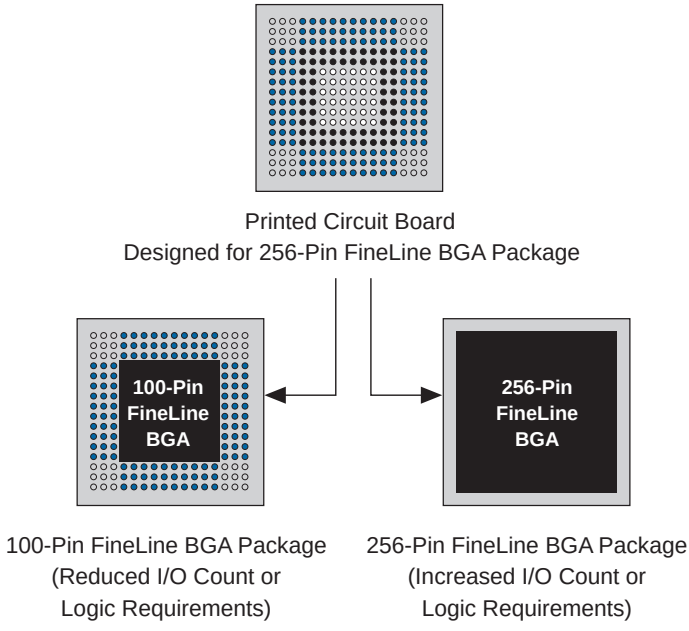
The MAX 7000B architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

SameFrame Pin-Outs

MAX 7000B devices support the SameFrame pin-out feature for FineLine BGA and 0.8-mm Ultra FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA and 0.8-mm Ultra FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. FineLine BGA packages are compatible with other FineLine BGA packages, and 0.8-mm Ultra FineLine BGA packages are compatible with other 0.8-mm Ultra FineLine BGA packages. A given printed circuit board (PCB) layout can support multiple device density / package combinations. For example, a single board layout can support a range of devices from an EPM7064B device in a 100-pin FineLine BGA package to an EPM7512B device in a 256-pin FineLine BGA package.

The Quartus and MAX+PLUS II software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The Quartus and MAX+PLUS II software generates pin-outs describing how to layout a board to take advantage of this migration (see Figure 7).

Figure 7. SameFrame Pin-Out Example



In-System Programmability (ISP)

MAX 7000B devices can be programmed in-system via an industry-standard 4-pin IEEE Std. 1149.1 (JTAG) interface. ISP offers quick, efficient iterations during design development and debugging cycles. The MAX 7000B architecture internally generates the high programming voltages required to program EEPROM cells, allowing in-system programming with only a single 2.5-V power supply. During in-system programming, the I/O pins are tri-stated and weakly pulled-up to eliminate board conflicts. The pull-up value is nominally 50 kΩ.

MAX 7000B devices have an enhanced ISP algorithm for faster programming. These devices also offer an ISP_Done bit that provides safe operation when in-system programming is interrupted. This ISP_Done bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a PCB with standard pick-and-place equipment before they are programmed. MAX 7000B devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera MasterBlaster communications cable, and the ByteBlasterMV parallel port download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000B devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. A constant algorithm uses a pre-defined (non-adaptive) programming sequence that does not take advantage of adaptive algorithm programming time improvements. Some in-circuit testers cannot program using an adaptive algorithm. Therefore, a constant algorithm must be used. MAX 7000B devices can be programmed with either an adaptive or constant (non-adaptive) algorithm.

The Jam Standard Test and Programming Language (STAPL), JEDEC standard JESD-71, can be used to program MAX 7000B devices with in-circuit testers, PCs, or embedded processors.

For more information on using the Jam language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)* and *Application Note 122 (Using STAPL for ISP & ICR via an Embedded Processor).*

Programming with External Hardware

MAX 7000B devices can be programmed on Windows-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.

For more information, see the *Altera Programming Hardware Data Sheet*.

The MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional device behavior with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers provide programming support for Altera devices. For more information, see *Programming Hardware Manufacturers*.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

MAX 7000B devices include the JTAG boundary-scan test circuitry defined by IEEE Std. 1149.1. Table 4 describes the JTAG instructions supported by MAX 7000B devices. The pin-out tables starting on page 54 of this data sheet show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

Table 4. MAX 7000B JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the boundary-scan test data to pass synchronously through a selected device to adjacent devices during normal operation.
CLAMP	Allows the values in the boundary-scan register to determine pin states while placing the 1-bit bypass register between the `TDI` and `TDO` pins.
IDCODE	Selects the IDCODE register and places it between the `TDI` and `TDO` pins, allowing the IDCODE to be serially shifted out of `TDO`.
USERCODE	Selects the 32-bit USERCODE register and places it between the `TDI` and `TDO` pins, allowing the USERCODE value to be shifted out of `TDO`.
ISP Instructions	These instructions are used when programming MAX 7000B devices via the JTAG ports with the MasterBlaster, ByteBlaster, or ByteBlasterMV download cable, or using a Jam File (**.jam**), Jam Byte-Code File (**.jbc**), or Serial Vector Format File (**.svf**) via an embedded processor or test equipment.

The instruction register length of MAX 7000B devices is ten bits. The MAX 7000B USERCODE register length is 32 bits. Tables 5 and 6 show the boundary-scan register length and device IDCODE information for MAX 7000B devices.

Table 5. MAX 7000B Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM7032B	96
EPM7064B	192
EPM7128B	288
EPM7256B	480
EPM7512B	624

Table 6. 32-Bit MAX 7000B Device IDCODE *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) *(2)*
EPM7032B	0010	0111 0000 0011 0010	00001101110	1
EPM7064B	0010	0111 0000 0110 0100	00001101110	1
EPM7128B	0010	0111 0001 0010 1000	00001101110	1
EPM7256B	0010	0111 0010 0101 0110	00001101110	1
EPM7512B	0010	0111 0101 0001 0010	00001101110	1

Notes:
(1) The most significant bit (MSB) is on the left.
(2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)* for more information on JTAG boundary-scan testing.

Figure 8 shows the timing information for the JTAG signals.

Figure 8. MAX 7000B JTAG Waveforms

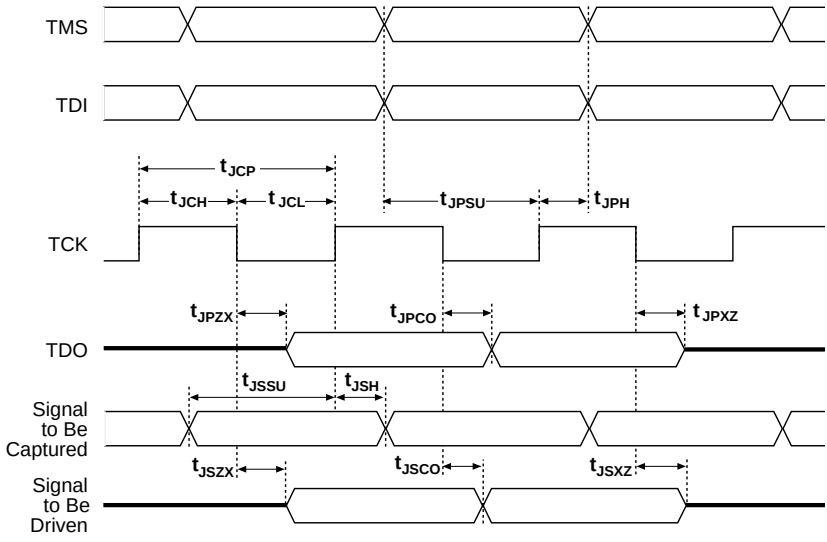


Table 7 shows the JTAG timing parameters and values for MAX 7000B devices.

Table 7. JTAG Timing Parameters & Values for MAX 7000B Devices
Note (1)

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		25	ns
t_{JSZX}	Update register high impedance to valid output		25	ns
t_{JSXZ}	Update register valid output to high impedance		25	ns

Note:
(1) Timing parameters in this table apply to all VCCIO levels.

Programmable Speed/Power Control

MAX 7000B devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000B device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters.

Output Configuration

MAX 7000B device outputs can be programmed to meet a variety of system-level requirements.

MultiVolt I/O Interface

The MAX 7000B device architecture supports the MultiVolt I/O interface feature, which allows MAX 7000B devices to connect to systems with differing supply voltages. MAX 7000B devices in all packages can be set for 3.3-V, 2.5-V, or 1.8-V pin operation. These devices have one set of V_{CC} pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCIO pins can be connected to either a 3.3-V, 2.5-V, or 1.8-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When the VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels of 2.5 V or 1.8 V incur a nominal timing delay adder.

Table 8 describes the MAX 7000B MultiVolt I/O support.

Table 8. MAX 7000B MultiVolt I/O Support

V_{CCIO} (V)	Input Signal (V)				Output Signal (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓	✓		✓			
2.5	✓	✓	✓			✓		
3.3	✓	✓	✓				✓	✓

Open-Drain Output Option

MAX 7000B devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

Programmable Ground Pins

Each unused I/O pin on MAX 7000B devices may be used as an additional ground pin. This programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

Slew-Rate Control

The output buffer for each MAX 7000B I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

Advanced I/O Standard Support

The MAX 7000B I/O pins support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, GTL+, SSTL-3 Class I and II, and SSTL-2 Class I and II.

MAX 7000B devices contain two I/O banks. Both banks support all standards. Each I/O bank has its own VCCIO pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Within a bank, any one of the terminated standards can be supported.

Figure 9 shows the arrangement of the MAX 7000B I/O banks.

Figure 9. MAX 7000B I/O Banks for Various Advanced I/O Standards

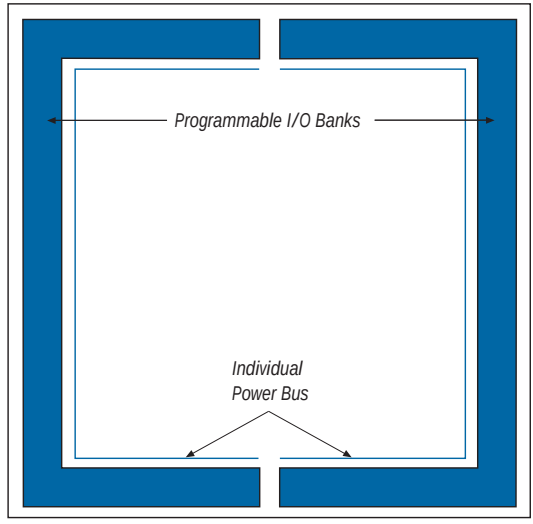


Table 9 shows which macrocells have pins in each I/O bank.

Table 9. Macrocells Contained in Each I/O Bank

Device	Bank 1	Bank 2
EPM7032B	1-16	17-32
EPM7064B	1-32	33-64
EPM7128B	1-64	65-128
EPM7256B	1-128, 177-181	129-176, 182-256
EPM7512B	1-265	266-512

Each MAX 7000B device has two VREF pins. Each can be set to a separate VREF level. Any I/O pin that uses one of the voltage-referenced standards (GTL+, SSTL2, or SSTL3) may use either of the two VREF pins. If these pins are not required as VREF pins, they may be individually programmed to function as user I/O pins.

Programmable Pull-Up Resistor

Each MAX 7000B device I/O pin provides an optional programmable pull-up resistor during user mode. When this feature is enabled for an I/O pin, the pull-up resistor (typically 50 kΩ) weakly holds the output to V_{CCIO} level.

Bus Hold

Each MAX 7000B device I/O pin provides an optional bus-hold feature. When this feature is enabled for an I/O pin, the bus-hold circuitry weakly holds the signal at its last driven state. By holding the last driven state of the pin until the next input signals is present, the bus-hold feature can eliminate the need to add external pull-up or pull-down resistors to hold a signal level when the bus is tri-stated. The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. This feature can be selected individually for each I/O pin. The bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals.

The bus-hold circuitry weakly pulls the signal level to the last driven state through a resistor with a nominal resistance (RBH) of approximately 8.5 kΩ. Table 10 gives specific sustaining current that will be driven through this resistor and overdrive current that will identify the next driven input level. This information is provided for each VCCIO voltage level.

Table 10. Bus Hold Parameters

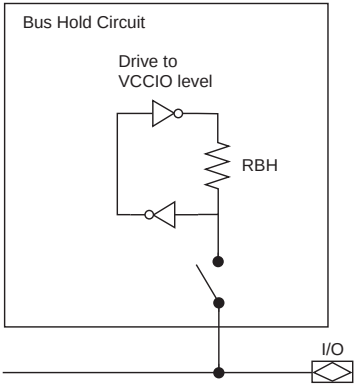
Parameter	Conditions	VCCIO Level						Units
		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	
Low sustaining current	$V_{IN} > V_{IL}$ (max)	30		50		70		µA
High sustaining current	$V_{IN} < V_{IH}$ (min)	–30		–50		–70		µA
Low overdrive current	$0 V < V_{IN} < V_{CCIO}$		200		300		500	µA
High overdrive current	$0 V < V_{IN} < V_{CCIO}$		–295		–435		–680	µA

The bus-hold circuitry is active only during user operation. At power-up, the bus-hold circuit initializes its initial hold value as V_{CC} approaches the recommended operation conditions. When transitioning from ISP to User Mode with bus hold enabled, the bus-hold circuit captures the value present on the pin at the end of programming.

Two inverters implement the bus-hold circuitry in a loop that weakly drives back to the I/O pin at the end of programming.

Figure 10 shows a block diagram of the bus-hold circuit.

Figure 10. Bus-Hold Circuit



Power Sequencing & Hot-Socketing

Because MAX 7000B devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into MAX 7000B devices before and during power up without damaging the device. Additionally, MAX 7000B devices do not drive out during power up. Once operating conditions are reached, MAX 7000B devices operate as specified by the user.

Design Security

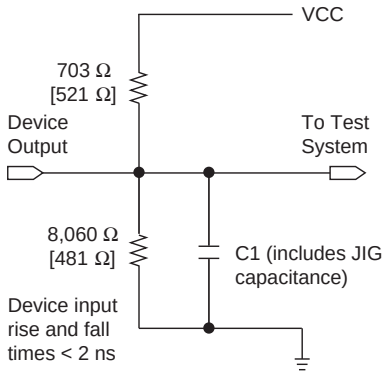
All MAX 7000B devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

Generic Testing

MAX 7000B devices are fully functionally tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 11. Test patterns can be used and then erased during early stages of the production flow.

Figure 11. MAX 7000B AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V outputs. Numbers without brackets are for 3.3-V outputs.



Operating Conditions

Tables 11 through 14 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 7000B devices.

Table 11. MAX 7000B Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage		–0.5	3.6	V
V_{CCIO}	Supply voltage		–0.5	3.6	V
V_I	DC input voltage	*(2)*	–2.0	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_A	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias	–65	135	° C

Table 12. MAX 7000B Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers		2.375	2.625	V
V_{CCIO}	Supply voltage for output drivers, 3.3-V operation		3.0	3.6	V
	Supply voltage for output drivers, 2.5-V operation		2.375	2.625	V
	Supply voltage for output drivers, 1.8-V operation		1.71	1.89	V
V_{CCISP}	Supply voltage during in-system programming		2.375	2.625	V
V_I	Input voltage	*(3)*	–0.5	3.9	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Junction temperature	For commercial use	0	90	° C
		For industrial use	–40	105	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 13. MAX 7000B Device DC Operating Conditions *Note (4)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage for 3.3 V TTL/CMOS and 2.5 V TTL/CMOS		1.7	3.9	V
	High-level input voltage for 1.8 V TTL/CMOS		0.65 VCCIO	2.25	V
V_{IL}	Low-level input voltage for 3.3 V TTL/CMOS, 2.5 V TTL/CMOS, and PCI compliance		–0.5	0.8	V
	Low-level input voltage for 1.8 V TTL/CMOS		–0.5	0.35 VCCIO	
V_{OH}	3.3-V high-level TTL output voltage	I_{OH} = –8 mA DC, V_{CCIO} = 3.00 V *(5)*	2.4		V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(5)*	V_{CCIO} – 0.2		V
	2.5-V high-level output voltage	I_{OH} = –100 µA DC, V_{CCIO} = 2.30 V *(5)*	2.1		V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V *(5)*	2.0		V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V *(5)*	1.7		V
	1.8-V high-level output voltage	I_{OH} = –2 mA DC, V_{CCIO} =1.65 V *(5)*	1.2		V
V_{OL}	3.3-V low-level TTL output voltage	I_{OL} = 8 mA DC, V_{CCIO} = 3.00 V *(6)*		0.4	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(6)*		0.2	V
	2.5-V low-level output voltage	I_{OL} = 100 µA DC, V_{CCIO} = 2.30 V *(6)*		0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(6)*		0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(6)*		0.7	V
	1.8-V low-level output voltage	I_{OL} = 2 mA DC, V_{CCIO} = 1.7 V *(6)*		0.4	V
I_I	Input leakage current	V_I = V_{CCINT} or ground	–5	5	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CCINT} or ground	–5	5	µA
R_{ISP}	Value of I/O pin pull-up resistor during in-system programming or during power-up	V_{CCIO} = 1.7 to 3.6 V *(7)*	20	74	kΩ

Table 14. MAX 7000B Device Capacitance *Note (8)*

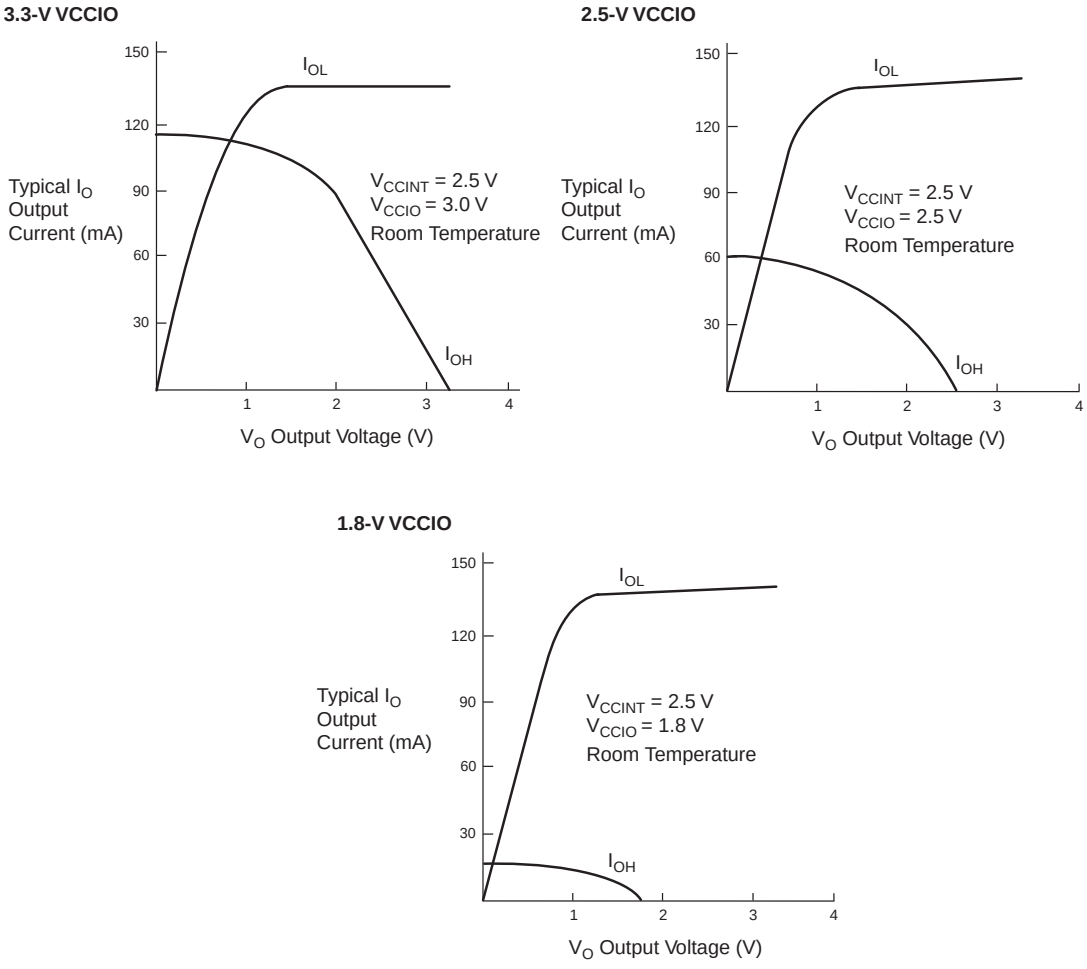
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) All pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(4) These values are specified under the Recommended Operating Conditions in Table 12 on page 25.
(5) The parameter is measured with 50% of the outputs each sourcing the specified current. The I_{OH} parameter refers to high-level TTL or CMOS output current.
(6) The parameter is measured with 50% of the outputs each sinking the specified current. The I_{OL} parameter refers to low-level TTL or CMOS output current.
(7) This pull-up exists while devices are being programmed in-system and in unprogrammed devices during power-up. The pull-up resistor is from the pins to V_{CCIO}.
(8) Capacitance is measured at 25° C and is sample-tested only. Two of the dedicated input pins (`OE1` and `GCLRN`) have a maximum capacitance of 15 pF.

Figure 12 shows the typical output drive characteristics of MAX 7000B devices.

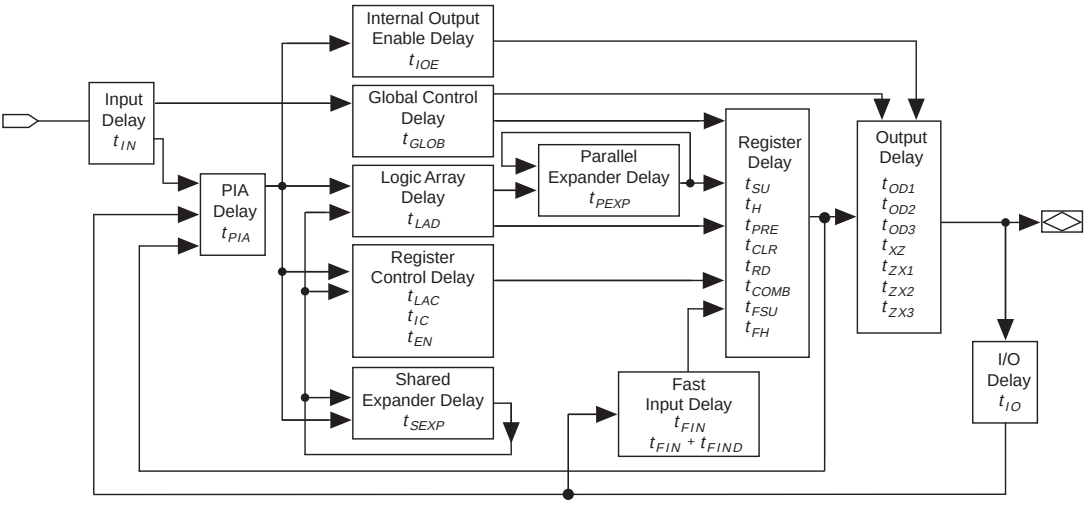
Figure 12. Output Drive Characteristics of MAX 7000B Devices



Timing Model

MAX 7000B device timing can be analyzed with the Quartus and MAX+PLUS II software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 13. MAX 7000B devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The MAX+PLUS II software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 13. MAX 7000B Timing Model

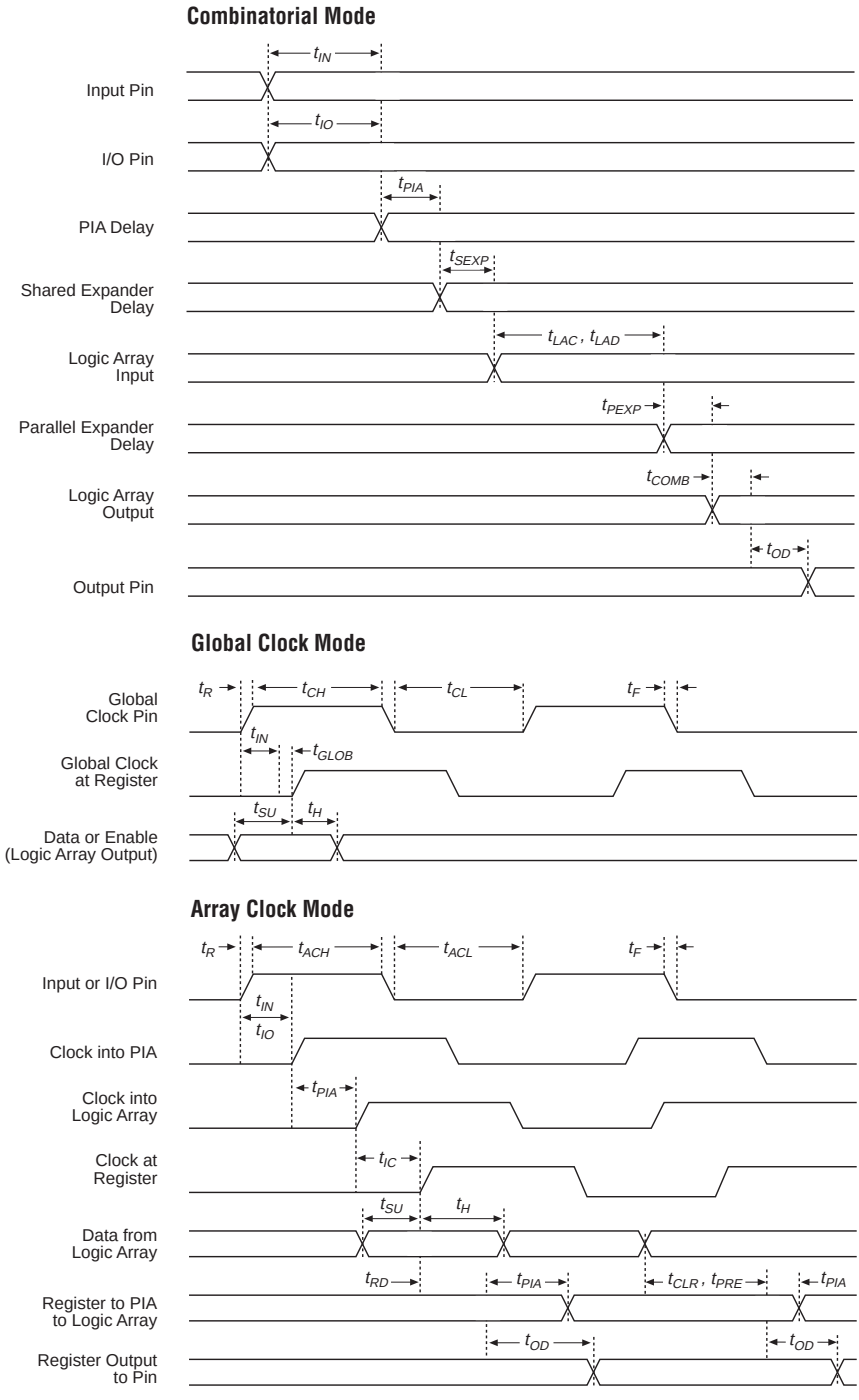


The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 14 shows the timing relationship between internal and external delay parameters.

See *Application Note 94 (Understanding MAX 7000 Timing)* for more information.

Figure 14. MAX 7000B Switching Waveforms

t_R & t_F < 2 ns. Inputs are driven at 3.0 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



Tables 15 and 16 show EPM7032B AC operating conditions.

Table 15. EPM7032B External Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3		-5		-7		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(3)*		3.5		5.0		7.5	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(3)*		3.5		5.0		7.5	ns
t_{SU}	Global clock setup time	*(3)*	2.8		4.0		5.7		ns
t_{H}	Global clock hold time	*(3)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.0		1.5		ns
t_{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		2.5		2.5		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	1.9	1.0	2.7	1.0	4.0	ns
t_{CH}	Global clock high time		1.5		2.0		3.0		ns
t_{CL}	Global clock low time		1.5		2.0		3.0		ns
t_{ASU}	Array clock setup time	*(3)*	1.7		2.5		3.5		ns
t_{AH}	Array clock hold time	*(3)*	0.0		0.0		0.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(3)*	1.0	3.0	1.0	4.2	1.0	6.2	ns
t_{ACH}	Array clock high time		1.5		2.0		3.0		ns
t_{ACL}	Array clock low time		1.5		2.0		3.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		1.5		2.0		3.0		ns
t_{CNT}	Minimum global clock period	*(3)*		3.5		5.0		7.2	ns
f_{CNT}	Maximum internal global clock frequency	*(3)*, *(4)*	285.7		200.0		138.9		MHz
t_{ACNT}	Minimum array clock period	*(3)*		3.5		5.0		7.2	ns
f_{ACNT}	Maximum internal array clock frequency	*(3)*, *(4)*	285.7		200.0		138.9		MHz

Table 16. EPM7032B Internal Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3		-5		-7		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.6		0.8		1.2	ns
t_{IO}	I/O input pad and buffer delay			0.6		0.8		1.2	ns
t_{FIN}	Fast input delay			0.1		0.2		0.3	ns
t_{FIND}	Programmable delay adder for fast input			1.5		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.1		3.1	ns
t_{PEXP}	Parallel expander delay			0.4		0.5		0.8	ns
t_{LAD}	Logic array delay			1.2		1.7		2.5	ns
t_{LAC}	Logic control array delay			0.5		0.7		1.0	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.6		0.9		1.3	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.6		5.9		6.3	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		4.0	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		9.0		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		4.0	ns
t_{SU}	Register setup time		1.0		1.5		2.0		ns
t_{H}	Register hold time		0.5		0.6		1.0		ns
t_{FSU}	Register setup time of fast input		1.0		1.0		1.5		ns
t_{FH}	Register hold time of fast input		1.5		1.5		1.5		ns
t_{RD}	Register delay			0.6		0.8		1.2	ns
t_{COMB}	Combinatorial delay			0.4		0.6		1.2	ns
t_{IC}	Array clock delay			0.5		0.7		1.0	ns
t_{EN}	Register enable time			0.5		0.7		1.0	ns
t_{GLOB}	Global control delay			0.1		0.2		0.3	ns
t_{PRE}	Register preset time			0.8		1.2		1.7	ns
t_{CLR}	Register clear time			0.6		0.9		1.3	ns
t_{PIA}	PIA delay	*(3)*		0.7		1.0		1.5	ns
t_{LPA}	Low-power adder	*(7)*		2.5		4.0		4.0	ns

Table 17. Selectable I/O Standard Input Adder Delays (Excluding Path to Fast Input Register)

I/O Standard	Speed Grade						Unit
	-3		-5		-7		
	Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS		0.0		0.0		0.0	ns
2.5 V TTL/CMOS		0.2		0.3		0.4	ns
1.8 V TTL/CMOS		0.4		0.5		0.8	ns
PCI		0.0		0.0		0.0	ns
GTL+		1.0		1.4		2.1	ns
SSTL-3 Class I		0.7		1.0		1.5	ns
SSTL-3 Class II		0.7		1.0		1.5	ns
SSTL-3 Class I		0.7		1.0		1.5	ns
SSTL-3 Class II		0.7		1.0		1.5	ns

Table 18. Selectable I/O Standard Input Adder Delays (Path to Fast Input Register)

I/O Standard	Speed Grade						Unit
	-3		-5		-7		
	Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS		0.0		0.0		0.0	ns
2.5 V TTL/CMOS		0.2		0.3		0.4	ns
1.8 V TTL/CMOS		0.4		0.5		0.8	ns
PCI		0.0		0.0		0.0	ns
GTL+		0.6		0.9		1.3	ns
SSTL-3 Class I		0.4		0.5		0.8	ns
SSTL-3 Class II		0.4		0.5		0.8	ns
SSTL-3 Class I		0.4		0.5		0.8	ns
SSTL-3 Class II		0.4		0.5		0.8	ns

Table 19. Selectable I/O Standard Output Adder Delays

I/O Standard	Speed Grade						Unit
	-3		-5		-7		
	Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS		0.0		0.0		0.0	ns
2.5 V TTL/CMOS		0.2		0.3		0.4	ns
1.8 V TTL/CMOS		1.2		1.7		2.5	ns
PCI		0.0		0.0		0.0	ns
GTL+		-0.2		-0.3		-0.4	ns
SSTL-3 Class I		-0.1		-0.1		-0.2	ns
SSTL-3 Class II		-0.1		-0.1		-0.2	ns
SSTL-3 Class I		-0.1		-0.1		-0.2	ns
SSTL-3 Class II		-0.1		-0.1		-0.2	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 12 on page 25.
(2) MAX 7000B timing values are preliminary.
(3) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(4) Measured with a 16-bit loadable, enabled, up / down counter programmed into each LAB.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Operating conditions: $V_{CCIO} = 2.5 \pm 5\%$ for commercial and industrial use.
(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Tables 20 and 21 show EPM7064B AC operating conditions.

Table 20. EPM7064B External Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3		-5		-7		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(3)*		3.5		5.0		7.5	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(3)*		3.5		5.0		7.5	ns
t_{SU}	Global clock setup time	*(3)*	2.7		3.8		5.6		ns
t_{H}	Global clock hold time	*(3)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.0		1.5		ns
t_{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		2.5		2.5		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	2.0	1.0	2.9	1.0	4.2	ns
t_{CH}	Global clock high time		1.5		2.0		3.0		ns
t_{CL}	Global clock low time		1.5		2.0		3.0		ns
t_{ASU}	Array clock setup time	*(3)*	1.7		2.5		3.5		ns
t_{AH}	Array clock hold time	*(3)*	0.0		0.0		0.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(3)*	1.0	3.0	1.0	4.2	1.0	6.3	ns
t_{ACH}	Array clock high time		1.5		2.0		3.0		ns
t_{ACL}	Array clock low time		1.5		2.0		3.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		1.5		5.1		7.4		ns
t_{CNT}	Minimum global clock period	*(3)*		3.6		5.1		7.4	ns
f_{CNT}	Maximum internal global clock frequency	*(3)*, *(4)*	277.8		196.1		135.1		MHz
t_{ACNT}	Minimum array clock period	*(3)*		3.6	5.1	5.1	7.4	7.4	ns
f_{ACNT}	Maximum internal array clock frequency	*(3)*, *(4)*	277.8		196.1		135.1		MHz

Table 21. EPM7064B Internal Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3		-5		-7		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.5		0.7		1.1	ns
t_{IO}	I/O input pad and buffer delay			0.5		0.7		1.1	ns
t_{FIN}	Fast input delay			0.3		0.5		0.6	ns
t_{FIND}	Programmable delay adder for fast input			1.5		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.5		2.0		3.0	ns
t_{PEXP}	Parallel expander delay			0.3		0.4		0.7	ns
t_{LAD}	Logic array delay			1.2		1.7		2.5	ns
t_{LAC}	Logic control array delay			0.5		0.7		1.0	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.6		0.9		1.3	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.6		5.9		6.3	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		4.0	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		9.0		9.0		9.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		4.0	ns
t_{SU}	Register setup time		1.0		1.5		2.0		ns
t_{H}	Register hold time		0.5		0.6		1.0		ns
t_{FSU}	Register setup time of fast input		1.0		1.0		1.5		ns
t_{FH}	Register hold time of fast input		1.5		1.5		1.5		ns
t_{RD}	Register delay			0.6		0.8		1.2	ns
t_{COMB}	Combinatorial delay			0.4		0.6		0.9	ns
t_{IC}	Array clock delay			0.5		0.7		1.0	ns
t_{EN}	Register enable time			0.5		0.7		1.0	ns
t_{GLOB}	Global control delay			0.3		0.5		0.6	ns
t_{PRE}	Register preset time			1.0		1.3		2.0	ns
t_{CLR}	Register clear time			0.6		0.9		1.3	ns
t_{PIA}	PIA delay	*(3)*		0.8		1.1		1.7	ns
t_{LPA}	Low-power adder	*(7)*		3.5		4.0		4.0	ns

Table 22. Selectable I/O Standard Input Adder Delays (Excluding Path to Fast Input Register)

I/O Standard	Speed Grade						Unit
	-3		-5		-7		
	Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS		0.0		0.0		0.0	ns
2.5 V TTL/CMOS		0.2		0.3		0.4	ns
1.8 V TTL/CMOS		0.3		0.5		0.8	ns
PCI		0.0		0.0		0.0	ns
GTL+		0.8		1.4		2.1	ns
SSTL-3 Class I		0.6		1.0		1.5	ns
SSTL-3 Class II		0.6		1.0		1.5	ns
SSTL-3 Class I		0.6		1.0		1.5	ns
SSTL-3 Class II		0.6		1.0		1.5	ns

Table 23. Selectable I/O Standard Input Adder Delays (Path to Fast Input Register)

I/O Standard	Speed Grade						Unit
	-3		-5		-7		
	Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS		0.0		0.0		0.0	ns
2.5 V TTL/CMOS		0.2		0.3		0.4	ns
1.8 V TTL/CMOS		0.3		0.5		0.8	ns
PCI		0.0		0.0		0.0	ns
GTL+		0.5		0.9		1.3	ns
SSTL-3 Class I		0.3		0.5		0.8	ns
SSTL-3 Class II		0.3		0.5		0.8	ns
SSTL-3 Class I		0.3		0.5		0.8	ns
SSTL-3 Class II		0.3		0.5		0.8	ns

Table 24. Selectable I/O Standard Output Adder Delays

I/O Standard	Speed Grade						Unit
	-3		-5		-7		
	Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS		0.0		0.0		0.0	ns
2.5 V TTL/CMOS		0.2		0.3		0.4	ns
1.8 V TTL/CMOS		1.0		1.7		2.5	ns
PCI		0.0		0.0		0.0	ns
GTL+		–0.2		–0.3		–0.4	ns
SSTL-3 Class I		–0.1		–0.1		–0.2	ns
SSTL-3 Class II		–0.1		–0.1		–0.2	ns
SSTL-3 Class I		–0.1		–0.1		–0.2	ns
SSTL-3 Class II		–0.1		–0.1		–0.2	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 12 on page 25.
(2) MAX 7000B timing values are preliminary.
(3) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(4) Measured with a 16-bit loadable, enabled, up / down counter programmed into each LAB.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Operating conditions: $V_{CCIO} = 2.5 \pm 5\%$ for commercial and industrial use.
(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Tables 25 and 26 show EPM7128B AC operating conditions.

Table 25. EPM7128B External Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(3)*		4.5		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(3)*		4.5		7.5		10.0	ns
t_{SU}	Global clock setup time	*(3)*	3.5		5.6		7.5		ns
t_{H}	Global clock hold time	*(3)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		2.5		3.0		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	2.5	1.0	4.3	1.0	5.6	ns
t_{CH}	Global clock high time		2.0		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(3)*	2.1		3.5		4.6		ns
t_{AH}	Array clock hold time	*(3)*	0.0		0.0		0.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(3)*	1.0	3.9	1.0	6.4	1.0	8.5	ns
t_{ACH}	Array clock high time		2.0		3.0		4.0		ns
t_{ACL}	Array clock low time		2.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		2.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(3)*		4.7		7.8		10.2	ns
f_{CNT}	Maximum internal global clock frequency	*(3)*, *(4)*	212.8		128.2		98.0		MHz
t_{ACNT}	Minimum array clock period	*(3)*		4.7		7.8		10.2	ns
f_{ACNT}	Maximum internal array clock frequency	*(3)*, *(4)*	212.8		128.2		98.0		MHz

Table 26. EPM7128B Internal Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.6		0.9		1.3	ns
t_{IO}	I/O input pad and buffer delay			0.6		0.9		1.3	ns
t_{FIN}	Fast input delay			0.5		1.0		1.1	ns
t_{FIND}	Programmable delay adder for fast input			1.5		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.8		3.0		3.8	ns
t_{PEXP}	Parallel expander delay			0.4		0.7		0.9	ns
t_{LAD}	Logic array delay			1.5		2.5		3.2	ns
t_{LAC}	Logic control array delay			0.7		1.1		1.4	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.7		1.2		1.6	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.7		6.2		6.6	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		3.0		4.0		5.0	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		8.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		3.0		4.0		5.0	ns
t_{SU}	Register setup time		1.3		2.1		2.8		ns
t_{H}	Register hold time		0.6		1.0		1.2		ns
t_{FSU}	Register setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Register hold time of fast input		1.5		1.5		1.5		ns
t_{RD}	Register delay			0.7		1.2		1.6	ns
t_{COMB}	Combinatorial delay			0.5		0.9		1.3	ns
t_{IC}	Array clock delay			0.7		1.1		1.4	ns
t_{EN}	Register enable time			0.7		1.1		1.4	ns
t_{GLOB}	Global control delay			0.5		1.0		1.1	ns
t_{PRE}	Register preset time			1.5		2.6		3.3	ns
t_{CLR}	Register clear time			0.7		1.2		1.6	ns
t_{PIA}	PIA delay	*(3)*		1.2		2.0		2.6	ns
t_{LPA}	Low-power adder	*(7)*		3.5		4.0		5.0	ns

Table 27. Selectable I/O Standard Input Adder Delays (Excluding Path to Fast Input Register)

I/O Standard	Speed Grade						Unit
	-4		-7		-10		
	Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS		0.0		0.0		0.0	ns
2.5 V TTL/CMOS		0.2		0.3		0.4	ns
1.8 V TTL/CMOS		0.4		0.7		0.9	ns
PCI		0.0		0.0		0.0	ns
GTL+		1.1		1.8		2.4	ns
SSTL-3 Class I		0.8		1.3		1.8	ns
SSTL-3 Class II		0.8		1.3		1.8	ns
SSTL-3 Class I		0.8		1.3		1.8	ns
SSTL-3 Class II		0.8		1.3		1.8	ns

Table 28. Selectable I/O Standard Input Adder Delays (Path to Fast Input Register)

I/O Standard	Speed Grade						Unit
	-4		-7		-10		
	Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS		0.0		0.0		0.0	ns
2.5 V TTL/CMOS		0.2		0.3		0.4	ns
1.8 V TTL/CMOS		0.4		0.7		0.9	ns
PCI		0.0		0.0		0.0	ns
GTL+		0.7		1.2		1.6	ns
SSTL-3 Class I		0.4		0.7		0.9	ns
SSTL-3 Class II		0.4		0.7		0.9	ns
SSTL-3 Class I		0.4		0.7		0.9	ns
SSTL-3 Class II		0.4		0.7		0.9	ns

Table 29. Selectable I/O Standard Output Adder Delays

I/O Standard	Speed Grade						Unit
	-4		-7		-10		
	Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS		0.0		0.0		0.0	ns
2.5 V TTL/CMOS		0.2		0.3		0.4	ns
1.8 V TTL/CMOS		1.3		2.2		2.9	ns
PCI		0.0		0.0		0.0	ns
GTL+		-0.2		-0.3		-0.4	ns
SSTL-3 Class I		-0.1		-0.2		-0.2	ns
SSTL-3 Class II		-0.1		-0.2		-0.2	ns
SSTL-3 Class I		-0.1		-0.2		-0.2	ns
SSTL-3 Class II		-0.1		-0.2		-0.2	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 12 on page 25.
(2) MAX 7000B timing values are preliminary.
(3) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(4) Measured with a 16-bit loadable, enabled, up / down counter programmed into each LAB.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Operating conditions: $V_{CCIO} = 2.5 \pm 5\%$ for commercial and industrial use.
(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Tables 30 and 31 show EPM7256B AC operating conditions.

Table 30. EPM7256B External Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(3)*		5.0		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(3)*		5.0		7.5		10.0	ns
t_{SU}	Global clock setup time	*(3)*	3.8		5.6		7.5		ns
t_{H}	Global clock hold time	*(3)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Global clock hold time for fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		2.5		3.0		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	2.9	1.0	4.4	1.0	5.8	ns
t_{CH}	Global clock high time		2.0		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(3)*	2.2		3.3		4.4		ns
t_{AH}	Array clock hold time	*(3)*	0.0		0.0		0.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(3)*	1.0	4.5	1.0	6.7	1.0	8.9	ns
t_{ACH}	Array clock high time		2.0		3.0		4.0		ns
t_{ACL}	Array clock low time		2.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		2.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(3)*		5.3		7.9		10.5	ns
f_{CNT}	Maximum internal global clock frequency	*(3)*, *(4)*	188.7		126.6		95.2		MHz
t_{ACNT}	Minimum array clock period	*(3)*		5.3		7.9		10.5	ns
f_{ACNT}	Maximum internal array clock frequency	*(3)*, *(4)*	188.7		126.6		95.2		MHz

Table 31. EPM7256B Internal Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.6		0.9		1.2	ns
t_{IO}	I/O input pad and buffer delay			0.6		0.9		1.2	ns
t_{FIN}	Fast input delay			0.7		1.1		1.4	ns
t_{FIND}	Programmable delay adder for fast input			1.5		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.9		2.8		3.7	ns
t_{PEXP}	Parallel expander delay			0.3		0.5		0.6	ns
t_{LAD}	Logic array delay			1.5		2.2		2.8	ns
t_{LAC}	Logic control array delay			0.7		1.0		1.3	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.8		1.2		1.6	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.8		6.2		6.6	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		5.0	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns
t_{SU}	Register setup time		1.4		2.1		2.9		ns
t_{H}	Register hold time		0.6		0.9		1.2		ns
t_{FSU}	Register setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Register hold time of fast input		1.5		1.5		1.5		ns
t_{RD}	Register delay			0.8		1.2		1.6	ns
t_{COMB}	Combinatorial delay			0.5		0.8		1.2	ns
t_{IC}	Array clock delay			0.7		1.0		1.3	ns
t_{EN}	Register enable time			0.7		1.0		1.3	ns
t_{GLOB}	Global control delay			0.7		1.1		1.4	ns
t_{PRE}	Register preset time			1.9		2.9		3.8	ns
t_{CLR}	Register clear time			0.8		1.2		1.6	ns
t_{PIA}	PIA delay	*(3)*		1.6		2.4		3.2	ns
t_{LPA}	Low-power adder	*(7)*		4.0		4.0		5.0	ns

Table 32. Selectable I/O Standard Input Adder Delays (Excluding Path to Fast Input Register)

I/O Standard	Speed Grade						Unit
	-5		-7		-10		
	Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS		0.0		0.0		0.0	ns
2.5 V TTL/CMOS		0.2		0.3		0.4	ns
1.8 V TTL/CMOS		0.4		0.7		0.9	ns
PCI		0.0		0.0		0.0	ns
GTL+		1.1		1.8		2.4	ns
SSTL-3 Class I		0.8		1.3		1.8	ns
SSTL-3 Class II		0.8		1.3		1.8	ns
SSTL-3 Class I		0.8		1.3		1.8	ns
SSTL-3 Class II		0.8		1.3		1.8	ns

Table 33. Selectable I/O Standard Input Adder Delays (Path to Fast Input Register)

I/O Standard	Speed Grade						Unit
	-5		-7		-10		
	Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS		0.0		0.0		0.0	ns
2.5 V TTL/CMOS		0.2		0.3		0.4	ns
1.8 V TTL/CMOS		0.4		0.7		0.9	ns
PCI		0.0		0.0		0.0	ns
GTL+		1.1		1.8		2.4	ns
SSTL-3 Class I		0.8		1.3		1.8	ns
SSTL-3 Class II		0.8		1.3		1.8	ns
SSTL-3 Class I		0.8		1.3		1.8	ns
SSTL-3 Class II		0.8		1.3		1.8	ns

Table 34. Standard Output Adder Delays

I/O Standard	Speed Grade						Unit
	-5		-7		-10		
	Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS		0.0		0.0		0.0	ns
2.5 V TTL/CMOS		0.2		0.3		0.4	ns
1.8 V TTL/CMOS		1.3		2.2		2.9	ns
PCI		0.0		0.0		0.0	ns
GTL+		–0.2		–0.3		–0.4	ns
SSTL-3 Class I		–0.1		–0.2		–0.2	ns
SSTL-3 Class II		–0.1		–0.2		–0.2	ns
SSTL-3 Class I		–0.1		–0.2		–0.2	ns
SSTL-3 Class II		–0.1		–0.2		–0.2	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 12 on page 25.
(2) MAX 7000B timing values are preliminary.
(3) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(4) Measured with a 16-bit loadable, enabled, up / down counter programmed into each LAB.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Operating conditions: $V_{CCIO} = 2.5 \pm 5\%$ for commercial and industrial use.
(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Tables 35 and 36 show EPM7512B AC operating conditions.

Table 35. EPM7512B External Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-6		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(3)*		6.0		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(3)*		6.0		7.5		10.0	ns
t_{SU}	Global clock setup time	*(3)*	4.3		5.4		7.2		ns
t_{H}	Global clock hold time	*(3)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		2.5		3.0		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.9	1.0	4.9	1.0	6.7	ns
t_{CH}	Global clock high time		3.0		3.0		4.0		ns
t_{CL}	Global clock low time		3.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(3)*	2.2		2.8		3.8		ns
t_{AH}	Array clock hold time	*(3)*	0.0		0.0		0.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(3)*	1.0	6.0	1.0	7.5	1.0	10.1	ns
t_{ACH}	Array clock high time		3.0		3.0		4.0		ns
t_{ACL}	Array clock low time		3.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		3.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(3)*		6.8		8.6		11.5	ns
f_{CNT}	Maximum internal global clock frequency	*(3)*, *(4)*	147.1		116.3		87.0		MHz
t_{ACNT}	Minimum array clock period	*(3)*		6.8		8.6		11.5	ns
f_{ACNT}	Maximum internal array clock frequency	*(3)*, *(4)*	147.1		116.3		87.0		MHz

Table 36. EPM7512B Internal Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-6		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.6		0.7		0.9	ns
t_{IO}	I/O input pad and buffer delay			0.6		0.7		0.9	ns
t_{FIN}	Fast input delay			1.5		1.9		2.6	ns
t_{FIND}	Programmable delay adder for fast input			1.5		1.5		1.5	ns
t_{SEXP}	Shared expander delay			2.1		2.7		3.5	ns
t_{PEXP}	Parallel expander delay			0.3		0.4		0.5	ns
t_{LAD}	Logic array delay			1.7		2.2		2.8	ns
t_{LAC}	Logic control array delay			0.8		1.0		1.3	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.8		1.0		1.5	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.8		6.0		6.5	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		4.0		5.0	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		9.0		9.0		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		4.0		5.0	ns
t_{SU}	Register setup time		1.7		2.1		3.0		ns
t_{H}	Register hold time		0.5		0.6		0.8		ns
t_{FSU}	Register setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Register hold time of fast input		1.5		1.5		1.5		ns
t_{RD}	Register delay			1.0		1.3		1.7	ns
t_{COMB}	Combinatorial delay			0.5		0.6		0.8	ns
t_{IC}	Array clock delay			1.2		1.5		2.0	ns
t_{EN}	Register enable time			0.8		1.0		1.3	ns
t_{GLOB}	Global control delay			1.5		1.9		2.6	ns
t_{PRE}	Register preset time			2.5		3.1		4.1	ns
t_{CLR}	Register clear time			0.8		1.0		1.4	ns
t_{PIA}	PIA delay	*(3)*		2.4		3.0		4.0	ns
t_{LPA}	Low-power adder	*(7)*		4.0		4.0		5.0	ns

Table 37. Selectable I/O Standard Input Adder Delays (Excluding Path to Fast Input Register)

I/O Standard	Speed Grade						Unit
	-6		-7		-10		
	Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS		0.0		0.0		0.0	ns
2.5 V TTL/CMOS		0.2		0.3		0.4	ns
1.8 V TTL/CMOS		0.4		0.7		0.9	ns
PCI		0.0		0.0		0.0	ns
GTL+		1.1		1.8		2.4	ns
SSTL-3 Class I		0.8		1.3		1.8	ns
SSTL-3 Class II		0.8		1.3		1.8	ns
SSTL-3 Class I		0.8		1.3		1.8	ns
SSTL-3 Class II		0.8		1.3		1.8	ns

Table 38. Selectable I/O Standard Input Adder Delays (Path to Fast Input Register)

I/O Standard	Speed Grade						Unit
	-6		-7		-10		
	Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS		0.0		0.0		0.0	ns
2.5 V TTL/CMOS		0.2		0.3		0.4	ns
1.8 V TTL/CMOS		0.4		0.7		0.9	ns
PCI		0.0		0.0		0.0	ns
GTL+		0.7		1.2		1.6	ns
SSTL-3 Class I		0.4		0.7		0.9	ns
SSTL-3 Class II		0.4		0.7		0.9	ns
SSTL-3 Class I		0.4		0.7		0.9	ns
SSTL-3 Class II		0.4		0.7		0.9	ns

Table 39. Selectable I/O Standard Output Adder Delays

I/O Standard	Speed Grade						Unit
	-6		-7		-10		
	Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS		0.0		0.0		0.0	ns
2.5 V TTL/CMOS		0.2		0.3		0.4	ns
1.8 V TTL/CMOS		1.3		2.2		2.9	ns
PCI		0.0		0.0		0.0	ns
GTL+		-0.2		-0.3		-0.4	ns
SSTL-3 Class I		-0.1		-0.2		-0.2	ns
SSTL-3 Class II		-0.1		-0.2		-0.2	ns
SSTL-3 Class I		-0.1		-0.2		-0.2	ns
SSTL-3 Class II		-0.1		-0.2		-0.2	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 12 on page 25.
(2) MAX 7000B timing values are preliminary.
(3) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(4) Measured with a 16-bit loadable, enabled, up / down counter programmed into each LAB.
(5) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(6) Operating conditions: $V_{CCIO} = 2.5 \pm 5\%$ for commercial and industrial use.
(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Power Consumption

Supply power (P) versus frequency ($\mathbf{f_{MAX}}$, in MHz) for MAX 7000B devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The I_{CCINT} value depends on the switching frequency and the application logic. The I_{CCINT} value is calculated with the following equation:

$$I_{CCINT} =$$

$$(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$$

The parameters in this equation are:

MC_{TON} = Number of macrocells with the Turbo Bit™ option turned on, as reported in the MAX+PLUS II Report File (**.rpt**)
MC_{DEV} = Number of macrocells in the device
MC_{USED} = Total number of macrocells in the design, as reported in the Report File
$\mathbf{f_{MAX}}$ = Highest clock frequency to the device
$\mathbf{tog_{LC}}$ = Average percentage of logic cells toggling at each clock (typically 12.5%)
A, B, C = Constants, shown in Table 40

Table 40. MAX 7000B I_{CC} Equation Constants

Device	A	B	C
EPM7032B	0.53	0.22	0.010
EPM7064B	0.53	0.22	0.010
EPM7128B	0.53	0.22	0.010
EPM7256B	0.53	0.22	0.010
EPM7512B	0.53	0.22	0.010

This calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up / down counter in each LAB with no output load. Actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 15. I_{CC} vs. Frequency for EPM7032B Devices

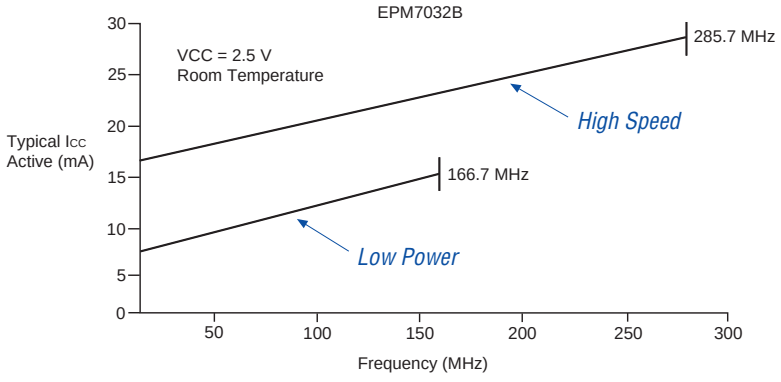


Figure 16. I_{CC} vs. Frequency for EPM7064B Devices

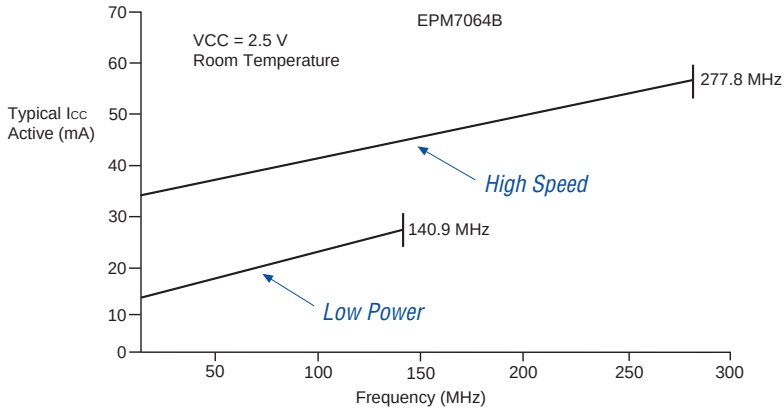


Figure 17. I_{CC} vs. Frequency for EPM7128B Devices

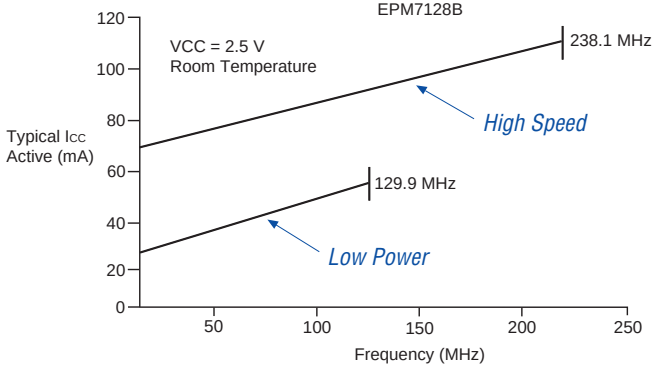


Figure 18. I_{CC} vs. Frequency for EPM7256B Devices

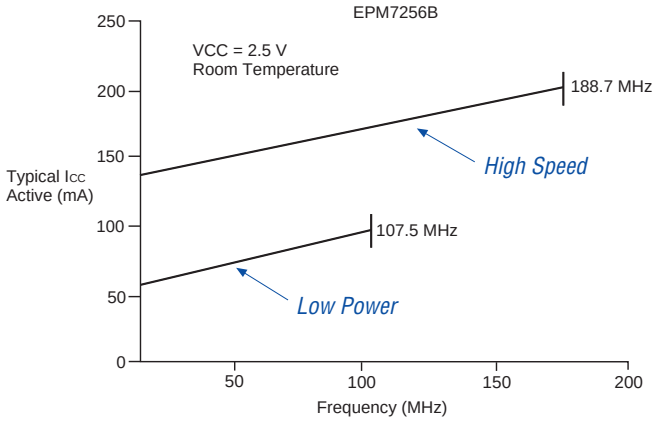
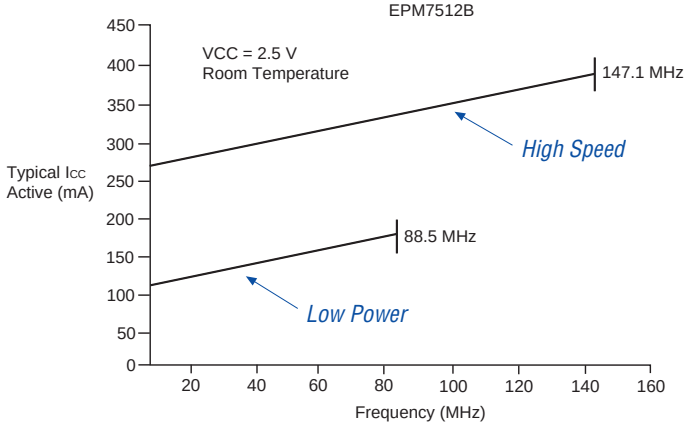


Figure 19. I_{CC} vs. Frequency for EPM7512B Devices



Device Pin-Outs

Tables 41 through 52 show the pin names and numbers for MAX 7000B device packages.

Table 41. EPM7032B Dedicated Pin-Outs

Dedicated Pin	44-Pin PLCC	44-Pin TQFP	48-Pin VTQFP
INPUT/GCLK1	43	37	41
INPUT/GCLRn	1	39	43
INPUT/OE1	44	38	42
INPUT/OE2/GCLK2	2	40	44
TDI *(1)*	7	1	2
TMS *(1)*	13	7	8
TCK *(1)*	32	26	29
TDO *(1)*	38	32	35
VREFA *(2)*	11	5	6
VREFB *(2)*	31	25	28
GNDINT	22, 42	16, 36	18, 40
GNDIO	10, 30	4, 24	5, 27
VCCINT (2.5 V)	3, 23	17, 41	19, 45
VCCIO1 (1.8 V, 2.5 V, or 3.3 V)	15	9	10
VCCIO2 (1.8 V, 2.5 V, or 3.3 V)	35	29	32
No Connect (N.C.)	–	–	1, 13, 24, 37
Total User I/O Pins *(3)*	36	36	36

Table 42. EPM7032B I/O Pin–Outs & I/O Standards

LAB	MC	44-Pin PLCC	44-Pin TQFP	48-Pin VTQFP	IOGND Groups (200 mA)	IOVCC Groups (100 mA)	I/O Bank
A	1	4	42	46	A	A	1
	2	5	43	47	A	A	1
	3	6	44	48	A	A	1
	4	7 *(1)*	1 *(1)*	2 *(1)*	A	A	1
	5	8	2	3	A	A	1
	6	9	3	4	A	A	1
	7	11 *(2)*	5 *(2)*	6 *(2)*	B	A	1
	8	12	6	7	B	A	1
	9	13 *(1)*	7 *(1)*	8 *(1)*	B	A	1
	10	14	8	9	B	A	1
	11	16	10	11	B	B	1
	12	17	11	12	B	B	1
	13	18	12	14	B	B	1
	14	19	13	15	B	B	1
	15	20	14	16	B	B	1
	16	21	15	17	B	B	1
B	17	41	35	39	A	D	2
	18	40	34	38	A	D	2
	19	39	33	36	A	D	2
	20	38 *(1)*	32 *(1)*	35 *(1)*	A	D	2
	21	37	31	34	A	D	2
	22	36	30	33	A	D	2
	23	34	28	31	A	C	2
	24	33	27	30	A	C	2
	25	32 *(1)*	26 *(1)*	29 *(1)*	A	C	2
	26	31 *(2)*	25 *(2)*	28 *(2)*	A	C	2
	27	29	23	26	B	C	2
	28	28	22	25	B	C	2
	29	27	21	23	B	C	2
	30	26	20	22	B	C	2
	31	25	19	21	B	C	2
	32	24	18	20	B	C	2

Notes to tables:

(1) This pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for in-system programming, this pin is not available as a user I/O pin.

(2) This pin may function as either a VREF pin or a user I/O pin. If this pin is programmed to be a VREF pin for using the advanced I/O standards, this pin is not available as a user I/O pin.

(3) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 43. EPM7064B Dedicated Pin-Outs

Dedicated Pin	44-Pin PLCC	44-Pin TQFP	48-Pin VTQFP	100-Pin TQFP	100-Pin FineLine BGA
INPUT/GCLK1	43	37	41	87	A6
INPUT/GCLRN	1	39	43	89	B5
INPUT/OE1	44	38	42	88	B6
INPUT/OE2/GLCK2	2	40	44	90	A5
TDI *(1)*	7	1	2	4	A1
TMS *(1)*	13	7	8	15	F3
TCK *(1)*	32	26	29	62	F8
TDO *(1)*	38	32	35	73	A10
VREFA *(2)*	11	5	6	12	F1
VREFB *(2)*	31	25	28	60	E8
GNDINT	22, 42	16, 36	18, 40	38, 86	D6, G5
GNDIO	10, 30	4, 24	5, 27	11, 26, 43, 59, 74, 95	C3, D7, E5, F6, G4, H8
VCCINT (2.5 V)	3, 23	17, 41	19, 45	39, 91	D5, G6
VCCIO1 (1.8 V, 2.5V, 3.3V)	15	9	10	3, 18, 34	D4, F5, H3
VCCIO2 (1.8 V, 2.5V, 3.3V)	35	29	32	51, 66, 82	C8, E6, G7
No Connect	–	–	–	1, 2, 5, 7, 22, 24, 27, 28, 49, 50, 53, 55, 70, 72, 77, 78	B1, B10, C1, C9, C10, D8, E3, E4, H1, H9, H10, J1, J2, J10, K1, K9
Total User I/O Pins (3)	36	36	40	68	68

Table 44. EPM7064B I/O Pins & I/O Standards (Part 1 of 2)

LAB	MC	44-Pin PLCC	44-Pin TQFP	48-Pin VTQFP	IOGND Group (200 mA)	IOVCC Group (100 mA)	I/O Bank
A	1	12	6	7	B	A	1
	2	–	–	–	–	–	1
	3	11 *(2)*	5 *(2)*	6 *(2)*	B	A	1
	4	9	3	4	A	A	1
	5	8	2	3	A	A	1
	6	–	–	–	–	–	1
	7	–	–	–	–	–	1
	8	7 *(1)*	1 *(1)*	2 *(1)*	A	A	1
	9	–	–	1	A	A	1
	10	–	–	–	–	–	1
	11	6	44	48	A	A	1
	12	–	–	–	–	–	1
	13	–	–	–	–	–	1
	14	5	43	47	A	A	1
	15	–	–	–	–	–	1
	16	4	42	46	A	A	1
B	17	21	15	17	B	B	1
	18	–	–	–	–	–	1
	19	20	14	16	B	B	1
	20	19	13	15	B	B	1
	21	18	12	14	B	B	1
	22	–	–	13	B	B	1
	23	–	–	–	–	–	1
	24	17	11	12	B	B	1
	25	16	10	11	B	B	1
	26	–	–	–	–	–	1
	27	–	–	–	–	–	1
	28	–	–	–	–	–	1
	29	–	–	–	–	–	1
	30	14	8	9	B	A	1
	31	–	–	–	–	–	1
	32	13 *(1)*	7 *(1)*	8 *(1)*	B	A	1

Table 44. EPM7064B I/O Pins & I/O Standards (Part 2 of 2)

LAB	MC	44-Pin PLCC	44-Pin TQFP	48-Pin VTQFP	IOGND Group (200 mA)	IOVCC Group (100 mA)	I/O Bank
C	33	24	18	20	B	C	2
	34	–	–	–	–	–	2
	35	25	19	21	B	C	2
	36	26	20	22	B	C	2
	37	27	21	23	B	C	2
	38	–	–	–	–	–	2
	39	–	–	24	B	C	2
	40	28	22	25	B	C	2
	41	29	23	26	B	C	2
	42	–	–	–	–	–	2
	43	–	–	–	–	–	2
	44	–	–	–	–	–	2
	45	–	–	–	–	–	2
	46	31 *(2)*	25 *(2)*	28 *(2)*	A	C	2
	47	–	–	–	–	–	2
	48	32 *(1)*	26 *(1)*	29 *(1)*	A	C	2
D	49	33	27	30	A	C	2
	50	–	–	–	–	–	2
	51	34	28	31	A	C	2
	52	36	30	33	A	D	2
	53	37	31	34	A	D	2
	54	–	–	–	–	–	2
	55	–	–	–	–	–	2
	56	38 *(1)*	32 *(1)*	35 *(1)*	A	D	2
	57	39	33	36	A	D	2
	58	–	–	–	–	–	2
	59	–	–	37	A	D	2
	60	–	–	–	–	–	2
	61	–	–	–	–	–	2
	62	40	34	38	A	D	2
	63	–	–	–	–	–	2
	64	41	35	39	A	D	2

Notes to tables:

(1) This pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for in-system programming, this pin is not available as a user I/O pin.

(2) This pin may function as either a VREF pin or a user I/O pin. If this pin is programmed to be a VREF pin for using the advanced I/O standards, this pin is not available as a user I/O pin.

(3) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 45. EPM7064B I/O Pins & I/O Standards (Part 1 of 3)

LAB	MC	100-Pin TQFP	100-Pin FineLine BGA	IOGND Group (200 mA)	IOVCC Group	I/O Bank
A	1	14	F4	C	B (200 mA)	1
	2	13	E2	C	B (200 mA)	1
	3	12 *(2)*	E1	C	B (200 mA)	1
	4	10	D2	B	B (200 mA)	1
	5	9	D1	B	B (200 mA)	1
	6	8	D3	B	B (200 mA)	1
	7	6	C2	B	B (200 mA)	1
	8	4 *(1)*	A1 *(1)*	B	B (200 mA)	1
	9	100	B2	B	A (100 mA)	1
	10	99	A2	B	A (100 mA)	1
	11	98	A3	B	A (100 mA)	1
	12	97	B3	B	A (100 mA)	1
	13	96	A4	B	A (100 mA)	1
	14	94	B4	A	A (100 mA)	1
	15	93	C4	A	A (100 mA)	1
	16	92	C5	A	A (100 mA)	1

Table 45. EPM7064B I/O Pins & I/O Standards (Part 2 of 3)

LAB	MC	100-Pin TQFP	100-Pin FineLine BGA	IOGND Group (200 mA)	IOVCC Group	I/O Bank
B	17	37	K5	D	D (100 mA)	1
	18	36	J5	D	D (100 mA)	1
	19	35	H5	D	D (100 mA)	1
	20	33	K4	D	C (200 mA)	1
	21	32	J4	D	C (200 mA)	1
	22	31	H4	D	C (200 mA)	1
	23	30	J3	D	C (200 mA)	1
	24	29	K3	D	C (200 mA)	1
	25	25	K2	C	C (200 mA)	1
	26	23	H2	C	C (200 mA)	1
	27	21	G2	C	C (200 mA)	1
	28	20	G1	C	C (200 mA)	1
	29	19	G3	C	C (200 mA)	1
	30	17	F2	C	B (200 mA)	1
	31	16	F1 *(2)*	C	B (200 mA)	1
	32	15 *(1)*	F3 *(1)*	C	B (200 mA)	1
C	33	40	K6	D	E (100 mA)	2
	34	41	J6	D	E (100 mA)	2
	35	42	H6	D	E (100 mA)	2
	36	44	K7	E	E (100 mA)	2
	37	45	J7	E	E (100 mA)	2
	38	46	H7	E	E (100 mA)	2
	39	47	J8	E	E (100 mA)	2
	40	48	K8	E	E (100 mA)	2
	41	52	K10	E	F (200 mA)	2
	42	54	J9	E	F (200 mA)	2
	43	56	G9	E	F (200 mA)	2
	44	57	G10	E	F (200 mA)	2
	45	58	G8	E	F (200 mA)	2
	46	60 *(2)*	F9	F	F (200 mA)	2
	47	61	F10	F	F (200 mA)	2
	48	62 *(1)*	F8 *(1)*	F	F (200 mA)	2

Table 45. EPM7064B I/O Pins & I/O Standards (Part 2 of 3)

LAB	MC	100-Pin TQFP	100-Pin FineLine BGA	IOGND Group (200 mA)	IOVCC Group	I/O Bank
B	17	37	K5	D	D (100 mA)	1
	18	36	J5	D	D (100 mA)	1
	19	35	H5	D	D (100 mA)	1
	20	33	K4	D	C (200 mA)	1
	21	32	J4	D	C (200 mA)	1
	22	31	H4	D	C (200 mA)	1
	23	30	J3	D	C (200 mA)	1
	24	29	K3	D	C (200 mA)	1
	25	25	K2	C	C (200 mA)	1
	26	23	H2	C	C (200 mA)	1
	27	21	G2	C	C (200 mA)	1
	28	20	G1	C	C (200 mA)	1
	29	19	G3	C	C (200 mA)	1
	30	17	F2	C	B (200 mA)	1
	31	16	F1 *(2)*	C	B (200 mA)	1
	32	15 *(1)*	F3 *(1)*	C	B (200 mA)	1
C	33	40	K6	D	E (100 mA)	2
	34	41	J6	D	E (100 mA)	2
	35	42	H6	D	E (100 mA)	2
	36	44	K7	E	E (100 mA)	2
	37	45	J7	E	E (100 mA)	2
	38	46	H7	E	E (100 mA)	2
	39	47	J8	E	E (100 mA)	2
	40	48	K8	E	E (100 mA)	2
	41	52	K10	E	F (200 mA)	2
	42	54	J9	E	F (200 mA)	2
	43	56	G9	E	F (200 mA)	2
	44	57	G10	E	F (200 mA)	2
	45	58	G8	E	F (200 mA)	2
	46	60 *(2)*	F9	F	F (200 mA)	2
	47	61	F10	F	F (200 mA)	2
	48	62 *(1)*	F8 *(1)*	F	F (200 mA)	2

Table 45. EPM7064B I/O Pins & I/O Standards (Part 3 of 3)

LAB	MC	100-Pin TQFP	100-Pin FineLine BGA	IOGND Group (200 mA)	IOVCC Group	I/O Bank
D	49	63	F7	F	F (200 mA)	2
	50	64	E9	F	F (200 mA)	2
	51	65	E10	F	F (200 mA)	2
	52	67	E8 *(2)*	F	G (200 mA)	2
	53	68	E7	F	G (200 mA)	2
	54	69	D9	F	G (200 mA)	2
	55	71	D10	F	G (200 mA)	2
	56	73 *(1)*	A10 *(1)*	F	G (200 mA)	2
	57	75	B9	A	G (200 mA)	2
	58	76	A9	A	G (200 mA)	2
	59	79	A8	A	G (200 mA)	2
	60	80	B8	A	G (200 mA)	2
	61	81	A7	A	G (200 mA)	2
	62	83	B7	A	H (100 mA)	2
	63	84	C7	A	H (100 mA)	2
	64	85	C6	A	H (100 mA)	2

Notes to tables:

(1) This pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for in-system programming, this pin is not available as a user I/O pin.

(2) This pin may function as either a VREF pin or a user I/O pin. If this pin is programmed to be a VREF pin for using the advanced I/O standards, then this pin is not available as a user I/O pin.

(3) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 46. EPM7128B Dedicated Pin-Outs

Dedicated Pin	48-Pin VTQFP	100-Pin TQFP	100-Pin FineLine BGA	144-Pin TQFP	256-Pin FineLine BGA
INPUT/GCLK1	41	87	A6	125	D9
INPUT/GCLRn	43	89	B5	127	E8
INPUT/OE1	42	88	B6	126	E9
INPUT/OE2/GCLK2	44	90	A5	128	D8
TDI *(1)*	2	4	A1	4	D4
TMS *(1)*	8	15	F3	20	J6
TCK *(1)*	29	62	F8	89	J11
TDO *(1)*	35	73	A10	104	D13
VREFA *(2)*	6	12	F1	14	J4
VREFB *(2)*	28	60	E8	87	H11
GNDINT	18, 40	38, 86	D6, G5	52, 57, 124, 129	A8, C9, G9, K8, P9
GNDIO	5, 27	11, 26, 43, 59, 74, 95	C3, D7, E5, F6, G4, H8	3, 13, 17, 33, 59, 64, 85, 105, 135	A3, B10, C2, D14, F6, G10, H8, J9, K7, L11, M3, P6, P10, R2, R3, T1, T15
VCCINT (2.5 V Only)	19, 45	39, 91	D5, G6	51, 58, 123, 130	B9, C8, G8, K9, P8
VCCIO1 (1.8 V, 2.5 V, or 3.3 V)	10	3, 18, 34	D4, F5, H3	24, 50, 144	B3, B5, G3, G7, J8, L3, L6, T2, T3
VCCIO2 (1.8 V, 2.5 V, or 3.3 V)	32	51, 66, 82	C8, E6, G7	73, 76, 95, 115	C14, E15, F11, G15, H9, K10, M15, P14
No Connect (N.C.)	–	–	–	1, 2, 12, 19, 34, 35, 36, 43, 46, 47, 48, 49, 66, 75, 90, 103, 108, 120, 121, 122	A1, A2, A4, A5, A6, A7, A9, A10, A11, A12, A13, A14, A15, A16, B1, B2, B4, B6, B7, B8, B11, B12, B13, B14, B 15, B16, C1, C3, C4, C6, C11, C13, C15, C16, D1, D2, D3, D15, D16, E1, E2, E3, E14, E16, F1, F2, F15, F16, G1, G2, G14, G16, H1, H2, H15, H16, J1, J2, J15, J16, K1, K2, K3, K14, K15, K16, L1, L2, L15, L16, M1, M14, M16, N1, N2, N3, N14, N15, N16, P1, P2, P3, P4, P12, P13, P15, P16, R1, R4, R5, R6, R7, R8, R9, R11, R12, R13, R14, R15, R16, T4, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T16
Total User I/O Pins *(2)*	40	84	84	100	100

Table 47. EPM7128B I/O Pins & I/O Standard Groups (Part 1 of 4)

LAB	MC	48-Pin VTQFP	IOGND Group for 48-Pin VTQFP (200 mA)	IOVCC Group for 48-Pin VTQFP (100 mA)	100-Pin TQFP	100-Pin FineLine BGA	144-Pin TQFP	256-Pin FineLine BGA	IOGND Group for Other Packages (200 mA)	IOVCC Group for Other Packages	I/O Bank
A	1	1	A	A	2	C1	143	F4	B	A (100 mA)	1
	2	–	–	–	–	–	–	–	–	–	1
	3	48	A	A	1	B1	142	E4	B	A (100 mA)	1
	4	–	–	–	–	–	141	C5	B	A (100 mA)	1
	5	–	–	–	100	B2	140	E5	B	A (100 mA)	1
	6	–	–	–	99	A2	139	D5	B	A (100 mA)	1
	7	–	–	–	–	–	–	–	–	–	1
	8	–	–	–	98	A3	138	D6	B	A (100 mA)	1
	9	–	–	–	97	B3	137	E6	B	A (100 mA)	1
	10	–	–	–	–	–	–	–	–	–	1
	11	47	A	A	96	A4	136	D7	B	A (100 mA)	1
	12	–	–	–	–	–	134	C7	A	A (100 mA)	1
	13	46	A	A	94	B4	133	E7	A	A (100 mA)	1
	14	–	–	–	93	C4	132	F7	A	A (100 mA)	1
	15	–	–	–	–	–	–	–	–	–	1
	16	–	–	–	92	C5	131	F8	A	A (100 mA)	1
B	17	–	–	–	14	F4	18	J7	C	B (200 mA)	1
	18	–	–	–	–	–	–	–	–	–	1
	19	7	B	A	13	E2	16	H5	C	B (200 mA)	1
	20	–	–	–	–	–	15	H3	C	B (200 mA)	1
	21	6 *(2)*	B	A	12 *(2)*	E1	14 *(2)*	H4	C	B (200 mA)	1
	22	–	–	–	10	E3	11	H6	B	B (200 mA)	1
	23	–	–	–	–	–	–	–	–	–	1
	24	–	–	–	9	E4	10	H7	B	B (200 mA)	1
	25	–	–	–	8	D2	9	G5	B	B (200 mA)	1
	26	–	–	–	–	–	–	–	–	–	1
	27	4	A	A	7	D1	8	G4	B	B (200 mA)	1
	28	–	–	–	–	–	7	F3	B	B (200 mA)	1
	29	3	A	A	6	D3	6	G6	B	B (200 mA)	1
	30	–	–	–	5	C2	5	F5	B	B (200 mA)	1
	31	–	–	–	–	–	–	–	–	–	1
	32	2 *(1)*	A	A	4 *(1)*	A1 *(1)*	4 *(1)*	D4 *(1)*	B	B (200 mA)	1

Table 47. EPM7128B I/O Pins & I/O Standard Groups (Part 2 of 4)

LAB	MC	48-Pin VTQFP	IOGND Group for 48-Pin VTQFP (200 mA)	IOVCC Group for 48-Pin VTQFP (100 mA)	100-Pin TQFP	100-Pin FineLine BGA	144-Pin TQFP	256-Pin FineLine BGA	IOGND Group for Other Packages (200 mA)	IOVCC Group for Other Packages	I/O Bank
C	33	13	B	B	25	K1	32	N4	C	C (200 mA)	1
	34	–	–	–	–	–	–	–	–	–	1
	35	12	B	B	24	J1	31	M4	C	C (200 mA)	1
	36	–	–	–	–	–	30	M2	C	C (200 mA)	1
	37	–	–	–	23	H1	29	L4	C	C (200 mA)	1
	38	–	–	–	22	H2	28	L5	C	C (200 mA)	1
	39	–	–	–	–	–	–	–	–	–	1
	40	–	–	–	21	G2	27	K5	C	C (200 mA)	1
	41	–	–	–	20	G1	26	K4	C	C (200 mA)	1
	42	–	–	–	–	–	–	–	–	–	1
	43	11	B	B	19	G3	25	K6	C	C (200 mA)	1
	44	–	–	–	–	–	23	J3	C	B (200 mA)	1
	45	9	B	A	17	F2	22	J5	C	B (200 mA)	1
	46	–	–	–	16	F1 *(2)*	21	J4 *(2)*	C	B (200 mA)	1
	47	–	–	–	–	–	–	–	–	–	1
	48	8 *(1)*	B	A	15 *(1)*	F3 *(1)*	20 *(1)*	J6 *(1)*	C	B (200 mA)	1
D	49	–	–	–	37	K5	56	N8	D	D (100 mA)	1
	50	–	–	–	–	–	–	–	–	–	1
	51	17	B	B	36	J5	55	M8	D	D (100 mA)	1
	52	–	–	–	–	–	54	P7	D	D (100 mA)	1
	53	–	–	–	35	H5	53	L8	D	D (100 mA)	1
	54	–	–	–	33	K4	45	N7	D	C (200 mA)	1
	55	–	–	–	–	–	–	–	–	–	1
	56	16	B	B	32	J4	44	M7	D	C (200 mA)	1
	57	–	–	–	31	H4	42	L7	D	C (200 mA)	1
	58	–	–	–	–	–	–	–	–	–	1
	59	15	B	B	30	J3	41	M6	D	C (200 mA)	1
	60	–	–	–	–	–	40	P5	D	C (200 mA)	1
	61	–	–	–	29	K3	39	N6	D	C (200 mA)	1
	62	–	–	–	28	J2	38	M5	D	C (200 mA)	1
	63	–	–	–	–	–	–	–	–	–	1
	64	14	B	B	27	K2	37	N5	D	C (200 mA)	1

Table 47. EPM7128B I/O Pins & I/O Standard Groups (Part 3 of 4)

LAB	MC	48-Pin VTQFP	IOGND Group for 48-Pin VTQFP (200 mA)	IOVCC Group for 48-Pin VTQFP (100 mA)	100-Pin TQFP	100-Pin FineLine BGA	144-Pin TQFP	256-Pin FineLine BGA	IOGND Group for Other Packages (200 mA)	IOVCC Group for Other Packages	I/O Bank
E	65	–	–	–	40	K6	60	N9	D	E (100 mA)	2
	66	–	–	–	–	–	–	–	–	–	2
	67	20	B	C	41	J6	61	M9	D	E (100 mA)	2
	68	–	–	–	–	–	62	R10	D	E (100 mA)	2
	69	21	B	C	42	H6	63	L9	D	E (100 mA)	2
	70	–	–	–	44	K7	65	N10	E	E (100 mA)	2
	71	–	–	–	–	–	–	–	–	–	2
	72	22	B	C	45	J7	67	M10	E	E (100 mA)	2
	73	–	–	–	46	H7	68	L10	E	E (100 mA)	2
	74	–	–	–	–	–	–	–	–	–	2
	75	23	B	C	47	J8	69	M11	E	E (100 mA)	2
	76	–	–	–	–	–	70	P11	E	E (100 mA)	2
	77	24	B	C	48	K8	71	N11	E	E (100 mA)	2
	78	–	–	–	49	K9	72	N12	E	E (100 mA)	2
	79	–	–	–	–	–	–	–	–	–	2
	80	–	–	–	50	K10	74	N13	E	E (100 mA)	2
F	81	–	–	–	52	J10	77	M13	E	F (200 mA)	2
	82	–	–	–	–	–	–	–	–	–	2
	83	25	B	C	53	H10	78	L13	E	F (200 mA)	2
	84	–	–	–	–	–	79	L14	E	F (200 mA)	2
	85	–	–	–	54	H9	80	L12	E	F (200 mA)	2
	86	–	–	–	55	J9	81	M12	E	F (200 mA)	2
	87	–	–	–	–	–	–	–	–	–	2
	88	–	–	–	56	G9	82	K12	E	F (200 mA)	2
	89	–	–	–	57	G10	83	K13	E	F (200 mA)	2
	90	–	–	–	–	–	–	–	–	–	2
	91	26	B	C	58	G8	84	K11	E	F (200 mA)	2
	92	–	–	–	–	–	86	J14	F	F (200 mA)	2
	93	28 *(2)*	A	C	60 *(2)*	F9	87 *(2)*	J12	F	F (200 mA)	2
	94	–	–	–	61	F10	88	J13	F	F (200 mA)	2
	95	–	–	–	–	–	–	–	–	–	2
	96	29 *(1)*	A	C	62 *(1)*	F8 *(1)*	89 *(1)*	J11 *(1)*	F	F (200 mA)	2

Table 47. EPM7128B I/O Pins & I/O Standard Groups (Part 4 of 4)

LAB	MC	48-Pin VTQFP	IOGND Group for 48-Pin VTQFP (200 mA)	IOVCC Group for 48-Pin VTQFP (100 mA)	100-Pin TQFP	100-Pin FineLine BGA	144-Pin TQFP	256-Pin FineLine BGA	IOGND Group for Other Packages (200 mA)	IOVCC Group for Other Packages	I/O Bank
G	97	–	–	–	63	F7	91	J10	F	F (200 mA)	2
	98	–	–	–	–	–	–	–	–	–	2
	99	30	A	C	64	E9	92	H12	F	F (200 mA)	2
	100	–	–	–	–	–	93	H14	F	F (200 mA)	2
	101	31	A	C	65	E10	94	H13	F	F (200 mA)	2
	102	–	–	–	67	E8 *(2)*	96	H11 *(2)*	F	G (200 mA)	2
	103	–	–	–	–	–	–	–	–	–	2
	104	–	–	–	68	E7	97	H10	F	G (200 mA)	2
	105	–	–	–	69	D9	98	G12	F	G (200 mA)	2
	106	–	–	–	–	–	–	–	–	–	2
	107	33	A	D	70	D10	99	G13	F	G (200 mA)	2
	108	–	–	–	–	–	100	F14	F	G (200 mA)	2
	109	34	A	D	71	D8	101	G11	F	G (200 mA)	2
	110	–	–	–	72	C9	102	F12	F	G (200 mA)	2
	111	–	–	–	–	–	–	–	–	–	2
	112	35 *(1)*	A	D	73 *(1)*	A10 *(1)*	104 *(1)*	D13 *(1)*	F	G (200 mA)	2
H	113	–	–	–	75	C10	106	F13	A	G (200 mA)	2
	114	–	–	–	–	–	–	–	–	–	2
	115	36	A	D	76	B10	107	E13	A	G (200 mA)	2
	116	–	–	–	–	–	109	C12	A	G (200 mA)	2
	117	37	A	D	77	B9	110	E12	A	G (200 mA)	2
	118	–	–	–	78	A9	111	D12	A	G (200 mA)	2
	119	–	–	–	–	–	–	–	–	–	2
	120	–	–	–	79	A8	112	D11	A	G (200 mA)	2
	121	–	–	–	80	B8	113	E11	A	G (200 mA)	2
	122	–	–	–	–	–	–	–	–	–	2
	123	38	A	D	81	A7	114	D10	A	G (200 mA)	2
	124	–	–	–	–	–	116	C10	A	H (100 mA)	2
	125	39	A	D	83	B7	117	E10	A	H (100 mA)	2
	126	–	–	–	84	C7	118	F10	A	H (100 mA)	2
	127	–	–	–	–	–	–	–	–	–	2
	128	–	–	–	85	C6	119	F9	A	H (100 mA)	2

Notes to tables:

(1) This pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for in-system programming, this pin is not available as a user I/O pin.

(2) This pin may function as either a VREF pin or a user I/O pin. If this pin is programmed to be a VREF pin for using the advanced I/O standards, then this pin is not available as a user I/O pin.

(3) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 48. EPM7256B Dedicated Pin-Outs

Dedicated Pin	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine BGA
INPUT/GCLK1	87	125	184	D9
INPUT/GCLRn	89	127	182	E8
INPUT/OE1	88	126	183	E9
INPUT/OE2/GCLK2	90	128	181	D8
TDI *(1)*	4	4	176	D4
TMS *(1)*	15	20	127	J6
TCK *(1)*	62	89	30	J11
TDO *(1)*	73	104	189	D13
VREFA *(2)*	12	14	128	J4
VREFB *(2)*	60	87	22	H11
GNDINT	38, 86	52, 57, 124, 129	75, 82, 180, 185	A8, C9, G9, K8, P9
GNDIO *(2)*	11, 26, 43, 59, 74, 95	3, 13, 17, 33, 59, 64, 85, 105, 135	14, 32, 50, 72, 94, 116, 134, 152, 174, 200	A3, B10, C2, D14, F6, G10, H8, J9, K7, L11, M3, P6, P10, R2, R3, T1, T15
VCCINT (2.5 V Only)	39, 91	51, 58, 123, 130	74, 83, 179, 186	B9, C8, G8, K9, P8
VCCIO1 (1.8 V, 2.5 V, or 3.3 V)	3, 18, 34	24, 50, 144	85, 107, 125, 143, 165	B3, B5, G3, G7, J8, L3, L6, T2, T3
VCCIO2 (1.8 V, 2.5 V, or 3.3 V)	51, 66, 82	73, 76, 95, 115	5, 23, 41, 63, 191	C14, E15, F11, G15, H9, K10, M15, P14
No Connect (N.C.)	–	–	1, 2, 51, 52, 53, 54, 103, 104, 105, 106, 155, 156, 157, 158, 207, 208	A1, A2, A6, A12, A13, A14, A15, A16, B1, B2, B15, B16, C1, C15, C16, D1, D3, D15, D16, G1, G16, H15, H16, J1, K1, L1, L2, M1, M16, N1, N2, N14, N15, N16, P1, P2, P15, P16, R1, R14, R15, R16, T7, T8, T10, T11, T14, T16
Total User I/O Pins	84	120	164	164

Table 49. EPM7256B I/O Pin-Outs & I/O Standards (Part 1 of 8)

Lab	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
A	1	–	–	–	–	–	–	1
	2	–	–	–	–	–	–	1
	3	–	–	–	2	B	B (200 mA)	1
	4	–	–	–	–	–	–	1
	5	–	–	–	1	B	B (200 mA)	1
	6	–	–	–	143	B	A (100 mA)	1
	7	–	–	–	–	–	–	1
	8	2	B	A (100 mA)	–	–	–	1
	9	1	B	A (100 mA)	–	–	–	1
	10	–	–	–	–	–	–	1
	11	100	B	A (100 mA)	142	B	A (100 mA)	1
	12	–	–	–	–	–	–	1
	13	–	–	–	141	B	A (100 mA)	1
	14	99	B	A (100 mA)	140	B	A (100 mA)	1
	15	–	–	–	–	–	–	1
	16	98	B	A (100 mA)	139	B	A (100 mA)	1
B	17	–	–	–	–	–	–	1
	18	–	–	–	–	–	–	1
	19	–	–	–	10	C	B (200 mA)	1
	20	–	–	–	–	–	–	1
	21	–	–	–	9	C	B (200 mA)	1
	22	–	–	–	–	–	–	1
	23	–	–	–	–	–	–	1
	24	8	B	B (200 mA)	8	C	B (200 mA)	1
	25	7	B	B (200 mA)	7	C	B (200 mA)	1
	26	–	–	–	–	–	–	1
	27	6	B	B (200 mA)	6	C	B (200 mA)	1
	28	–	–	–	–	–	–	1
	29	5	B	B (200 mA)	5	C	B (200 mA)	1
	30	–	–	–	–	–	–	1
	31	–	–	–	–	–	–	1
	32	4 *(1)*	B	B (200 mA)	4 *(1)*	C	B (200 mA)	1

Table 49. EPM7256B I/O Pin-Outs & I/O Standards (Part 2 of 8)

Lab	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
C	33	–	–	–	36	D	C (200 mA)	1
	34	–	–	–	–	–	–	1
	35	–	–	–	35	D	C (200 mA)	1
	36	–	–	–	–	–	–	1
	37	–	–	–	34	D	C (200 mA)	1
	38	–	–	–	–	–	–	1
	39	–	–	–	–	–	–	1
	40	25	C	C (200 mA)	32	C	C (200 mA)	1
	41	24	C	C (200 mA)	31	C	C (200 mA)	1
	42	–	–	–	–	–	–	1
	43	23	C	C (200 mA)	30	C	C (200 mA)	1
	44	–	–	–	–	–	–	1
	45	22	C	C (200 mA)	29	C	C (200 mA)	1
	46	–	–	–	–	–	–	1
	47	–	–	–	–	–	–	1
	48	21	C	C (200 mA)	28	C	C (200 mA)	1
D	49	31	D	C (200 mA)	44	D	C (200 mA)	1
	50	–	–	–	–	–	–	1
	51	30	D	C (200 mA)	43	D	C (200 mA)	1
	52	–	–	–	–	–	–	1
	53	29	D	C (200 mA)	42	D	C (200 mA)	1
	54	28	D	C (200 mA)	41	D	C (200 mA)	1
	55	–	–	–	–	–	–	1
	56	–	–	–	40	D	C (200 mA)	1
	57	–	–	–	–	–	–	1
	58	–	–	–	–	–	–	1
	59	–	–	–	39	D	C (200 mA)	1
	60	–	–	–	–	–	–	1
	61	–	–	–	38	D	C (200 mA)	1
	62	–	–	–	–	–	–	1
	63	–	–	–	–	–	–	1
	64	27	D	C (200 mA)	37	D	C (200 mA)	1

Table 49. EPM7256B I/O Pin-Outs & I/O Standards (Part 3 of 8)

Lab	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
E	65	–	–	–	–	–	–	1
	66	–	–	–	–	–	–	1
	67	–	–	–	–	–	–	1
	68	–	–	–	–	–	–	1
	69	–	–	–	138	B	A (100 mA)	1
	70	–	–	–	–	–	–	1
	71	–	–	–	–	–	–	1
	72	97	B	A (100 mA)	137	B	A (100 mA)	1
	73	96	B	A (100 mA)	136	B	A (100 mA)	1
	74	–	–	–	–	–	–	1
	75	94	A	A (100 mA)	134	A	A (100 mA)	1
	76	–	–	–	–	–	–	1
	77	93	A	A (100 mA)	133	A	A (100 mA)	1
	78	–	–	–	132	A	A (100 mA)	1
	79	–	–	–	–	–	–	1
	80	92	A	A (100 mA)	131	A	A (100 mA)	1
F	81	–	–	–	–	–	–	1
	82	–	–	–	–	–	–	1
	83	–	–	–	19	C	B (200 mA)	1
	84	–	–	–	–	–	–	1
	85	–	–	–	18	C	B (200 mA)	1
	86	–	–	–	–	–	–	1
	87	–	–	–	–	–	–	1
	88	14	C	B (200 mA)	16	C	B (200 mA)	1
	89	13	C	B (200 mA)	15	C	B (200 mA)	1
	90	–	–	–	–	–	–	1
	91	12 *(2)*	C	B (200 mA)	14 *(2)*	C	B (200 mA)	1
	92	–	–	–	–	–	–	1
	93	10	B	B (200 mA)	12	C	B (200 mA)	1
	94	–	–	–	–	–	–	1
	95	–	–	–	–	–	–	1
	96	9	B	B (200 mA)	11	C	B (200 mA)	1

Table 49. EPM7256B I/O Pin-Outs & I/O Standards (Part 4 of 8)

Lab	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
G	97	–	–	–	–	–	–	1
	98	–	–	–	–	–	–	1
	99	–	–	–	27	C	C (200 mA)	1
	100	–	–	–	–	–	–	1
	101	–	–	–	26	C	C (200 mA)	1
	102	–	–	–	–	–	–	1
	103	–	–	–	–	–	–	1
	104	20	C	C (200 mA)	25	C	C (200 mA)	1
	105	19	C	C (200 mA)	23	C	B (200 mA)	1
	106	–	–	–	–	–	–	1
	107	17	C	B (200 mA)	22	C	B (200 mA)	1
	108	–	–	–	–	–	–	1
	109	16	C	B (200 mA)	21	C	B (200 mA)	1
	110	–	–	–	–	–	–	1
	111	–	–	–	–	–	–	1
	112	15 *(1)*	C	B (200 mA)	20 *(1)*	C	B (200 mA)	1
H	113	37	D	D (58 mA)	–	–	–	1
	114	–	–	–	–	–	–	1
	115	36	D	D (58 mA)	54	D	D (58 mA)	1
	116	–	–	–	–	–	–	1
	117	–	–	–	53	D	D (58 mA)	1
	118	35	D	D (58 mA)	–	–	–	1
	119	–	–	–	–	–	–	1
	120	–	–	–	49	D	C (200 mA)	1
	121	–	–	–	48	D	C (200 mA)	1
	122	–	–	–	–	–	–	1
	123	–	–	–	47	D	C (200 mA)	1
	124	–	–	–	–	–	–	1
	125	33	D	C (200 mA)	46	D	C (200 mA)	1
	126	–	–	–	–	–	–	1
	127	–	–	–	–	–	–	1
	128	32	D	C (200 mA)	45	D	C (200 mA)	1

Table 49. EPM7256B I/O Pin-Outs & I/O Standards (Part 5 of 8)

Lab	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
I	129	80	A	G (200 mA)	114	A	H (200 mA)	2
	130	–	–	–	–	–	–	2
	131	81	A	G (200 mA)	116	A	I (100 mA)	2
	132	–	–	–	–	–	–	2
	133	–	–	–	117	A	I (100 mA)	2
	134	–	–	–	–	–	–	2
	135	–	–	–	–	–	–	2
	136	–	–	–	118	A	I (100 mA)	2
	137	–	–	–	119	A	I (100 mA)	2
	138	–	–	–	–	–	–	2
	139	83	A	H (100 mA)	120	A	I (100 mA)	2
	140	–	–	–	–	–	–	2
	141	84	A	H (100 mA)	121	A	I (100 mA)	2
	142	–	–	–	–	–	–	2
	143	–	–	–	–	–	–	2
	144	85	A	H (100 mA)	122	A	I (100 mA)	2
J	145	63	F	F (200 mA)	–	–	–	2
	146	–	–	–	–	–	–	2
	147	64	F	F (200 mA)	90	G	G (200 mA)	2
	148	–	–	–	–	–	–	2
	149	65	F	F (200 mA)	91	G	G (200 mA)	2
	150	–	–	–	–	–	–	2
	151	–	–	–	–	–	–	2
	152	–	–	–	92	G	G (200 mA)	2
	153	–	–	–	93	G	G (200 mA)	2
	154	–	–	–	–	–	–	2
	155	67	F	G (200 mA)	94	G	G (200 mA)	2
	156	–	–	–	–	–	–	2
	157	–	–	–	96	G	H (200 mA)	2
	158	–	–	–	–	–	–	2
	159	–	–	–	–	–	–	2
	160	68	F	G (200 mA)	97	G	H (200 mA)	2

Table 49. EPM7256B I/O Pin-Outs & I/O Standards (Part 6 of 8)

Lab	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
K	161	–	–	–	–	–	–	2
	162	–	–	–	–	–	–	2
	163	57	E	F (200 mA)	82	F	G (200 mA)	2
	164	–	–	–	–	–	–	2
	165	–	–	–	83	F	G (200 mA)	2
	166	–	–	–	–	–	–	2
	167	–	–	–	–	–	–	2
	168	58	E	F (200 mA)	84	F	G (200 mA)	2
	169	–	–	–	86	G	G (200 mA)	2
	170	–	–	–	–	–	–	2
	171	60 *(2)*	F	F (200 mA)	87 *(2)*	G	G (200 mA)	2
	172	–	–	–	–	–	–	2
	173	61	F	F (200 mA)	88	G	G (200 mA)	2
	174	–	–	–	–	–	–	2
	175	–	–	–	–	–	–	2
	176	62 *(1)*	F	F (200 mA)	89 *(1)*	G	G (100 mA)	2
L	177	–	–	–	–	–	–	1
	178	–	–	–	–	–	–	1
	179	–	–	–	55	D	D (58 mA)	1
	180	–	–	–	–	–	–	1
	181	–	–	–	56	D	D (58 mA)	1
	182	–	–	–	–	–	–	2
	183	–	–	–	–	–	–	2
	184	40	D	E (100 mA)	60	E	E (100 mA)	2
	185	41	D	E (100 mA)	61	E	E (100 mA)	2
	186	–	–	–	–	–	–	2
	187	42	D	E (100 mA)	62	E	E (100 mA)	2
	188	–	–	–	–	–	–	2
	189	44	E	E (100 mA)	63	E	E (100 mA)	2
	190	–	–	–	–	–	–	2
	191	–	–	–	–	–	–	2
	192	45	E	E (100 mA)	65	F	E (100 mA)	2

Table 49. EPM7256B I/O Pin-Outs & I/O Standards (Part 7 of 8)

Lab	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
M	193	–	–	–	106	A	H (200 mA)	2
	194	–	–	–	–	–	–	2
	195	75	A	G (200 mA)	107	A	H (200 mA)	2
	196	–	–	–	–	–	–	2
	197	–	–	–	108	A	H (200 mA)	2
	198	–	–	–	–	–	–	2
	199	–	–	–	–	–	–	2
	200	–	–	–	109	A	H (200 mA)	2
	201	76	A	G (200 mA)	110	A	H (200 mA)	2
	202	–	–	–	–	–	–	2
	203	77	A	G (200 mA)	111	A	H (200 mA)	2
	204	–	–	–	–	–	–	2
	205	–	–	–	–	–	–	2
	206	78	A	G (200 mA)	112	A	H (200 mA)	2
	207	–	–	–	–	–	–	2
	208	79	A	G (200 mA)	113	A	H (200 mA)	2
N	209	–	–	–	–	–	–	2
	210	–	–	–	–	–	–	2
	211	69	F	G (200 mA)	98	G	H (200 mA)	2
	212	–	–	–	–	–	–	2
	213	–	–	–	99	G	H (200 mA)	2
	214	–	–	–	–	–	–	2
	215	–	–	–	–	–	–	2
	216	70	F	G (200 mA)	100	G	H (200 mA)	2
	217	–	–	–	101	G	H (200 mA)	2
	218	–	–	–	–	–	–	2
	219	71	F	G (200 mA)	102	G	H (200 mA)	2
	220	–	–	–	–	–	–	2
	221	72	F	G (200 mA)	103	G	H (200 mA)	2
	222	–	–	–	–	–	–	2
	223	–	–	–	–	–	–	2
	224	73 *(1)*	F	G (200 mA)	104 *(1)*	G	H (200 mA)	2

Table 49. EPM7256B I/O Pin-Outs & I/O Standards (Part 8 of 8)

Lab	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
P	225	–	–	–	–	–	–	2
	226	–	–	–	–	–	–	2
	227	–	–	–	74	F	F (200 mA)	2
	228	–	–	–	–	–	–	2
	229	–	–	–	75	F	F (200 mA)	2
	230	–	–	–	–	–	–	2
	231	–	–	–	–	–	–	2
	232	52	E	F (200 mA)	77	F	G (200 mA)	2
	233	53	E	F (200 mA)	78	F	G (200 mA)	2
	234	–	–	–	–	–	–	2
	235	54	E	F (200 mA)	79	F	G (200 mA)	2
	236	–	–	–	–	–	–	2
	237	55	E	F (200 mA)	80	F	G (200 mA)	2
	238	–	–	–	–	–	–	2
	239	–	–	–	–	–	–	2
	240	56	E	F (200 mA)	81	F	G (200 mA)	2
Q	241	46	E	E (100 mA)	66	F	E (100 mA)	2
	242	–	–	–	–	–	–	2
	243	47	E	E (100 mA)	67	F	E (100 mA)	2
	244	–	–	–	–	–	–	2
	245	48	E	E (100 mA)	68	F	E (100 mA)	2
	246	49	E	E (100 mA)	69	F	E (100 mA)	2
	247	–	–	–	–	–	–	2
	248	–	–	–	–	–	–	2
	249	–	–	–	70	F	E (100 mA)	2
	250	–	–	–	–	–	–	2
	251	–	–	–	–	–	–	2
	252	–	–	–	–	–	–	2
	253	–	–	–	71	F	E (100 mA)	2
	254	–	–	–	–	–	–	2
	255	–	–	–	–	–	–	2
	256	50	E	E (100 mA)	72	F	E (100 mA)	2

Notes to tables:

(1) This pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for in-system programming, this pin is not available as a user I/O pin.

(2) This pin may function as either a VREF pin or a user I/O pin. If this pin is programmed to be a VREF pin for using the advanced I/O standards, then this pin is not available as a user I/O pin.

(3) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 50. EPM7256B I/O Pin-Outs & I/O Standards (Part 1 of 9)

LAB	MC	208-Pin PQFP *(4)*	IOGND group for 208-Pin PQFP (200 mA)	256-Pin FineLine BGA	IOGND group for 256-Pin FineLine BGA (200 mA)	IOVCC group for 208 & 256-Pin Packages	I/O Bank
A	1	153	B	C3	B	B (200 mA)	1
	2	–	–	–	–	–	1
	3	154	B	C4	B	B (200 mA)	1
	4	–	–	–	–	–	1
	5	159	B	E5	B	B (200 mA)	1
	6	160	B	D5	B	B (200 mA)	1
	7	–	–	–	–	–	1
	8	161	B	C5	B	B (200 mA)	1
	9	162	B	B4	B	B (200 mA)	1
	10	–	–	–	–	–	1
	11	163	B	A4	B	B (200 mA)	1
	12	–	–	–	–	–	1
	13	164	B	A5	B	B (200 mA)	1
	14	166	B	D6	B	A (100 mA)	1
	15	–	–	–	–	–	1
	16	167	B	C6	B	A (100 mA)	1

Table 50. EPM7256B I/O Pin-Outs & I/O Standards (Part 2 of 9)

LAB	MC	208-Pin PQFP *(4)*	IOGND group for 208-Pin PQFP (200 mA)	256-Pin FineLine BGA	IOGND group for 256-Pin FineLine BGA (200 mA)	IOVCC group for 208 & 256-Pin Packages	I/O Bank
B	17	141	C	F5	C	C (200 mA)	1
	18	–	–	–	–	–	1
	19	142	C	F2	C	C (200 mA)	1
	20	–	–	–	–	–	1
	21	144	C	E1	C	B (200 mA)	1
	22	145	C	F4	C	B (200 mA)	1
	23	–	–	–	–	–	1
	24	146	C	F3	C	B (200 mA)	1
	25	147	C	E2	C	B (200 mA)	1
	26	–	–	–	–	–	1
	27	148	C	D2	C	B (200 mA)	1
	28	–	–	–	–	–	1
	29	149	C	E3	C	B (200 mA)	1
	30	150	C	E4	C	B (200 mA)	1
	31	–	–	–	–	–	1
	32	151	C	D4 *(1)*	C	B (200 mA)	1
C	33	108	E	N4	E	D (200 mA)	1
	34	–	–	–	–	–	1
	35	109	E	P3	E	D (200 mA)	1
	36	–	–	–	–	–	1
	37	110	E	N3	E	D (200 mA)	1
	38	111	E	M4	E	D (200 mA)	1
	39	–	–	–	–	–	1
	40	112	E	M2	E	D (200 mA)	1
	41	113	E	L4	E	D (200 mA)	1
	42	–	–	–	–	–	1
	43	114	E	L5	E	D (200 mA)	1
	44	–	–	–	–	–	1
	45	115	E	K6	E	D (200 mA)	1
	46	117	D	K5	D	D (200 mA)	1
	47	–	–	–	–	–	1
	48	118	D	K4	D	D (200 mA)	1

Table 50. EPM7256B I/O Pin-Outs & I/O Standards (Part 3 of 9)

LAB	MC	208-Pin PQFP *(4)*	IOGND group for 208-Pin PQFP (200 mA)	256-Pin FineLine BGA	IOGND group for 256-Pin FineLine BGA (200 mA)	IOVCC group for 208 & 256-Pin Packages	I/O Bank
D	49	92	F	N6	F	E (200 mA)	1
	50	–	–	–	–	–	1
	51	93	F	T5	F	E (200 mA)	1
	52	–	–	–	–	–	1
	53	95	E	M6	E	E (200 mA)	1
	54	96	E	R5	E	E (200 mA)	1
	55	–	–	–	–	–	1
	56	97	E	M5	E	E (200 mA)	1
	57	98	E	P5	E	E (200 mA)	1
	58	–	–	–	–	–	1
	59	99	E	N5	E	E (200 mA)	1
	60	–	–	–	–	–	1
	61	100	E	T4	E	E (200 mA)	1
	62	101	E	R4	E	E (200 mA)	1
	63	–	–	–	–	–	1
	64	102	E	P4	E	E (200 mA)	1
E	65	168	B	B6	B	A (100 mA)	1
	66	–	–	–	–	–	1
	67	169	B	E6	B	A (100 mA)	1
	68	–	–	–	–	–	1
	69	170	B	F7	B	A (100 mA)	1
	70	171	B	E7	B	A (100 mA)	1
	71	–	–	–	–	–	1
	72	172	B	D7	B	A (100 mA)	1
	73	173	B	C7	B	A (100 mA)	1
	74	–	–	–	–	–	1
	75	175	A	B7	A	A (100 mA)	1
	76	–	–	–	–	–	1
	77	176 *(1)*	A	A7	A	A (100 mA)	1
	78	177	A	F8	A	A (100 mA)	1
	79	–	–	–	–	–	1
	80	178	A	B8	A	A (100 mA)	1

Table 50. EPM7256B I/O Pin-Outs & I/O Standards (Part 4 of 9)

LAB	MC	208-Pin PQFP *(4)*	IOGND group for 208-Pin PQFP (200 mA)	256-Pin FineLine BGA	IOGND group for 256-Pin FineLine BGA (200 mA)	IOVCC group for 208 & 256-Pin Packages	I/O Bank
F	81	130	D	H5	D	C (200 mA)	1
	82	–	–	–	–	–	1
	83	131	D	H1	D	C (200 mA)	1
	84	–	–	–	–	–	1
	85	132	D	H2	D	C (200 mA)	1
	86	133	D	H3	D	C (200 mA)	1
	87	–	–	–	–	–	1
	88	135	C	H4	C	C (200 mA)	1
	89	136	C	G6	C	C (200 mA)	1
	90	–	–	–	–	–	1
	91	137	C	G5	C	C (200 mA)	1
	92	–	–	–	–	–	1
	93	138	C	G2	C	C (200 mA)	1
	94	139	C	G4	C	C (200 mA)	1
	95	–	–	–	–	–	1
	96	140	C	F1	C	C (200 mA)	1
G	97	119	D	K3	D	D (200 mA)	1
	98	–	–	–	–	–	1
	99	120	D	K2	D	D (200 mA)	1
	100	–	–	–	–	–	1
	101	121	D	J7	D	D (200 mA)	1
	102	122	D	H7	D	D (200 mA)	1
	103	–	–	–	–	–	1
	104	123	D	J5	D	D (200 mA)	1
	105	124	D	J2	D	D (200 mA)	1
	106	–	–	–	–	–	1
	107	126	D	J3	D	C (200 mA)	1
	108	–	–	–	–	–	1
	109	127 *(1)*	D	J4 *(2)*	D	C (200 mA)	1
	110	128 *(2)*	D	H6	D	C (200 mA)	1
	111	–	–	–	–	–	1
	112	129	D	J6 *(1)*	D	C (200 mA)	1

Table 50. EPM7256B I/O Pin-Outs & I/O Standards (Part 5 of 9)

LAB	MC	208-Pin PQFP *(4)*	IOGND group for 208-Pin PQFP (200 mA)	256-Pin FineLine BGA	IOGND group for 256-Pin FineLine BGA (200 mA)	IOVCC group for 208 & 256-Pin Packages	I/O Bank
H	113	79	F	M8	F	F (100 mA)	1
	114	–	–	–	–	–	1
	115	80	F	N8	F	F (100 mA)	1
	116	–	–	–	–	–	1
	117	81	F	L8	F	F (100 mA)	1
	118	84	F	R7	F	F (100 mA)	1
	119	–	–	–	–	–	1
	120	86	F	P7	F	E (200 mA)	1
	121	87	F	N7	F	E (200 mA)	1
	122	–	–	–	–	–	1
	123	88	F	M7	F	E (200 mA)	1
	124	–	–	–	–	–	1
	125	89	F	L7	F	E (200 mA)	1
	126	90	F	T6	F	E (200 mA)	1
	127	–	–	–	–	–	1
	128	91	F	R6	F	E (200 mA)	1
I	129	197	A	C11	A	K (200 mA)	2
	130	–	–	–	–	–	2
	131	196	A	B11	A	K (200 mA)	2
	132	–	–	–	–	–	2
	133	195	A	A11	A	K (200 mA)	2
	134	194	A	F10	A	K (200 mA)	2
	135	–	–	–	–	–	2
	136	193	A	E10	A	K (200 mA)	2
	137	192	A	A10	A	K (200 mA)	2
	138	–	–	–	–	–	2
	139	190	A	C10	A	L (100 mA)	2
	140	–	–	–	–	–	2
	141	189 *(1)*	A	D10	A	L (100 mA)	2
	142	188	A	F9	A	L (100 mA)	2
	143	–	–	–	–	–	2
	144	187	A	A9	A	L (100 mA)	2

Table 50. EPM7256B I/O Pin-Outs & I/O Standards (Part 6 of 9)

LAB	MC	208-Pin PQFP *(4)*	IOGND group for 208-Pin PQFP (200 mA)	256-Pin FineLine BGA	IOGND group for 256-Pin FineLine BGA (200 mA)	IOVCC group for 208 & 256-Pin Packages	I/O Bank
J	145	27	I	J15	I	I (200 mA)	2
	146	–	–	–	–	–	2
	147	26	I	J16	I	I (200 mA)	2
	148	–	–	–	–	–	2
	149	25	I	J10	I	I (200 mA)	2
	150	24	I	H14	I	I (200 mA)	2
	151	–	–	–	–	–	2
	152	22 *(2)*	I	H13	I	J (200 mA)	2
	153	21	I	H12	I	J (200 mA)	2
	154	–	–	–	–	–	2
	155	20	I	H11 *(2)*	I	J (200 mA)	2
	156	–	–	–	–	–	2
	157	19	I	H10	I	J (200 mA)	2
	158	18	I	G11	I	J (200 mA)	2
	159	–	–	–	–	–	2
	160	17	I	G14	I	J (200 mA)	2
K	161	38	H	K11	H	I (200 mA)	2
	162	–	–	–	–	–	2
	163	37	H	K12	H	I (200 mA)	2
	164	–	–	–	–	–	2
	165	36	H	K14	H	I (200 mA)	2
	166	35	H	K13	H	I (200 mA)	2
	167	–	–	–	–	–	2
	168	34	H	K15	H	I (200 mA)	2
	169	33	H	K16	H	I (200 mA)	2
	170	–	–	–	–	–	2
	171	31	I	J13	I	I (200 mA)	2
	172	–	–	–	–	–	2
	173	30 *(1)*	I	J14	I	I (200 mA)	2
	174	29	I	J12	I	I (200 mA)	2
	175	–	–	–	–	–	2
	176	28	I	J11 *(1)*	I	I (200 mA)	2

Table 50. EPM7256B I/O Pin-Outs & I/O Standards (Part 7 of 9)

LAB	MC	208-Pin PQFP *(4)*	IOGND group for 208-Pin PQFP (200 mA)	256-Pin FineLine BGA	IOGND group for 256-Pin FineLine BGA (200 mA)	IOVCC group for 208 & 256-Pin Packages	I/O Bank
L	177	78	F	R8	F	F (100 mA)	2
	178	–	–	–	–	–	2
	179	77	F	T9	F	F (100 mA)	2
	180	–	–	–	–	–	2
	181	76	F	R9	F	F (100 mA)	2
	182	73	F	N9	F	G (100 mA)	2
	183	–	–	–	–	–	2
	184	71	G	M9	G	G (100 mA)	2
	185	70	G	L9	G	G (100 mA)	2
	186	–	–	–	–	–	2
	187	69	G	R10	G	G (100 mA)	2
	188	–	–	–	–	–	2
	189	68	G	N10	G	G (100 mA)	2
	190	67	G	M10	G	G (100 mA)	2
	191	–	–	–	–	–	2
	192	66	G	L10	G	G (100 mA)	2
M	193	4	J	B14	J	K (200 mA)	2
	194	–	–	–	–	–	2
	195	3	J	C13	J	K (200 mA)	2
	196	–	–	–	–	–	2
	197	206	J	B13	J	K (200 mA)	2
	198	205	J	F12	J	K (200 mA)	2
	199	–	–	–	–	–	2
	200	204	J	E12	J	K (200 mA)	2
	201	203	J	D12	J	K (200 mA)	2
	202	–	–	–	–	–	2
	203	202	J	C12	J	K (200 mA)	2
	204	–	–	–	–	–	2
	205	201	J	B12	J	K (200 mA)	2
	206	199	A	E11	A	K (200 mA)	2
	207	–	–	–	–	–	2
	208	198	A	D11	A	K (200 mA)	2

Table 50. EPM7256B I/O Pin-Outs & I/O Standards (Part 8 of 9)

LAB	MC	208-Pin PQFP *(4)*	IOGND group for 208-Pin PQFP (200 mA)	256-Pin FineLine BGA	IOGND group for 256-Pin FineLine BGA (200 mA)	IOVCC group for 208 & 256-Pin Packages	I/O Bank
N	209	16	I	G13	I	J (200 mA)	2
	210	–	–	–	–	–	2
	211	15	I	G12	I	J (200 mA)	2
	212	–	–	–	–	–	2
	213	13	J	F16	J	J (200 mA)	2
	214	12	J	F15	J	J (200 mA)	2
	215	–	–	–	–	–	2
	216	11	J	F13	J	J (200 mA)	2
	217	10	J	F14	J	J (200 mA)	2
	218	–	–	–	–	–	2
	219	9	J	E16	J	J (200 mA)	2
	220	–	–	–	–	–	2
	221	8	J	E14	J	J (200 mA)	2
	222	7	J	E13	J	J (200 mA)	2
	223	–	–	–	–	–	2
	224	6	J	D13 *(1)*	J	J (200 mA)	2
O	225	49	H	R13	H	H (200 mA)	2
	226	–	–	–	–	–	2
	227	48	H	P13	H	H (200 mA)	2
	228	–	–	–	–	–	2
	229	47	H	N13	H	H (200 mA)	2
	230	46	H	M14	H	H (200 mA)	2
	231	–	–	–	–	–	2
	232	45	H	M13	H	H (200 mA)	2
	233	44	H	L13	H	H (200 mA)	2
	234	–	–	–	–	–	2
	235	43	H	L14	H	H (200 mA)	2
	236	–	–	–	–	–	2
	237	42	H	L12	H	H (200 mA)	2
	238	40	H	L15	H	I (200 mA)	2
	239	–	–	–	–	–	2
	240	39	H	L16	H	I (200 mA)	2

Table 50. EPM7256B I/O Pin-Outs & I/O Standards (Part 9 of 9)

LAB	MC	208-Pin PQFP *(4)*	IOGND group for 208-Pin PQFP (200 mA)	256-Pin FineLine BGA	IOGND group for 256-Pin FineLine BGA (200 mA)	IOVCC group for 208 & 256-Pin Packages	I/O Bank
P	241	65	G	R11	G	G (100 mA)	2
	242	–	–	–	–	–	2
	243	64	G	P11	G	G (100 mA)	2
	244	–	–	–	–	–	2
	245	62	G	N11	G	H (200 mA)	2
	246	61	G	M11	G	H (200 mA)	2
	247	–	–	–	–	–	2
	248	60	G	T12	G	H (200 mA)	2
	249	59	G	R12	G	H (200 mA)	2
	250	–	–	–	–	–	2
	251	58	G	M12	G	H (200 mA)	2
	252	–	–	–	–	–	2
	253	57	G	P12	G	H (200 mA)	2
	254	56	G	N12	G	H (200 mA)	2
	255	–	–	–	–	–	2
	256	55	G	T13	G	H (200 mA)	2

Notes to tables:

(1) This pin can function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for in-system programming, this pin is not available as a user I/O pin.

(2) This pin may function as either a VREF pin or a user I/O pin. If this pin is programmed to be a VREF pin for using the advanced I/O standards, this pin is not available as a user I/O pin.

(3) The user I/O pin count includes dedicated input pins and all I/O pins.

(4) EPM7512B devices in the 208-pin PQFP package support vertical migration from EPM7256E, EPM7256S, and EPM7256B devices. EPM7512B devices contain additional I/O pins which are no connects on the EPM7256E, EPM7256S, and EPM7256B devices. To support these additional I/O pins, EPM7512B devices have two additional VCCIO1 (pin 105), VCCIO2 (pin 207) and GNDIO (pins 51 and 158) pins that are no-connect pins on the EPM7256E, EPM7256S, and EPM7256B devices. To achieve vertical migration between the EPM7256B and EPM7512B devices, the no-connect pin 105 may be tied to VCCIO1, pin 207 may be tied to VCCIO2, and pins 51 and 158 may be tied to GNDIO on EPM7256B devices.

Table 51. EPM7512B Dedicated Pin-Outs

Dedicated Pin	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP *(1)*	256-Pin BGA	256-Pin FineLine BGA
INPUT/GCLK1	87	125	184	L1	D9
INPUT/GCLRn	89	127	182	K2	E8
INPUT/OE1	88	126	183	K1	E9
INPUT/OE2/GCLK2	90	128	181	K3	D8
TDI *(2)*	4	4	176	A2	D4
TMS *(2)*	15	20	127	B12	J6
TCK *(2)*	62	89	30	V12	J11
TDO *(2)*	73	104	189	Y2	D13
VREFA *(2)*	12	14	128	C12	J4
VREFB *(2)*	60	87	22	V10	H11
GNDINT	38, 86	52, 57, 124, 129	75, 82, 180, 185	J20, K4, K18, L2, L17	A8, C9, G9, K8, P9
GNDIO	11, 26, 43, 59, 74, 95	3, 13, 17, 33, 59, 64, 85, 105, 135	14, 32, 50, 51, 72, 94, 116, 134, 152, 158, 174, 200	A1, B2, B19, B20, C3, C18, D4, D17, U4, U17, V3, V18, V19, W2, W19, Y1, Y20	A3, B10, C2, D14, F6, G10, H8, J9, K7, L11, M3, P6, P10, R2, R3, T1, T15
VCCINT (2.5 V)	39, 91	51, 58, 123, 130	74, 83, 179, 186	J1, J19, L4, M19, M20	B9, C8, G8, K9, P8
VCCIO1 (1.8 V, 2.5 V, 3.3 V)	3, 18, 34	24, 50, 144	85, 105, 107, 125, 143, 165	C4, C17, D3, D5, D16, D18, E4, E17	B3, B5, G3, G7, J8, L3, L6, T2, T3
VCCIO2 (1.8 V, 2.5 V, 3.3 V)	51, 66, 82	73, 76, 95, 115	5, 23, 41, 63, 191, 207	T4, T17, U3, U5, U16, U18, V2, V4, V17	C14, E15, F11,G15, H9, K10, M15, P14
No Connect (N.C.)	–	–	–	–	–
Total User I/O Pins *(3)*	84	120	176	212	212

Table 52. EPM7512B I/O Pin-Outs & I/O Standards (Part 1 of 16)

LAB	MC	100-Pin TQFP	144-Pin TQFP	IOGND Group for TQFP (200 mA)		IOVCC Group for TQFP		I/O Bank
				100 Pin	144 Pin	100 Pin	144 Pin	
A	1	94	134	A	A	A (100 mA)	A (100 mA)	1
	2	–	–	–	–	–	–	1
	3	–	–	–	–	–	–	1
	4	–	–	–	–	–	–	1
	5	–	–	–	–	–	–	1
	6	–	–	–	–	–	–	1
	7	–	–	–	–	–	–	1
	8	–	–	–	–	–	–	1
	9	–	–	–	–	–	–	1
	10	–	–	–	–	–	–	1
	11	93	133	A	A	A (100 mA)	A (100 mA)	1
	12	–	–	–	–	–	–	1
	13	–	–	–	–	–	–	1
	14	92	132	A	A	A (100 mA)	A (100 mA)	1
	15	–	–	–	–	–	–	1
	16	–	131	–	A	A (100 mA)	A (100 mA)	1
B	17	–	–	–	–	–	–	1
	18	–	–	–	–	–	–	1
	19	–	–	–	–	–	–	1
	20	–	–	–	–	–	–	1
	21	–	138	–	B	A (100 mA)	A (100 mA)	1
	22	–	–	–	–	–	–	1
	23	–	–	–	–	–	–	1
	24	–	–	–	–	–	–	1
	25	97	137	B	B	A (100 mA)	A (100 mA)	1
	26	–	–	–	–	–	–	1
	27	96	136	B	B	A (100 mA)	A (100 mA)	1
	28	–	–	–	–	–	–	1
	29	–	–	–	–	–	–	1
	30	–	–	–	–	–	–	1
	31	–	–	–	–	–	–	1
	32	–	–	–	–	–	–	1

Table 52. EPM7512B I/O Pin-Outs & I/O Standards (Part 2 of 16)

LAB	MC	100-Pin TQFP	144-Pin TQFP	IOGND Group for TQFP (200 mA)		IOVCC Group for TQFP		I/O Bank
				100 Pin	144 Pin	100 Pin	144 Pin	
C	33	–	142	–	B	A (100 mA)	A (100 mA)	1
	34	–	–	–	–	–	–	1
	35	–	–	–	–	–	–	1
	36	–	–	–	–	–	–	1
	37	100	141	B	B	A (100 mA)	A (100 mA)	1
	38	–	–	–	–	–	–	1
	39	–	–	–	–	–	–	1
	40	–	–	–	–	–	–	1
	41	99	140	B	B	A (100 mA)	A (100 mA)	1
	42	–	–	–	–	–	–	1
	43	–	–	–	–	–	–	1
	44	–	–	–	–	–	–	1
	45	–	–	–	–	–	–	1
	46	98	139	B	B	A (100 mA)	A (100 mA)	1
	47	–	–	–	–	–	–	1
	48	–	–	–	–	–	–	1
D	49	–	2	–	B	B (200 mA)	B (200 mA)	1
	50	–	–	–	–	–	–	1
	51	–	–	–	–	–	–	1
	52	–	–	–	–	–	–	1
	53	–	1	–	B	B (200 mA)	B (200 mA)	1
	54	–	–	–	–	–	–	1
	55	–	–	–	–	–	–	1
	56	–	–	–	–	–	–	1
	57	–	–	–	–	–	–	1
	58	–	–	–	–	–	–	1
	59	2	–	B	–	A (100 mA)	A (100 mA)	1
	60	–	–	–	–	–	–	1
	61	–	–	–	–	–	–	1
	62	–	–	–	–	–	–	1
	63	–	–	–	–	–	–	1
	64	1	143	B	B	A (100 mA)	A (100 mA)	1

Table 52. EPM7512B I/O Pin-Outs & I/O Standards (Part 3 of 16)

LAB	MC	100-Pin TQFP	144-Pin TQFP	IOGND Group for TQFP (200 mA)		IOVCC Group for TQFP		I/O Bank
				100 Pin	144 Pin	100 Pin	144 Pin	
E	65	–	–	–	–	–	–	1
	66	–	–	–	–	–	–	1
	67	–	7	–	C	B (200 mA)	B (200 mA)	1
	68	–	–	–	–	–	–	1
	69	–	–	–	–	–	–	1
	70	–	–	–	–	–	–	1
	71	–	–	–	–	–	–	1
	72	–	–	–	–	–	–	1
	73	–	–	–	–	–	–	1
	74	–	–	–	–	–	–	1
	75	6	6	B	C	B (200 mA)	B (200 mA)	1
	76	–	–	–	–	–	–	1
	77	–	–	–	–	–	–	1
	78	5	5	B	C	B (200 mA)	B (200 mA)	1
	79	–	–	–	–	–	–	1
	80	4 *(1)*	4 *(1)*	B	C	B (200 mA)	B (200 mA)	1
F	81	–	–	–	–	–	–	1
	82	–	–	–	–	–	–	1
	83	–	–	–	–	–	–	1
	84	–	–	–	–	–	–	1
	85	9	11	B	C	B (200 mA)	B (200 mA)	1
	86	–	–	–	–	–	–	1
	87	–	–	–	–	–	–	1
	88	–	–	–	–	–	–	1
	89	–	–	–	–	–	–	1
	90	–	–	–	–	–	–	1
	91	8	10	B	C	B (200 mA)	B (200 mA)	1
	92	–	–	–	–	–	–	1
	93	–	–	–	–	–	–	1
	94	7	9	B	C	B (200 mA)	B (200 mA)	1
	95	–	–	–	–	–	–	1
	96	–	8	–	C	B (200 mA)	B (200 mA)	1

Table 52. EPM7512B I/O Pin-Outs & I/O Standards (Part 4 of 16)

LAB	MC	100-Pin TQFP	144-Pin TQFP	IOGND Group for TQFP (200 mA)		IOVCC Group for TQFP		I/O Bank
				100 Pin	144 Pin	100 Pin	144 Pin	
G	97	–	–	–	–	–	–	1
	98	–	–	–	–	–	–	1
	99	–	15	–	D	B (200 mA)	B (200 mA)	1
	100	–	–	–	–	–	–	1
	101	12 *(2)*	14 *(2)*	C	D	B (200 mA)	B (200 mA)	1
	102	–	–	–	–	–	–	1
	103	–	–	–	–	–	–	1
	104	–	–	–	–	–	–	1
	105	–	–	–	–	–	–	1
	106	–	–	–	–	–	–	1
	107	–	–	–	–	–	–	1
	108	–	–	–	–	–	–	1
	109	–	–	–	–	–	–	1
	110	10	12	B	C	B (200 mA)	B (200 mA)	1
	111	–	–	–	–	–	–	1
	112	–	–	–	–	–	–	1
H	113	14	19	C	E	B (200 mA)	B (200 mA)	1
	114	–	–	–	–	–	–	1
	115	–	–	–	–	–	–	1
	116	–	–	–	–	–	–	1
	117	13	18	C	E	B (200 mA)	B (200 mA)	1
	118	–	–	–	–	–	–	1
	119	–	–	–	–	–	–	1
	120	–	–	–	–	–	–	1
	121	–	–	–	–	–	–	1
	122	–	–	–	–	–	–	1
	123	–	–	–	–	–	–	1
	124	–	–	–	–	–	–	1
	125	–	–	–	–	–	–	1
	126	–	–	–	–	–	–	1
	127	–	–	–	–	–	–	1
	128	–	16	–	D	B (200 mA)	B (200 mA)	1

Table 52. EPM7512B I/O Pin-Outs & I/O Standards (Part 5 of 16)

LAB	MC	100-Pin TQFP	144-Pin TQFP	IOGND Group for TQFP (200 mA)		IOVCC Group for TQFP		I/O Bank
				100 Pin	144 Pin	100 Pin	144 Pin	
I	129	–	–	–	–	–	–	1
	130	–	–	–	–	–	–	1
	131	–	–	–	–	–	–	1
	132	–	–	–	–	–	–	1
	133	15 *(1)*	20 *(1)*	C	E	B (200 mA)	B (200 mA)	1
	134	–	–	–	–	–	–	1
	135	–	–	–	–	–	–	1
	136	–	–	–	–	–	–	1
	137	–	–	–	–	–	–	1
	138	–	–	–	–	–	–	1
	139	–	–	–	–	–	–	1
	140	–	–	–	–	–	–	1
	141	–	–	–	–	–	–	1
	142	–	–	–	–	–	–	1
	143	–	–	–	–	–	–	1
	144	–	–	–	–	–	–	1
J	145	–	–	–	–	–	–	1
	146	–	–	–	–	–	–	1
	147	–	–	–	–	–	–	1
	148	–	–	–	–	–	–	1
	149	20	26	C	E	C (200 mA)	C (200 mA)	1
	150	–	–	–	–	–	–	1
	151	–	–	–	–	–	–	1
	152	–	–	–	–	–	–	1
	153	19	25	C	E	C (200 mA)	C (200 mA)	1
	154	–	–	–	–	–	–	1
	155	–	23	–	E	B (200 mA)	B (200 mA)	1
	156	–	–	–	–	–	–	1
	157	–	–	–	–	–	–	1
	158	17	22	C	E	B (200 mA)	B (200 mA)	1
	159	–	–	–	–	–	–	1
	160	16	21	C	E	B (200 mA)	B (200 mA)	1

Table 52. EPM7512B I/O Pin-Outs & I/O Standards (Part 6 of 16)

LAB	MC	100-Pin TQFP	144-Pin TQFP	IOGND Group for TQFP (200 mA)		IOVCC Group for TQFP		I/O Bank
				100 Pin	144 Pin	100 Pin	144 Pin	
K	161	22	29	C	E	C (200 mA)	C (200 mA)	1
	162	–	–	–	–	–	–	1
	163	–	–	–	–	–	–	1
	164	–	–	–	–	–	–	1
	165	–	–	–	–	–	–	1
	166	–	–	–	–	–	–	1
	167	–	–	–	–	–	–	1
	168	–	–	–	–	–	–	1
	169	21	28	C	E	C (200 mA)	C (200 mA)	1
	170	–	–	–	–	–	–	1
	171	–	–	–	–	–	–	1
	172	–	–	–	–	–	–	1
	173	–	–	–	–	–	–	1
	174	–	–	–	–	–	–	1
	175	–	–	–	–	–	–	1
	176	–	27	–	E	C (200 mA)	C (200 mA)	1
L	177	–	34	–	F	C (200 mA)	C (200 mA)	1
	178	–	–	–	–	–	–	1
	179	–	–	–	–	–	–	1
	180	–	–	–	–	–	–	1
	181	25	32	C	E	C (200 mA)	C (200 mA)	1
	182	–	–	–	–	–	–	1
	183	–	–	–	–	–	–	1
	184	–	–	–	–	–	–	1
	185	–	–	–	–	–	–	1
	186	–	–	–	–	–	–	1
	187	–	–	–	–	–	–	1
	188	–	–	–	–	–	–	1
	189	–	–	–	–	–	–	1
	190	24	31	C	E	C (200 mA)	C (200 mA)	1
	191	–	–	–	–	–	–	1
	192	23	30	C	E	C (200 mA)	C (200 mA)	1

Table 52. EPM7512B I/O Pin-Outs & I/O Standards (Part 7 of 16)

LAB	MC	100-Pin TQFP	144-Pin TQFP	IOGND Group for TQFP (200 mA)		IOVCC Group for TQFP		I/O Bank
				100 Pin	144 Pin	100 Pin	144 Pin	
M	193	–	–	–	–	–	–	1
	194	–	–	–	–	–	–	1
	195	–	–	–	–	–	–	1
	196	–	–	–	–	–	–	1
	197	–	–	–	–	–	–	1
	198	–	–	–	–	–	–	1
	199	–	–	–	–	–	–	1
	200	–	–	–	–	–	–	1
	201	–	37	–	F	C (200 mA)	C (200 mA)	1
	202	–	–	–	–	–	–	1
	203	–	–	–	–	–	–	1
	204	–	–	–	–	–	–	1
	205	–	–	–	–	–	–	1
	206	27	36	D	F	C (200 mA)	C (200 mA)	1
	207	–	–	–	–	–	–	1
	208	–	35	–	F	C (200 mA)	C (200 mA)	1
N	209	30	42	D	F	C (200 mA)	C (200 mA)	1
	210	–	–	–	–	–	–	1
	211	–	–	–	–	–	–	1
	212	–	–	–	–	–	–	1
	213	29	41	D	F	C (200 mA)	C (200 mA)	1
	214	–	–	–	–	–	–	1
	215	–	–	–	–	–	–	1
	216	–	–	–	–	–	–	1
	217	28	40	D	F	C (200 mA)	C (200 mA)	1
	218	–	–	–	–	–	–	1
	219	–	39	–	F	C (200 mA)	C (200 mA)	1
	220	–	–	–	–	–	–	1
	221	–	–	–	–	–	–	1
	222	–	–	–	–	–	–	1
	223	–	–	–	–	–	–	1
	224	–	38	–	F	C (200 mA)	C (200 mA)	1

Table 52. EPM7512B I/O Pin-Outs & I/O Standards (Part 8 of 16)

LAB	MC	100-Pin TQFP	144-Pin TQFP	IOGND Group for TQFP (200 mA)		IOVCC Group for TQFP		I/O Bank
				100 Pin	144 Pin	100 Pin	144 Pin	
O	225	–	47	–	F	C (200 mA)	C (200 mA)	1
	226	–	–	–	–	–	–	1
	227	33	46	D	F	C (200 mA)	C (200 mA)	1
	228	–	–	–	–	–	–	1
	229	–	45	–	F	C (200 mA)	C (200 mA)	1
	230	–	–	–	–	–	–	1
	231	–	–	–	–	–	–	1
	232	–	–	–	–	–	–	1
	233	–	–	–	–	–	–	1
	234	–	–	–	–	–	–	1
	235	32	44	D	F	C (200 mA)	C (200 mA)	1
	236	–	–	–	–	–	–	1
	237	–	–	–	–	–	–	1
	238	–	–	–	–	–	–	1
	239	–	–	–	–	–	–	1
	240	31	43	D	F	C (200 mA)	C (200 mA)	1
P	241	36	54	D	F	D (58 mA)	D (58 mA)	1
	242	–	–	–	–	–	–	1
	243	–	–	–	–	–	–	1
	244	–	–	–	–	–	–	1
	245	–	–	–	–	–	–	1
	246	–	–	–	–	–	–	1
	247	–	–	–	–	–	–	1
	248	–	–	–	–	–	–	1
	249	35	53	D	F	D (58 mA)	D (58 mA)	1
	250	–	–	–	–	–	–	1
	251	–	–	–	–	–	–	1
	252	–	–	–	–	–	–	1
	253	–	–	–	–	–	–	1
	254	–	49	–	F	C (200 mA)	C (200 mA)	1
	255	–	–	–	–	–	–	1
	256	–	48	–	F	C (200 mA)	C (200 mA)	1

Table 52. EPM7512B I/O Pin-Outs & I/O Standards (Part 9 of 16)

LAB	MC	100-Pin TQFP	144-Pin TQFP	IOGND Group for TQFP (200 mA)		IOVCC Group for TQFP		I/O Bank
				100 Pin	144 Pin	100 Pin	144 Pin	
Q	257	–	55	–	F	D (100 mA)	D (100 mA)	1
	258	–	–	–	–	–	–	1
	259	–	–	–	–	–	–	1
	260	–	–	–	–	–	–	1
	261	–	–	–	–	–	–	1
	262	–	–	–	–	–	–	1
	263	–	–	–	–	–	–	1
	264	–	–	–	–	–	–	1
	265	37	56	D	F	D (100 mA)	D (100 mA)	1
	266	–	–	–	–	–	–	1
	267	–	–	–	–	–	–	2
	268	–	–	–	–	–	–	2
	269	–	–	–	–	–	–	2
	270	40	60	D	G	E (100 mA)	E (100 mA)	2
	271	–	–	–	–	–	–	2
	272	–	61	–	G	E (100 mA)	E (100 mA)	2
R	273	41	62	D	G	E (100 mA)	E (100 mA)	2
	274	–	–	–	–	–	–	2
	275	42	63	D	G	E (100 mA)	E (100 mA)	2
	276	–	–	–	–	–	–	2
	277	–	–	–	–	–	–	2
	278	–	–	–	–	–	–	2
	279	–	–	–	–	–	–	2
	280	–	–	–	–	–	–	2
	281	–	–	–	–	–	–	2
	282	–	–	–	–	–	–	2
	283	44	65	E	H	E (100 mA)	E (100 mA)	2
	284	–	–	–	–	–	–	2
	285	–	–	–	–	–	–	2
	286	–	–	–	–	–	–	2
	287	–	–	–	–	–	–	2
	288	–	–	–	–	–	–	2

Table 52. EPM7512B I/O Pin-Outs & I/O Standards (Part 10 of 16)

LAB	MC	100-Pin TQFP	144-Pin TQFP	IOGND Group for TQFP (200 mA)		IOVCC Group for TQFP		I/O Bank
				100 Pin	144 Pin	100 Pin	144 Pin	
S	289	–	66	–	H	E (100 mA)	E (100 mA)	2
	290	–	–	–	–	–	–	2
	291	–	–	–	–	–	–	2
	292	–	–	–	–	–	–	2
	293	45	67	E	H	E (100 mA)	E (100 mA)	2
	294	–	–	–	–	–	–	2
	295	–	–	–	–	–	–	2
	296	–	–	–	–	–	–	2
	297	–	68	–	H	E (100 mA)	E (100 mA)	2
	298	–	–	–	–	–	–	2
	299	46	69	E	H	E (100 mA)	E (100 mA)	2
	300	–	–	–	–	–	–	2
	301	–	–	–	–	–	–	2
	302	–	–	–	–	–	–	2
	303	–	–	–	–	–	–	2
	304	–	70	–	H	E (100 mA)	E (100 mA)	2
T	305	–	–	–	–	–	–	2
	306	–	–	–	–	–	–	2
	307	–	–	–	–	–	–	2
	308	–	–	–	–	–	–	2
	309	–	–	–	–	–	–	2
	310	–	–	–	–	–	–	2
	311	–	–	–	–	–	–	2
	312	–	–	–	–	–	–	2
	313	47	71	E	H	E (100 mA)	E (100 mA)	2
	314	–	–	–	–	–	–	2
	315	48	72	E	H	E (100 mA)	E (100 mA)	2
	316	–	–	–	–	–	–	2
	317	–	–	–	–	–	–	2
	318	–	–	–	–	–	–	2
	319	–	–	–	–	–	–	2
	320	49	74	E	H	E (200 mA)	F (200 mA)	2

Table 52. EPM7512B I/O Pin-Outs & I/O Standards (Part 11 of 16)

LAB	MC	100-Pin TQFP	144-Pin TQFP	IOGND Group for TQFP (200 mA)		IOVCC Group for TQFP		I/O Bank
				100 Pin	144 Pin	100 Pin	144 Pin	
U	321	50	75	E	H	E (200 mA)	F (200 mA)	2
	322	–	–	–	–	–	–	2
	323	–	–	–	–	–	–	2
	324	–	–	–	–	–	–	2
	325	–	–	–	–	–	–	2
	326	–	–	–	–	–	–	2
	327	–	–	–	–	–	–	2
	328	–	–	–	–	–	–	2
	329	–	–	–	–	–	–	2
	330	–	–	–	–	–	–	2
	331	–	–	–	–	–	–	2
	332	–	–	–	–	–	–	2
	333	–	–	–	–	–	–	2
	334	52	77	E	H	F (200 mA)	G (200 mA)	2
	335	–	–	–	–	–	–	2
	336	53	78	E	H	F (200 mA)	G (200 mA)	2
V	337	54	79	E	H	F (200 mA)	G (200 mA)	2
	338	–	–	–	–	–	–	2
	339	55	80	E	H	F (200 mA)	G (200 mA)	2
	340	–	–	–	–	–	–	2
	341	–	–	–	–	–	–	2
	342	–	–	–	–	–	–	2
	343	–	–	–	–	–	–	2
	344	–	–	–	–	–	–	2
	345	56	81	E	H	F (200 mA)	G (200 mA)	2
	346	–	–	–	–	–	–	2
	347	–	–	–	–	–	–	2
	348	–	–	–	–	–	–	2
	349	–	–	–	–	–	–	2
	350	–	–	–	–	–	–	2
	351	–	–	–	–	–	–	2
	352	–	–	–	–	–	–	2

Table 52. EPM7512B I/O Pin-Outs & I/O Standards (Part 12 of 16)

LAB	MC	100-Pin TQFP	144-Pin TQFP	IOGND Group for TQFP (200 mA)		IOVCC Group for TQFP		I/O Bank
				100 Pin	144 Pin	100 Pin	144 Pin	
W	353	57	82	E	H	F (200 mA)	G (200 mA)	2
	354	–	–	–	–	–	–	2
	355	–	–	–	–	–	–	2
	356	–	–	–	–	–	–	2
	357	–	83	–	H	F (200 mA)	G (200 mA)	2
	358	–	–	–	–	–	–	2
	359	–	–	–	–	–	–	2
	360	–	–	–	–	–	–	2
	361	58	84	E	H	F (200 mA)	G (200 mA)	2
	362	–	–	–	–	–	–	2
	363	–	86	–	I	F (200 mA)	G (200 mA)	2
	364	–	–	–	–	–	–	2
	365	–	–	–	–	–	–	2
	366	60 *(2)*	87 *(2)*	F	I	F (200 mA)	G (200 mA)	2
	367	–	–	–	–	–	–	2
	368	61	88	F	I	F (200 mA)	G (200 mA)	2
X	369	62 *(1)*	89 *(1)*	F	I	F (200 mA)	G (200 mA)	2
	370	–	–	–	–	–	–	2
	371	–	–	–	–	–	–	2
	372	–	–	–	–	–	–	2
	373	–	–	–	–	–	–	2
	374	–	–	–	–	–	–	2
	375	–	–	–	–	–	–	2
	376	–	–	–	–	–	–	2
	377	–	–	–	–	–	–	2
	378	–	–	–	–	–	–	2
	379	–	–	–	–	–	–	2
	380	–	–	–	–	–	–	2
	381	–	–	–	–	–	–	2
	382	–	–	–	–	–	–	2
	383	–	–	–	–	–	–	2
	384	63	90	F	I	F (200 mA)	G (200 mA)	2

Table 52. EPM7512B I/O Pin-Outs & I/O Standards (Part 13 of 16)

LAB	MC	100-Pin TQFP	144-Pin TQFP	IOGND Group for TQFP (200 mA)		IOVCC Group for TQFP		I/O Bank
				100 Pin	144 Pin	100 Pin	144 Pin	
Y	385	–	91	–	I	F (200 mA)	G (200 mA)	2
	386	–	–	–	–	–	–	2
	387	–	–	–	–	–	–	2
	388	–	–	–	–	–	–	2
	389	64	92	F	I	F (200 mA)	G (200 mA)	2
	390	–	–	–	–	–	–	2
	391	–	–	–	–	–	–	2
	392	–	–	–	–	–	–	2
	393	–	–	–	–	–	–	2
	394	–	–	–	–	–	–	2
	395	–	–	–	–	–	–	2
	396	–	–	–	–	–	–	2
	397	–	–	–	–	–	–	2
	398	–	–	–	–	–	–	2
	399	–	–	–	–	–	–	2
	400	65	93	F	I	F (200 mA)	G (200 mA)	2
Z	401	–	–	–	–	–	–	2
	402	–	–	–	–	–	–	2
	403	–	–	–	–	–	–	2
	404	–	–	–	–	–	–	2
	405	–	94	–	I	F (200 mA)	G (200 mA)	2
	406	–	–	–	–	–	–	2
	407	–	–	–	–	–	–	2
	408	–	–	–	–	–	–	2
	409	67	96	F	I	G (200 mA)	H (200 mA)	2
	410	–	–	–	–	–	–	2
	411	–	–	–	–	–	–	2
	412	–	–	–	–	–	–	2
	413	–	–	–	–	–	–	2
	414	68	97	F	I	G (200 mA)	H (200 mA)	2
	415	–	–	–	–	–	–	2
	416	–	–	–	–	–	–	2

Table 52. EPM7512B I/O Pin-Outs & I/O Standards (Part 14 of 16)

LAB	MC	100-Pin TQFP	144-Pin TQFP	IOGND Group for TQFP (200 mA)		IOVCC Group for TQFP		I/O Bank
				100 Pin	144 Pin	100 Pin	144 Pin	
AA	417	–	–	–	–	–	–	2
	418	–	–	–	–	–	–	2
	419	–	–	–	–	–	–	2
	420	–	–	–	–	–	–	2
	421	69	98	F	I	G (200 mA)	H (200 mA)	2
	422	–	–	–	–	–	–	2
	423	–	–	–	–	–	–	2
	424	–	–	–	–	–	–	2
	425	–	–	–	–	–	–	2
	426	–	–	–	–	–	–	2
	427	70	99	F	I	G (200 mA)	H (200 mA)	2
	428	–	–	–	–	–	–	2
	429	–	–	–	–	–	–	2
	430	71	100	F	I	G (200 mA)	H (200 mA)	2
	431	–	–	–	–	–	–	2
	432	–	101	–	I	G (200 mA)	H (200 mA)	2
BB	433	–	–	–	–	–	–	2
	434	–	–	–	–	–	–	2
	435	72	102	F	I	G (200 mA)	H (200 mA)	2
	436	–	–	–	–	–	–	2
	437	–	–	–	–	–	–	2
	438	–	–	–	–	–	–	2
	439	–	–	–	–	–	–	2
	440	–	–	–	–	–	–	2
	441	–	–	–	–	–	–	2
	442	–	–	–	–	–	–	2
	443	–	103	–	I	G (200 mA)	H (200 mA)	2
	444	–	–	–	–	–	–	2
	445	–	–	–	–	–	–	2
	446	73 *(1)*	104 *(1)*	F	I	G (200 mA)	H (200 mA)	2
	447	–	–	–	–	–	–	2
	448	75	106	A	A	G (200 mA)	H (200 mA)	2

Table 52. EPM7512B I/O Pin-Outs & I/O Standards (Part 15 of 16)

LAB	MC	100-Pin TQFP	144-Pin TQFP	IOGND Group for TQFP (200 mA)		IOVCC Group for TQFP		I/O Bank
				100 Pin	144 Pin	100 Pin	144 Pin	
CC	449	–	–	–	–	–	–	2
	450	–	–	–	–	–	–	2
	451	–	–	–	–	–	–	2
	452	–	–	–	–	–	–	2
	453	76	107	A	A	G (200 mA)	H (200 mA)	2
	454	–	–	–	–	–	–	2
	455	–	–	–	–	–	–	2
	456	–	–	–	–	–	–	2
	457	77	108	A	A	G (200 mA)	H (200 mA)	2
	458	–	–	–	–	–	–	2
	459	–	–	–	–	–	–	2
	460	–	–	–	–	–	–	2
	461	–	–	–	–	–	–	2
	462	–	–	–	–	–	–	2
	463	–	–	–	–	–	–	2
	464	78	109	A	A	G (200 mA)	H (200 mA)	2
DD	465	–	–	–	–	–	–	2
	466	–	–	–	–	–	–	2
	467	–	–	–	–	–	–	2
	468	–	–	–	–	–	–	2
	469	79	110	A	A	G (200 mA)	H (200 mA)	2
	470	–	–	–	–	–	–	2
	471	–	–	–	–	–	–	2
	472	–	–	–	–	–	–	2
	473	80	111	A	A	G (200 mA)	H (200 mA)	2
	474	–	–	–	–	–	–	2
	475	–	–	–	–	–	–	2
	476	–	–	–	–	–	–	2
	477	–	–	–	–	–	–	2
	478	–	112	–	A	G (200 mA)	H (200 mA)	2
	479	–	–	–	–	–	–	2
	480	–	–	–	–	–	–	2

Table 52. EPM7512B I/O Pin-Outs & I/O Standards (Part 16 of 16)

LAB	MC	100-Pin TQFP	144-Pin TQFP	IOGND Group for TQFP (200 mA)		IOVCC Group for TQFP		I/O Bank
				100 Pin	144 Pin	100 Pin	144 Pin	
EE	481	–	–	–	–	–	–	2
	482	–	–	–	–	–	–	2
	483	–	–	–	–	–	–	2
	484	–	–	–	–	–	–	2
	485	–	113	–	A	G (200 mA)	H (200 mA)	2
	486	–	–	–	–	–	–	2
	487	–	–	–	–	–	–	2
	488	–	–	–	–	–	–	2
	489	81	114	A	A	G (200 mA)	H (200 mA)	2
	490	–	–	–	–	–	–	2
	491	83	116	A	A	H (100 mA)	I (100 mA)	2
	492	–	–	–	–	–	–	2
	493	–	–	–	–	–	–	2
	494	–	117	–	A	H (100 mA)	I (100 mA)	2
	495	–	–	–	–	–	–	2
	496	–	–	–	–	–	–	2
FF	497	–	118	–	A	H (100 mA)	I (100 mA)	2
	498	–	–	–	–	–	–	2
	499	–	–	–	–	–	–	2
	500	–	–	–	–	–	–	2
	501	–	–	–	–	–	–	2
	502	–	–	–	–	–	–	2
	503	–	–	–	–	–	–	2
	504	–	–	–	–	–	–	2
	505	84	119	A	A	H (100 mA)	I (100 mA)	2
	506	–	–	–	–	–	–	2
	507	–	120	–	A	H (100 mA)	I (100 mA)	2
	508	–	–	–	–	–	–	2
	509	–	–	–	–	–	–	2
	510	–	121	–	A	H (100 mA)	I (100 mA)	2
	511	–	–	–	–	–	–	2
	512	85	122	A	A	H (100 mA)	I (100 mA)	2

Table 53. EPM7512B I/O Pin-Outs & I/O Standards (Part 1 of 16)

LAB	MC	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin Packages (200 mA)		IOVCC Group for 256-Pin Packages	I/O Bank
							BGA	FBGA		
A	1	173	B	A (100 mA)	H3	D7	B	B	B (200 mA)	1
	2	–	–	–	–	–	–	–	–	1
	3	–	–	–	–	–	–	–	–	1
	4	–	–	–	–	–	–	–	–	1
	5	–	–	–	H2	C7	B	B	B (200 mA)	1
	6	–	–	–	–	–	–	–	–	1
	7	–	–	–	–	–	–	–	–	1
	8	–	–	–	–	–	–	–	–	1
	9	175	A	A (100 mA)	H1	B7	A	A	A (100 mA)	1
	10	–	–	–	–	–	–	–	–	1
	11	176 *(1)*	A	A (100 mA)	J4	A7	A	A	A (100 mA)	1
	12	–	–	–	–	–	–	–	–	1
	13	–	–	–	–	–	–	–	–	1
	14	177	A	A (100 mA)	J3	F8	A	A	A (100 mA)	1
	15	–	–	–	–	–	–	–	–	1
	16	178	A	A (100 mA)	J2	B8	A	A	A (100 mA)	1
B	17	169	B	A (100 mA)	G4	D6	C	C	B (200 mA)	1
	18	–	–	–	–	–	–	–	–	1
	19	–	–	–	–	–	–	–	–	1
	20	–	–	–	–	–	–	–	–	1
	21	170	B	A (100 mA)	F1	C6	C	C	B (200 mA)	1
	22	–	–	–	–	–	–	–	–	1
	23	–	–	–	–	–	–	–	–	1
	24	–	–	–	–	–	–	–	–	1
	25	171	B	A (100 mA)	G3	B6	C	C	B (200 mA)	1
	26	–	–	–	–	–	–	–	–	1
	27	172	B	A (100 mA)	G2	A6	C	C	B (200 mA)	1
	28	–	–	–	–	–	–	–	–	1
	29	–	–	–	–	–	–	–	–	1
	30	–	–	–	G1	F7	B	B	B (200 mA)	1
	31	–	–	–	–	–	–	–	–	1
	32	–	–	–	H4	E7	B	B	B (200 mA)	1

Table 53. EPM7512B I/O Pin-Outs & I/O Standards (Part 2 of 16)

LAB	MC	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin Packages (200 mA)		IOVCC Group for 256-Pin Packages	I/O Bank
							BGA	FBGA		
C	33	163	B	B (200 mA)	F4	E4	C	C	C (200 mA)	1
	34	–	–	–	–	–	–	–	–	1
	35	–	–	–	–	–	–	–	–	1
	36	–	–	–	–	–	–	–	–	1
	37	164	B	B (200 mA)	E3	C5	C	C	C (200 mA)	1
	38	–	–	–	–	–	–	–	–	1
	39	–	–	–	–	–	–	–	–	1
	40	–	–	–	–	–	–	–	–	1
	41	166	B	A (100 mA)	E2	A5	C	C	B (200 mA)	1
	42	–	–	–	–	–	–	–	–	1
	43	167	B	A (100 mA)	F3	D5	C	C	B (200 mA)	1
	44	–	–	–	–	–	–	–	–	1
	45	–	–	–	–	–	–	–	–	1
	46	168	B	A (100 mA)	E1	E5	C	C	B (200 mA)	1
	47	–	–	–	–	–	–	–	–	1
	48	–	–	–	F2	E6	C	C	B (200 mA)	1
D	49	–	–	–	B3	B2	D	D	D (200 mA)	1
	50	–	–	–	–	–	–	–	–	1
	51	–	–	–	–	–	–	–	–	1
	52	–	–	–	–	–	–	–	–	1
	53	–	–	–	C2	A2	D	D	D (200 mA)	1
	54	–	–	–	–	–	–	–	–	1
	55	–	–	–	–	–	–	–	–	1
	56	–	–	–	–	–	–	–	–	1
	57	159	B	B (200 mA)	B1	B4	C	C	C (200 mA)	1
	58	–	–	–	–	–	–	–	–	1
	59	160	B	B (200 mA)	C1	A4	C	C	C (200 mA)	1
	60	–	–	–	–	–	–	–	–	1
	61	–	–	–	–	–	–	–	–	1
	62	161	B	B (200 mA)	D2	C4	C	C	C (200 mA)	1
	63	–	–	–	–	–	–	–	–	1
	64	162	B	B (200 mA)	D1	C3	C	C	C (200 mA)	1

Table 53. EPM7512B I/O Pin-Outs & I/O Standards (Part 3 of 16)

LAB	MC	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin Packages (200 mA)		IOVCC Group for 256-Pin Packages	I/O Bank
							BGA	FBGA		
E	65	–	–	–	B5	E3	E	E	D (200 mA)	1
	66	–	–	–	–	–	–	–	–	1
	67	153	C	B (200 mA)	C5	C1	E	E	D (200 mA)	1
	68	–	–	–	–	–	–	–	–	1
	69	–	–	–	D6	B1	E	E	D (200 mA)	1
	70	–	–	–	–	–	–	–	–	1
	71	–	–	–	–	–	–	–	–	1
	72	–	–	–	–	–	–	–	–	1
	73	154	C	B (200 mA)	A4	A1	E	E	D (200 mA)	1
	74	–	–	–	–	–	–	–	–	1
	75	155	C	B (200 mA)	B4	D2	E	E	D (200 mA)	1
	76	–	–	–	–	–	–	–	–	1
	77	–	–	–	–	–	–	–	–	1
	78	156	C	B (200 mA)	A3	D3	E	E	D (200 mA)	1
	79	–	–	–	–	–	–	–	–	1
	80	157	C	B (200 mA)	A2 *(1)*	D4 *(1)*	E	E	D (200 mA)	1
F	81	147	D	B (200 mA)	B7	F2	F	F	D (200 mA)	1
	82	–	–	–	–	–	–	–	–	1
	83	148	D	B (200 mA)	C7	F3	F	F	D (200 mA)	1
	84	–	–	–	–	–	–	–	–	1
	85	149	D	B (200 mA)	A6	F1	F	F	D (200 mA)	1
	86	–	–	–	–	–	–	–	–	1
	87	–	–	–	–	–	–	–	–	1
	88	–	–	–	–	–	–	–	–	1
	89	–	–	–	D7	F4	F	F	D (200 mA)	1
	90	–	–	–	–	–	–	–	–	1
	91	150	D	B (200 mA)	B6	E1	F	F	D (200 mA)	1
	92	–	–	–	–	–	–	–	–	1
	93	–	–	–	–	–	–	–	–	1
	94	151	D	B (200 mA)	A5	D1	F	F	D (200 mA)	1
	95	–	–	–	–	–	–	–	–	1
	96	–	–	–	C6	E2	E	E	D (200 mA)	1

Table 53. EPM7512B I/O Pin-Outs & I/O Standards (Part 4 of 16)

LAB	MC	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin Packages (200 mA)		IOVCC Group for 256-Pin Packages	I/O Bank
							BGA	FBGA		
G	97	–	–	–	C9	H6	G	G	E (200 mA)	1
	98	–	–	–	–	–	–	–	–	1
	99	141	D	C (200 mA)	D9	G5	G	G	E (200 mA)	1
	100	–	–	–	–	–	–	–	–	1
	101	142	D	C (200 mA)	A8	G4	G	G	E (200 mA)	1
	102	–	–	–	–	–	–	–	–	1
	103	–	–	–	–	–	–	–	–	1
	104	–	–	–	–	–	–	–	–	1
	105	144	D	B (200 mA)	B8	G2	F	F	D (200 mA)	1
	106	–	–	–	–	–	–	–	–	1
	107	145	D	B (200 mA)	C8	G1	F	F	D (200 mA)	1
	108	–	–	–	–	–	–	–	–	1
	109	–	–	–	–	–	–	–	–	1
	110	146	D	B (200 mA)	D8	G6	F	F	D (200 mA)	1
	111	–	–	–	–	–	–	–	–	1
	112	–	–	–	A7	F5	F	F	D (200 mA)	1
H	113	135	D	C (200 mA)	A11	J1	H	H	E (200 mA)	1
	114	–	–	–	–	–	–	–	–	1
	115	136	D	C (200 mA)	A10	H7	H	H	E (200 mA)	1
	116	–	–	–	–	–	–	–	–	1
	117	137	D	C (200 mA)	B10	H5	H	H	E (200 mA)	1
	118	–	–	–	–	–	–	–	–	1
	119	–	–	–	–	–	–	–	–	1
	120	–	–	–	–	–	–	–	–	1
	121	–	–	–	D10	H2	H	H	E (200 mA)	1
	122	–	–	–	–	–	–	–	–	1
	123	138	D	C (200 mA)	C10	H3	G	G	E (200 mA)	1
	124	–	–	–	–	–	–	–	–	1
	125	–	–	–	–	–	–	–	–	1
	126	139	D	C (200 mA)	A9	H1	G	G	E (200 mA)	1
	127	–	–	–	–	–	–	–	–	1
	128	140	D	C (200 mA)	B9	H4	G	G	E (200 mA)	1

Table 53. EPM7512B I/O Pin-Outs & I/O Standards (Part 5 of 16)

LAB	MC	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin Packages (200 mA)		IOVCC Group for 256-Pin Packages	I/O Bank
							BGA	FBGA		
I	129	–	–	–	D12	K1	I	I	E (200 mA)	1
	130	–	–	–	–	–	–	–	–	1
	131	129	E	C (200 mA)	C12 *(2)*	J7	I	I	E (200 mA)	1
	132	–	–	–	–	–	–	–	–	1
	133	130 *(1)*	E	C (200 mA)	B12 *(1)*	J6 *(1)*	I	I	E (200 mA)	1
	134	–	–	–	–	–	–	–	–	1
	135	–	–	–	–	–	–	–	–	1
	136	–	–	–	–	–	–	–	–	1
	137	131	E	C (200 mA)	A12	J5	I	I	E (200 mA)	1
	138	–	–	–	–	–	–	–	–	1
	139	–	–	–	D11	J4 *(2)*	I	I	E (200 mA)	1
	140	–	–	–	–	–	–	–	–	1
	141	–	–	–	–	–	–	–	–	1
	142	132	E	C (200 mA)	C11	J3	I	I	E (200 mA)	1
	143	–	–	–	–	–	–	–	–	1
	144	133	E	C (200 mA)	B11	J2	I	I	E (200 mA)	1
J	145	122	E	D (200 mA)	C14	L2	I	I	F (200 mA)	1
	146	–	–	–	–	–	–	–	–	1
	147	–	–	–	B14	L1	I	I	F (200 mA)	1
	148	–	–	–	–	–	–	–	–	1
	149	123	E	D (200 mA)	A14	K6	I	I	F (200 mA)	1
	150	–	–	–	–	–	–	–	–	1
	151	–	–	–	–	–	–	–	–	1
	152	–	–	–	–	–	–	–	–	1
	153	124	E	D (200 mA)	D13	K5	I	I	F (200 mA)	1
	154	–	–	–	–	–	–	–	–	1
	155	126	E	C (200 mA)	C13	K4	I	I	E (200 mA)	1
	156	–	–	–	–	–	–	–	–	1
	157	–	–	–	–	–	–	–	–	1
	158	127 *(1)*	E	C (200 mA)	B13	K3	I	I	E (200 mA)	1
	159	–	–	–	–	–	–	–	–	1
	160	128 *(2)*	E	C (200 mA)	A13	K2	I	I	E (200 mA)	1

Table 53. EPM7512B I/O Pin-Outs & I/O Standards (Part 6 of 16)

LAB	MC	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin Packages (200 mA)		IOVCC Group for 256-Pin Packages	I/O Bank
							BGA	FBGA		
K	161	115	F	D (200 mA)	B16	N4	J	J	F (200 mA)	1
	162	–	–	–	–	–	–	–	–	1
	163	117	E	D (200 mA)	C15	M2	I	I	F (200 mA)	1
	164	–	–	–	–	–	–	–	–	1
	165	118	E	D (200 mA)	A17	M1	I	I	F (200 mA)	1
	166	–	–	–	–	–	–	–	–	1
	167	–	–	–	–	–	–	–	–	1
	168	–	–	–	–	–	–	–	–	1
	169	119	E	D (200 mA)	B15	M4	I	I	F (200 mA)	1
	170	–	–	–	–	–	–	–	–	1
	171	–	–	–	D14	M5	I	I	F (200 mA)	1
	172	–	–	–	–	–	–	–	–	1
	173	–	–	–	–	–	–	–	–	1
	174	120	E	D (200 mA)	A16	L5	I	I	F (200 mA)	1
	175	–	–	–	–	–	–	–	–	1
	176	121	E	D (200 mA)	A15	L4	I	I	F (200 mA)	1
L	177	109	F	D (200 mA)	A20	R1	J	K	F (200 mA)	1
	178	–	–	–	–	–	–	–	–	1
	179	–	–	–	–	–	–	–	–	1
	180	–	–	–	–	–	–	–	–	1
	181	110	F	D (200 mA)	A19	P2	J	J	F (200 mA)	1
	182	–	–	–	–	–	–	–	–	1
	183	–	–	–	–	–	–	–	–	1
	184	–	–	–	–	–	–	–	–	1
	185	111	F	D (200 mA)	B17	N3	J	J	F (200 mA)	1
	186	–	–	–	–	–	–	–	–	1
	187	112	F	D (200 mA)	A18	N2	J	J	F (200 mA)	1
	188	–	–	–	–	–	–	–	–	1
	189	–	–	–	–	–	–	–	–	1
	190	113	F	D (200 mA)	D15	P1	J	J	F (200 mA)	1
	191	–	–	–	–	–	–	–	–	1
	192	114	F	D (200 mA)	C16	N1	J	J	F (200 mA)	1

Table 53. EPM7512B I/O Pin-Outs & I/O Standards (Part 7 of 16)

LAB	MC	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin Packages (200 mA)		IOVCC Group for 256-Pin Packages	I/O Bank
							BGA	FBGA		
M	193	101	F	F (200 mA)	E18	P5	K	J	H (200 mA)	1
	194	–	–	–	–	–	–	–	–	1
	195	–	–	–	–	–	–	–	–	1
	196	–	–	–	–	–	–	–	–	1
	197	102	F	F (200 mA)	D20	N5	K	J	H (200 mA)	1
	198	–	–	–	–	–	–	–	–	1
	199	–	–	–	–	–	–	–	–	1
	200	–	–	–	–	–	–	–	–	1
	201	103	F	F (200 mA)	D19	T4	K	J	H (200 mA)	1
	202	–	–	–	–	–	–	–	–	1
	203	104	F	F (200 mA)	C20	R4	K	J	H (200 mA)	1
	204	–	–	–	–	–	–	–	–	1
	205	–	–	–	–	–	–	–	–	1
	206	106	F	E (200 mA)	C19	P4	K	J	G (200 mA)	1
	207	–	–	–	–	–	–	–	–	1
	208	108	F	D (200 mA)	B18	P3	K	J	F (200 mA)	1
N	209	95	F	F (200 mA)	G17	R6	K	J	I (200 mA)	1
	210	–	–	–	–	–	–	–	–	1
	211	–	–	–	–	–	–	–	–	1
	212	–	–	–	–	–	–	–	–	1
	213	96	F	F (200 mA)	F19	T6	K	J	I (200 mA)	1
	214	–	–	–	–	–	–	–	–	1
	215	–	–	–	–	–	–	–	–	1
	216	–	–	–	–	–	–	–	–	1
	217	97	F	F (200 mA)	E20	N6	K	J	I (200 mA)	1
	218	–	–	–	–	–	–	–	–	1
	219	98	F	F (200 mA)	F18	M6	K	J	I (200 mA)	1
	220	–	–	–	–	–	–	–	–	1
	221	–	–	–	–	–	–	–	–	1
	222	99	F	F (200 mA)	E19	R5	K	J	I (200 mA)	1
	223	–	–	–	–	–	–	–	–	1
	224	100	F	F (200 mA)	F17	T5	K	J	H (200 mA)	1

Table 53. EPM7512B I/O Pin-Outs & I/O Standards (Part 8 of 16)

LAB	MC	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin Packages (200 mA)		IOVCC Group for 256-Pin Packages	I/O Bank
							BGA	FBGA		
O	225	88	G	F (200 mA)	H19	R7	L	K	I (200 mA)	1
	226	–	–	–	–	–	–	–	–	1
	227	89	G	F (200 mA)	H18	P7	L	K	I (200 mA)	1
	228	–	–	–	–	–	–	–	–	1
	229	90	G	F (200 mA)	H17	T7	L	K	I (200 mA)	1
	230	–	–	–	–	–	–	–	–	1
	231	–	–	–	–	–	–	–	–	1
	232	–	–	–	–	–	–	–	–	1
	233	91	G	F (200 mA)	G20	L8	L	K	I (200 mA)	1
	234	–	–	–	–	–	–	–	–	1
	235	92	G	F (200 mA)	G19	N7	L	K	I (200 mA)	1
	236	–	–	–	–	–	–	–	–	1
	237	–	–	–	–	–	–	–	–	1
	238	–	–	–	G18	M7	L	K	I (200 mA)	1
	239	–	–	–	–	–	–	–	–	1
	240	93	G	F (200 mA)	F20	L7	L	K	I (200 mA)	1
P	241	79	G	G (200 mA)	K20	M9	L	K	J (200 mA)	1
	242	–	–	–	–	–	–	–	–	1
	243	–	–	–	–	–	–	–	–	1
	244	–	–	–	–	–	–	–	–	1
	245	80	G	G (200 mA)	K19	L9	L	K	J (200 mA)	1
	246	–	–	–	–	–	–	–	–	1
	247	–	–	–	–	–	–	–	–	1
	248	–	–	–	–	–	–	–	–	1
	249	81	G	G (200 mA)	K17	R8	L	K	J (200 mA)	1
	250	–	–	–	–	–	–	–	–	1
	251	84	G	G (200 mA)	J18	T8	L	K	J (200 mA)	1
	252	–	–	–	–	–	–	–	–	1
	253	–	–	–	–	–	–	–	–	1
	254	86	G	F (200 mA)	J17	N8	L	K	I (200 mA)	1
	255	–	–	–	–	–	–	–	–	1
	256	87	G	F (200 mA)	H20	M8	L	K	I (200 mA)	1

Table 53. EPM7512B I/O Pin-Outs & I/O Standards (Part 9 of 16)

LAB	MC	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin Packages (200 mA)		IOVCC Group for 256-Pin Packages	I/O Bank
							BGA	FBGA		
Q	257	78	G	G (100 mA)	L20	N9	L	K	J (100 mA)	1
	258	–	–	–	–	–	–	–	–	1
	259	–	–	–	–	–	–	–	–	1
	260	–	–	–	–	–	–	–	–	1
	261	77	G	G (100 mA)	L19	T9	L	K	J (100 mA)	1
	262	–	–	–	–	–	–	–	–	1
	263	–	–	–	–	–	–	–	–	1
	264	–	–	–	–	–	–	–	–	1
	265	76	G	G (100 mA)	L18	R9	L	K	J (100 mA)	1
	266	–	–	–	–	–	–	–	–	1
	267	73	G	H (100 mA)	M18	L10	L	K	K (100 mA)	2
	268	–	–	–	–	–	–	–	–	2
	269	–	–	–	–	–	–	–	–	2
	270	71	H	H (100 mA)	M17	M10	M	L	K (100 mA)	2
	271	–	–	–	–	–	–	–	–	2
	272	70	H	H (100 mA)	N20	N10	M	L	K (100 mA)	2
R	273	69	H	H (100 mA)	N19	R10	M	L	K (100 mA)	2
	274	–	–	–	–	–	–	–	–	2
	275	68	H	H (100 mA)	N18	T10	M	L	K (100 mA)	2
	276	–	–	–	–	–	–	–	–	2
	277	67	H	H (100 mA)	N17	M11	N	M	K (100 mA)	2
	278	–	–	–	–	–	–	–	–	2
	279	–	–	–	–	–	–	–	–	2
	280	–	–	–	–	–	–	–	–	2
	281	66	H	H (100 mA)	P20	N11	N	M	K (100 mA)	2
	282	–	–	–	–	–	–	–	–	2
	283	65	H	H (100 mA)	P19	P11	N	M	K (100 mA)	2
	284	–	–	–	–	–	–	–	–	2
	285	–	–	–	–	–	–	–	–	2
	286	–	–	–	P18	R11	N	M	K (100 mA)	2
	287	–	–	–	–	–	–	–	–	2
	288	64	H	H (100 mA)	R20	T11	N	M	K (100 mA)	2

Table 53. EPM7512B I/O Pin-Outs & I/O Standards (Part 10 of 16)

LAB	MC	208-Pin PQFP (4)	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin Packages (200 mA)		IOVCC Group for 256-Pin Packages	I/O Bank
							BGA	FBGA		
S	289	62	H	I (200 mA)	P17	K11	N	M	L (200 mA)	2
	290	–	–	–	–	–	–	–	–	2
	291	–	–	–	–	–	–	–	–	2
	292	–	–	–	–	–	–	–	–	2
	293	61	H	I (200 mA)	R19	M12	N	M	L (200 mA)	2
	294	–	–	–	–	–	–	–	–	2
	295	–	–	–	–	–	–	–	–	2
	296	–	–	–	–	–	–	–	–	2
	297	60	H	I (200 mA)	T20	N12	N	M	L (200 mA)	2
	298	–	–	–	–	–	–	–	–	2
	299	59	H	I (200 mA)	R18	T12	N	M	L (200 mA)	2
	300	–	–	–	–	–	–	–	–	2
	301	–	–	–	–	–	–	–	–	2
	302	58	H	I (200 mA)	T19	R12	N	M	L (200 mA)	2
	303	–	–	–	–	–	–	–	–	2
	304	57	H	I (200 mA)	T18	T13	N	M	L (200 mA)	2
T	305	56	H	I (200 mA)	R17	P12	N	M	L (200 mA)	2
	306	–	–	–	–	–	–	–	–	2
	307	–	–	–	–	–	–	–	–	2
	308	–	–	–	–	–	–	–	–	2
	309	55	H	I (200 mA)	U20	T14	N	M	L (200 mA)	2
	310	–	–	–	–	–	–	–	–	2
	311	–	–	–	–	–	–	–	–	2
	312	–	–	–	–	–	–	–	–	2
	313	54	H	I (200 mA)	U19	P13	N	M	L (200 mA)	2
	314	–	–	–	–	–	–	–	–	2
	315	53	H	I (200 mA)	V20	R13	N	M	L (200 mA)	2
	316	–	–	–	–	–	–	–	–	2
	317	–	–	–	–	–	–	–	–	2
	318	52	H	I (200 mA)	W20	R14	N	M	M (200 mA)	2
	319	–	–	–	–	–	–	–	–	2
	320	49	I	I (200 mA)	W18	R15	O	N	M (200 mA)	2

Table 53. EPM7512B I/O Pin-Outs & I/O Standards (Part 11 of 16)

LAB	MC	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin Packages (200 mA)		IOVCC Group for 256-Pin Packages	I/O Bank
							BGA	FBGA		
U	321	48	I	I (200 mA)	Y19	P15	O	N	M (200 mA)	2
	322	–	–	–	–	–	–	–	–	2
	323	–	–	–	–	–	–	–	–	2
	324	–	–	–	–	–	–	–	–	2
	325	47	I	I (200 mA)	Y18	N15	O	N	N (200 mA)	2
	326	–	–	–	–	–	–	–	–	2
	327	–	–	–	–	–	–	–	–	2
	328	–	–	–	–	–	–	–	–	2
	329	46	I	I (200 mA)	W17	T16	O	N	N (200 mA)	2
	330	–	–	–	–	–	–	–	–	2
	331	45	I	I (200 mA)	Y17	R16	O	N	N (200 mA)	2
	332	–	–	–	–	–	–	–	–	2
	333	–	–	–	–	–	–	–	–	2
	334	44	I	I (200 mA)	U15	P16	O	N	N (200 mA)	2
	335	–	–	–	–	–	–	–	–	2
	336	43	I	I (200 mA)	V16	N14	O	N	N (200 mA)	2
V	337	42	I	I (200 mA)	W16	N16	O	N	N (200 mA)	2
	338	–	–	–	–	–	–	–	–	2
	339	40	I	J (200 mA)	V15	M14	O	N	O (200 mA)	2
	340	–	–	–	–	–	–	–	–	2
	341	39	I	J (200 mA)	Y16	N13	O	N	O (200 mA)	2
	342	–	–	–	–	–	–	–	–	2
	343	–	–	–	–	–	–	–	–	2
	344	–	–	–	–	–	–	–	–	2
	345	38	I	J (200 mA)	W15	M16	O	N	O (200 mA)	2
	346	–	–	–	–	–	–	–	–	2
	347	–	–	–	U14	M13	O	N	O (200 mA)	2
	348	–	–	–	–	–	–	–	–	2
	349	–	–	–	–	–	–	–	–	2
	350	37	I	J (200 mA)	Y15	L14	O	N	O (200 mA)	2
	351	–	–	–	–	–	–	–	–	2
	352	36	I	J (200 mA)	V14	L15	O	N	O (200 mA)	2

Table 53. EPM7512B I/O Pin-Outs & I/O Standards (Part 12 of 16)

LAB	MC	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin Packages (200 mA)		IOVCC Group for 256-Pin Packages	I/O Bank
							BGA	FBGA		
W	353	35	I	J (200 mA)	W14	L16	O	N	O (200 mA)	2
	354	–	–	–	–	–	–	–	–	2
	355	–	–	–	Y14	L13	O	N	O (200 mA)	2
	356	–	–	–	–	–	–	–	–	2
	357	34	I	J (200 mA)	U13	L12	O	N	O (200 mA)	2
	358	–	–	–	–	–	–	–	–	2
	359	–	–	–	–	–	–	–	–	2
	360	–	–	–	–	–	–	–	–	2
	361	33	I	J (200 mA)	V13	K12	O	N	O (200 mA)	2
	362	–	–	–	–	–	–	–	–	2
	363	31	J	J (200 mA)	W13	K14	P	O	O (200 mA)	2
	364	–	–	–	–	–	–	–	–	2
	365	–	–	–	–	–	–	–	–	2
	366	30 *(1)*	J	J (200 mA)	Y13	K15	P	O	O (200 mA)	2
	367	–	–	–	–	–	–	–	–	2
	368	29	J	J (200 mA)	U12	K16	P	O	O (200 mA)	2
X	369	–	–	–	V12 *(1)*	J11 *(1)*	P	O	O (200 mA)	2
	370	–	–	–	–	–	–	–	–	2
	371	28	J	J (200 mA)	W12	J12	P	O	O (200 mA)	2
	372	–	–	–	–	–	–	–	–	2
	373	27	J	J (200 mA)	Y12	J13	P	O	O (200 mA)	2
	374	–	–	–	–	–	–	–	–	2
	375	–	–	–	–	–	–	–	–	2
	376	–	–	–	–	–	–	–	–	2
	377	26	J	J (200 mA)	V11	J14	P	O	O (200 mA)	2
	378	–	–	–	–	–	–	–	–	2
	379	–	–	–	U11	J15	P	O	O (200 mA)	2
	380	–	–	–	–	–	–	–	–	2
	381	–	–	–	–	–	–	–	–	2
	382	25	J	J (200 mA)	W11	K13	P	O	O (200 mA)	2
	383	–	–	–	–	–	–	–	–	2
	384	24	J	J (200 mA)	Y11	J16	P	O	O (200 mA)	2

Table 53. EPM7512B I/O Pin-Outs & I/O Standards (Part 13 of 16)

LAB	MC	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin Packages (200 mA)		IOVCC Group for 256-Pin Packages	I/O Bank
							BGA	FBGA		
Y	385	22 *(2)*	J	K (200 mA)	Y10	H10	P	O	P (200 mA)	2
	386	–	–	–	–	–	–	–	–	2
	387	21	J	K (200 mA)	W10	H11 *(2)*	P	O	P (200 mA)	2
	388	–	–	–	–	–	–	–	–	2
	389	20	J	K (200 mA)	V10 *(2)*	H12	P	O	P (200 mA)	2
	390	–	–	–	–	–	–	–	–	2
	391	–	–	–	–	–	–	–	–	2
	392	–	–	–	–	–	–	–	–	2
	393	–	–	–	U10	H15	P	O	P (200 mA)	2
	394	–	–	–	–	–	–	–	–	2
	395	19	J	K (200 mA)	Y9	H16	P	O	P (200 mA)	2
	396	–	–	–	–	–	–	–	–	2
	397	–	–	–	–	–	–	–	–	2
	398	18	J	K (200 mA)	W9	H14	P	O	P (200 mA)	2
	399	–	–	–	–	–	–	–	–	2
	400	17	J	K (200 mA)	V9	H13	P	O	P (200 mA)	2
Z	401	–	–	–	U9	G12	P	O	P (200 mA)	2
	402	–	–	–	–	–	–	–	–	2
	403	16	J	K (200 mA)	Y8	G13	P	O	P (200 mA)	2
	404	–	–	–	–	–	–	–	–	2
	405	15	J	K (200 mA)	W8	G14	P	O	P (200 mA)	2
	406	–	–	–	–	–	–	–	–	2
	407	–	–	–	–	–	–	–	–	2
	408	–	–	–	–	–	–	–	–	2
	409	13	K	K (200 mA)	V8	G16	Q	P	Q (200 mA)	2
	410	–	–	–	–	–	–	–	–	2
	411	12	K	K (200 mA)	U8	G11	Q	P	Q (200 mA)	2
	412	–	–	–	–	–	–	–	–	2
	413	–	–	–	–	–	–	–	–	2
	414	11	K	K (200 mA)	Y7	F12	Q	P	Q (200 mA)	2
	415	–	–	–	–	–	–	–	–	2
	416	–	–	–	W7	F13	Q	P	Q (200 mA)	2

Table 53. EPM7512B I/O Pin-Outs & I/O Standards (Part 14 of 16)

LAB	MC	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin Packages (200 mA)		IOVCC Group for 256-Pin Packages	I/O Bank
							BGA	FBGA		
AA	417	10	K	K (200 mA)	V7	F14	Q	P	Q (200 mA)	2
	418	–	–	–	–	–	–	–	–	2
	419	9	K	K (200 mA)	Y6	F15	Q	P	Q (200 mA)	2
	420	–	–	–	–	–	–	–	–	2
	421	8	K	K (200 mA)	U7	F16	Q	P	Q (200 mA)	2
	422	–	–	–	–	–	–	–	–	2
	423	–	–	–	–	–	–	–	–	2
	424	–	–	–	–	–	–	–	–	2
	425	–	–	–	W6	E12	Q	P	Q (200 mA)	2
	426	–	–	–	–	–	–	–	–	2
	427	7	K	K (200 mA)	Y5	E13	Q	P	Q (200 mA)	2
	428	–	–	–	–	–	–	–	–	2
	429	–	–	–	–	–	–	–	–	2
	430	6	K	K (200 mA)	V6	E14	Q	P	Q (200 mA)	2
	431	–	–	–	–	–	–	–	–	2
	432	–	–	–	W5	E16	Q	P	R (200 mA)	2
BB	433	–	–	–	V5	D16	Q	P	R (200 mA)	2
	434	–	–	–	–	–	–	–	–	2
	435	4	K	L (200 mA)	U6	C16	Q	P	R (200 mA)	2
	436	–	–	–	–	–	–	–	–	2
	437	–	–	–	Y4	B16	Q	P	R (200 mA)	2
	438	–	–	–	–	–	–	–	–	2
	439	–	–	–	–	–	–	–	–	2
	440	–	–	–	–	–	–	–	–	2
	441	3	K	L (200 mA)	W4	A16	Q	P	R (200 mA)	2
	442	–	–	–	–	–	–	–	–	2
	443	2	K	L (200 mA)	Y3	D15	Q	P	R (200 mA)	2
	444	–	–	–	–	–	–	–	–	2
	445	–	–	–	–	–	–	–	–	2
	446	1	K	L (200 mA)	Y2 *(1)*	D13 *(1)*	Q	P	R (200 mA)	2
	447	–	–	–	–	–	–	–	–	2
	448	208	K	L (200 mA)	W3	C15	R	Q	R (200 mA)	2

Table 53. EPM7512B I/O Pin-Outs & I/O Standards (Part 15 of 16)

LAB	MC	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin Packages (200 mA)		IOVCC Group for 256-Pin Packages	I/O Bank
							BGA	FBGA		
CC	449	–	–	–	W1	B15	R	Q	S (200 mA)	2
	450	–	–	–	–	–	–	–	–	2
	451	–	–	–	–	–	–	–	–	2
	452	–	–	–	–	–	–	–	–	2
	453	–	–	–	V1	A15	R	Q	S (200 mA)	2
	454	–	–	–	–	–	–	–	–	2
	455	–	–	–	–	–	–	–	–	2
	456	–	–	–	–	–	–	–	–	2
	457	206	K	M (200 mA)	U2	B14	R	Q	S (200 mA)	2
	458	–	–	–	–	–	–	–	–	2
	459	205	K	M (200 mA)	U1	A14	R	Q	S (200 mA)	2
	460	–	–	–	–	–	–	–	–	2
	461	–	–	–	–	–	–	–	–	2
	462	204	K	M (200 mA)	T3	B13	R	Q	S (200 mA)	2
	463	–	–	–	–	–	–	–	–	2
	464	203	K	M (200 mA)	R4	A13	R	Q	S (200 mA)	2
DD	465	202	K	M (200 mA)	T2	C13	R	Q	S (200 mA)	2
	466	–	–	–	–	–	–	–	–	2
	467	–	–	–	–	–	–	–	–	2
	468	–	–	–	–	–	–	–	–	2
	469	201	K	M (200 mA)	R3	D12	R	Q	S (200 mA)	2
	470	–	–	–	–	–	–	–	–	2
	471	–	–	–	–	–	–	–	–	2
	472	–	–	–	–	–	–	–	–	2
	473	199	A	M (200 mA)	T1	C12	S	R	S (200 mA)	2
	474	–	–	–	–	–	–	–	–	2
	475	198	A	M (200 mA)	R2	B12	S	R	S (200 mA)	2
	476	–	–	–	–	–	–	–	–	2
	477	–	–	–	–	–	–	–	–	2
	478	197	A	M (200 mA)	P4	A12	S	R	S (200 mA)	2
	479	–	–	–	–	–	–	–	–	2
	480	–	–	–	R1	E11	S	R	S (200 mA)	2

Table 53. EPM7512B I/O Pin-Outs & I/O Standards (Part 16 of 16)

LAB	MC	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin Packages (200 mA)		IOVCC Group for 256-Pin Packages	I/O Bank
							BGA	FBGA		
EE	481	196	A	M (200 mA)	P3	D11	S	R	S (200 mA)	2
	482	–	–	–	–	–	–	–	–	2
	483	–	–	–	–	–	–	–	–	2
	484	–	–	–	–	–	–	–	–	2
	485	195	A	M (200 mA)	P2	C11	S	R	S (200 mA)	2
	486	–	–	–	–	–	–	–	–	2
	487	–	–	–	–	–	–	–	–	2
	488	–	–	–	–	–	–	–	–	2
	489	194	A	M (200 mA)	P1	A11	S	R	S (200 mA)	2
	490	–	–	–	–	–	–	–	–	2
	491	193	A	M (200 mA)	N4	B11	S	R	T (200 mA)	2
	492	–	–	–	–	–	–	–	–	2
	493	–	–	–	–	–	–	–	–	2
	494	–	–	–	N3	F10	S	R	T (200 mA)	2
	495	–	–	–	–	–	–	–	–	2
	496	–	–	–	N2	E10	S	R	T (200 mA)	2
FF	497	192	A	M (200 mA)	N1	D10	S	R	T (200 mA)	2
	498	–	–	–	–	–	–	–	–	2
	499	–	–	–	–	–	–	–	–	2
	500	–	–	–	–	–	–	–	–	2
	501	–	–	–	M4	C10	S	R	T (200 mA)	2
	502	–	–	–	–	–	–	–	–	2
	503	–	–	–	–	–	–	–	–	2
	504	–	–	–	–	–	–	–	–	2
	505	190	A	N (100 mA)	M3	A10	A	A	U (100 mA)	2
	506	–	–	–	–	–	–	–	–	2
	507	189 *(1)*	A	N (100 mA)	M2	J10	A	A	U (100 mA)	2
	508	–	–	–	–	–	–	–	–	2
	509	–	–	–	–	–	–	–	–	2
	510	188	A	N (100 mA)	M1	F9	A	A	U (100 mA)	2
	511	–	–	–	–	–	–	–	–	2
	512	187	A	N (100 mA)	L3	A9	A	A	U (100 mA)	2

Notes to tables:

(1) The EPM7512B device in the 208-pin PQFP package supports vertical migration from the EPM7256E, EPM7256S, and EPM7256B devices. The EPM7512B device contains additional I/O pins which are no connects on the EPM7256E, EPM7256S, and EPM7256B devices. To support these additional I/O pins, the EPM7512B device has two additional `VCCIO` (pins 105 and 207) and `GNDIO` (pins 51 and 158) pins that are no-connect pins on the EPM7256E, EPM7256S, and EPM7256B devices. To achieve vertical migration between the EPM7256B and EPM7512B devices, the no-connect pins 105 and 207 may be tied to `VCCIO`, and pins 51 and 158 may be tied to `GNDIO` on the EPM7256B devices. On the EPM7256E and EPM7256S devices, these no-connect pins must not be tied to `VCCIO` or `GNDIO`. EPM7512B devices have identical pin-outs.

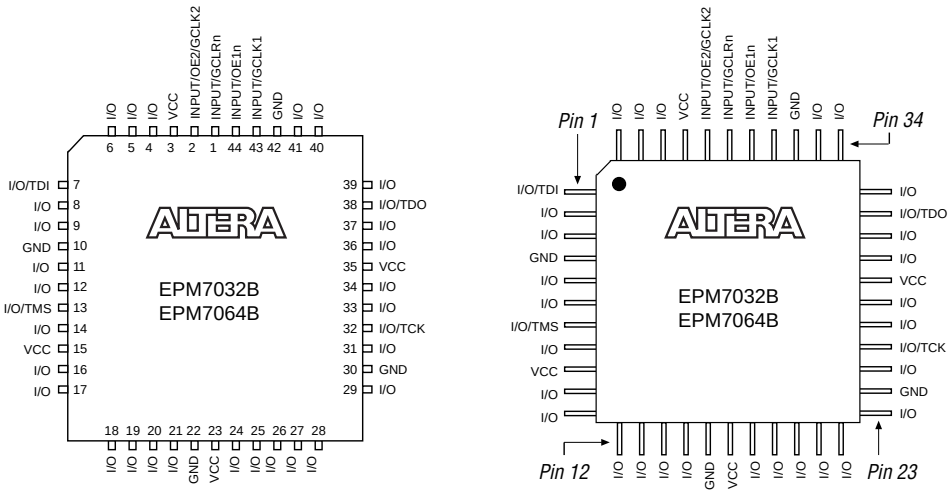
(2) This pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for in-system programming, this pin is not available as a user I/O pin.

(3) The user I/O pin count includes dedicated input pins and all I/O pins.

Figures 20 through 27 show the package pin-out diagrams for MAX 7000B devices.

Figure 20. 44-Pin PLCC/TQFP Package Pin-Out Diagram

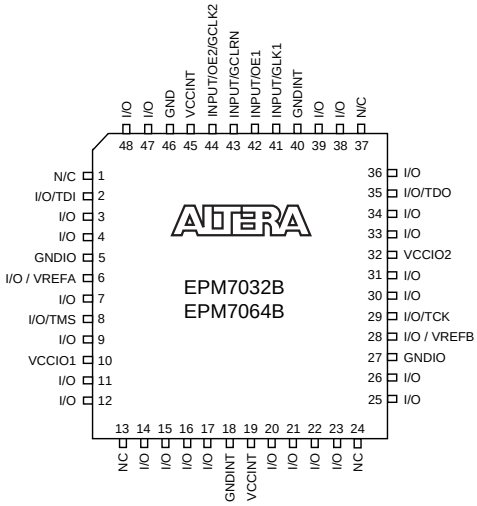
Package outlines not drawn to scale.



44-Pin PLCC 44-Pin TQFP

Figure 21. 48-Pin VTQFP Package Pin-Out Diagram

Package outlines not drawn to scale.



48-Pin VTQFP

Figure 22. 100-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

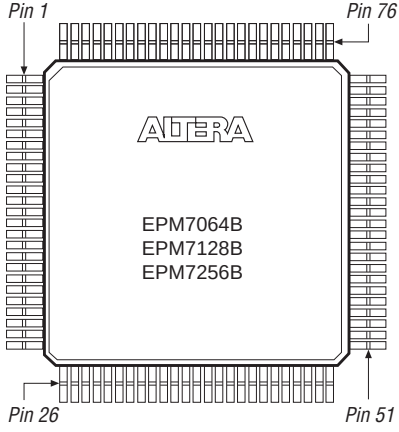


Figure 23. 100-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.

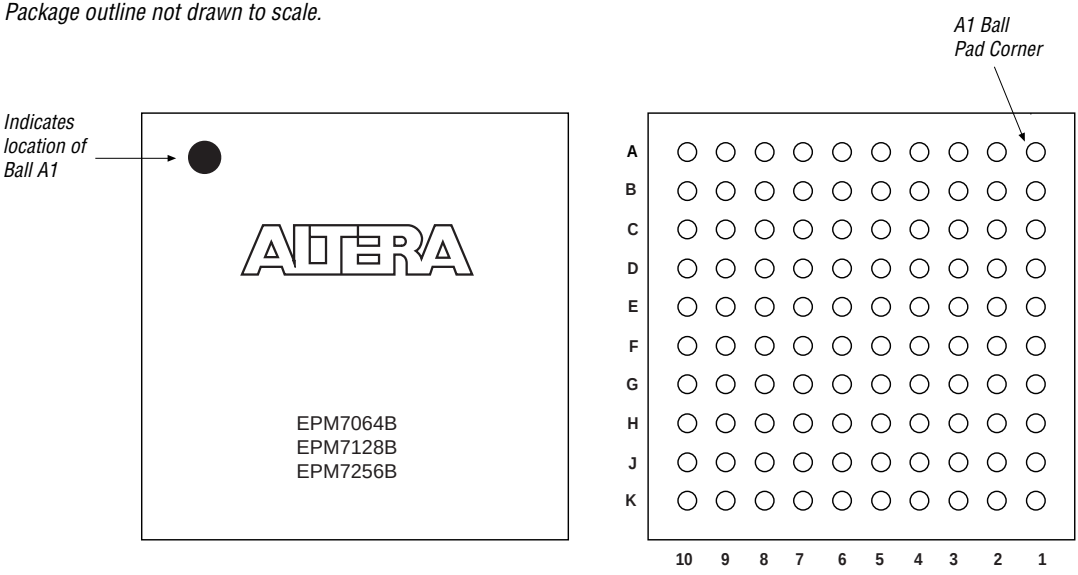


Figure 24. 144-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

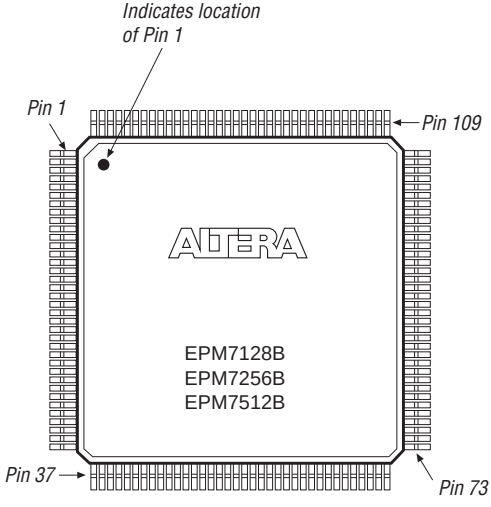


Figure 25. 208-Pin PQFP Package Pin-Out Diagram

Package outline not drawn to scale.

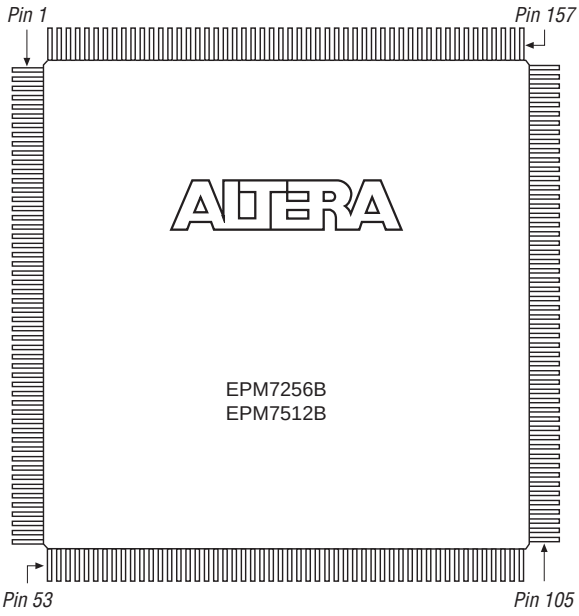


Figure 26. 256-Pin BGA Package Pin-Out Diagram

Package outline not drawn to scale.

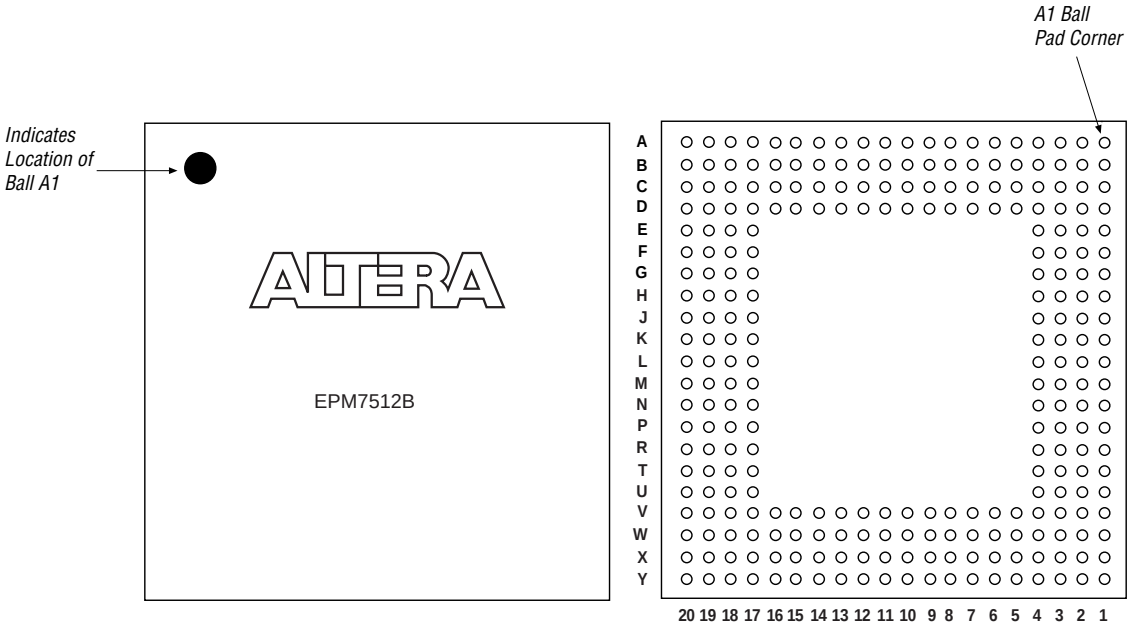
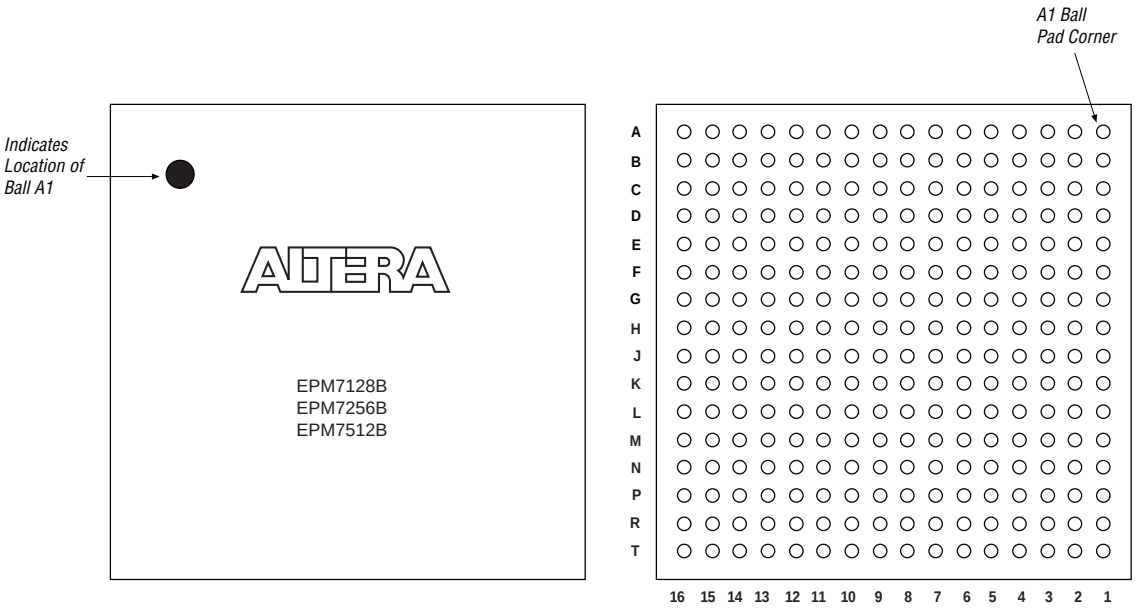


Figure 27. 256-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.



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