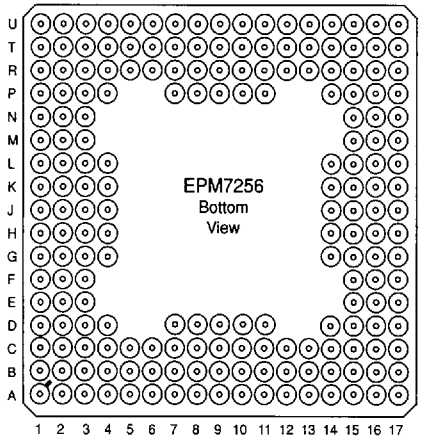
EPM7256 EPLD

Features

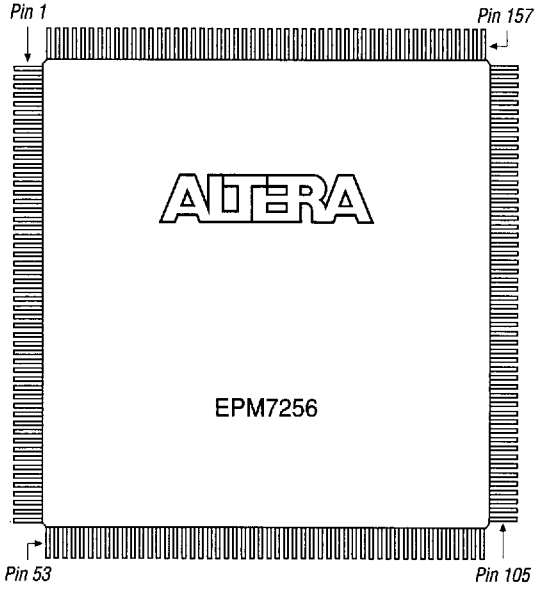
- High-density, erasable CMOS EPLD based on second-generation MAX architecture
  - 5,000 usable gates
  - Combinatorial speeds with t_{PD} = 20 ns (Higher speed versions under development)
  - Counter frequencies up to 62.5 MHz
- Advanced 0.8-micron CMOS EPROM technology
- Programmable I/O architecture with up to 164 inputs or 160 outputs
- 256 advanced macrocells to efficiently implement registered and complex combinatorial logic
- Configurable expander product-term distribution allowing up to 32 product terms in a single macrocell
- Available in the following packages (see Figure 34):
  - 192-pin pin-grid array (PGA)
  - 208-pin power quad flat pack (RQFP)
  - 208-pin metal quad flat pack (MQFP)

Figure 34. EPM7256 Package Pin-Out Diagrams

Package outlines not drawn to scale. See Tables 13 and 14 in this data sheet for pin-out information.



192-Pin PGA



208-Pin QFP

General Description

The Altera EPM7256 is a high-density, high-performance CMOS EPLD based on Altera's second-generation MAX architecture. See Figure 35. Fabricated on a 0.8-micron EPROM technology, the EPM7256 provides 5,000 usable gates, counter speeds of 62.5 MHz and propagation delays of

20 ns. The EPM7256 architecture supports 100% TTL emulation and allows high integration of SSI, MSI, and LSI logic functions. With 256 macrocells, the EPM7256 implements complete system-level designs. It easily integrates multiple programmable logic devices ranging from PALs, GALs, and 22V10s to MACH devices and FPGAs. The high density and high I/O pin count make the EPM7256 appropriate for prototyping gate arrays. The EPM7256 can accommodate both logic- and I/O-intensive designs.

Figure 35. EPM7256 Block Diagram

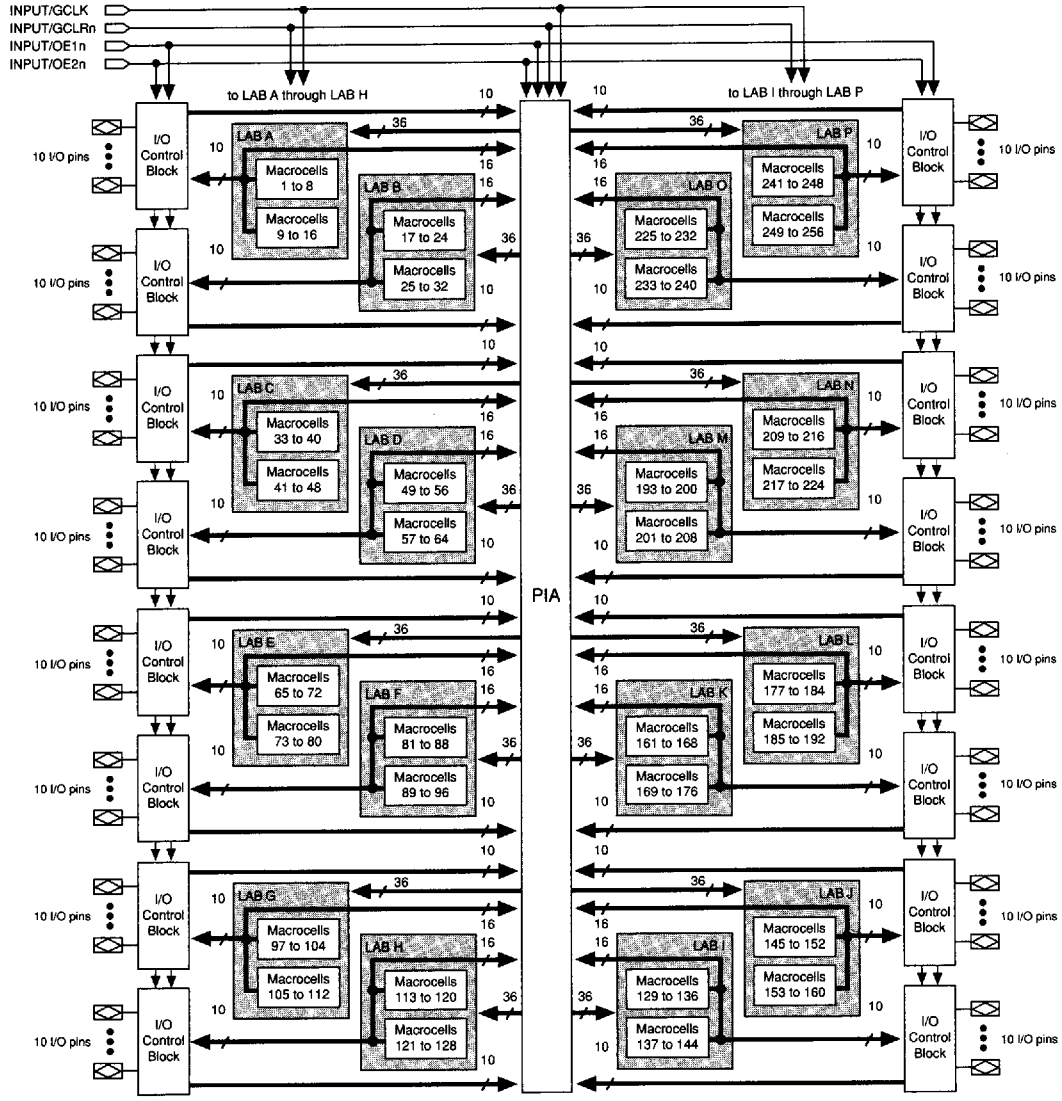


Figure 36 shows the output drive characteristics of EPM7256 I/O pins.

Figure 36. EPM7256 Output Drive Characteristics

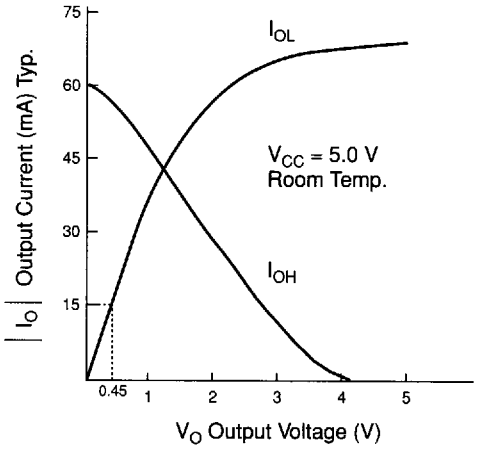


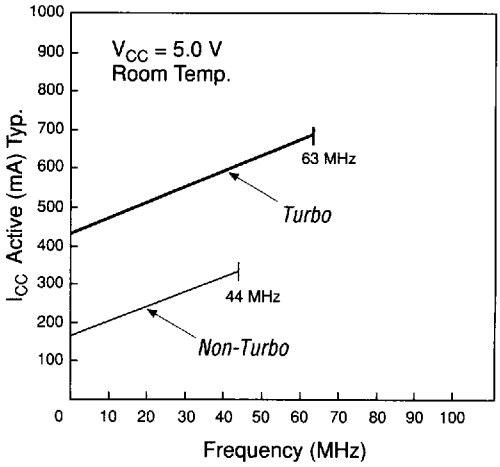
Figure 37 shows typical supply current versus frequency for the EPM7256.

Figure 37. EPM7256 I_{CC} vs. Frequency

I_{CC} is calculated with the following equation:
$I_{CC} = (1.7 \times MC_{TON}) + (0.59 \times MC_{TOFF}) + [(0.015 \times MC) \times f_{MAX}]$

The parameters for this equation are:
MC_{TON} = number of macrocells used with Turbo Bit on
MC_{TOFF} = number of macrocells used with Turbo Bit off
MC = total number of macrocells used in the design ($MC_{TON} + MC_{TOFF}$)
f_{MAX} = highest Clock frequency to the device

This measurement provides an I_{CC} estimate based on typical conditions (V_{CC} = 5.0 V, room temperature) using a typical pattern of a 16-bit loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation since this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.



Absolute Maximum Ratings

See *Operating Requirements for Altera Devices* in this data book.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (1)*	–2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current			800	mA
I_{OUT}	DC output current, per pin		–25	25	mA
P_D	Power dissipation			4000	mW
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

DC Operating Conditions

Notes (2), (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC			0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND	–10		10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40		40	µA
I_{CC1}	V_{CC} supply current (low-power mode, standby)	V_I = GND, No load *Note (4)*		150		mA
I_{CC2}	V_{CC} supply current (low-power mode, active)	V_I = GND, No load, f = 1.0 MHz, *Note (4)*		155		mA

Capacitance

Note (5)

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz		15	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

AC Operating Conditions *Note (3)*

External Timing Parameters			EPM7256-20		EPM7256-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		20		25	ns
t_{PD2}	I/O input to non-registered output			20		25	ns
t_{SU}	Global clock setup time		12		15		ns
t_{H}	Global clock hold time		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		12		15	ns
t_{CH}	Global clock high time		6		8		ns
t_{CL}	Global clock low time		6		8		ns
t_{ASU}	Array clock setup time		5		6		ns
t_{AH}	Array clock hold time		5		6		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		20		25	ns
t_{ACH}	Array clock high time		8		12.5		ns
t_{ACL}	Array clock low time		8		12.5		ns
t_{CNT}	Minimum global clock period			16		20	ns
f_{CNT}	Max. internal global clock frequency	*Note (4)*	62.5		50		MHz
t_{ACNT}	Minimum array clock period			16		25	ns
f_{ACNT}	Max. internal array clock frequency	*Note (4)*	62.5		40		MHz
f_{MAX}	Maximum clock frequency	*Note (6)*	83.3		62.5		MHz

Internal Timing Parameters			EPM7256-20		EPM7256-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad and buffer delay			3		4	ns
t_{IO}	I/O input pad and buffer delay			3		4	ns
t_{SEXP}	Shared expander delay			8		10	ns
t_{PEXP}	Parallel expander delay			2		3	ns
t_{LAD}	Logic array delay			8		10	ns
t_{LAC}	Logic control array delay			8		10	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5		6	ns
t_{ZX}	Output buffer enable delay			9		12	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		9		12	ns
t_{SU}	Register setup time		4		5		ns
t_{H}	Register hold time		5		6		ns
t_{RD}	Register delay			1		1	ns
t_{COMB}	Combinatorial delay			1		1	ns
t_{IC}	Array clock delay			8		10	ns
t_{EN}	Register enable time			8		10	ns
t_{GLOB}	Global control delay			3		4	ns
t_{PRE}	Register preset time			4		4	ns
t_{CLR}	Register clear time			4		4	ns
t_{PIA}	Prog. Interconnect Array delay			3		4	ns
t_{LPA}	Low power adder	*Note (7)*		7		8	ns

Notes to tables:

(1) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(2) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(3) Operating conditions: V_{CC} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CC} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CC} = 5.0 V ± 10%, T_C = –55° C to 125° C for military use.
(4) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} measured at 0° C.
(5) Capacitance measured at 25° C. Sample-tested only. The OE1n pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.
(6) The f_{MAX} values represent the highest frequency for pipelined data.
(7) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Product Availability

Product Grade		Availability
Commercial Temp.	(0° C to 70° C)	EPM7256-20, EPM7256-25
Industrial Temp.	(–40° C to 85° C)	EPM7256-25
Military Temp.	(–55° C to 125° C)	Consult factory

New Speed-Grade Ordering Codes

Speed-grade codes for EPM7256 devices have changed. The following table provides the new codes, which indicate the actual propagation delay times.

Old Speed Grade	New Speed Grade
EPM7256-2	EPM7256-20
EPM7256	EPM7256-25

Pin-Out Information

Tables 13 and 14 provide pin-out information for the EPM7256 packages.

Table 13. EPM7256 Dedicated Pin-Outs *Note (1)*

Dedicated Pin	192-Pin PGA	208-Pin MQFP, RQFP
GCLK	P9	184
GCLRn	R9	182
OE1n	T9	183
OE2n	U9	181
GND	C7, C13, D4, D8, D10, G14, H4, K14, L4, P8, P10, P15, R4, R11	14, 32, 50, 72, 75, 82, 94, 116, 134, 152, 174, 180, 185, 200
VCC	C5, C11, D7, D11, D14, G4, H14, K4, L14, P3, P7, P11, R5, R14	5, 23, 41, 63, 74, 83, 85, 107, 125, 143, 165, 179, 186, 191
No Connect (N.C.)	–	1, 2, 51, 52, 53, 54, 103, 104, 105, 106, 155, 156, 157, 158, 207, 208

Note to tables:

(1) CQFP pin-out information differs from the MQFP and RQFP pin-out information given in this table. Contact Altera Applications for CQFP pin-out information.

Table 14. EPM7256 I/O Pin-Outs (Part 1 of 3)

MC	LAB	192-Pin PGA	208-Pin MQFP & RQFP	MC	LAB	192-Pin PGA	208-Pin MQFP & RQFP	MC	LAB	192-Pin PGA	208-Pin MQFP & RQFP
1	A	U17	153	17	B	N17	141	33	C	B17	108
2	A	–	–	18	B	–	–	34	C	–	–
3	A	R16	154	19	B	M16	142	35	C	C15	109
4	A	–	–	20	B	–	–	36	C	–	–
5	A	P14	159	21	B	M15	144	37	C	C17	110
6	A	U16	160	22	B	P17	145	38	C	C16	111
7	A	–	–	23	B	–	–	39	C	–	–
8	A	R15	161	24	B	N16	146	40	C	D17	112
9	A	U15	162	25	B	R17	147	41	C	D15	113
10	A	–	–	26	B	–	–	42	C	–	–
11	A	T15	163	27	B	P16	148	43	C	E17	114
12	A	–	–	28	B	–	–	44	C	–	–
13	A	U14	164	29	B	T17	149	45	C	D16	115
14	A	U13	166	30	B	N15	150	46	C	E15	117
15	A	–	–	31	B	–	–	47	C	–	–
16	A	T14	167	32	B	T16	151	48	C	F16	118
49	D	A14	92	65	E	U12	168	81	F	J16	130
50	D	–	–	66	E	–	–	82	F	–	–
51	D	B12	93	67	E	R13	169	83	F	J15	131
52	D	–	–	68	E	–	–	84	F	–	–
53	D	B13	95	69	E	U11	170	85	F	K17	132
54	D	A15	96	70	E	T13	171	86	F	J14	133
55	D	–	–	71	E	–	–	87	F	–	–
56	D	B14	97	72	E	T11	172	88	F	K16	135
57	D	A16	98	73	E	T12	173	89	F	K15	136
58	D	–	–	74	E	–	–	90	F	–	–
59	D	C14	99	75	E	R12	175	91	F	L17	137
60	D	–	–	76	E	–	–	92	F	–	–
61	D	B16	100	77	E	U10	176	93	F	L16	138
62	D	B15	101	78	E	R10	177	94	F	M17	139
63	D	–	–	79	E	–	–	95	F	–	–
64	D	A17	102	80	E	T10	178	96	F	L15	140

Table 14. EPM7256 I/O Pin-Outs (Part 2 of 3)

MC	LAB	192-Pin PGA	208-Pin MQFP & RQFP	MC	LAB	192-Pin PGA	208-Pin MQFP & RQFP	MC	LAB	192-Pin PGA	208-Pin MQFP & RQFP
97	G	E16	119	113	H	C9	79	129	I	U6	197
98	G	–	–	114	H	–	–	130	I	–	–
99	G	F17	120	115	H	D9	80	131	I	T5	196
100	G	–	–	116	H	–	–	132	I	–	–
101	G	F15	121	117	H	C10	81	133	I	U7	195
102	G	G16	122	118	H	A10	84	134	I	T6	194
103	G	–	–	119	H	–	–	135	I	–	–
104	G	G15	123	120	H	A11	86	136	I	T7	193
105	G	G17	124	121	H	B10	87	137	I	R6	192
106	G	–	–	122	H	–	–	138	I	–	–
107	G	H17	126	123	H	A12	88	139	I	R7	190
108	G	–	–	124	H	–	–	140	I	–	–
109	G	H15	127	125	H	B11	89	141	I	U8	189
110	G	J17	128	126	H	A13	90	142	I	R8	188
111	G	–	–	127	H	–	–	143	I	–	–
112	G	H16	129	128	H	C12	91	144	I	T8	187
145	J	J2	27	161	K	F3	38	177	L	B9	78
146	J	–	–	162	K	–	–	178	L	–	–
147	J	J3	26	163	K	F1	37	179	L	C8	77
148	J	–	–	164	K	–	–	180	L	–	–
149	J	K1	25	165	K	E2	36	181	L	A9	76
150	J	J4	24	166	K	G2	35	182	L	A8	73
151	J	–	–	167	K	–	–	183	L	–	–
152	J	K2	22	168	K	G3	34	184	L	A7	71
153	J	K3	21	169	K	G1	33	185	L	B8	70
154	J	–	–	170	K	–	–	186	L	–	–
155	J	L1	20	171	K	H1	31	187	L	A6	69
156	J	–	–	172	K	–	–	188	L	–	–
157	J	L2	19	173	K	H3	30	189	L	B7	68
158	J	M1	18	174	K	J1	29	190	L	A5	67
159	J	–	–	175	K	–	–	191	L	–	–
160	J	L3	17	176	K	H2	28	192	L	C6	66

Table 14. EPM7256 I/O Pin-Outs (Part 3 of 3)

MC	LAB	192-Pin PGA	208-Pin MQFP & RQFP	MC	LAB	192-Pin PGA	208-Pin MQFP & RQFP
193	M	U1	4	209	N	N1	16
194	M	–	–	210	N	–	–
195	M	R2	3	211	N	M2	15
196	M	–	–	212	N	–	–
197	M	R3	206	213	N	M3	13
198	M	U2	205	214	N	P1	12
199	M	–	–	215	N	–	–
200	M	P4	204	216	N	N2	11
201	M	U3	203	217	N	R1	10
202	M	–	–	218	N	–	–
203	M	T3	202	219	N	P2	9
204	M	–	–	220	N	–	–
205	M	U4	201	221	N	T1	8
206	M	U5	199	222	N	N3	7
207	M	–	–	223	N	–	–
208	M	T4	198	224	N	T2	6
225	O	B1	49	241	P	A4	65
226	O	–	–	242	P	–	–
227	O	C3	48	243	P	B6	64
228	O	–	–	244	P	–	–
229	O	C1	47	245	P	B5	62
230	O	D3	46	246	P	A3	61
231	O	–	–	247	P	–	–
232	O	D1	45	248	P	B4	60
233	O	C2	44	249	P	A2	59
234	O	–	–	250	P	–	–
235	O	E1	43	251	P	C4	58
236	O	–	–	252	P	–	–
237	O	E3	42	253	P	B2	57
238	O	D2	40	254	P	B3	56
239	O	–	–	255	P	–	–
240	O	F2	39	256	P	A1	55