MAX 7000B

Programmable Logic Device Family

October 2000, ver. 2.1 Data Sheet

Features...

Preliminary Information

- High-performance 2.5-V CMOS EEPROM-based programmable logic devices (PLDs) built on second-generation Multiple Array MatriX (MAX®) architecture (see Table 1)
  - Pin-compatible with the popular 5.0-V MAX 7000S and 3.3-V MAX 7000A device families
  - High-density PLDs ranging from 600 to 10,000 usable gates
  - 3.5-ns pin-to-pin logic delays with counter frequencies in excess of 285.7 MHz
- Advanced 2.5-V in-system programmability (ISP)
  - Programs through the built-in IEEE Std. 1149.1 Joint Test Action Group (JTAG) interface with advanced pin-locking capability
  - Enhanced ISP algorithm for faster programming
  - ISP_Done bit to ensure complete programming
  - Pull-up resistor on I/O pins during in-system programming
  - ISP circuitry compliant with IEEE Std. 1532

For information on in-system programmable 5.0-V MAX 7000S or 3.3-V MAX 7000A devices, see the *MAX 7000 Programmable Logic Device Family Data Sheet* or the *MAX 7000A Programmable Logic Device Family Data Sheet*.

Table 1. MAX 7000B Device Features *Note (1)*

Feature	EPM7032B	EPM7064B	EPM7128B	EPM7256B	EPM7512B
Usable gates	600	1,250	2,500	5,000	10,000
Macrocells	32	64	128	256	512
Logic array blocks	2	4	8	16	32
Maximum user I/O pins	36	68	100	164	212
t_{PD} (ns)	3.5	3.5	4.0	5.0	6.0
t_{SU} (ns)	2.3	2.3	2.8	3.5	3.9
t_{FSU} (ns)	1.0	1.0	1.0	1.0	1.0
t_{CO1} (ns)	2.3	2.3	2.8	3.5	3.7
f_{CNT} (MHz)	285.7	285.7	238.1	188.7	163.9

Note:
(1) Contact Altera for up-to-date information on timing information.

…and More Features

- System-level features
  - MultiVolt™ I/O interface enabling device core to run at 2.5 V, while I/O pins are compatible with 3.3-V, 2.5-V, and 1.8-V logic levels
  - Programmable power-saving mode for 50% or greater power reduction in each macrocell
  - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
  - Support for advanced I/O standards, including SSTL-2 and SSTL-3, and GTL+
  - Bus-hold option on I/O pins
  - PCI compatible
  - Bus friendly architecture including programmable slew-rate control
  - Open-drain output option
  - Programmable security bit for protection of proprietary designs
  - Built-in boundary-scan test circuitry compliant with IEEE Std. 1149.1
  - Supports hot-socketing operation
  - Programmable ground pins
- Advanced architecture features
  - Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
  - Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
  - Programmable macrocell registers with individual clear, preset, clock, and clock enable controls
  - Two global clock signals with optional inversion
  - Programmable power-up states for macrocell registers
  - 6 to 10 pin- or logic-driven output enable signals
- Advanced package options
  - Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), ball-grid array (BGA), space-saving FineLine BGA™, 0.8-mm Ultra FineLine BGA, and plastic J-lead chip carrier (PLCC) packages
  - Pin-compatibility with other MAX 7000B devices in the same package
- Advanced software support
  - Software design support and automatic place-and-route provided by Altera's MAX+PLUS® II development system for Windows-based PCs and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations

- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPMs), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), MasterBlaster™ serial/universal serial bus (USB) communications cable, and ByteBlasterMV™ parallel port download cable, as well as programming hardware from third-party manufacturers and any Jam™ STAPL File (**.jam**), Jam Byte-Code File (**.jbc**), or Serial Vector Format File (**.svf**)-capable in-circuit tester

General Description

MAX 7000B devices are high-density, high-performance devices based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000B devices operate with a 2.5-V supply voltage and provide 600 to 10,000 usable gates, ISP, pin-to-pin delays as fast as 3.5 ns, and counter speeds up to 285.7 MHz. See Table 2.

Table 2. MAX 7000B Speed Grades *Notes (1), (2)*

Device	Speed Grade					
	-3	-4	-5	-6	-7	-10
EPM7032B	✓		✓		✓	
EPM7064B	✓		✓		✓	
EPM7128B		✓			✓	✓
EPM7256B			✓		✓	✓
EPM7512B			✓	✓	✓	✓

Notes:
(1) Contact Altera Marketing for up-to-date information on available device speed grades.
(2) Timing parameters are preliminary.

The MAX 7000B architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH and pLSI devices. MAX 7000B devices are available in a wide range of packages, including PLCC, BGA, FineLine BGA, 0.8-mm Ultra FineLine BGA, PQFP, TQFP, and VTQFP packages. See Table 3.

Table 3. MAX 7000B Maximum User I/O Pins *Notes (1), (2)*

Device	44-Pin PLCC	44-Pin TQFP	48-Pin VTQFP	49-Pin 0.8-mm Ultra FineLine BGA *(3)*	100-Pin TQFP	100-Pin FineLine BGA *(4)*	144-Pin TQFP	169-Pin 0.8-mm Ultra FineLine BGA *(3)*	208-Pin PQFP	256-Pin BGA	256-Pin FineLine BGA *(4)*
EPM7032B	36	36	36	36							
EPM7064B	36	36	40	41	68	68					
EPM7128B			40	41	84	84	100	100			100
EPM7256B					84		120	141	164		164
EPM7512B					84		120	141	176	212	212

Notes:

(1) Contact Altera for up-to-date information on available device package options.

(2) When the IEEE Std. 1149.1 (JTAG) interface is used for in-system programming or boundary-scan testing, four I/O pins become JTAG pins.

(3) All 0.8-mm BGA packages are footprint-compatible via the SameFrame™ pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 14 for more details.

(4) All FineLine BGA packages are footprint-compatible via the SameFrame pin-out feature. Therefore, designers can design a board to support a variety of devices, providing a flexible migration path across densities and pin counts. Device migration is fully supported by Altera development tools. See "SameFrame Pin-Outs" on page 14 for more details.

MAX 7000B devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000B architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased up to 100 times.

MAX 7000B devices contain 32 to 512 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

MAX 7000B devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate up to 50% lower power while adding only a nominal timing delay. MAX 7000B devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000B devices can be set for 3.3 V, 2.5 V, or 1.8 V and all input pins are 3.3-V, 2.5-V, and 1.8-V tolerant, allowing MAX 7000B devices to be used in mixed-voltage systems.

MAX 7000B devices are supported by the MAX+PLUS II development system, which are integrated packages that offer schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry, compilation and logic synthesis, simulation and timing analysis, and device programming. The MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The MAX+PLUS II software runs on Windows-based PCs, as well as Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations.

For more information on development tools, see the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet*.

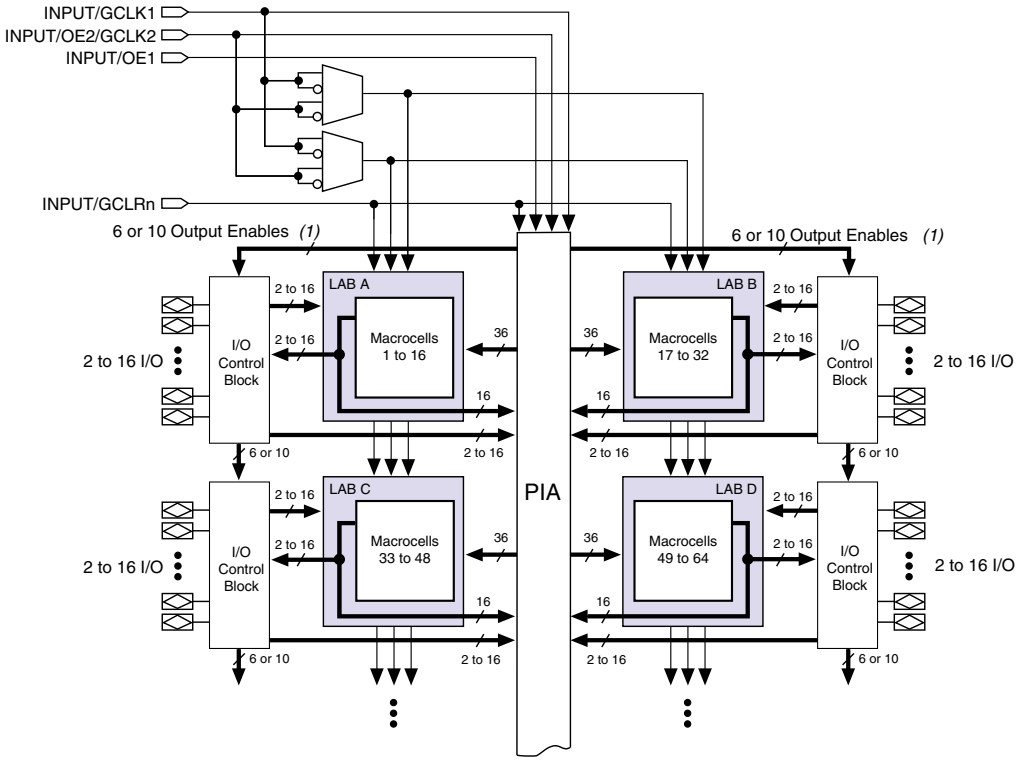
Functional Description

The MAX 7000B architecture includes the following elements:

- LABs
- Macrocells
- Expander product terms (shareable and parallel)
- PIA
- I/O control blocks

The MAX 7000B architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of MAX 7000B devices.

Figure 1. MAX 7000B Device Block Diagram



Note:

(1) EPM7032B, EPM7064B, EPM7128B, and EPM7256B devices have six output enables. EPM7512B devices have ten output enables.

Logic Array Blocks

The MAX 7000B device architecture is based on the linking of high-performance LABs. LABs consist of 16 macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the PIA, a global bus that is fed by all dedicated input pins, I/O pins, and macrocells.

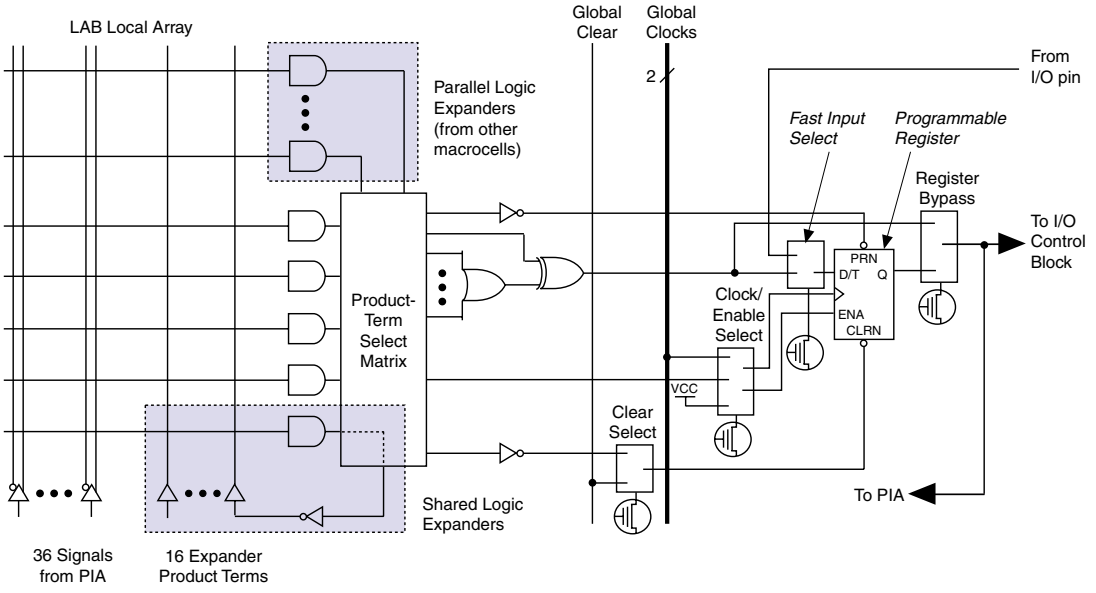
Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

Macrocells

The MAX 7000B macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. Figure 2 shows the MAX 7000B macrocell.

Figure 2. MAX 7000B Macrocell



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The MAX+PLUS II development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the MAX+PLUS II software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- Global clock signal. This mode achieves the fastest clock-to-output performance.
- Global clock signal enabled by an active-high clock enable. A clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- Array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available in MAX 7000B devices. As shown in Figure 1, these global clock signals can be the true or the complement of either of the global clock pins, `GCLK1` or `GCLK2`.

Each register also supports asynchronous preset and clear functions. As shown in Figure 2, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear from the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (`GCLRn`). Upon power-up, each register in a MAX 7000B device may be set to either a high or low state. This power-up state is specified at design entry.

All MAX 7000B I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be clocked to an input D flipflop with an extremely fast input setup time. The input path from the I/O pin to the register has a programmable delay element that can be selected to either guarantee zero hold time or to get the fastest possible set-up time (as fast as 1.0 ns).

Expander Product Terms

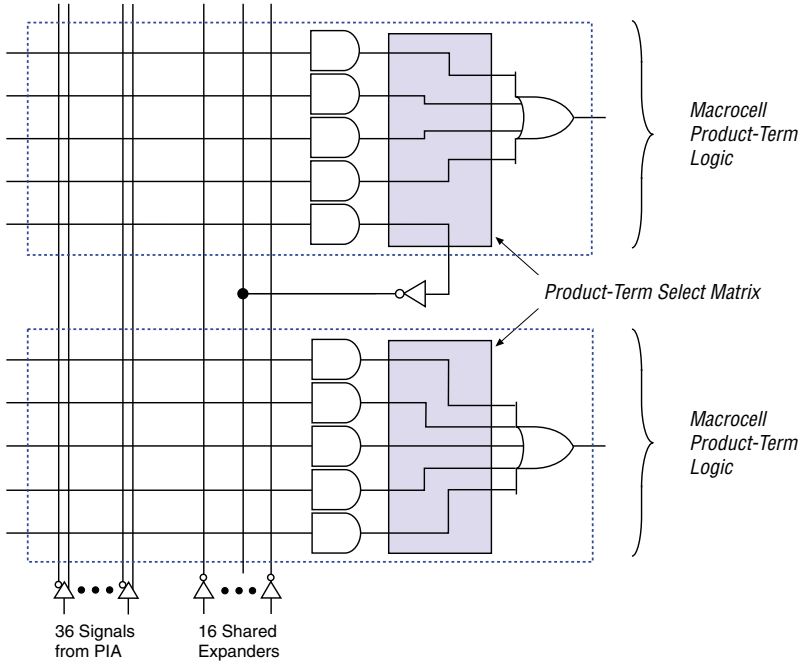
Although most logic functions can be implemented with the five product terms available in each macrocell, more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources. However, the MAX 7000B architecture also offers both shareable and parallel expander product terms ("expanders") that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay (t_{SEXP}) is incurred when shareable expanders are used. Figure 3 shows how shareable expanders can feed multiple macrocells.

Figure 3. MAX 7000B Shareable Expanders

Shareable expanders can be shared by any or all macrocells in an LAB.



Parallel Expanders

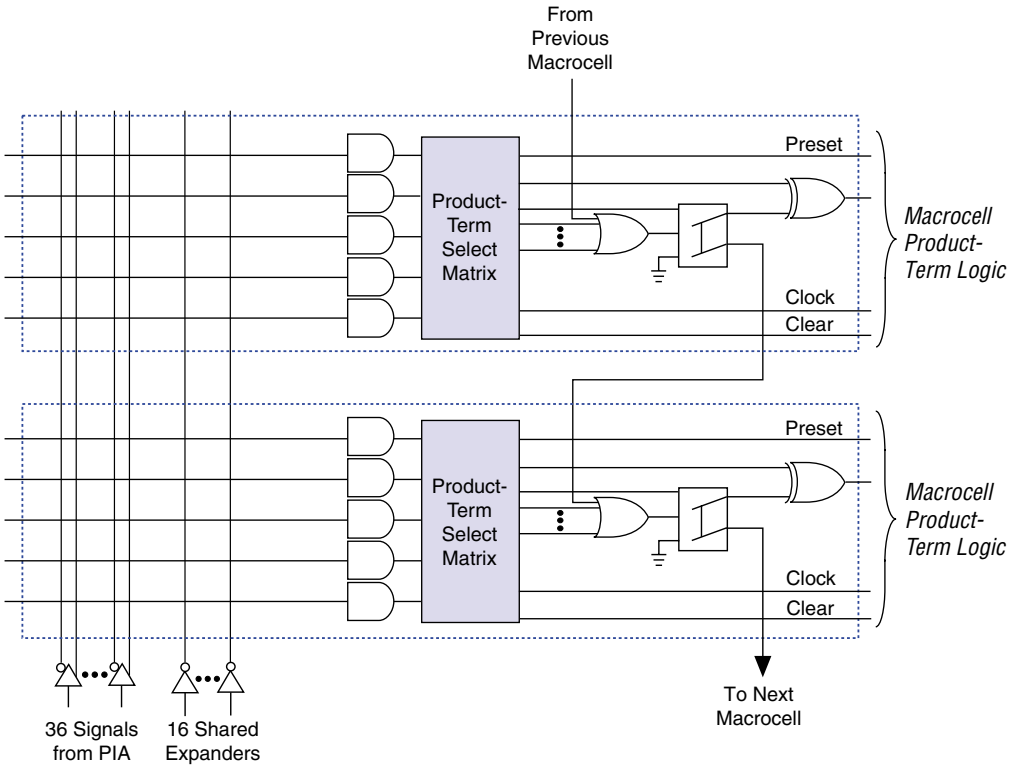
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with five product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The MAX+PLUS II Compiler can automatically allocate up to three sets of up to five parallel expanders to the macrocells that require additional product terms. Each set of five parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the five dedicated product terms within the macrocell and allocates two sets of parallel expanders; the first set includes five product terms and the second set includes four product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of eight macrocells within each LAB (e.g., macrocells 1 through 8, and 9 through 16) form two chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of eight, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 4. MAX 7000B Parallel Expanders

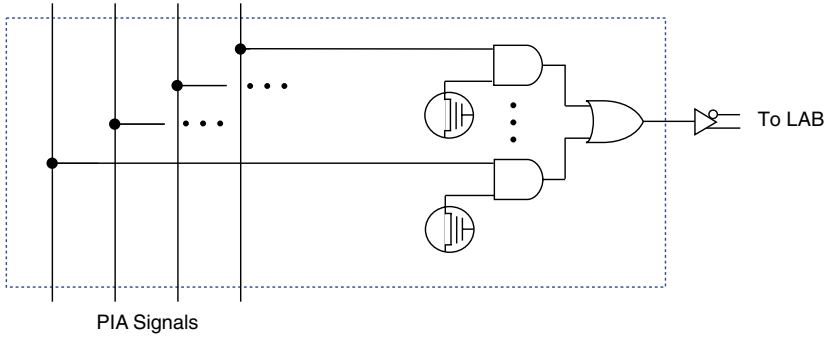
Unused product terms in a macrocell can be allocated to a neighboring macrocell.



Programmable Interconnect Array

Logic is routed between LABs on the PIA. This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000B dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a two-input AND gate, which selects a PIA signal to drive into the LAB.

Figure 5. MAX 7000B PIA Routing

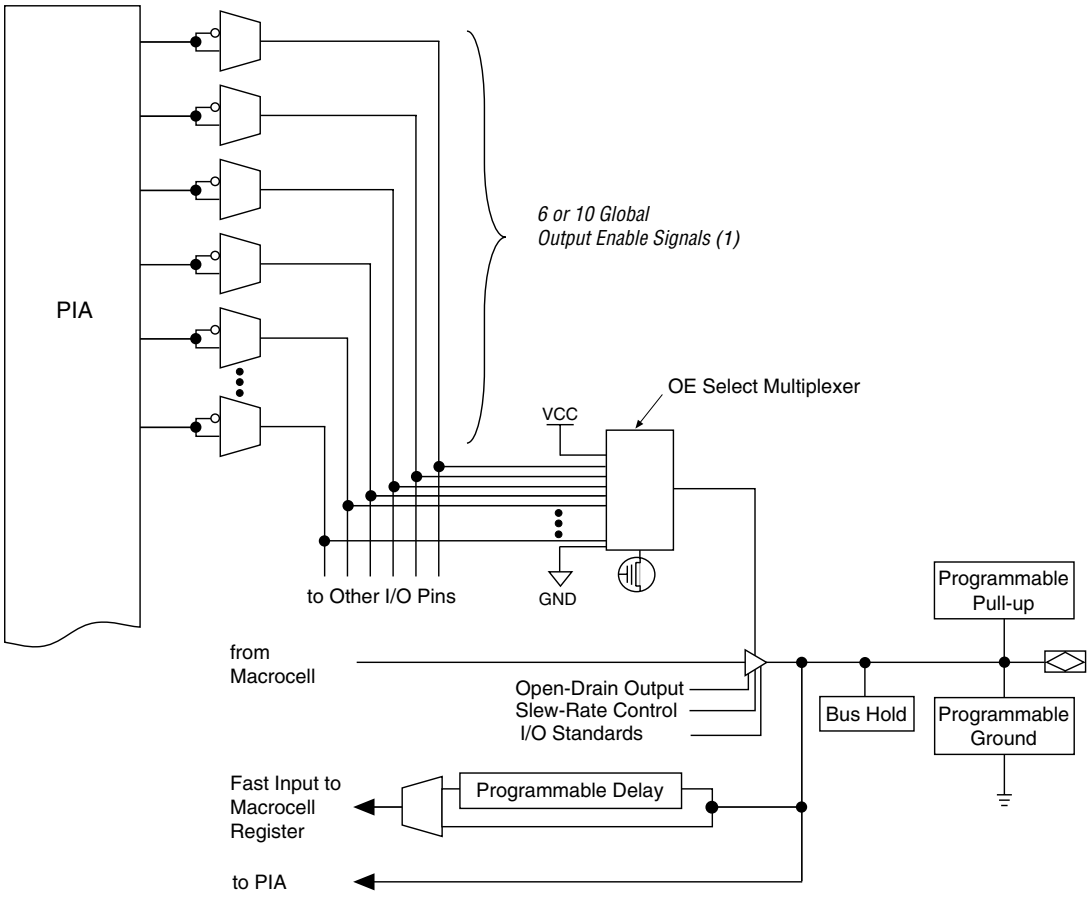


While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 7000B PIA has a predictable delay. The PIA makes a design's timing performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC}. Figure 6 shows the I/O control block for MAX 7000B devices. The I/O control block has six or ten global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

Figure 6. I/O Control Block of MAX 7000B Devices



Note:
(1) EPM7032B, EPM7064B, EPM7128B, and EPM7256B devices have six output enable signals. EPM7512B devices have ten output enable signals.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to V_{CC}, the output is enabled.

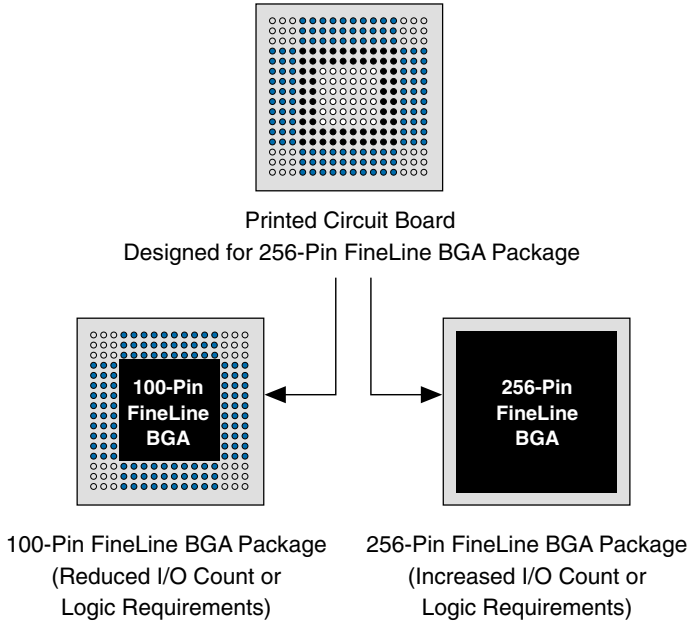
The MAX 7000B architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

SameFrame Pin-Outs

MAX 7000B devices support the SameFrame pin-out feature for FineLine BGA and 0.8-mm Ultra FineLine BGA packages. The SameFrame pin-out feature is the arrangement of balls on FineLine BGA and 0.8-mm Ultra FineLine BGA packages such that the lower-ball-count packages form a subset of the higher-ball-count packages. SameFrame pin-outs provide the flexibility to migrate not only from device to device within the same package, but also from one package to another. FineLine BGA packages are compatible with other FineLine BGA packages, and 0.8-mm Ultra FineLine BGA packages are compatible with other 0.8-mm Ultra FineLine BGA packages. A given printed circuit board (PCB) layout can support multiple device density/package combinations. For example, a single board layout can support a range of devices from an EPM7064B device in a 100-pin FineLine BGA package to an EPM7512B device in a 256-pin FineLine BGA package.

The MAX+PLUS II software provides support to design PCBs with SameFrame pin-out devices. Devices can be defined for present and future use. The MAX+PLUS II software generates pin-outs describing how to layout a board to take advantage of this migration (see Figure 7).

Figure 7. SameFrame Pin-Out Example



In-System Programmability (ISP)

MAX 7000B devices can be programmed in-system via an industry-standard 4-pin IEEE Std. 1149.1 (JTAG) interface. ISP offers quick, efficient iterations during design development and debugging cycles. The MAX 7000B architecture internally generates the high programming voltages required to program EEPROM cells, allowing in-system programming with only a single 2.5-V power supply. During in-system programming, the I/O pins are tri-stated and weakly pulled-up to eliminate board conflicts. The pull-up value is nominally 50 kΩ.

MAX 7000B devices have an enhanced ISP algorithm for faster programming. These devices also offer an ISP_Done bit that provides safe operation when in-system programming is interrupted. This ISP_Done bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a PCB with standard pick-and-place equipment before they are programmed. MAX 7000B devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera MasterBlaster communications cable, and the ByteBlasterMV parallel port download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000B devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

In-system programming can be accomplished with either an adaptive or constant algorithm. An adaptive algorithm reads information from the unit and adapts subsequent programming steps to achieve the fastest possible programming time for that unit. A constant algorithm uses a pre-defined (non-adaptive) programming sequence that does not take advantage of adaptive algorithm programming time improvements. Some in-circuit testers cannot program using an adaptive algorithm. Therefore, a constant algorithm must be used. MAX 7000B devices can be programmed with either an adaptive or constant (non-adaptive) algorithm.

The Jam Standard Test and Programming Language (STAPL), JEDEC standard JESD-71, can be used to program MAX 7000B devices with in-circuit testers, PCs, or embedded processors.

For more information on using the Jam language, see *Application Note 88 (Using the Jam Language for ISP & ICR via an Embedded Processor)* and *Application Note 122 (Using STAPL for ISP & ICR via an Embedded Processor)*.

The ISP circuitry in MAX 7000B devices is compliant with the IEEE Std. 1532 specification. The IEEE Std. 1532 is a standard developed to allow concurrent ISP between multiple PLD vendors.

Programming with External Hardware

MAX 7000B devices can be programmed on Windows-based PCs with an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.

For more information, see the *Altera Programming Hardware Data Sheet*.

The MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional device behavior with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers provide programming support for Altera devices. For more information, see *Programming Hardware Manufacturers*.

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

MAX 7000B devices include the JTAG boundary-scan test circuitry defined by IEEE Std. 1149.1. Table 4 describes the JTAG instructions supported by MAX 7000B devices. The pin-out tables starting on page 55 of this data sheet show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

Table 4. MAX 7000B JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the boundary-scan test data to pass synchronously through a selected device to adjacent devices during normal operation.
CLAMP	Allows the values in the boundary-scan register to determine pin states while placing the 1-bit bypass register between the `TDI` and `TDO` pins.
IDCODE	Selects the IDCODE register and places it between the `TDI` and `TDO` pins, allowing the IDCODE to be serially shifted out of `TDO`.
USERCODE	Selects the 32-bit USERCODE register and places it between the `TDI` and `TDO` pins, allowing the USERCODE value to be shifted out of `TDO`.
ISP Instructions	These instructions are used when programming MAX 7000B devices via the JTAG ports with the MasterBlaster, ByteBlaster, or ByteBlasterMV download cable, or using a Jam File (**.jam**), Jam Byte-Code File (**.jbc**), or Serial Vector Format File (**.svf**) via an embedded processor or test equipment.

The instruction register length of MAX 7000B devices is ten bits. The MAX 7000B USERCODE register length is 32 bits. Tables 5 and 6 show the boundary-scan register length and device IDCODE information for MAX 7000B devices.

Table 5. MAX 7000B Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM7032B	96
EPM7064B	192
EPM7128B	288
EPM7256B	480
EPM7512B	624

Table 6. 32-Bit MAX 7000B Device IDCODE *Note (1)*

Device	IDCODE (32 Bits)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer's Identity (11 Bits)	1 (1 Bit) *(2)*
EPM7032B	0010	0111 0000 0011 0010	00001101110	1
EPM7064B	0010	0111 0000 0110 0100	00001101110	1
EPM7128B	0010	0111 0001 0010 1000	00001101110	1
EPM7256B	0010	0111 0010 0101 0110	00001101110	1
EPM7512B	0010	0111 0101 0001 0010	00001101110	1

Notes:
(1) The most significant bit (MSB) is on the left.
(2) The least significant bit (LSB) for all JTAG IDCODEs is 1.

See *Application Note 39 (IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)* for more information on JTAG boundary-scan testing.

Figure 8 shows the timing information for the JTAG signals.

Figure 8. MAX 7000B JTAG Waveforms

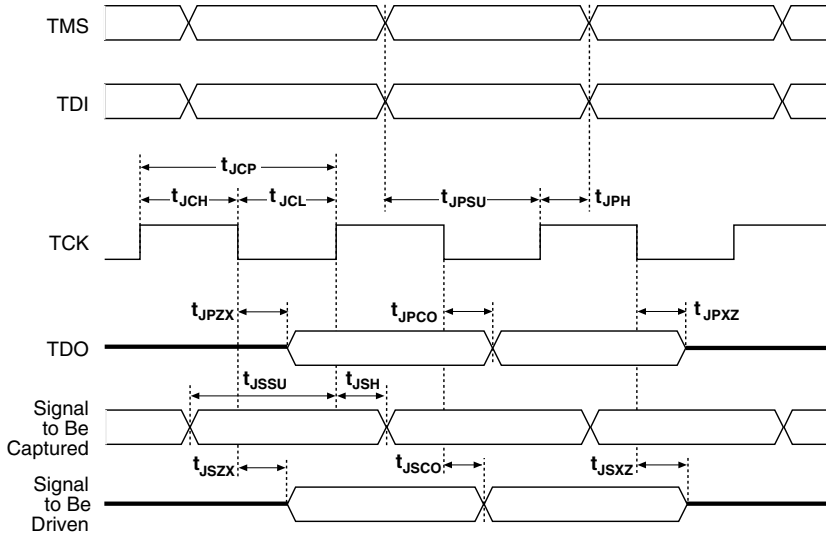


Table 7 shows the JTAG timing parameters and values for MAX 7000B devices.

Table 7. JTAG Timing Parameters & Values for MAX 7000B Devices
Note (1)

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		25	ns
t_{JSZX}	Update register high impedance to valid output		25	ns
t_{JSXZ}	Update register valid output to high impedance		25	ns

Note:
(1) Timing parameters in this table apply to all V_{CCIO} levels.

Programmable Speed/Power Control

MAX 7000B devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000B device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters.

Output Configuration

MAX 7000B device outputs can be programmed to meet a variety of system-level requirements.

MultiVolt I/O Interface

The MAX 7000B device architecture supports the MultiVolt I/O interface feature, which allows MAX 7000B devices to connect to systems with differing supply voltages. MAX 7000B devices in all packages can be set for 3.3-V, 2.5-V, or 1.8-V pin operation. These devices have one set of V_{CC} pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCIO pins can be connected to either a 3.3-V, 2.5-V, or 1.8-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When the VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels of 2.5 V or 1.8 V incur a nominal timing delay adder.

Table 8 describes the MAX 7000B MultiVolt I/O support.

Table 8. MAX 7000B MultiVolt I/O Support

V_{CCIO} (V)	Input Signal (V)				Output Signal (V)			
	1.8	2.5	3.3	5.0	1.8	2.5	3.3	5.0
1.8	✓	✓	✓		✓			
2.5	✓	✓	✓			✓		
3.3	✓	✓	✓				✓	✓

Open-Drain Output Option

MAX 7000B devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

Programmable Ground Pins

Each unused I/O pin on MAX 7000B devices may be used as an additional ground pin. This programmable ground feature does not require the use of the associated macrocell; therefore, the buried macrocell is still available for user logic.

Slew-Rate Control

The output buffer for each MAX 7000B I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low-noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

Advanced I/O Standard Support

The MAX 7000B I/O pins support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, GTL+, SSTL-3 Class I and II, and SSTL-2 Class I and II.

MAX 7000B devices contain two I/O banks. Both banks support all standards. Each I/O bank has its own VCCIO pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Within a bank, any one of the terminated standards can be supported.

Figure 9 shows the arrangement of the MAX 7000B I/O banks.

Figure 9. MAX 7000B I/O Banks for Various Advanced I/O Standards

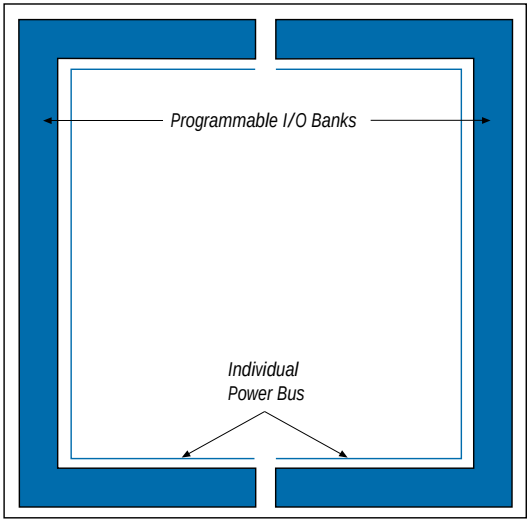


Table 9 shows which macrocells have pins in each I/O bank.

Table 9. Macrocells Contained in Each I/O Bank

Device	Bank 1	Bank 2
EPM7032B	1-16	17-32
EPM7064B	1-32	33-64
EPM7128B	1-64	65-128
EPM7256B	1-128, 177-181	129-176, 182-256
EPM7512B	1-265	266-512

Each MAX 7000B device has two VREF pins. Each can be set to a separate VREF level. Any I/O pin that uses one of the voltage-referenced standards (GTL+, SSTL2, or SSTL3) may use either of the two VREF pins. If these pins are not required as VREF pins, they may be individually programmed to function as user I/O pins.

Programmable Pull-Up Resistor

Each MAX 7000B device I/O pin provides an optional programmable pull-up resistor during user mode. When this feature is enabled for an I/O pin, the pull-up resistor (typically 50 kΩ) weakly holds the output to V_{CCIO} level.

Bus Hold

Each MAX 7000B device I/O pin provides an optional bus-hold feature. When this feature is enabled for an I/O pin, the bus-hold circuitry weakly holds the signal at its last driven state. By holding the last driven state of the pin until the next input signals is present, the bus-hold feature can eliminate the need to add external pull-up or pull-down resistors to hold a signal level when the bus is tri-stated. The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. This feature can be selected individually for each I/O pin. The bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals.

The bus-hold circuitry weakly pulls the signal level to the last driven state through a resistor with a nominal resistance (RBH) of approximately 8.5 kΩ. Table 10 gives specific sustaining current that will be driven through this resistor and overdrive current that will identify the next driven input level. This information is provided for each VCCIO voltage level.

Table 10. Bus Hold Parameters

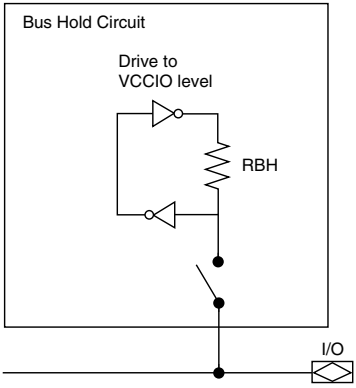
Parameter	Conditions	VCCIO Level						Units
		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	
Low sustaining current	$V_{IN} > V_{IL}$ (max)	30		50		70		µA
High sustaining current	$V_{IN} < V_{IH}$ (min)	–30		–50		–70		µA
Low overdrive current	$0 V < V_{IN} < V_{CCIO}$		200		300		500	µA
High overdrive current	$0 V < V_{IN} < V_{CCIO}$		–295		–435		–680	µA

The bus-hold circuitry is active only during user operation. At power-up, the bus-hold circuit initializes its initial hold value as V_{CC} approaches the recommended operation conditions. When transitioning from ISP to User Mode with bus hold enabled, the bus-hold circuit captures the value present on the pin at the end of programming.

Two inverters implement the bus-hold circuitry in a loop that weakly drives back to the I/O pin in user mode.

Figure 10 shows a block diagram of the bus-hold circuit.

Figure 10. Bus-Hold Circuit



PCI Compatibility

MAX 7000B devices are compatible with PCI applications as well as all 3.3-V electrical specifications in the PCI Local Bus Specification Revision 2.2 except for the clamp diode. While having multiple clamp diodes on a signal trace may be redundant, designers can add an external clamp diode to meet the specification. Table 11 shows the MAX 7000B device speed grades that meet the PCI timing specifications.

Table 11. MAX 7000B Device Speed Grades that Meet PCI Timing Specifications

Device	Specification	
	33-MHz PCI	66-MHz PCI
EPM7032B	All speed grades	-3
EPM7064B	All speed grades	-3
EPM7128B	All speed grades	-4
EPM7256B	All speed grades	-5 *(1)*
EPM7512B	All speed grades	-5 *(1)*

Note:

(1) The EPM7256B and EPM7512B devices in a -5 speed grade meet all PCI timing specifications for 66-MHz operation except the Input Setup Time to CLK—Bused Signal parameter. However, these devices are within 1 ns of that parameter. EPM7256B and EPM7512B devices meet all other 66-MHz PCI timing specifications.

Power Sequencing & Hot-Socketing

Because MAX 7000B devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. The V_{CCIO} and V_{CCINT} power planes can be powered in any order.

Signals can be driven into MAX 7000B devices before and during power-up without damaging the device. Additionally, MAX 7000B devices do not drive out during power-up. Once operating conditions are reached, MAX 7000B devices operate as specified by the user.

Design Security

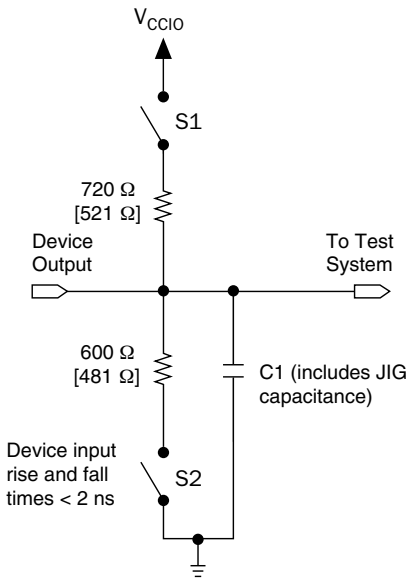
All MAX 7000B devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

Generic Testing

MAX 7000B devices are fully functionally tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 11. Test patterns can be used and then erased during early stages of the production flow.

Figure 11. MAX 7000B AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in brackets are for 2.5-V outputs. Numbers without brackets are for 3.3-V outputs. Switches S1 and S2 are open for all tests except output disable timing parameters.



Operating Conditions

Tables 12 through 15 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 7000B devices.

Table 12. MAX 7000B Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage		–0.5	3.6	V
V_{CCIO}	Supply voltage		–0.5	3.6	V
V_I	DC input voltage	*(2)*	–2.0	4.6	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_A	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias	–65	135	° C

Table 13. MAX 7000B Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers		2.375	2.625	V
V_{CCIO}	Supply voltage for output drivers, 3.3-V operation		3.0	3.6	V
	Supply voltage for output drivers, 2.5-V operation		2.375	2.625	V
	Supply voltage for output drivers, 1.8-V operation		1.71	1.89	V
V_{CCISP}	Supply voltage during in-system programming		2.375	2.625	V
V_I	Input voltage	*(3)*	–0.5	3.9	V
V_O	Output voltage		0	V_{CCIO}	V
T_J	Junction temperature	For commercial use	0	90	° C
		For industrial use	–40	105	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Table 14. MAX 7000B Device DC Operating Conditions *Note (4)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage for 3.3 V TTL/CMOS and 2.5 V TTL/CMOS		1.7	3.9	V
	High-level input voltage for 1.8 V TTL/CMOS		0.65 × V_{CCIO}	2.25	V
V_{IL}	Low-level input voltage for 3.3 V TTL/CMOS, 2.5 V TTL/CMOS, and PCI compliance		–0.5	0.8	V
	Low-level input voltage for 1.8 V TTL/CMOS		–0.5	0.35 × V_{CCIO}	
V_{OH}	3.3-V high-level TTL output voltage	I_{OH} = –8 mA DC, V_{CCIO} = 3.00 V *(5)*	2.4		V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V *(5)*	V_{CCIO} – 0.2		V
	2.5-V high-level output voltage	I_{OH} = –100 µA DC, V_{CCIO} = 2.30 V *(5)*	2.1		V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V *(5)*	2.0		V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V *(5)*	1.7		V
	1.8-V high-level output voltage	I_{OH} = –2 mA DC, V_{CCIO} =1.65 V *(5)*	1.2		V
V_{OL}	3.3-V low-level TTL output voltage	I_{OL} = 8 mA DC, V_{CCIO} = 3.00 V *(6)*		0.4	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V *(6)*		0.2	V
	2.5-V low-level output voltage	I_{OL} = 100 µA DC, V_{CCIO} = 2.30 V *(6)*		0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V *(6)*		0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V *(6)*		0.7	V
	1.8-V low-level output voltage	I_{OL} = 2 mA DC, V_{CCIO} = 1.7 V *(6)*		0.4	V
I_I	Input leakage current	V_I = V_{CCINT} or ground	–5	5	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CCINT} or ground	–5	5	µA
R_{ISP}	Value of I/O pin pull-up resistor during in-system programming or during power-up	V_{CCIO} = 1.7 to 3.6 V *(7)*	20	74	kΩ

Table 15. MAX 7000B Device Capacitance *Note (8)*

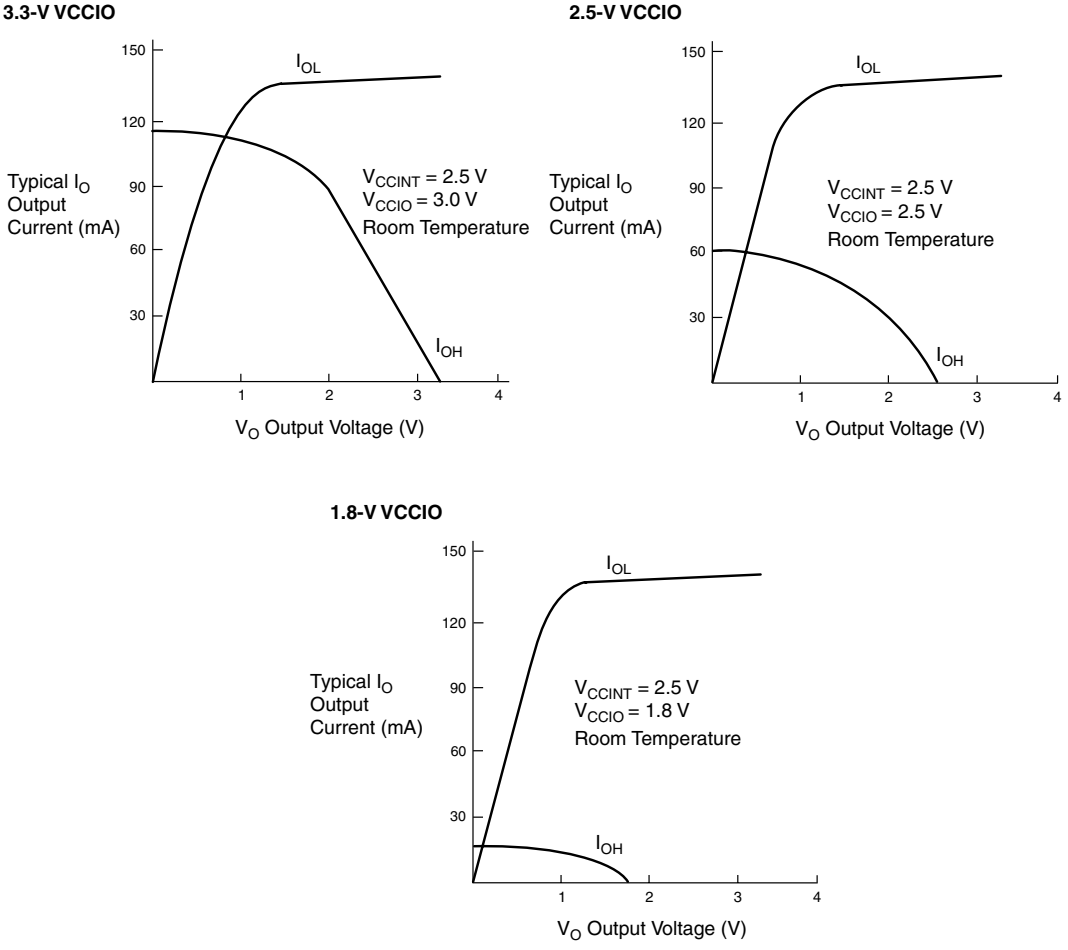
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) All pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
(4) These values are specified under the Recommended Operating Conditions in Table 13 on page 25.
(5) The parameter is measured with 50% of the outputs each sourcing the specified current. The I_{OH} parameter refers to high-level TTL or CMOS output current.
(6) The parameter is measured with 50% of the outputs each sinking the specified current. The I_{OL} parameter refers to low-level TTL or CMOS output current.
(7) This pull-up exists while devices are being programmed in-system and in unprogrammed devices during power-up. The pull-up resistor is from the pins to V_{CCIO}.
(8) Capacitance is measured at 25° C and is sample-tested only. Two of the dedicated input pins (`OE1` and `GCLRN`) have a maximum capacitance of 15 pF.

Figure 12 shows the typical output drive characteristics of MAX 7000B devices.

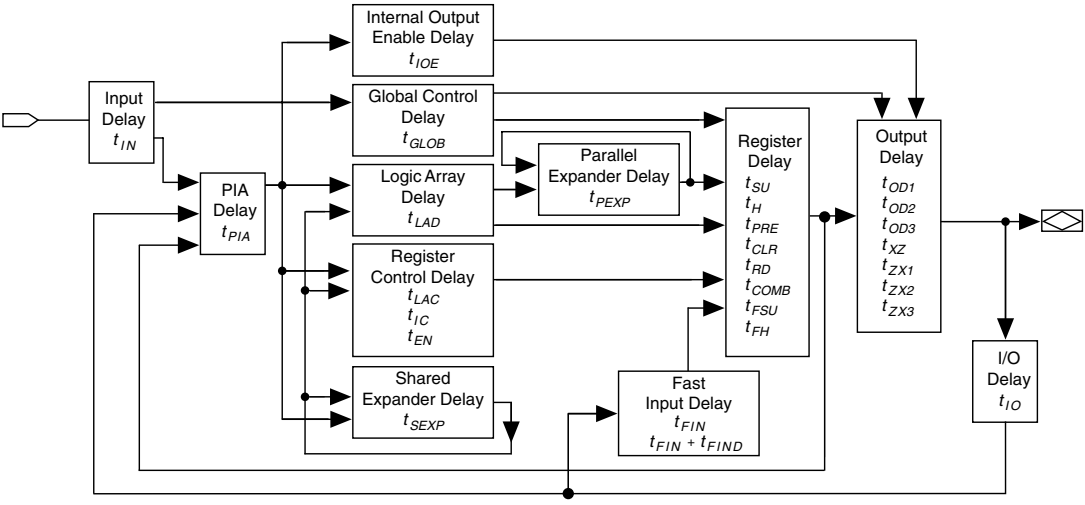
Figure 12. Output Drive Characteristics of MAX 7000B Devices



Timing Model

MAX 7000B device timing can be analyzed with the Quartus and MAX+PLUS II software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 13. MAX 7000B devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The MAX+PLUS II software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 13. MAX 7000B Timing Model

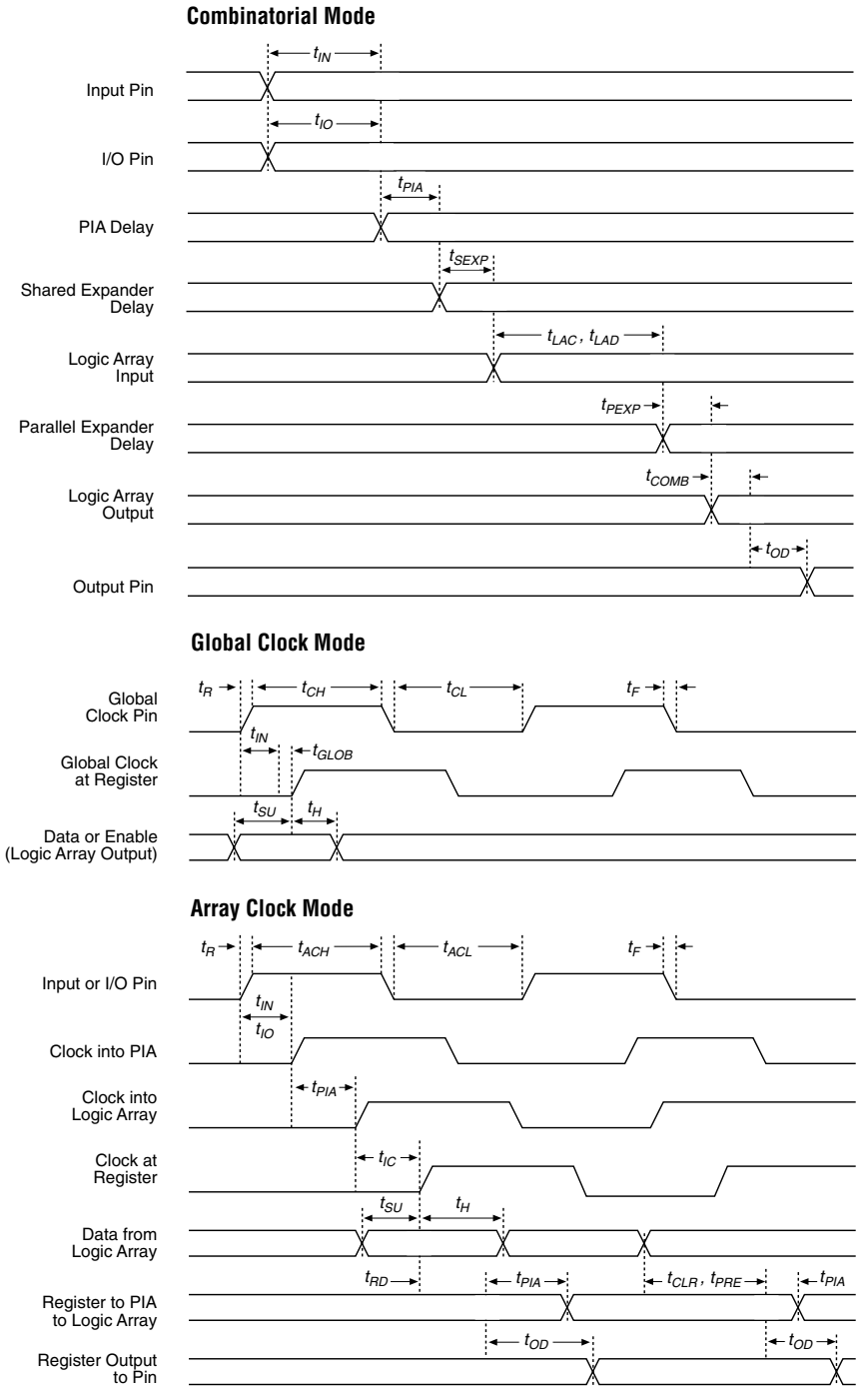


The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 14 shows the timing relationship between internal and external delay parameters.

See *Application Note 94 (Understanding MAX 7000 Timing)* for more information.

Figure 14. MAX 7000B Switching Waveforms

t_R & t_F < 2 ns. Inputs are driven at 3.0 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



Tables 16 through 30 show MAX 7000B device timing parameters.

Table 16. EPM7032B External Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3		-5		-7		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(3)*		3.5		5.0		7.5	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(3)*		3.5		5.0		7.5	ns
t_{SU}	Global clock setup time	*(3)*	2.3		3.6		5.4		ns
t_{H}	Global clock hold time	*(3)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.0		1.5		ns
t_{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		2.0		2.5		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	2.3	1.0	3.5	1.0	5.0	ns
t_{CH}	Global clock high time		1.5		2.0		3.0		ns
t_{CL}	Global clock low time		1.5		2.0		3.0		ns
t_{ASU}	Array clock setup time	*(3)*	1.0		1.8		2.6		ns
t_{AH}	Array clock hold time	*(3)*	0.4		0.6		0.9		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(3)*	1.0	3.6	1.0	5.3	1.0	7.8	ns
t_{ACH}	Array clock high time		1.5		2.0		3.0		ns
t_{ACL}	Array clock low time		1.5		2.0		3.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		1.5		2.0		3.0		ns
t_{CNT}	Minimum global clock period	*(3)*		3.5		5.4		7.9	ns
f_{CNT}	Maximum internal global clock frequency	*(3)*, *(4)*	285.7		185.2		126.6		MHz
t_{ACNT}	Minimum array clock period	*(3)*		3.5		5.4		7.9	ns
f_{ACNT}	Maximum internal array clock frequency	*(3)*, *(4)*	285.7		185.2		126.6		MHz

Table 17. EPM7032B Internal Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3		-5		-7		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.6		0.9		1.4	ns
t_{IO}	I/O input pad and buffer delay			0.6		0.9		1.4	ns
t_{FIN}	Fast input delay			0.8		0.8		0.8	ns
t_{FIND}	Programmable delay adder for fast input			1.0		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.6		2.3		3.4	ns
t_{PEXP}	Parallel expander delay			0.4		0.6		0.9	ns
t_{LAD}	Logic array delay			1.0		1.4		2.1	ns
t_{LAC}	Logic control array delay			0.4		0.5		0.8	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.5		0.8		1.1	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.5		5.8		6.1	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		2.6		3.8		5.6	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		7.6		8.8		10.6	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		2.6		3.8		5.6	ns
t_{SU}	Register setup time		1.0		1.8		2.6		ns
t_{H}	Register hold time		0.4		0.6		0.9		ns
t_{FSU}	Register setup time of fast input		0.9		1.2		2.1		ns
t_{FH}	Register hold time of fast input		1.1		0.8		0.4		ns
t_{RD}	Register delay			0.5		0.8		1.1	ns
t_{COMB}	Combinatorial delay			0.4		0.5		0.8	ns
t_{IC}	Array clock delay			1.0		1.4		2.1	ns
t_{EN}	Register enable time			0.4		0.5		0.8	ns
t_{GLOB}	Global control delay			0.7		1.0		1.4	ns
t_{PRE}	Register preset time			1.1		1.6		2.4	ns
t_{CLR}	Register clear time			1.1		1.6		2.4	ns
t_{PIA}	PIA delay	*(3)*		1.0		1.4		2.1	ns
t_{LPA}	Low-power adder	*(5)*		3.0		4.0		4.0	ns

Table 18. EPM7032B Selectable I/O Standard Timing Adder Delays

I/O Standard	Parameter	Speed Grade						Unit
		-3		-5		-7		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to (PIA)		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.3		0.4		0.6	ns
	Input to global clock and clear		0.3		0.4		0.6	ns
	Input to fast input register		0.2		0.3		0.4	ns
	All outputs		0.2		0.3		0.4	ns
1.8 V TTL/CMOS	Input to PIA		0.5		0.8		1.1	ns
	Input to global clock and clear		0.5		0.8		1.1	ns
	Input to fast input register		0.4		0.5		0.8	ns
	All outputs		1.2		1.8		2.6	ns
SSTL-2 Class I	Input to PIA		1.3		1.9		2.8	ns
	Input to global clock and clear		1.2		1.8		2.6	ns
	Input to fast input register		0.9		1.3		1.9	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.3		1.9		2.8	ns
	Input to global clock and clear		1.2		1.8		2.6	ns
	Input to fast input register		0.9		1.3		1.9	ns
	All outputs		–0.1		–0.1		–0.2	ns
SSTL-3 Class I	Input to PIA		1.2		1.8		2.6	ns
	Input to global clock and clear		0.9		1.3		1.9	ns
	Input to fast input register		0.8		1.1		1.7	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.2		1.8		2.6	ns
	Input to global clock and clear		0.9		1.3		1.9	ns
	Input to fast input register		0.8		1.1		1.7	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.6		2.3		3.4	ns
	Input to global clock and clear		1.5		2.1		3.2	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Table 18. EPM7032B Selectable I/O Standard Timing Adder Delays

I/O Standard	Parameter	Speed Grade						Unit
		-3		-5		-7		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 13 on page 25.
(2) MAX 7000B timing values are preliminary.
(3) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(4) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(5) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Table 19. EPM7064B External Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3		-5		-7		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(3)*		3.5		5.0		7.5	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(3)*		3.5		5.0		7.5	ns
t_{SU}	Global clock setup time	*(3)*	2.3		3.2		4.3		ns
t_{H}	Global clock hold time	*(3)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.0		1.5		ns
t_{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		2.0		2.5		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	2.3	1.0	3.3	1.0	5.5	ns
t_{CH}	Global clock high time		1.5		2.0		3.0		ns
t_{CL}	Global clock low time		1.5		2.0		3.0		ns
t_{ASU}	Array clock setup time	*(3)*	1.0		1.4		2.1		ns
t_{AH}	Array clock hold time	*(3)*	0.4		0.6		0.9		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(3)*	1.0	3.6	1.0	5.1	1.0	7.7	ns
t_{ACH}	Array clock high time		1.5		2.0		3.0		ns
t_{ACL}	Array clock low time		1.5		2.0		3.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		1.5		2.0		3.0		ns
t_{CNT}	Minimum global clock period	*(3)*		3.5		5.0		7.5	ns
f_{CNT}	Maximum internal global clock frequency	*(3)*, *(4)*	285.7		200.0		133.3		MHz
t_{ACNT}	Minimum array clock period	*(3)*		3.5		5.0		7.5	ns
f_{ACNT}	Maximum internal array clock frequency	*(3)*, *(4)*	285.7		200.0		133.3		MHz

Table 20. EPM7064B Internal Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-3		-5		-7		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.6		0.8		1.2	ns
t_{IO}	I/O input pad and buffer delay			0.6		0.8		1.2	ns
t_{FIN}	Fast input delay			0.8		0.8		1.7	ns
t_{FIND}	Programmable delay adder for fast input			1.0		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.6		2.3		3.5	ns
t_{PEXP}	Parallel expander delay			0.4		0.6		0.9	ns
t_{LAD}	Logic array delay			1.0		1.5		2.2	ns
t_{LAC}	Logic control array delay			0.4		0.6		0.9	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.5		0.7		1.1	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.5		5.7		6.1	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		5.7		8.6	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		9.0		10.7		13.6	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		5.7		8.6	ns
t_{SU}	Register setup time		1.0		1.4		2.1		ns
t_{H}	Register hold time		0.4		0.6		0.9		ns
t_{FSU}	Register setup time of fast input		0.9		1.3		1.9		ns
t_{FH}	Register hold time of fast input		1.1		0.7		0.6		ns
t_{RD}	Register delay			0.5		0.7		1.1	ns
t_{COMB}	Combinatorial delay			0.4		0.6		0.9	ns
t_{IC}	Array clock delay			1.0		1.5		2.2	ns
t_{EN}	Register enable time			0.4		0.6		0.9	ns
t_{GLOB}	Global control delay			0.7		1.1		2.1	ns
t_{PRE}	Register preset time			1.1		1.6		2.4	ns
t_{CLR}	Register clear time			1.1		1.6		2.4	ns
t_{PIA}	PIA delay	*(3)*		1.0		1.4		2.1	ns
t_{LPA}	Low-power adder	*(5)*		3.0		4.0		4.0	ns

Table 21. EPM7064B Selectable I/O Standard Timing Adder Delays

I/O Standard	Parameter	Speed Grade						Unit
		-3		-5		-7		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.3		0.4		0.6	ns
	Input to global clock and clear		0.3		0.4		0.6	ns
	Input to fast input register		0.2		0.3		0.4	ns
	All outputs		0.2		0.3		0.4	ns
1.8 V TTL/CMOS	Input to PIA		0.5		0.7		1.1	ns
	Input to global clock and clear		0.5		0.7		1.1	ns
	Input to fast input register		0.4		0.6		0.9	ns
	All outputs		1.2		1.7		2.6	ns
SSTL-2 Class I	Input to PIA		1.3		1.9		2.8	ns
	Input to global clock and clear		1.2		1.7		2.6	ns
	Input to fast input register		0.9		1.3		1.9	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.3		1.9		2.8	ns
	Input to global clock and clear		1.2		1.7		2.6	ns
	Input to fast input register		0.9		1.3		1.9	ns
	All outputs		–0.1		–0.1		–0.2	ns
SSTL-3 Class I	Input to PIA		1.2		1.7		2.6	ns
	Input to global clock and clear		0.9		1.3		1.9	ns
	Input to fast input register		0.8		1.1		1.7	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.2		1.7		2.6	ns
	Input to global clock and clear		0.9		1.3		1.9	ns
	Input to fast input register		0.8		1.1		1.7	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.6		2.3		3.4	ns
	Input to global clock and clear		1.5		2.3		3.4	ns
	Input to fast input register		1.5		2.1		3.2	ns
	All outputs		0.0		0.0		0.0	ns

Table 21. EPM7064B Selectable I/O Standard Timing Adder Delays

I/O Standard	Parameter	Speed Grade						Unit
		-3		-5		-7		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 13 on page 25.
(2) MAX 7000B timing values are preliminary.
(3) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(4) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(5) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Table 22. EPM7128B External Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(3)*		4.0		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(3)*		4.0		7.5		10.0	ns
t_{SU}	Global clock setup time	*(3)*	2.8		5.0		6.6		ns
t_{H}	Global clock hold time	*(3)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		2.0		3.0		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	2.8	1.0	5.5	1.0	7.2	ns
t_{CH}	Global clock high time		2.0		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(3)*	1.4		2.7		3.5		ns
t_{AH}	Array clock hold time	*(3)*	0.4		0.9		1.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(3)*	1.0	4.2	1.0	7.8	1.0	10.3	ns
t_{ACH}	Array clock high time		2.0		3.0		4.0		ns
t_{ACL}	Array clock low time		2.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		2.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(3)*		4.2		8.1		10.6	ns
f_{CNT}	Maximum internal global clock frequency	*(3)*, *(4)*	238.1		123.5		94.3		MHz
t_{ACNT}	Minimum array clock period	*(3)*		4.2		8.1		10.6	ns
f_{ACNT}	Maximum internal array clock frequency	*(3)*, *(4)*	238.1		123.5		94.3		MHz

Table 23. EPM7128B Internal Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-4		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.8		1.2		1.6	ns
t_{IO}	I/O input pad and buffer delay			0.8		1.2		1.6	ns
t_{FIN}	Fast input delay			0.9		2.5		3.0	ns
t_{FIND}	Programmable delay adder for fast input			1.0		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.6		3.0		4.0	ns
t_{PEXP}	Parallel expander delay			0.4		1.0		1.3	ns
t_{LAD}	Logic array delay			1.1		2.2		2.9	ns
t_{LAC}	Logic control array delay			0.4		0.8		1.1	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.6		1.2		1.6	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.6		6.2		6.6	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		3.0		5.1		5.0	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		8.0		10.1		10.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		3.0		5.1		5.0	ns
t_{SU}	Register setup time		1.4		2.7		3.5		ns
t_{H}	Register hold time		0.4		0.9		1.0		ns
t_{FSU}	Register setup time of fast input		0.9		0.9		0.9		ns
t_{FH}	Register hold time of fast input		1.1		1.6		1.6		ns
t_{RD}	Register delay			0.6		1.2		1.6	ns
t_{COMB}	Combinatorial delay			0.4		0.9		1.3	ns
t_{IC}	Array clock delay			1.1		2.2		2.9	ns
t_{EN}	Register enable time			0.4		0.8		1.1	ns
t_{GLOB}	Global control delay			0.8		1.9		2.4	ns
t_{PRE}	Register preset time			1.3		2.6		3.3	ns
t_{CLR}	Register clear time			1.3		2.6		3.3	ns
t_{PIA}	PIA delay	*(3)*		1.1		2.0		2.6	ns
t_{LPA}	Low-power adder	*(5)*		3.5		4.0		5.0	ns

Table 24. EPM7128B Selectable I/O Standard Timing Adder Delays

I/O Standard	Parameter	Speed Grade						Unit
		-4		-7		-10		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.3		0.6		0.8	ns
	Input to global clock and clear		0.3		0.6		0.8	ns
	Input to fast input register		0.2		0.4		0.5	ns
	All outputs		0.2		0.4		0.5	ns
1.8 V TTL/CMOS	Input to PIA		0.5		0.9		1.3	ns
	Input to global clock and clear		0.5		0.9		1.3	ns
	Input to fast input register		0.4		0.8		1.0	ns
	All outputs		1.2		2.3		3.0	ns
SSTL-2 Class I	Input to PIA		1.4		2.6		3.5	ns
	Input to global clock and clear		1.2		2.3		3.0	ns
	Input to fast input register		1.0		1.9		2.5	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.4		2.6		3.5	ns
	Input to global clock and clear		1.2		2.3		3.0	ns
	Input to fast input register		1.0		1.9		2.5	ns
	All outputs		–0.1		–0.2		–0.3	ns
SSTL-3 Class I	Input to PIA		1.3		2.4		3.3	ns
	Input to global clock and clear		1.0		1.9		2.5	ns
	Input to fast input register		0.9		1.7		2.3	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.3		2.4		3.3	ns
	Input to global clock and clear		1.0		1.9		2.5	ns
	Input to fast input register		0.9		1.7		2.3	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.7		3.2		4.3	ns
	Input to global clock and clear		1.7		3.2		4.3	ns
	Input to fast input register		1.6		3.0		4.0	ns
	All outputs		0.0		0.0		0.0	ns

Table 24. EPM7128B Selectable I/O Standard Timing Adder Delays

I/O Standard	Parameter	Speed Grade						Unit
		-4		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 13 on page 25.
(2) MAX 7000B timing values are preliminary.
(3) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(4) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(5) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Table 25. EPM7256B External Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(3)*		5.0		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(3)*		5.0		7.5		10.0	ns
t_{SU}	Global clock setup time	*(3)*	3.5		5.3		7.0		ns
t_{H}	Global clock hold time	*(3)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Global clock hold time for fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		2.5		3.0		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.5	1.0	5.3	1.0	7.0	ns
t_{CH}	Global clock high time		2.0		3.0		4.0		ns
t_{CL}	Global clock low time		2.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(3)*	1.7		2.6		3.4		ns
t_{AH}	Array clock hold time	*(3)*	0.5		0.8		1.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(3)*	1.0	5.3	1.0	8.0	1.0	10.6	ns
t_{ACH}	Array clock high time		2.0		3.0		4.0		ns
t_{ACL}	Array clock low time		2.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		2.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(3)*		5.3		8.1		10.6	ns
f_{CNT}	Maximum internal global clock frequency	*(3)*, *(4)*	188.7		123.5		94.3		MHz
t_{ACNT}	Minimum array clock period	*(3)*		5.3		8.1		10.6	ns
f_{ACNT}	Maximum internal array clock frequency	*(3)*, *(4)*	188.7		123.5		94.3		MHz

Table 26. EPM7256B Internal Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.9		1.3		1.8	ns
t_{IO}	I/O input pad and buffer delay			0.9		1.3		1.8	ns
t_{FIN}	Fast input delay			1.1		1.7		2.2	ns
t_{FIND}	Programmable delay adder for fast input			1.5		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.6		2.4		3.2	ns
t_{PEXP}	Parallel expander delay			0.4		0.6		0.8	ns
t_{LAD}	Logic array delay			1.5		2.3		3.0	ns
t_{LAC}	Logic control array delay			0.6		0.9		1.2	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.8		1.2		1.6	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.8		6.2		6.6	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		4.0		6.0		8.0	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		9.0		11.0		13.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4.0		6.0		8.0	ns
t_{SU}	Register setup time		1.7		2.6		3.4		ns
t_{H}	Register hold time		0.5		0.8		1.0		ns
t_{FSU}	Register setup time of fast input		0.9		1.4		1.3		ns
t_{FH}	Register hold time of fast input		1.1		1.1		1.2		ns
t_{RD}	Register delay			0.8		1.2		1.6	ns
t_{COMB}	Combinatorial delay			0.5		0.7		1.0	ns
t_{IC}	Array clock delay			1.5		2.3		3.0	ns
t_{EN}	Register enable time			0.6		0.9		1.2	ns
t_{GLOB}	Global control delay			1.0		1.6		2.0	ns
t_{PRE}	Register preset time			1.7		2.6		3.4	ns
t_{CLR}	Register clear time			1.7		2.6		3.4	ns
t_{PIA}	PIA delay	*(3)*		1.3		2.0		2.6	ns
t_{LPA}	Low-power adder	*(5)*		4.0		4.0		5.0	ns

Table 27. EPM7256B Selectable I/O Standard Timing Adder Delays

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.4		0.6		0.8	ns
	Input to global clock and clear		0.3		0.5		0.6	ns
	Input to fast input register		0.2		0.3		0.4	ns
	All outputs		0.2		0.3		0.4	ns
1.8 V TTL/CMOS	Input to PIA		0.6		0.9		1.2	ns
	Input to global clock and clear		0.6		0.9		1.2	ns
	Input to fast input register		0.5		0.8		1.0	ns
	All outputs		1.3		2.0		2.6	ns
SSTL-2 Class I	Input to PIA		1.5		2.3		3.0	ns
	Input to global clock and clear		1.3		2.0		2.6	ns
	Input to fast input register		1.1		1.7		2.2	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.5		2.3		3.0	ns
	Input to global clock and clear		1.3		2.0		2.6	ns
	Input to fast input register		1.1		1.7		2.2	ns
	All outputs		–0.1		–0.2		–0.2	ns
SSTL-3 Class I	Input to PIA		1.4		2.1		2.8	ns
	Input to global clock and clear		1.1		1.7		2.2	ns
	Input to fast input register		1.0		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.4		2.1		2.8	ns
	Input to global clock and clear		1.1		1.7		2.2	ns
	Input to fast input register		1.0		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.8		2.7		3.6	ns
	Input to global clock and clear		1.8		2.7		3.6	ns
	Input to fast input register		1.7		2.6		3.4	ns
	All outputs		0.0		0.0		0.0	ns

Table 27. EPM7256B Selectable I/O Standard Timing Adder Delays

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 13 on page 25.
(2) MAX 7000B timing values are preliminary.
(3) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(4) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(5) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Table 28. EPM7512B External Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF *(3)*		5.5		7.5		10.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF *(3)*		5.5		7.5		10.0	ns
t_{SU}	Global clock setup time	*(3)*	3.9		5.3		7.0		ns
t_{H}	Global clock hold time	*(3)*	0.0		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input		1.0		1.5		1.5		ns
t_{FH}	Global clock hold time of fast input		1.0		1.0		1.0		ns
t_{FZHSU}	Global clock setup time of fast input with zero hold time		3.0		3.0		3.0		ns
t_{FZHH}	Global clock hold time of fast input with zero hold time		0.0		0.0		0.0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF	1.0	3.7	1.0	5.2	1.0	6.9	ns
t_{CH}	Global clock high time		3.0		3.0		4.0		ns
t_{CL}	Global clock low time		3.0		3.0		4.0		ns
t_{ASU}	Array clock setup time	*(3)*	2.2		2.9		3.8		ns
t_{AH}	Array clock hold time	*(3)*	0.4		0.7		0.9		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF *(3)*	1.0	5.4	1.0	7.6	1.0	10.1	ns
t_{ACH}	Array clock high time		3.0		3.0		4.0		ns
t_{ACL}	Array clock low time		3.0		3.0		4.0		ns
t_{CPPW}	Minimum pulse width for clear and preset		3.0		3.0		4.0		ns
t_{CNT}	Minimum global clock period	*(3)*		6.1		8.4		11.0	ns
f_{CNT}	Maximum internal global clock frequency	*(3)*, *(4)*	163.9		119.0		90.9		MHz
t_{ACNT}	Minimum array clock period	*(3)*		6.1		8.4		11.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(3)*, *(4)*	163.9		119.0		90.9		MHz

Table 29. EPM7512B Internal Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	Speed Grade						Unit
			-5		-7		-10		
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			0.8		1.1		1.6	ns
t_{IO}	I/O input pad and buffer delay			0.8		1.1		1.6	ns
t_{FIN}	Fast input delay			1.4		1.9		2.4	ns
t_{FIND}	Programmable delay adder for fast input			1.5		1.5		1.5	ns
t_{SEXP}	Shared expander delay			1.6		2.3		3.0	ns
t_{PEXP}	Parallel expander delay			0.4		0.5		0.7	ns
t_{LAD}	Logic array delay			1.8		2.5		3.3	ns
t_{LAC}	Logic control array delay			0.7		1.0		1.3	ns
t_{IOE}	Internal output enable delay			0.0		0.0		0.0	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		0.7		1.0		1.3	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.7		6.0		6.3	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF		3.7		5.0		6.7	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		8.7		10.0		11.7	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		3.7		5.0		6.7	ns
t_{SU}	Register setup time		1.7		2.3		3.0		ns
t_{H}	Register hold time		0.9		1.3		1.7		ns
t_{FSU}	Register setup time of fast input		0.9		1.4		1.4		ns
t_{FH}	Register hold time of fast input		1.1		1.1		1.1		ns
t_{RD}	Register delay			0.9		1.3		1.7	ns
t_{COMB}	Combinatorial delay			0.5		0.6		0.8	ns
t_{IC}	Array clock delay			1.3		1.9		2.5	ns
t_{EN}	Register enable time			0.7		1.0		1.3	ns
t_{GLOB}	Global control delay			1.3		1.8		2.3	ns
t_{PRE}	Register preset time			1.8		2.5		3.3	ns
t_{CLR}	Register clear time			1.8		2.5		3.3	ns
t_{PIA}	PIA delay	*(3)*		1.7		2.3		3.0	ns
t_{LPA}	Low-power adder	*(5)*		4.0		4.5		5.0	ns

Table 30. EPM7512B Selectable I/O Standard Timing Adder Delays

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
3.3 V TTL/CMOS	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns
2.5 V TTL/CMOS	Input to PIA		0.4		0.5		0.7	ns
	Input to global clock and clear		0.3		0.4		0.5	ns
	Input to fast input register		0.2		0.3		0.3	ns
	All outputs		0.2		0.3		0.3	ns
1.8 V TTL/CMOS	Input to PIA		0.7		1.0		1.3	ns
	Input to global clock and clear		0.6		0.8		1.0	ns
	Input to fast input register		0.5		0.6		0.8	ns
	All outputs		1.3		1.8		2.3	ns
SSTL-2 Class I	Input to PIA		1.5		2.0		2.7	ns
	Input to global clock and clear		1.4		1.9		2.5	ns
	Input to fast input register		1.1		1.5		2.0	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-2 Class II	Input to PIA		1.5		2.0		2.7	ns
	Input to global clock and clear		1.4		1.9		2.5	ns
	Input to fast input register		1.1		1.5		2.0	ns
	All outputs		–0.1		–0.1		–0.2	ns
SSTL-3 Class I	Input to PIA		1.4		1.9		2.5	ns
	Input to global clock and clear		1.2		1.6		2.2	ns
	Input to fast input register		1.0		1.4		1.8	ns
	All outputs		0.0		0.0		0.0	ns
SSTL-3 Class II	Input to PIA		1.4		1.9		2.5	ns
	Input to global clock and clear		1.2		1.6		2.2	ns
	Input to fast input register		1.0		1.4		1.8	ns
	All outputs		0.0		0.0		0.0	ns
GTL+	Input to PIA		1.8		2.5		3.3	ns
	Input to global clock and clear		1.9		2.6		3.5	ns
	Input to fast input register		1.8		2.5		3.3	ns
	All outputs		0.0		0.0		0.0	ns

Table 30. EPM7512B Selectable I/O Standard Timing Adder Delays

I/O Standard	Parameter	Speed Grade						Unit
		-5		-7		-10		
		Min	Max	Min	Max	Min	Max	
PCI	Input to PIA		0.0		0.0		0.0	ns
	Input to global clock and clear		0.0		0.0		0.0	ns
	Input to fast input register		0.0		0.0		0.0	ns
	All outputs		0.0		0.0		0.0	ns

Notes to tables:

(1) These values are specified under the Recommended Operating Conditions in Table 13 on page 25.
(2) MAX 7000B timing values are preliminary.
(3) These values are specified for a PIA fan-out of one LAB (16 macrocells). For each additional LAB fan-out in these devices, add an additional 0.1 ns to the PIA timing value.
(4) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(5) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{CPPW}, t_{EN}, and t_{SEXP} parameters for macrocells running in low-power mode.

Power Consumption

Supply power (P) versus frequency ($\mathbf{f_{MAX}}$, in MHz) for MAX 7000B devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)*.

The I_{CCINT} value depends on the switching frequency and the application logic. The I_{CCINT} value is calculated with the following equation:

$$I_{CCINT} = (A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$$

The parameters in this equation are:

MC_{TON} = Number of macrocells with the Turbo Bit™ option turned on, as reported in the MAX+PLUS II Report File (**.rpt**)
MC_{DEV} = Number of macrocells in the device
MC_{USED} = Total number of macrocells in the design, as reported in the Report File
$\mathbf{f_{MAX}}$ = Highest clock frequency to the device
$\mathbf{tog_{LC}}$ = Average percentage of logic cells toggling at each clock (typically 12.5%)
A, B, C = Constants, shown in Table 31

Table 31. MAX 7000B I_{CC} Equation Constants

Device	A	B	C
EPM7032B	0.91	0.54	0.010
EPM7064B	0.91	0.54	0.012
EPM7128B	0.91	0.54	0.016
EPM7256B	0.91	0.54	0.017
EPM7512B	0.91	0.54	0.019

This calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 15. I_{CC} vs. Frequency for EPM7032B Devices

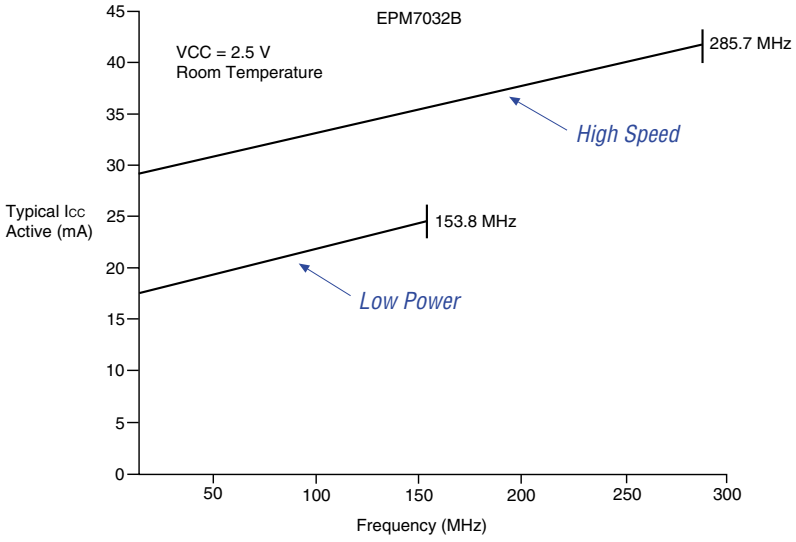


Figure 16. I_{CC} vs. Frequency for EPM7064B Devices

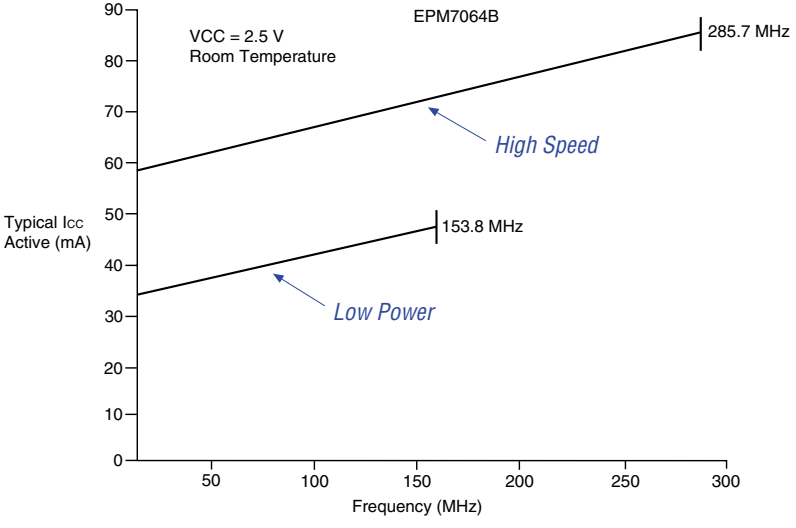


Figure 17. I_{CC} vs. Frequency for EPM7128B Devices

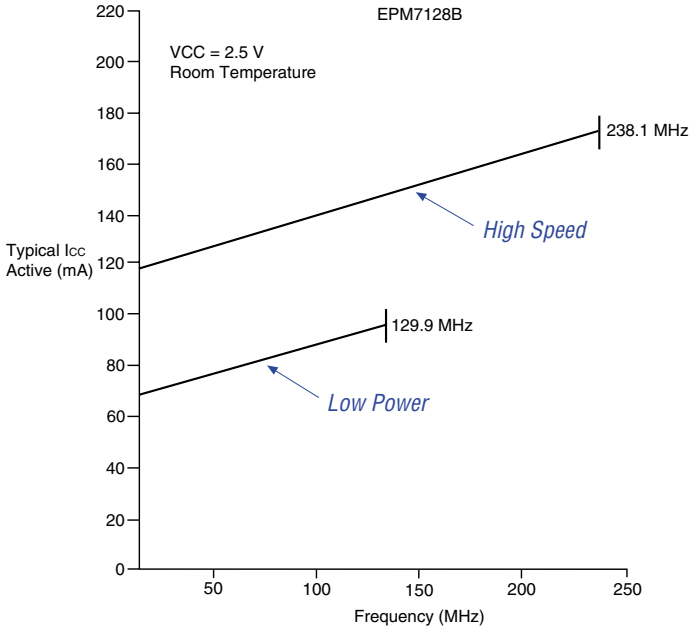


Figure 18. I_{CC} vs. Frequency for EPM7256B Devices

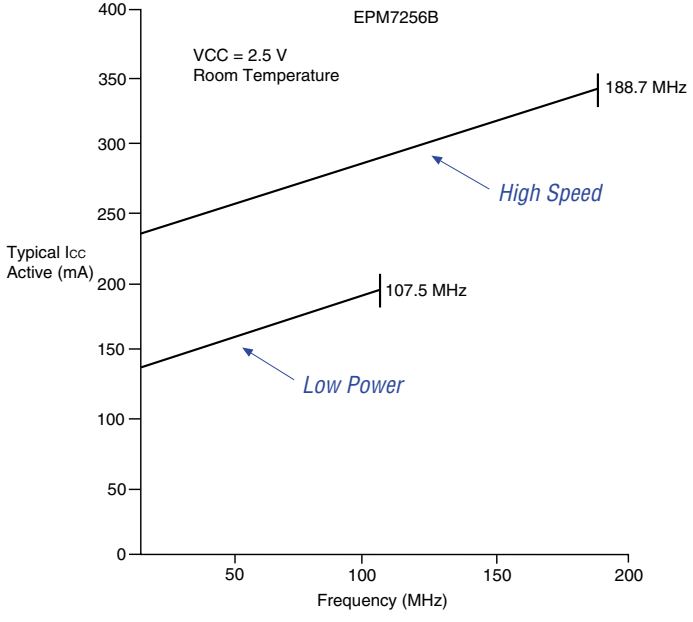
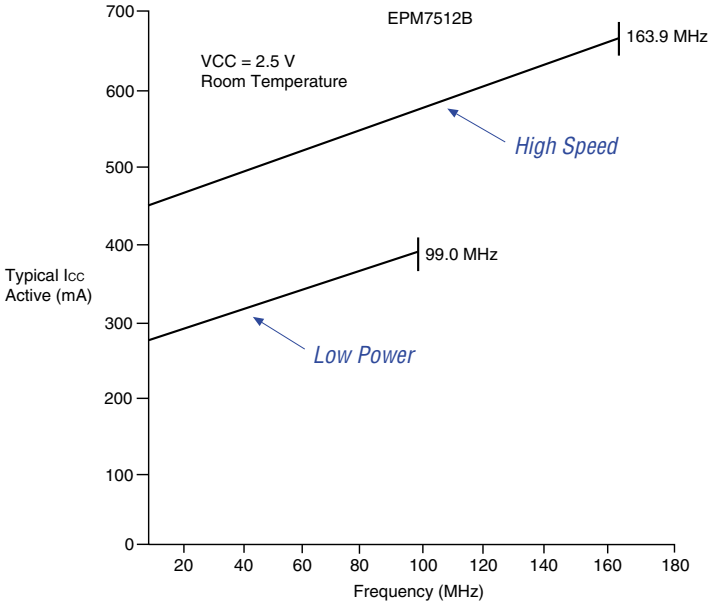


Figure 19. I_{CC} vs. Frequency for EPM7512B Devices



Device Pin-Outs

Tables 32 through 44 show the pin names and numbers for MAX 7000B device packages.

Table 32. EPM7032B Dedicated Pin-Outs

Dedicated Pin	44-Pin PLCC	44-Pin TQFP	48-Pin VTQFP	49-Pin Ultra FineLine BGA
INPUT/GCLK1	43	37	41	A5
INPUT/GCLRn	1	39	43	A3
INPUT/OE1	44	38	42	A4
INPUT/OE2/GCLK2	2	40	44	B4
TDI *(1)*	7	1	2	B1
TMS *(1)*	13	7	8	F1
TCK *(1)*	32	26	29	F7
TDO *(1)*	38	32	35	B7
VREFA *(2)*	11	5	6	D1
VREFB *(2)*	31	25	28	E7
GNDINT	22, 42	16, 36	18, 40	B5, F4
GNDIO	10, 30	4, 24	5, 27	C2, E6
VCCINT (2.5 V)	3, 23	17, 41	19, 45	B3, E4
VCCIO1 (1.8 V, 2.5 V, or 3.3 V)	15	9	10	E2
VCCIO2 (1.8 V, 2.5 V, or 3.3 V)	35	29	32	C6
No Connect (N.C.)	–	–	1, 13, 24, 37	D2, D3, D4, D5, D6
Total User I/O Pins *(3)*	36	36	36	36

Table 33. EPM7032B I/O Pin–Outs & I/O Standards

LAB	MC	44-Pin PLCC	44-Pin TQFP	48-Pin VTQFP	49-Pin Ultra FineLine BGA	IOGND Groups (200 mA)	IOVCC Groups (100 mA)	I/O Bank
A	1	4	42	46	C3	A	A	1
	2	5	43	47	A2	A	A	1
	3	6	44	48	A1	A	A	1
	4	7 *(1)*	1 *(1)*	2 *(1)*	B1 *(1)*	A	A	1
	5	8	2	3	B2	A	A	1
	6	9	3	4	C1	A	A	1
	7	11 *(2)*	5 *(2)*	6 *(2)*	D1 *(2)*	B	A	1
	8	12	6	7	E1	B	A	1
	9	13 *(1)*	7 *(1)*	8 *(1)*	F1 *(1)*	B	A	1
	10	14	8	9	F2	B	A	1
	11	16	10	11	G1	B	B	1
	12	17	11	12	G2	B	B	1
	13	18	12	14	F3	B	B	1
	14	19	13	15	G3	B	B	1
	15	20	14	16	E3	B	B	1
	16	21	15	17	G4	B	B	1
B	17	41	35	39	C4	A	D	2
	18	40	34	38	C5	A	D	2
	19	39	33	36	A6	A	D	2
	20	38 *(1)*	32 *(1)*	35 *(1)*	B7 *(1)*	A	D	2
	21	37	31	34	A7	A	D	2
	22	36	30	33	B6	A	D	2
	23	34	28	31	C7	A	C	2
	24	33	27	30	D7	A	C	2
	25	32 *(1)*	26 *(1)*	29 *(1)*	F7 *(1)*	A	C	2
	26	31 *(2)*	25 *(2)*	28 *(2)*	E7 *(2)*	A	C	2
	27	29	23	26	F6	B	C	2
	28	28	22	25	G7	B	C	2
	29	27	21	23	G6	B	C	2
	30	26	20	22	F5	B	C	2
	31	25	19	21	G5	B	C	2
	32	24	18	20	E5	B	C	2

Notes to tables:

(1) This pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for in-system programming, this pin is not available as a user I/O pin.

(2) This pin may function as either a VREF pin or a user I/O pin. If this pin is programmed to be a VREF pin for using the advanced I/O standards, this pin is not available as a user I/O pin.

(3) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 34. EPM7064B Dedicated Pin-Outs

Dedicated Pin	44-Pin PLCC	44-Pin TQFP	48-Pin VTQFP	49-Pin Ultra FineLine BGA	100-Pin TQFP	100-Pin FineLine BGA
INPUT/GCLK1	43	37	41	A5	87	A6
INPUT/GCLRN	1	39	43	A3	89	B5
INPUT/OE1	44	38	42	A4	88	B6
INPUT/OE2/GCLK2	2	40	44	B4	90	A5
TDI *(1)*	7	1	2	B1	4	A1
TMS *(1)*	13	7	8	F1	15	F3
TCK *(1)*	32	26	29	F7	62	F8
TDO *(1)*	38	32	35	B7	73	A10
VREFA *(2)*	11	5	6	D1	12	F1
VREFB *(2)*	31	25	28	E7	60	E8
GNDINT	22, 42	16, 36	18, 40	B5, F4	38, 86	D6, G5
GNDIO	10, 30	4, 24	5, 27	C2, E6	11, 26, 43, 59, 74, 95	C3, D7, E5, F6, G4, H8
VCCINT (2.5 V)	3, 23	17, 41	19, 45	B3, E4	39, 91	D5, G6
VCCIO1 (1.8 V, 2.5V, 3.3V)	15	9	10	E2	3, 18, 34	D4, F5, H3
VCCIO2 (1.8 V, 2.5V, 3.3V)	35	29	32	C6	51, 66, 82	C8, E6, G7
No Connect	–	–	–	–	1, 2, 5, 7, 22, 24, 27, 28, 49, 50, 53, 55, 70, 72, 77, 78	B1, B10, C1, C9, C10, D8, E3, E4, H1, H9, H10, J1, J2, J10, K1, K9
Total User I/O Pins *(3)*	36	36	40	41	68	68

Table 35. EPM7064B I/O Pins & I/O Standards (Part 1 of 2)

LAB	MC	44-Pin PLCC	44-Pin TQFP	48-Pin VTQFP	IOGND Group (200 mA)	IOVCC Group (100 mA)	I/O Bank
A	1	12	6	7	B	A	1
	2	–	–	–	–	–	1
	3	11 *(2)*	5 *(2)*	6 *(2)*	B	A	1
	4	9	3	4	A	A	1
	5	8	2	3	A	A	1
	6	–	–	–	–	–	1
	7	–	–	–	–	–	1
	8	7 *(1)*	1 *(1)*	2 *(1)*	A	A	1
	9	–	–	1	A	A	1
	10	–	–	–	–	–	1
	11	6	44	48	A	A	1
	12	–	–	–	–	–	1
	13	–	–	–	–	–	1
	14	5	43	47	A	A	1
	15	–	–	–	–	–	1
	16	4	42	46	A	A	1
B	17	21	15	17	B	B	1
	18	–	–	–	–	–	1
	19	20	14	16	B	B	1
	20	19	13	15	B	B	1
	21	18	12	14	B	B	1
	22	–	–	13	B	B	1
	23	–	–	–	–	–	1
	24	17	11	12	B	B	1
	25	16	10	11	B	B	1
	26	–	–	–	–	–	1
	27	–	–	–	–	–	1
	28	–	–	–	–	–	1
	29	–	–	–	–	–	1
	30	14	8	9	B	A	1
	31	–	–	–	–	–	1
	32	13 *(1)*	7 *(1)*	8 *(1)*	B	A	1

Table 35. EPM7064B I/O Pins & I/O Standards (Part 2 of 2)

LAB	MC	44-Pin PLCC	44-Pin TQFP	48-Pin VTQFP	IOGND Group (200 mA)	IOVCC Group (100 mA)	I/O Bank
C	33	24	18	20	B	C	2
	34	–	–	–	–	–	2
	35	25	19	21	B	C	2
	36	26	20	22	B	C	2
	37	27	21	23	B	C	2
	38	–	–	–	–	–	2
	39	–	–	24	B	C	2
	40	28	22	25	B	C	2
	41	29	23	26	B	C	2
	42	–	–	–	–	–	2
	43	–	–	–	–	–	2
	44	–	–	–	–	–	2
	45	–	–	–	–	–	2
	46	31 *(2)*	25 *(2)*	28 *(2)*	A	C	2
	47	–	–	–	–	–	2
	48	32 *(1)*	26 *(1)*	29 *(1)*	A	C	2
D	49	33	27	30	A	C	2
	50	–	–	–	–	–	2
	51	34	28	31	A	C	2
	52	36	30	33	A	D	2
	53	37	31	34	A	D	2
	54	–	–	–	–	–	2
	55	–	–	–	–	–	2
	56	38 *(1)*	32 *(1)*	35 *(1)*	A	D	2
	57	39	33	36	A	D	2
	58	–	–	–	–	–	2
	59	–	–	37	A	D	2
	60	–	–	–	–	–	2
	61	–	–	–	–	–	2
	62	40	34	38	A	D	2
	63	–	–	–	–	–	2
	64	41	35	39	A	D	2

Notes to tables:

(1) This pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for in-system programming, this pin is not available as a user I/O pin.

(2) This pin may function as either a VREF pin or a user I/O pin. If this pin is programmed to be a VREF pin for using the advanced I/O standards, this pin is not available as a user I/O pin.

(3) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 36. EPM7064B I/O Pins & I/O Standards (Part 1 of 3)

LAB	MC	49-Pin Ultra FineLine BGA	100-Pin TQFP	100-Pin FineLine BGA	IOGND Group (200 mA)	IOVCC Group	I/O Bank
A	1	D2	14	F4	C	B (200 mA)	1
	2	–	13	E2	C	B (200 mA)	1
	3	D1 *(2)*	12 *(2)*	E1	C	B (200 mA)	1
	4	D4	10	D2	B	B (200 mA)	1
	5	C1	9	D1	B	B (200 mA)	1
	6	–	8	D3	B	B (200 mA)	1
	7	–	6	C2	B	B (200 mA)	1
	8	B1 *(1)*	4 *(1)*	A1 *(1)*	B	B (200 mA)	1
	9	B2	100	B2	B	A (100 mA)	1
	10	–	99	A2	B	A (100 mA)	1
	11	A1	98	A3	B	A (100 mA)	1
	12	–	97	B3	B	A (100 mA)	1
	13	–	96	A4	B	A (100 mA)	1
	14	A2	94	B4	A	A (100 mA)	1
	15	–	93	C4	A	A (100 mA)	1
	16	C3	92	C5	A	A (100 mA)	1

Table 36. EPM7064B I/O Pins & I/O Standards (Part 2 of 3)

LAB	MC	49-Pin Ultra FineLine BGA	100-Pin TQFP	100-Pin FineLine BGA	IOGND Group (200 mA)	IOVCC Group	I/O Bank
B	17	G4	37	K5	D	D (100 mA)	1
	18	E3	36	J5	D	D (100 mA)	1
	19	G3	35	H5	D	D (100 mA)	1
	20	F3	33	K4	D	C (200 mA)	1
	21	G2	32	J4	D	C (200 mA)	1
	22	G1	31	H4	D	C (200 mA)	1
	23	–	30	J3	D	C (200 mA)	1
	24	F2	29	K3	D	C (200 mA)	1
	25	D3	25	K2	C	C (200 mA)	1
	26	–	23	H2	C	C (200 mA)	1
	27	–	21	G2	C	C (200 mA)	1
	28	–	20	G1	C	C (200 mA)	1
	29	–	19	G3	C	C (200 mA)	1
	30	E1	17	F2	C	B (200 mA)	1
	31	–	16	F1 *(2)*	C	B (200 mA)	1
	32	F1 *(1)*	15 *(1)*	F3 *(1)*	C	B (200 mA)	1
C	33	E5	40	K6	D	E (100 mA)	2
	34	–	41	J6	D	E (100 mA)	2
	35	G5	42	H6	D	E (100 mA)	2
	36	F5	44	K7	E	E (100 mA)	2
	37	G6	45	J7	E	E (100 mA)	2
	38	–	46	H7	E	E (100 mA)	2
	39	G7	47	J8	E	E (100 mA)	2
	40	F6	48	K8	E	E (100 mA)	2
	41	D5	52	K10	E	F (200 mA)	2
	42	–	54	J9	E	F (200 mA)	2
	43	–	56	G9	E	F (200 mA)	2
	44	–	57	G10	E	F (200 mA)	2
	45	–	58	G8	E	F (200 mA)	2
	46	E7 *(2)*	60 *(2)*	F9	F	F (200 mA)	2
	47	–	61	F10	F	F (200 mA)	2
	48	F7 *(1)*	62 *(1)*	F8 *(1)*	F	F (200 mA)	2

Table 36. EPM7064B I/O Pins & I/O Standards (Part 3 of 3)

LAB	MC	49-Pin Ultra FineLine BGA	100-Pin TQFP	100-Pin FineLine BGA	IOGND Group (200 mA)	IOVCC Group	I/O Bank
D	49	D7	63	F7	F	F (200 mA)	2
	50	–	64	E9	F	F (200 mA)	2
	51	D6	65	E10	F	F (200 mA)	2
	52	C7	67	E8 *(2)*	F	G (200 mA)	2
	53	B6	68	E7	F	G (200 mA)	2
	54	–	69	D9	F	G (200 mA)	2
	55	–	71	D10	F	G (200 mA)	2
	56	B7 *(1)*	73 *(1)*	A10 *(1)*	F	G (200 mA)	2
	57	A7	75	B9	A	G (200 mA)	2
	58	–	76	A9	A	G (200 mA)	2
	59	A6	79	A8	A	G (200 mA)	2
	60	–	80	B8	A	G (200 mA)	2
	61	–	81	A7	A	G (200 mA)	2
	62	C5	83	B7	A	H (100 mA)	2
	63	–	84	C7	A	H (100 mA)	2
	64	C4	85	C6	A	H (100 mA)	2

Notes to tables:

(1) This pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for in-system programming, this pin is not available as a user I/O pin.

(2) This pin may function as either a VREF pin or a user I/O pin. If this pin is programmed to be a VREF pin for using the advanced I/O standards, then this pin is not available as a user I/O pin.

(3) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 37. EPM7128B Dedicated Pin-Outs (Part 1 of 2)

Dedicated Pin	48-Pin VTQFP	49-Pin Ultra FineLine BGA	100-Pin TQFP	100-Pin FineLine BGA	144-Pin TQFP	169-Pin Ultra FineLine BGA	256-Pin FineLine BGA
INPUT/GCLK1	41	A5	87	A6	125	D8	D9
INPUT/GCLRn	43	A3	89	B5	127	D6	E8
INPUT/OE1	42	A4	88	B6	126	D7	E9
INPUT/OE2/GCLK2	44	B4	90	A5	128	E7	D8
TDI *(1)*	2	B1	4	A1	4	E4	D4
TMS *(1)*	8	F1	15	F3	20	J4	J6
TCK *(1)*	29	F7	62	F8	89	J10	J11
TDO *(1)*	35	B7	73	A10	104	E10	D13
VREFA *(2)*	6	D1	12	F1	14	G4	J4
VREFB *(2)*	28	E7	60	E8	87	H10	H11
GNDINT	18, 40	B5, F4	38, 86	D6, G5	52, 57, 124, 129	A7, E8, J7, N7	A8, C9, G9, K8, P9
GNDIO	5, 27	C2, E6	11, 26, 43, 59, 74, 95	C3, D7, E5, F6, G4, H8	3, 13, 17, 33, 59, 64, 85, 105, 135	A3, A12, E1, F5, F13, H1, H9, J13, N2, N11	A3, B10, C2, D14, F6, G10, H8, J9, K7, L11, M3, P6, P10, R2, R3, T1, T15
VCCINT (2.5 V Only)	19, 45	B3, E4	39, 91	D5, G6	51, 58, 123, 130	B7, E6, H7, M7	B9, C8, G8, K9, P8
VCCIO1 (1.8 V, 2.5 V, or 3.3 V)	10	E2	3, 18, 34	D4, F5, H3	24, 50, 144	A2, F1, H5, J1, N3	B3, B5, G3, G7, J8, L3, L6, T2, T3
VCCIO2 (1.8 V, 2.5 V, or 3.3 V)	32	C6	51, 66, 82	C8, E6, G7	73, 76, 95, 115	A11, E13, F9, H13, N12	C14, E15, F11, G15, H9, K10, M15, P14

Table 37. EPM7128B Dedicated Pin-Outs (Part 2 of 2)

Dedicated Pin	48-Pin VTQFP	49-Pin Ultra FineLine BGA	100-Pin TQFP	100-Pin FineLine BGA	144-Pin TQFP	169-Pin Ultra FineLine BGA	256-Pin FineLine BGA
No Connect (N.C.)	–	–	–	–	1, 2, 12, 19, 34, 35, 36, 43, 46, 47, 48, 49, 66, 75, 90, 103, 108, 120, 121, 122	B5, B6, B8, B9, C5, C6, C7, C8, C9, C10, E2, E3, E11, E12, F2, F3, F11, F12, G1, G2, G3, G11, G12, H2, H3, H11, H12, J2, J3, J11, J12, L4, L5, L6, L7, L8, L9, M5, M6, M8, M9	A1, A2, A4, A5, A6, A7, A9, A10, A11, A12, A13, A14, A15, A16, B1, B2, B4, B6, B7, B8, B11, B12, B13, B14, B 15, B16, C1, C3, C4, C6, C11, C13, C15, C16, D1, D2, D3, D15, D16, E1, E2, E3, E14, E16, F1, F2, F15, F16, G1, G2, G14, G16, H1, H2, H15, H16, J1, J2, J15, J16, K1, K2, K3, K14, K15, K16, L1, L2, L15, L16, M1, M14, M16, N1, N2, N3, N14, N15, N16,
Total User I/O Pins *(3)*	40	41	84	84	100	100	100

Table 38. EPM7128B I/O Pins & I/O Standard Groups (Part 1 of 4)

LAB	MC	48-Pin VTQFP	IOGND Group for 48-Pin VTQFP (200 mA)	IOVCC Group for 48-Pin VTQFP (100 mA)	I/O Bank
A	1	1	A	A	1
	2	–	–	–	1
	3	48	A	A	1
	4	–	–	–	1
	5	–	–	–	1
	6	–	–	–	1
	7	–	–	–	1
	8	–	–	–	1
	9	–	–	–	1
	10	–	–	–	1
	11	47	A	A	1
	12	–	–	–	1
	13	46	A	A	1
	14	–	–	–	1
	15	–	–	–	1
	16	–	–	–	1
B	17	–	–	–	1
	18	–	–	–	1
	19	7	B	A	1
	20	–	–	–	1
	21	6 *(2)*	B	A	1
	22	–	–	–	1
	23	–	–	–	1
	24	–	–	–	1
	25	–	–	–	1
	26	–	–	–	1
	27	4	A	A	1
	28	–	–	–	1
	29	3	A	A	1
	30	–	–	–	1
	31	–	–	–	1
	32	2 *(1)*	A	A	1

Table 38. EPM7128B I/O Pins & I/O Standard Groups (Part 2 of 4)

LAB	MC	48-Pin VTQFP	IOGND Group for 48-Pin VTQFP (200 mA)	IOVCC Group for 48-Pin VTQFP (100 mA)	I/O Bank
C	33	13	B	B	1
	34	–	–	–	1
	35	12	B	B	1
	36	–	–	–	1
	37	–	–	–	1
	38	–	–	–	1
	39	–	–	–	1
	40	–	–	–	1
	41	–	–	–	1
	42	–	–	–	1
	43	11	B	B	1
	44	–	–	–	1
	45	9	B	A	1
	46	–	–	–	1
	47	–	–	–	1
	48	8 *(1)*	B	A	1
D	49	–	–	–	1
	50	–	–	–	1
	51	17	B	B	1
	52	–	–	–	1
	53	–	–	–	1
	54	–	–	–	1
	55	–	–	–	1
	56	16	B	B	1
	57	–	–	–	1
	58	–	–	–	1
	59	15	B	B	1
	60	–	–	–	1
	61	–	–	–	1
	62	–	–	–	1
	63	–	–	–	1
	64	14	B	B	1

Table 38. EPM7128B I/O Pins & I/O Standard Groups (Part 3 of 4)

LAB	MC	48-Pin VTQFP	IOGND Group for 48-Pin VTQFP (200 mA)	IOVCC Group for 48-Pin VTQFP (100 mA)	I/O Bank
E	65	–	–	–	2
	66	–	–	–	2
	67	20	B	C	2
	68	–	–	–	2
	69	21	B	C	2
	70	–	–	–	2
	71	–	–	–	2
	72	22	B	C	2
	73	–	–	–	2
	74	–	–	–	2
	75	23	B	C	2
	76	–	–	–	2
	77	24	B	C	2
	78	–	–	–	2
	79	–	–	–	2
	80	–	–	–	2
F	81	–	–	–	2
	82	–	–	–	2
	83	25	B	C	2
	84	–	–	–	2
	85	–	–	–	2
	86	–	–	–	2
	87	–	–	–	2
	88	–	–	–	2
	89	–	–	–	2
	90	–	–	–	2
	91	26	B	C	2
	92	–	–	–	2
	93	28 *(2)*	A	C	2
	94	–	–	–	2
	95	–	–	–	2
	96	29 *(1)*	A	C	2

Table 38. EPM7128B I/O Pins & I/O Standard Groups (Part 4 of 4)

LAB	MC	48-Pin VTQFP	IOGND Group for 48-Pin VTQFP (200 mA)	IOVCC Group for 48-Pin VTQFP (100 mA)	I/O Bank
G	97	–	–	–	2
	98	–	–	–	2
	99	30	A	C	2
	100	–	–	–	2
	101	31	A	C	2
	102	–	–	–	2
	103	–	–	–	2
	104	–	–	–	2
	105	–	–	–	2
	106	–	–	–	2
	107	33	A	D	2
	108	–	–	–	2
	109	34	A	D	2
	110	–	–	–	2
	111	–	–	–	2
	112	35 *(1)*	A	D	2
H	113	–	–	–	2
	114	–	–	–	2
	115	36	A	D	2
	116	–	–	–	2
	117	37	A	D	2
	118	–	–	–	2
	119	–	–	–	2
	120	–	–	–	2
	121	–	–	–	2
	122	–	–	–	2
	123	38	A	D	2
	124	–	–	–	2
	125	39	A	D	2
	126	–	–	–	2
	127	–	–	–	2
	128	–	–	–	2

Table 39. EPM7128B I/O Pins & I/O Standard Groups (Part 1 of 4)

LAB	MC	49-Pin Ultra FineLine BGA	100-Pin TQFP	100-Pin FineLine BGA	144-Pin TQFP	169-Pin Ultra FineLine BGA	256-Pin FineLine BGA	IOGND Group for Other Packages (200 mA)	IOVCC Group for Other Packages	I/O Bank
A	1	B2	2	C1	143	E5	F4	B	A (100 mA)	1
	2	–	–	–	–	–	–	–	–	1
	3	A1	1	B1	142	D4	E4	B	A (100 mA)	1
	4	–	–	–	141	B2	C5	B	A (100 mA)	1
	5	–	100	B2	140	B3	E5	B	A (100 mA)	1
	6	–	99	A2	139	C3	D5	B	A (100 mA)	1
	7	–	–	–	–	–	–	–	–	1
	8	–	98	A3	138	C4	D6	B	A (100 mA)	1
	9	–	97	B3	137	B4	E6	B	A (100 mA)	1
	10	–	–	–	–	–	–	–	–	1
	11	A2	96	A4	136	A4	D7	B	A (100 mA)	1
	12	–	–	–	134	D5	C7	A	A (100 mA)	1
	13	C3	94	B4	133	A5	E7	A	A (100 mA)	1
	14	–	93	C4	132	F6	F7	A	A (100 mA)	1
	15	–	–	–	–	–	–	–	–	1
	16	–	92	C5	131	A6	F8	A	A (100 mA)	1
B	17	–	14	F4	18	D1	J7	C	B (200 mA)	1
	18	–	–	–	–	–	–	–	–	1
	19	D2	13	E2	16	G5	H5	C	B (200 mA)	1
	20	–	–	–	15	D2	H3	C	B (200 mA)	1
	21	D1 *(2)*	12 *(2)*	E1	14 *(2)*	G4 *(2)*	H4	C	B (200 mA)	1
	22	–	10	E3	11	D3	H6	B	B (200 mA)	1
	23	–	–	–	–	–	–	–	–	1
	24	–	9	E4	10	C1	H7	B	B (200 mA)	1
	25	–	8	D2	9	C2	G5	B	B (200 mA)	1
	26	–	–	–	–	–	–	–	–	1
	27	D4	7	D1	8	G7	G4	B	B (200 mA)	1
	28	–	–	–	7	B1	F3	B	B (200 mA)	1
	29	C1	6	D3	6	F4	G6	B	B (200 mA)	1
	30	–	5	C2	5	A1	F5	B	B (200 mA)	1
	31	–	–	–	–	–	–	–	–	1
	32	B1 *(1)*	4 *(1)*	A1 *(1)*	4 *(1)*	E4 *(1)*	D4 *(1)*	B	B (200 mA)	1

Table 39. EPM7128B I/O Pins & I/O Standard Groups (Part 2 of 4)

LAB	MC	49-Pin Ultra FineLine BGA	100-Pin TQFP	100-Pin FineLine BGA	144-Pin TQFP	169-Pin Ultra FineLine BGA	256-Pin FineLine BGA	IOGND Group for Other Packages (200 mA)	IOVCC Group for Other Packages	I/O Bank
C	33	G1	25	K1	32	K4	N4	C	C (200 mA)	1
	34	–	–	–	–	–	–	–	–	1
	35	F2	24	J1	31	J5	M4	C	C (200 mA)	1
	36	–	–	–	30	N1	M2	C	C (200 mA)	1
	37	–	23	H1	29	M1	L4	C	C (200 mA)	1
	38	–	22	H2	28	L1	L5	C	C (200 mA)	1
	39	–	–	–	–	–	–	–	–	1
	40	–	21	G2	27	L2	K5	C	C (200 mA)	1
	41	–	20	G1	26	K3	K4	C	C (200 mA)	1
	42	–	–	–	–	–	–	–	–	1
	43	D3	19	G3	25	G6	K6	C	C (200 mA)	1
	44	–	–	–	23	K2	J3	C	B (200 mA)	1
	45	E1	17	F2	22	H4	J5	C	B (200 mA)	1
	46	–	16	F1 *(2)*	21	K1	J4 *(2)*	C	B (200 mA)	1
	47	–	–	–	–	–	–	–	–	1
	48	F1 *(1)*	15 *(1)*	F3 *(1)*	20 *(1)*	J4 *(1)*	J6 *(1)*	C	B (200 mA)	1
D	49	–	37	K5	56	N6	N8	D	D (100 mA)	1
	50	–	–	–	–	–	–	–	–	1
	51	G4	36	J5	55	K7	M8	D	D (100 mA)	1
	52	–	–	–	54	N5	P7	D	D (100 mA)	1
	53	E3	35	H5	53	H6	L8	D	D (100 mA)	1
	54	–	33	K4	45	N4	N7	D	C (200 mA)	1
	55	–	–	–	–	–	–	–	–	1
	56	G3	32	J4	44	K6	M7	D	C (200 mA)	1
	57	–	31	H4	42	M4	L7	D	C (200 mA)	1
	58	–	–	–	–	–	–	–	–	1
	59	F3	30	J3	41	J6	M6	D	C (200 mA)	1
	60	–	–	–	40	M3	P5	D	C (200 mA)	1
	61	–	29	K3	39	L3	N6	D	C (200 mA)	1
	62	–	28	J2	38	M2	M5	D	C (200 mA)	1
	63	–	–	–	–	–	–	–	–	1
	64	G2	27	K2	37	K5	N5	D	C (200 mA)	1

Table 39. EPM7128B I/O Pins & I/O Standard Groups (Part 3 of 4)

LAB	MC	49-Pin Ultra FineLine BGA	100-Pin TQFP	100-Pin FineLine BGA	144-Pin TQFP	169-Pin Ultra FineLine BGA	256-Pin FineLine BGA	IOGND Group for Other Packages (200 mA)	IOVCC Group for Other Packages	I/O Bank
E	65	–	40	K6	60	L10	N9	D	E (100 mA)	2
	66	–	–	–	–	–	–	–	–	2
	67	E5	41	J6	61	H8	M9	D	E (100 mA)	2
	68	–	–	–	62	N8	R10	D	E (100 mA)	2
	69	G5	42	H6	63	K8	L9	D	E (100 mA)	2
	70	–	44	K7	65	N9	N10	E	E (100 mA)	2
	71	–	–	–	–	–	–	–	–	2
	72	F5	45	J7	67	J8	M10	E	E (100 mA)	2
	73	–	46	H7	68	M10	L10	E	E (100 mA)	2
	74	–	–	–	–	–	–	–	–	2
	75	G6	47	J8	69	K9	M11	E	E (100 mA)	2
	76	–	–	–	70	N10	P11	E	E (100 mA)	2
	77	G7	48	K8	71	K10	N11	E	E (100 mA)	2
	78	–	49	K9	72	L11	N12	E	E (100 mA)	2
	79	–	–	–	–	–	–	–	–	2
	80	–	50	K10	74	M11	N13	E	E (100 mA)	2
F	81	–	52	J10	77	M12	M13	E	F (200 mA)	2
	82	–	–	–	–	–	–	–	–	2
	83	F6	53	H10	78	J9	L13	E	F (200 mA)	2
	84	–	–	–	79	N13	L14	E	F (200 mA)	2
	85	–	54	H9	80	M13	L12	E	F (200 mA)	2
	86	–	55	J9	81	L13	M12	E	F (200 mA)	2
	87	–	–	–	–	–	–	–	–	2
	88	–	56	G9	82	L12	K12	E	F (200 mA)	2
	89	–	57	G10	83	K13	K13	E	F (200 mA)	2
	90	–	–	–	–	–	–	–	–	2
	91	D5	58	G8	84	G8	K11	E	F (200 mA)	2
	92	–	–	–	86	K12	J14	F	F (200 mA)	2
	93	E7 *(2)*	60 *(2)*	F9	87 *(2)*	H10 *(2)*	J12	F	F (200 mA)	2
	94	–	61	F10	88	K11	J13	F	F (200 mA)	2
	95	–	–	–	–	–	–	–	–	2
	96	F7 *(1)*	62 *(1)*	F8 *(1)*	89 *(1)*	J10 *(1)*	J11 *(1)*	F	F (200 mA)	2

Table 39. EPM7128B I/O Pins & I/O Standard Groups (Part 4 of 4)

LAB	MC	49-Pin Ultra FineLine BGA	100-Pin TQFP	100-Pin FineLine BGA	144-Pin TQFP	169-Pin Ultra FineLine BGA	256-Pin FineLine BGA	IOGND Group for Other Packages (200 mA)	IOVCC Group for Other Packages	I/O Bank
G	97	–	63	F7	91	G13	J10	F	F (200 mA)	2
	98	–	–	–	–	–	–	–	–	2
	99	D7	64	E9	92	G10	H12	F	F (200 mA)	2
	100	–	–	–	93	D13	H14	F	F (200 mA)	2
	101	D6	65	E10	94	G9	H13	F	F (200 mA)	2
	102	–	67	E8 *(2)*	96	D12	H11 *(2)*	F	G (200 mA)	2
	103	–	–	–	–	–	–	–	–	2
	104	–	68	E7	97	D11	H10	F	G (200 mA)	2
	105	–	69	D9	98	C13	G12	F	G (200 mA)	2
	106	–	–	–	–	–	–	–	–	2
	107	C7	70	D10	99	F10	G13	F	G (200 mA)	2
	108	–	–	–	100	C12	F14	F	G (200 mA)	2
	109	B6	71	D8	101	E9	G11	F	G (200 mA)	2
	110	–	72	C9	102	B13	F12	F	G (200 mA)	2
	111	–	–	–	–	–	–	–	–	2
	112	B7 *(1)*	73 *(1)*	A10 *(1)*	104 *(1)*	E10 *(1)*	D13 *(1)*	F	G (200 mA)	2
H	113	–	75	C10	106	A13	F13	A	G (200 mA)	2
	114	–	–	–	–	–	–	–	–	2
	115	A7	76	B10	107	D10	E13	A	G (200 mA)	2
	116	–	–	–	109	B12	C12	A	G (200 mA)	2
	117	A6	77	B9	110	D9	E12	A	G (200 mA)	2
	118	–	78	A9	111	C11	D12	A	G (200 mA)	2
	119	–	–	–	–	–	–	–	–	2
	120	–	79	A8	112	B11	D11	A	G (200 mA)	2
	121	–	80	B8	113	B10	E11	A	G (200 mA)	2
	122	–	–	–	–	–	–	–	–	2
	123	C5	81	A7	114	F8	D10	A	G (200 mA)	2
	124	–	–	–	116	A10	C10	A	H (100 mA)	2
	125	C4	83	B7	117	F7	E10	A	H (100 mA)	2
	126	–	84	C7	118	A9	F10	A	H (100 mA)	2
	127	–	–	–	–	–	–	–	–	2
	128	–	85	C6	119	A8	F9	A	H (100 mA)	2

Notes to tables:

(1) This pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for in-system programming, this pin is not available as a user I/O pin.

(2) This pin may function as either a VREF pin or a user I/O pin. If this pin is programmed to be a VREF pin for using the advanced I/O standards, then this pin is not available as a user I/O pin.

(3) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 40. EPM7256B Dedicated Pin-Outs

Dedicated Pin	100-Pin TQFP	144-Pin TQFP	169-Pin Ultra FineLine BGA	208-Pin PQFP	256-Pin FineLine BGA
INPUT/GCLK1	87	125	D8	184	D9
INPUT/GCLRn	89	127	D6	182	E8
INPUT/OE1	88	126	D7	183	E9
INPUT/OE2/GCLK2	90	128	E7	181	D8
TDI *(1)*	4	4	E4	176	D4
TMS *(1)*	15	20	J4	127	J6
TCK *(1)*	62	89	J10	30	J11
TDO *(1)*	73	104	E10	189	D13
VREFA *(2)*	12	14	G4	128	J4
VREFB *(2)*	60	87	H10	22	H11
GNDINT	38, 86	52, 57, 124, 129	A7, E8, J7, N7	75, 82, 180, 185	A8, C9, G9, K8, P9
GNDIO *(2)*	11, 26, 43, 59, 74, 95	3, 13, 17, 33, 59, 64, 85, 105, 135	A3, A12, E1, F5, F13, H1, H9, J13, N2, N11	14, 32, 50, 72, 94, 116, 134, 152, 174, 200	A3, B10, C2, D14, F6, G10, H8, J9, K7, L11, M3, P6, P10, R2, R3, T1, T15
VCCINT (2.5 V Only)	39, 91	51, 58, 123, 130	B7, E6, H7, M7	74, 83, 179, 186	B9, C8, G8, K9, P8
VCCIO1 (1.8 V, 2.5 V, or 3.3 V)	3, 18, 34	24, 50, 144	A2, F1, H5, J1, N3	85, 107, 125, 143, 165	B3, B5, G3, G7, J8, L3, L6, T2, T3
VCCIO2 (1.8 V, 2.5 V, or 3.3 V)	51, 66, 82	73, 76, 95, 115	A11, E13, F9, H13, N12	5, 23, 41, 63, 191	C14, E15, F11, G15, H9, K10, M15, P14
No Connect (N.C.)	–	–	–	1, 2, 51, 52, 53, 54, 103, 104, 105, 106, 155, 156, 157, 158, 207, 208	A1, A2, A6, A12, A13, A14, A15, A16, B1, B2, B15, B16, C1, C15, C16, D1, D3, D15, D16, G1, G16, H15, H16, J1, K1, L1, L2, M1, M16, N1, N2, N14, N15, N16, P1, P2, P15, P16, R1, R14, R15, R16, T7, T8, T10, T11, T14, T16
Total User I/O Pins	84	120	141	164	164

Table 41. EPM7256B I/O Pin-Outs & I/O Standards (Part 1 of 8)

Lab	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
A	1	–	–	–	–	–	–	1
	2	–	–	–	–	–	–	1
	3	–	–	–	2	B	B (200 mA)	1
	4	–	–	–	–	–	–	1
	5	–	–	–	1	B	B (200 mA)	1
	6	–	–	–	143	B	A (100 mA)	1
	7	–	–	–	–	–	–	1
	8	2	B	A (100 mA)	–	–	–	1
	9	1	B	A (100 mA)	–	–	–	1
	10	–	–	–	–	–	–	1
	11	100	B	A (100 mA)	142	B	A (100 mA)	1
	12	–	–	–	–	–	–	1
	13	–	–	–	141	B	A (100 mA)	1
	14	99	B	A (100 mA)	140	B	A (100 mA)	1
	15	–	–	–	–	–	–	1
	16	98	B	A (100 mA)	139	B	A (100 mA)	1
B	17	–	–	–	–	–	–	1
	18	–	–	–	–	–	–	1
	19	–	–	–	10	C	B (200 mA)	1
	20	–	–	–	–	–	–	1
	21	–	–	–	9	C	B (200 mA)	1
	22	–	–	–	–	–	–	1
	23	–	–	–	–	–	–	1
	24	8	B	B (200 mA)	8	C	B (200 mA)	1
	25	7	B	B (200 mA)	7	C	B (200 mA)	1
	26	–	–	–	–	–	–	1
	27	6	B	B (200 mA)	6	C	B (200 mA)	1
	28	–	–	–	–	–	–	1
	29	5	B	B (200 mA)	5	C	B (200 mA)	1
	30	–	–	–	–	–	–	1
	31	–	–	–	–	–	–	1
	32	4 *(1)*	B	B (200 mA)	4 *(1)*	C	B (200 mA)	1

Table 41. EPM7256B I/O Pin-Outs & I/O Standards (Part 2 of 8)

Lab	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
C	33	–	–	–	36	E	C (200 mA)	1
	34	–	–	–	–	–	–	1
	35	–	–	–	35	E	C (200 mA)	1
	36	–	–	–	–	–	–	1
	37	–	–	–	34	E	C (200 mA)	1
	38	–	–	–	–	–	–	1
	39	–	–	–	–	–	–	1
	40	25	C	C (200 mA)	32	D	C (200 mA)	1
	41	24	C	C (200 mA)	31	D	C (200 mA)	1
	42	–	–	–	–	–	–	1
	43	23	C	C (200 mA)	30	D	C (200 mA)	1
	44	–	–	–	–	–	–	1
	45	22	C	C (200 mA)	29	D	C (200 mA)	1
	46	–	–	–	–	–	–	1
	47	–	–	–	–	–	–	1
	48	21	C	C (200 mA)	28	D	C (200 mA)	1
D	49	31	D	C (200 mA)	44	E	C (200 mA)	1
	50	–	–	–	–	–	–	1
	51	30	D	C (200 mA)	43	E	C (200 mA)	1
	52	–	–	–	–	–	–	1
	53	29	D	C (200 mA)	42	E	C (200 mA)	1
	54	28	D	C (200 mA)	41	E	C (200 mA)	1
	55	–	–	–	–	–	–	1
	56	–	–	–	40	E	C (200 mA)	1
	57	–	–	–	–	–	–	1
	58	–	–	–	–	–	–	1
	59	–	–	–	39	E	C (200 mA)	1
	60	–	–	–	–	–	–	1
	61	–	–	–	38	E	C (200 mA)	1
	62	–	–	–	–	–	–	1
	63	–	–	–	–	–	–	1
	64	27	D	C (200 mA)	37	E	C (200 mA)	1

Table 41. EPM7256B I/O Pin-Outs & I/O Standards (Part 3 of 8)

Lab	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
E	65	–	–	–	–	–	–	1
	66	–	–	–	–	–	–	1
	67	–	–	–	–	–	–	1
	68	–	–	–	–	–	–	1
	69	–	–	–	138	B	A (100 mA)	1
	70	–	–	–	–	–	–	1
	71	–	–	–	–	–	–	1
	72	97	B	A (100 mA)	137	B	A (100 mA)	1
	73	96	B	A (100 mA)	136	B	A (100 mA)	1
	74	–	–	–	–	–	–	1
	75	94	A	A (100 mA)	134	A	A (100 mA)	1
	76	–	–	–	–	–	–	1
	77	93	A	A (100 mA)	133	A	A (100 mA)	1
	78	–	–	–	132	A	A (100 mA)	1
	79	–	–	–	–	–	–	1
	80	92	A	A (100 mA)	131	A	A (100 mA)	1
F	81	–	–	–	–	–	–	1
	82	–	–	–	–	–	–	1
	83	–	–	–	19	D	B (200 mA)	1
	84	–	–	–	–	–	–	1
	85	–	–	–	18	D	B (200 mA)	1
	86	–	–	–	–	–	–	1
	87	–	–	–	–	–	–	1
	88	14	C	B (200 mA)	16	C	B (200 mA)	1
	89	13	C	B (200 mA)	15	C	B (200 mA)	1
	90	–	–	–	–	–	–	1
	91	12 *(2)*	C	B (200 mA)	14 *(2)*	C	B (200 mA)	1
	92	–	–	–	–	–	–	1
	93	10	B	B (200 mA)	12	C	B (200 mA)	1
	94	–	–	–	–	–	–	1
	95	–	–	–	–	–	–	1
	96	9	B	B (200 mA)	11	C	B (200 mA)	1

Table 41. EPM7256B I/O Pin-Outs & I/O Standards (Part 4 of 8)

Lab	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
G	97	–	–	–	–	–	–	1
	98	–	–	–	–	–	–	1
	99	–	–	–	27	D	C (200 mA)	1
	100	–	–	–	–	–	–	1
	101	–	–	–	26	D	C (200 mA)	1
	102	–	–	–	–	–	–	1
	103	–	–	–	–	–	–	1
	104	20	C	C (200 mA)	25	D	C (200 mA)	1
	105	19	C	C (200 mA)	23	D	B (200 mA)	1
	106	–	–	–	–	–	–	1
	107	17	C	B (200 mA)	22	D	B (200 mA)	1
	108	–	–	–	–	–	–	1
	109	16	C	B (200 mA)	21	D	B (200 mA)	1
	110	–	–	–	–	–	–	1
	111	–	–	–	–	–	–	1
	112	15 *(1)*	C	B (200 mA)	20 *(1)*	D	B (200 mA)	1
H	113	37	D	D (58 mA)	–	–	–	1
	114	–	–	–	–	–	–	1
	115	36	D	D (58 mA)	54	E	D (58 mA)	1
	116	–	–	–	–	–	–	1
	117	–	–	–	53	E	D (58 mA)	1
	118	35	D	D (58 mA)	–	–	–	1
	119	–	–	–	–	–	–	1
	120	–	–	–	49	E	C (200 mA)	1
	121	–	–	–	48	E	C (200 mA)	1
	122	–	–	–	–	–	–	1
	123	–	–	–	47	E	C (200 mA)	1
	124	–	–	–	–	–	–	1
	125	33	D	C (200 mA)	46	E	C (200 mA)	1
	126	–	–	–	–	–	–	1
	127	–	–	–	–	–	–	1
	128	32	D	C (200 mA)	45	E	C (200 mA)	1

Table 41. EPM7256B I/O Pin-Outs & I/O Standards (Part 5 of 8)

Lab	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
I	129	80	A	G (200 mA)	114	A	H (200 mA)	2
	130	–	–	–	–	–	–	2
	131	81	A	G (200 mA)	116	A	I (100 mA)	2
	132	–	–	–	–	–	–	2
	133	–	–	–	117	A	I (100 mA)	2
	134	–	–	–	–	–	–	2
	135	–	–	–	–	–	–	2
	136	–	–	–	118	A	I (100 mA)	2
	137	–	–	–	119	A	I (100 mA)	2
	138	–	–	–	–	–	–	2
	139	83	A	H (100 mA)	120	A	I (100 mA)	2
	140	–	–	–	–	–	–	2
	141	84	A	H (100 mA)	121	A	I (100 mA)	2
	142	–	–	–	–	–	–	2
	143	–	–	–	–	–	–	2
	144	85	A	H (100 mA)	122	A	I (100 mA)	2
J	145	63	F	F (200 mA)	–	–	–	2
	146	–	–	–	–	–	–	2
	147	64	F	F (200 mA)	90	H	G (200 mA)	2
	148	–	–	–	–	–	–	2
	149	65	F	F (200 mA)	91	H	G (200 mA)	2
	150	–	–	–	–	–	–	2
	151	–	–	–	–	–	–	2
	152	–	–	–	92	H	G (200 mA)	2
	153	–	–	–	93	H	G (200 mA)	2
	154	–	–	–	–	–	–	2
	155	67	F	G (200 mA)	94	H	G (200 mA)	2
	156	–	–	–	–	–	–	2
	157	–	–	–	96	H	H (200 mA)	2
	158	–	–	–	–	–	–	2
	159	–	–	–	–	–	–	2
	160	68	F	G (200 mA)	97	H	H (200 mA)	2

Table 41. EPM7256B I/O Pin-Outs & I/O Standards (Part 6 of 8)

Lab	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
K	161	–	–	–	–	–	–	2
	162	–	–	–	–	–	–	2
	163	57	E	F (200 mA)	82	G	G (200 mA)	2
	164	–	–	–	–	–	–	2
	165	–	–	–	83	G	G (200 mA)	2
	166	–	–	–	–	–	–	2
	167	–	–	–	–	–	–	2
	168	58	E	F (200 mA)	84	G	G (200 mA)	2
	169	–	–	–	86	H	G (200 mA)	2
	170	–	–	–	–	–	–	2
	171	60 *(2)*	F	F (200 mA)	87 *(2)*	H	G (200 mA)	2
	172	–	–	–	–	–	–	2
	173	61	F	F (200 mA)	88	H	G (200 mA)	2
	174	–	–	–	–	–	–	2
	175	–	–	–	–	–	–	2
	176	62 *(1)*	F	F (200 mA)	89 *(1)*	H	G (100 mA)	2
L	177	–	–	–	–	–	–	1
	178	–	–	–	–	–	–	1
	179	–	–	–	55	E	D (58 mA)	1
	180	–	–	–	–	–	–	1
	181	–	–	–	56	E	D (58 mA)	1
	182	–	–	–	–	–	–	2
	183	–	–	–	–	–	–	2
	184	40	D	E (100 mA)	60	F	E (100 mA)	2
	185	41	D	E (100 mA)	61	F	E (100 mA)	2
	186	–	–	–	–	–	–	2
	187	42	D	E (100 mA)	62	F	E (100 mA)	2
	188	–	–	–	–	–	–	2
	189	44	E	E (100 mA)	63	F	E (100 mA)	2
	190	–	–	–	–	–	–	2
	191	–	–	–	–	–	–	2
	192	45	E	E (100 mA)	65	G	E (100 mA)	2

Table 41. EPM7256B I/O Pin-Outs & I/O Standards (Part 7 of 8)

Lab	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
M	193	–	–	–	106	A	H (200 mA)	2
	194	–	–	–	–	–	–	2
	195	75	A	G (200 mA)	107	A	H (200 mA)	2
	196	–	–	–	–	–	–	2
	197	–	–	–	108	A	H (200 mA)	2
	198	–	–	–	–	–	–	2
	199	–	–	–	–	–	–	2
	200	–	–	–	109	A	H (200 mA)	2
	201	76	A	G (200 mA)	110	A	H (200 mA)	2
	202	–	–	–	–	–	–	2
	203	77	A	G (200 mA)	111	A	H (200 mA)	2
	204	–	–	–	–	–	–	2
	205	–	–	–	–	–	–	2
	206	78	A	G (200 mA)	112	A	H (200 mA)	2
	207	–	–	–	–	–	–	2
	208	79	A	G (200 mA)	113	A	H (200 mA)	2
N	209	–	–	–	–	–	–	2
	210	–	–	–	–	–	–	2
	211	69	F	G (200 mA)	98	H	H (200 mA)	2
	212	–	–	–	–	–	–	2
	213	–	–	–	99	H	H (200 mA)	2
	214	–	–	–	–	–	–	2
	215	–	–	–	–	–	–	2
	216	70	F	G (200 mA)	100	H	H (200 mA)	2
	217	–	–	–	101	H	H (200 mA)	2
	218	–	–	–	–	–	–	2
	219	71	F	G (200 mA)	102	H	H (200 mA)	2
	220	–	–	–	–	–	–	2
	221	72	F	G (200 mA)	103	H	H (200 mA)	2
	222	–	–	–	–	–	–	2
	223	–	–	–	–	–	–	2
	224	73 *(1)*	F	G (200 mA)	104 *(1)*	H	H (200 mA)	2

Table 41. EPM7256B I/O Pin-Outs & I/O Standards (Part 8 of 8)

Lab	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
P	225	–	–	–	–	–	–	2
	226	–	–	–	–	–	–	2
	227	–	–	–	74	G	F (200 mA)	2
	228	–	–	–	–	–	–	2
	229	–	–	–	75	G	F (200 mA)	2
	230	–	–	–	–	–	–	2
	231	–	–	–	–	–	–	2
	232	52	E	F (200 mA)	77	G	G (200 mA)	2
	233	53	E	F (200 mA)	78	G	G (200 mA)	2
	234	–	–	–	–	–	–	2
	235	54	E	F (200 mA)	79	G	G (200 mA)	2
	236	–	–	–	–	–	–	2
	237	55	E	F (200 mA)	80	G	G (200 mA)	2
	238	–	–	–	–	–	–	2
	239	–	–	–	–	–	–	2
	240	56	E	F (200 mA)	81	G	G (200 mA)	2
Q	241	46	E	E (100 mA)	66	G	E (100 mA)	2
	242	–	–	–	–	–	–	2
	243	47	E	E (100 mA)	67	G	E (100 mA)	2
	244	–	–	–	–	–	–	2
	245	48	E	E (100 mA)	68	G	E (100 mA)	2
	246	49	E	E (100 mA)	69	G	E (100 mA)	2
	247	–	–	–	–	–	–	2
	248	–	–	–	–	–	–	2
	249	–	–	–	70	G	E (100 mA)	2
	250	–	–	–	–	–	–	2
	251	–	–	–	–	–	–	2
	252	–	–	–	–	–	–	2
	253	–	–	–	71	G	E (100 mA)	2
	254	–	–	–	–	–	–	2
	255	–	–	–	–	–	–	2
	256	50	E	E (100 mA)	72	G	E (100 mA)	2

Notes to tables:

(1) This pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for in-system programming, this pin is not available as a user I/O pin.

(2) This pin may function as either a VREF pin or a user I/O pin. If this pin is programmed to be a VREF pin for using the advanced I/O standards, then this pin is not available as a user I/O pin.

(3) The user I/O pin count includes dedicated input pins and all I/O pins.

Table 42. EPM7256B I/O Pin-Outs & I/O Standards (Part 1 of 9)

LAB	MC	169-Pin Ultra FineLine BGA	256-Pin FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA & 256-pin FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA & 256-pin FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
A	1	–	C3	–	–	153	B	B (200 mA)	1
	2	–	–	–	–	–	–	–	1
	3	B1	C4	B	D (200 mA)	154	B	B (200 mA)	1
	4	–	–	–	–	–	–	–	1
	5	A1	E5	B	D (200 mA)	159	B	B (200 mA)	1
	6	B2	D5	B	C (200 mA)	160	B	B (200 mA)	1
	7	–	–	–	–	–	–	–	1
	8	C3	C5	B	B (200 mA)	161	B	B (200 mA)	1
	9	–	B4	–	–	162	B	B (200 mA)	1
	10	–	–	–	–	–	–	–	1
	11	B3	A4	B	B (200 mA)	163	B	B (200 mA)	1
	12	–	–	–	–	–	–	–	1
	13	C4	A5	B	B (200 mA)	164	B	B (200 mA)	1
	14	B4	D6	B	A (100 mA)	166	B	A (100 mA)	1
	15	–	–	–	–	–	–	–	1
	16	A4	C6	B	A (100 mA)	167	B	A (100 mA)	1

Table 42. EPM7256B I/O Pin-Outs & I/O Standards (Part 2 of 9)

LAB	MC	169-Pin Ultra FineLine BGA	256-Pin FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA & 256-pin FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA & 256-pin FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
B	17	E3	F5	C	E (200 mA)	141	C	C (200 mA)	1
	18	–	–	–	–	–	–	–	1
	19	E2	F2	C	E (200 mA)	142	C	C (200 mA)	1
	20	–	–	–	–	–	–	–	1
	21	D4	E1	C	D (200 mA)	144	C	B (200 mA)	1
	22	D3	F4	C	D (200 mA)	145	C	B (200 mA)	1
	23	–	–	–	–	–	–	–	1
	24	D2	F3	C	D (200 mA)	146	C	B (200 mA)	1
	25	D1	E2	C	D (200 mA)	147	C	B (200 mA)	1
	26	–	–	–	–	–	–	–	1
	27	C2	D2	C	D (200 mA)	148	C	B (200 mA)	1
	28	–	–	–	–	–	–	–	1
	29	C1	E3	C	D (200 mA)	149	C	B (200 mA)	1
	30	–	E4	–	–	150	C	B (200 mA)	1
	31	–	–	–	–	–	–	–	1
	32	E4	D4 *(1)*	C	D (200 mA)	151	C	B (200 mA)	1
C	33	M1	N4	G	G (200 mA)	108	E	D (200 mA)	1
	34	–	–	–	–	–	–	–	1
	35	L1	P3	G	G (200 mA)	109	E	D (200 mA)	1
	36	–	–	–	–	–	–	–	1
	37	L2	N3	G	G (200 mA)	110	E	D (200 mA)	1
	38	–	M4	–	–	111	E	D (200 mA)	1
	39	–	–	–	–	–	–	–	1
	40	K2	M2	F	G (200 mA)	112	E	D (200 mA)	1
	41	K3	L4	F	G (200 mA)	113	E	D (200 mA)	1
	42	–	–	–	–	–	–	–	1
	43	K4	L5	F	G (200 mA)	114	E	D (200 mA)	1
	44	–	–	–	–	–	–	–	1
	45	K1	K6	F	G (200 mA)	115	E	D (200 mA)	1
	46	–	K5	–	–	117	D	D (200 mA)	1
	47	–	–	–	–	–	–	–	1
	48	J5	K4	E	G (200 mA)	118	D	D (200 mA)	1

Table 42. EPM7256B I/O Pin-Outs & I/O Standards (Part 3 of 9)

LAB	MC	169-Pin Ultra FineLine BGA	256-Pin FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA & 256-pin FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA & 256-pin FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
D	49	M5	N6	H	H (200 mA)	92	F	E (200 mA)	1
	50	–	–	–	–	–	–	–	1
	51	N5	T5	H	H (200 mA)	93	F	E (200 mA)	1
	52	–	–	–	–	–	–	–	1
	53	L4	M6	G	H (200 mA)	95	E	E (200 mA)	1
	54	M4	R5	G	H (200 mA)	96	E	E (200 mA)	1
	55	–	–	–	–	–	–	–	1
	56	N4	M5	G	H (200 mA)	97	E	E (200 mA)	1
	57	L3	P5	G	H (200 mA)	98	E	E (200 mA)	1
	58	–	–	–	–	–	–	–	1
	59	M3	N5	G	H (200 mA)	99	E	E (200 mA)	1
	60	–	–	–	–	–	–	–	1
	61	M2	T4	G	H (200 mA)	100	E	E (200 mA)	1
	62	–	R4	–	–	101	E	E (200 mA)	1
	63	–	–	–	–	–	–	–	1
	64	N1	P4	G	H (200 mA)	102	E	E (200 mA)	1
E	65	D5	B6	B	A (100 mA)	168	B	A (100 mA)	1
	66	–	–	–	–	–	–	–	1
	67	C5	E6	B	A (100 mA)	169	B	A (100 mA)	1
	68	–	–	–	–	–	–	–	1
	69	B5	F7	B	A (100 mA)	170	B	A (100 mA)	1
	70	–	E7	–	–	171	B	A (100 mA)	1
	71	–	–	–	–	–	–	–	1
	72	A5	D7	B	A (100 mA)	172	B	A (100 mA)	1
	73	F6	C7	B	A (100 mA)	173	B	A (100 mA)	1
	74	–	–	–	–	–	–	–	1
	75	C6	B7	A	A (100 mA)	175	A	A (100 mA)	1
	76	–	–	–	–	–	–	–	1
	77	B6	A7	A	A (100 mA)	176 *(1)*	A	A (100 mA)	1
	78	A6	F8	A	A (100 mA)	177	A	A (100 mA)	1
	79	–	–	–	–	–	–	–	1
	80	C7	B8	A	A (100 mA)	178	A	A (100 mA)	1

Table 42. EPM7256B I/O Pin-Outs & I/O Standards (Part 4 of 9)

LAB	MC	169-Pin Ultra FineLine BGA	256-Pin FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA & 256-pin FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA & 256-pin FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
F	81	G5	H5	E	E (200 mA)	130	D	C (200 mA)	1
	82	–	–	–	–	–	–	–	1
	83	G3	H1	E	E (200 mA)	131	D	C (200 mA)	1
	84	–	–	–	–	–	–	–	1
	85	G2	H2	E	E (200 mA)	132	D	C (200 mA)	1
	86	G1	H3	E	E (200 mA)	133	D	C (200 mA)	1
	87	–	–	–	–	–	–	–	1
	88	F4	H4	D	E (200 mA)	135	C	C (200 mA)	1
	89	F3	G6	D	E (200 mA)	136	C	C (200 mA)	1
	90	–	–	–	–	–	–	–	1
	91	G4	G5	D	E (200 mA)	137	C	C (200 mA)	1
	92	–	–	–	–	–	–	–	1
	93	F2	G2	C	E (200 mA)	138	C	C (200 mA)	1
	94	–	G4	–	–	139	C	C (200 mA)	1
	95	–	–	–	–	–	–	–	1
	96	E5	F1	C	E (200 mA)	140	C	C (200 mA)	1
G	97	J3	K3	E	G (200 mA)	119	D	D (200 mA)	1
	98	–	–	–	–	–	–	–	1
	99	J2	K2	E	G (200 mA)	120	D	D (200 mA)	1
	100	–	–	–	–	–	–	–	1
	101	H4	J7	E	G (200 mA)	121	D	D (200 mA)	1
	102	–	H7	–	–	122	D	D (200 mA)	1
	103	–	–	–	–	–	–	–	1
	104	H3	J5	E	G (200 mA)	123	D	D (200 mA)	1
	105	H2	J2	E	F (200 mA)	124	D	D (200 mA)	1
	106	–	–	–	–	–	–	–	1
	107	G7	J3	E	E (200 mA)	126	D	C (200 mA)	1
	108	–	–	–	–	–	–	–	1
	109	G6	J4 *(2)*	E	E (200 mA)	127 *(1)*	D	C (200 mA)	1
	110	–	H6	–	–	128 *(2)*	D	C (200 mA)	1
	111	–	–	–	–	–	–	–	1
	112	J4	J6 *(1)*	E	E (200 mA)	129	D	C (200 mA)	1

Table 42. EPM7256B I/O Pin-Outs & I/O Standards (Part 5 of 9)

LAB	MC	169-Pin Ultra FineLine BGA	256-Pin FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA & 256-pin FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA & 256-pin FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
H	113	–	M8	–	–	79	F	F (58 mA)	1
	114	–	–	–	–	–	–	–	1
	115	H6	N8	H	I (58 mA)	80	F	F (58 mA)	1
	116	–	–	–	–	–	–	–	1
	117	J6	L8	H	I (58 mA)	81	F	F (58 mA)	1
	118	K6	R7	H	I (58 mA)	84	F	F (58 mA)	1
	119	–	–	–	–	–	–	–	1
	120	L6	P7	H	H (200 mA)	86	F	E (200 mA)	1
	121	M6	N7	H	H (200 mA)	87	F	E (200 mA)	1
	122	–	–	–	–	–	–	–	1
	123	N6	M7	H	H (200 mA)	88	F	E (200 mA)	1
	124	–	–	–	–	–	–	–	1
	125	K5	L7	H	H (200 mA)	89	F	E (200 mA)	1
	126	–	T6	–	–	90	F	E (200 mA)	1
	127	–	–	–	–	–	–	–	1
	128	L5	R6	H	H (200 mA)	91	F	E (200 mA)	1
I	129	D9	C11	A	Q (200 mA)	197	A	K (200 mA)	2
	130	–	–	–	–	–	–	–	2
	131	C9	B11	A	R (200 mA)	196	A	K (200 mA)	2
	132	–	–	–	–	–	–	–	2
	133	B9	A11	A	R (200 mA)	195	A	K (200 mA)	2
	134	–	F10	–	–	194	A	K (200 mA)	2
	135	–	–	–	–	–	–	–	2
	136	A9	E10	A	R (200 mA)	193	A	K (200 mA)	2
	137	F8	A10	A	R (200 mA)	192	A	K (200 mA)	2
	138	–	–	–	–	–	–	–	2
	139	C8	C10	A	S(100 mA)	190	A	L (100 mA)	2
	140	–	–	–	–	–	–	–	2
	141	B8	D10	A	S (100 mA)	189 *(1)*	A	L (100 mA)	2
	142	A8	F9	A	S (100 mA)	188	A	L (100 mA)	2
	143	–	–	–	–	–	–	–	2
	144	F7	A9	A	S (100 mA)	187	A	L (100 mA)	2

Table 42. EPM7256B I/O Pin-Outs & I/O Standards (Part 6 of 9)

LAB	MC	169-Pin Ultra FineLine BGA	256-Pin FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA & 256-pin FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA & 256-pin FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
J	145	H12	J15	N	N (200 mA)	27	I	I (200 mA)	2
	146	–	–	–	–	–	–	–	2
	147	G11	J16	N	N (200 mA)	26	I	I (200 mA)	2
	148	–	–	–	–	–	–	–	2
	149	G12	J10	N	N (200 mA)	25	I	I (200 mA)	2
	150	G13	H14	N	N (200 mA)	24	I	I (200 mA)	2
	151	–	–	–	–	–	–	–	2
	152	G9	H13	N	O (200 mA)	22 *(2)*	I	J (200 mA)	2
	153	G8	H12	N	O (200 mA)	21	I	J (200 mA)	2
	154	–	–	–	–	–	–	–	2
	155	F12	H11 *(2)*	N	O (200 mA)	20	I	J (200 mA)	2
	156	–	–	–	–	–	–	–	2
	157	F11	H10	N	P (200 mA)	19	I	J (200 mA)	2
	158	–	G11	–	–	18	I	J (200 mA)	2
	159	–	–	–	–	–	–	–	2
	160	E12	G14	N	P (200 mA)	17	I	J (200 mA)	2
K	161	K13	K11	L	N (200 mA)	38	H	I (200 mA)	2
	162	–	–	–	–	–	–	–	2
	163	J9	K12	L	N (200 mA)	37	H	I (200 mA)	2
	164	–	–	–	–	–	–	–	2
	165	G10	K14	L	N (200 mA)	36	H	I (200 mA)	2
	166	–	K13	–	–	35	H	I (200 mA)	2
	167	–	–	–	–	–	–	–	2
	168	J11	K15	L	N (200 mA)	34	H	I (200 mA)	2
	169	J12	K16	M	N (200 mA)	33	H	I (200 mA)	2
	170	–	–	–	–	–	–	–	2
	171	H10	J13	N	N (200 mA)	31	I	I (200 mA)	2
	172	–	–	–	–	–	–	–	2
	173	H11	J14	N	N (200 mA)	30 *(1)*	I	I (200 mA)	2
	174	–	J12	–	–	29	I	I (200 mA)	2
	175	–	–	–	–	–	–	–	2
	176	J10	J11 *(1)*	N	N (200 mA)	28	I	I (200 mA)	2

Table 42. EPM7256B I/O Pin-Outs & I/O Standards (Part 7 of 9)

LAB	MC	169-Pin Ultra FineLine BGA	256-Pin FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA & 256-pin FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA & 256-pin FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
L	177	–	R8	–	–	78	F	F (58 mA)	2
	178	–	–	–	–	–	–	–	2
	179	K7	T9	H	I (58 mA)	77	F	F (58 mA)	2
	180	–	–	–	–	–	–	–	2
	181	L7	R9	H	I (58 mA)	76	F	F (58 mA)	2
	182	H8	N9	H	J (100 mA)	73	F	G (100 mA)	2
	183	–	–	–	–	–	–	–	2
	184	J8	M9	I	J (100 mA)	71	G	G (100 mA)	2
	185	K8	L9	I	J (100 mA)	70	G	G (100 mA)	2
	186	–	–	–	–	–	–	–	2
	187	L8	R10	I	J (100 mA)	69	G	G (100 mA)	2
	188	–	–	–	–	–	–	–	2
	189	M8	N10	J	J (100 mA)	68	G	G (100 mA)	2
	190	N8	M10	K	J (100 mA)	67	G	G (100 mA)	2
	191	–	–	–	–	–	–	–	2
	192	K9	L10	K	J (100 mA)	66	G	G (100 mA)	2
M	193	C13	B14	P	Q (200 mA)	4	J	K (200 mA)	2
	194	–	–	–	–	–	–	–	2
	195	B13	C13	P	Q (200 mA)	3	J	K (200 mA)	2
	196	–	–	–	–	–	–	–	2
	197	A13	B13	P	Q (200 mA)	206	J	K (200 mA)	2
	198	–	F12	–	–	205	J	K (200 mA)	2
	199	–	–	–	–	–	–	–	2
	200	B12	E12	P	Q (200 mA)	204	J	K (200 mA)	2
	201	C11	D12	P	Q (200 mA)	203	J	K (200 mA)	2
	202	–	–	–	–	–	–	–	2
	203	B11	C12	P	Q (200 mA)	202	J	K (200 mA)	2
	204	–	–	–	–	–	–	–	2
	205	C10	B12	P	Q (200 mA)	201	J	K (200 mA)	2
	206	B10	E11	A	Q (200 mA)	199	A	K (200 mA)	2
	207	–	–	–	–	–	–	–	2
	208	A10	D11	A	Q (200 mA)	198	A	K (200 mA)	2

Table 42. EPM7256B I/O Pin-Outs & I/O Standards (Part 8 of 9)

LAB	MC	169-Pin Ultra FineLine BGA	256-Pin FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA & 256-pin FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA & 256-pin FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
N	209	E11	G13	N	P (200 mA)	16	I	J (200 mA)	2
	210	–	–	–	–	–	–	–	2
	211	F10	G12	N	P (200 mA)	15	I	J (200 mA)	2
	212	–	–	–	–	–	–	–	2
	213	E9	F16	O	P (200 mA)	13	J	J (200 mA)	2
	214	D10	F15	O	P (200 mA)	12	J	J (200 mA)	2
	215	–	–	–	–	–	–	–	2
	216	D11	F13	O	P (200 mA)	11	J	J (200 mA)	2
	217	D12	F14	O	P (200 mA)	10	J	J (200 mA)	2
	218	–	–	–	–	–	–	–	2
	219	D13	E16	O	P (200 mA)	9	J	J (200 mA)	2
	220	–	–	–	–	–	–	–	2
	221	C12	E14	O	P (200 mA)	8	J	J (200 mA)	2
	222	–	E13	–	–	7	J	J (200 mA)	2
	223	–	–	–	–	–	–	–	2
	224	E10	D13 *(1)*	O	P (200 mA)	6	J	J (200 mA)	2
O	225	N13	R13	L	L (200 mA)	49	H	H (200 mA)	2
	226	–	–	–	–	–	–	–	2
	227	M12	P13	L	L (200 mA)	48	H	H (200 mA)	2
	228	–	–	–	–	–	–	–	2
	229	M13	N13	L	L (200 mA)	47	H	H (200 mA)	2
	230	–	M14	–	–	46	H	H (200 mA)	2
	231	–	–	–	–	–	–	–	2
	232	L12	M13	L	M (200 mA)	45	H	H (200 mA)	2
	233	L13	L13	L	M (200 mA)	44	H	H (200 mA)	2
	234	–	–	–	–	–	–	–	2
	235	K10	L14	L	M (200 mA)	43	H	H (200 mA)	2
	236	–	–	–	–	–	–	–	2
	237	K11	L12	L	M (200 mA)	42	H	H (200 mA)	2
	238	–	L15	–	–	40	H	I (200 mA)	2
	239	–	–	–	–	–	–	–	2
	240	K12	L16	L	N (200 mA)	39	H	I (200 mA)	2

Table 42. EPM7256B I/O Pin-Outs & I/O Standards (Part 9 of 9)

LAB	MC	169-Pin Ultra FineLine BGA	256-Pin FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA & 256-pin FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA & 256-pin FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
P	241	L9	R11	K	J (100 mA)	65	G	G (100 mA)	2
	242	–	–	–	–	–	–	–	2
	243	M9	P11	K	J (100 mA)	64	G	G (100 mA)	2
	244	–	–	–	–	–	–	–	2
	245	N9	N11	K	K (200 mA)	62	G	H (200 mA)	2
	246	L10	M11	K	K (200 mA)	61	G	H (200 mA)	2
	247	–	–	–	–	–	–	–	2
	248	–	T12	–	–	60	G	H (200 mA)	2
	249	M10	R12	K	K (200 mA)	59	G	H (200 mA)	2
	250	–	–	–	–	–	–	–	2
	251	N10	M12	K	K (200 mA)	58	G	H (200 mA)	2
	252	–	–	–	–	–	–	–	2
	253	L11	P12	K	K (200 mA)	57	G	H (200 mA)	2
	254	–	N12	–	–	56	G	H (200 mA)	2
	255	–	–	–	–	–	–	–	2
	256	M11	T13	K	K (200 mA)	55	G	H (200 mA)	2

Notes to tables:

(1) This pin can function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for in-system programming, this pin is not available as a user I/O pin.

(2) This pin may function as either a VREF pin or a user I/O pin. If this pin is programmed to be a VREF pin for using the advanced I/O standards, this pin is not available as a user I/O pin.

(3) The user I/O pin count includes dedicated input pins and all I/O pins.

(4) EPM7512B devices in the 208-pin PQFP package support vertical migration from EPM7256E, EPM7256S, and EPM7256B devices. EPM7512B devices contain additional I/O pins which are no connects on the EPM7256E, EPM7256S, and EPM7256B devices. To support these additional I/O pins, EPM7512B devices have two additional VCCIO1 (pin 105), VCCIO2 (pin 207) and GNDIO (pins 51 and 158) pins that are no-connect pins on the EPM7256E, EPM7256S, and EPM7256B devices. To achieve vertical migration between the EPM7256B and EPM7512B devices, the no-connect pin 105 may be tied to VCCIO1, pin 207 may be tied to VCCIO2, and pins 51 and 158 may be tied to GNDIO on EPM7256B devices.

Table 43. EPM7512B Dedicated Pin-Outs

Dedicated Pin	100-Pin TQFP	144-Pin TQFP	169-Pin Ultra FineLine BGA	208-Pin PQFP *(1)*	256-Pin BGA	256-Pin FineLine BGA
INPUT/GCLK1	87	125	D8	184	L1	D9
INPUT/GCLRn	89	127	D6	182	K2	E8
INPUT/OE1	88	126	D7	183	K1	E9
INPUT/OE2/GCLK2	90	128	E7	181	K3	D8
TDI *(2)*	4	4	E4	176	A2	D4
TMS *(2)*	15	20	J4	127	B12	J6
TCK *(2)*	62	89	J10	30	V12	J11
TDO *(2)*	73	104	E10	189	Y2	D13
VREFA *(2)*	12	14	G4	128	C12	J4
VREFB *(2)*	60	87	H10	22	V10	H11
GNDINT	38, 86	52, 57, 124, 129	A7, E8, J7, N7	75, 82, 180, 185	J20, K4, K18, L2, L17	A8, C9, G9, K8, P9
GNDIO	11, 26, 43, 59, 74, 95	3, 13, 17, 33, 59, 64, 85, 105, 135	A3, A12, E1, F5, F13, H1, H9, J13, N2, N11	14, 32, 50, 51, 72, 94, 116, 134, 152, 158, 174, 200	A1, B2, B19, B20, C3, C18, D4, D17, U4, U17, V3, V18, V19, W2, W19, Y1, Y20	A3, B10, C2, D14, F6, G10, H8, J9, K7, L11, M3, P6, P10, R2, R3, T1, T15
VCCINT (2.5 V)	39, 91	51, 58, 123, 130	B7, E6, H7, M7	74, 83, 179, 186	J1, J19, L4, M19, M20	B9, C8, G8, K9, P8
VCCIO1 (1.8 V, 2.5 V, 3.3 V)	3, 18, 34	24, 50, 144	A2, F1, H5, J1, N3	85, 105, 107, 125, 143, 165	C4, C17, D3, D5, D16, D18, E4, E17	B3, B5, G3, G7, J8, L3, L6, T2, T3
VCCIO2 (1.8 V, 2.5 V, 3.3 V)	51, 66, 82	73, 76, 95, 115	A11, E13, F9, H13, N12	5, 23, 41, 63, 191, 207	T4, T17, U3, U5, U16, U18, V2, V4, V17	C14, E15, F11,G15, H9, K10, M15, P14
No Connect (N.C.)	–	–	–	–	–	–
Total User I/O Pins *(3)*	84	120	141	176	212	212

Table 44. EPM7512B I/O Pin-Outs & I/O Standards (Part 1 of 16)

LAB	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
A	1	94	A	A (100 mA)	134	A	A (100 mA)	1
	2	–	–	–	–	–	–	1
	3	–	–	–	–	–	–	1
	4	–	–	–	–	–	–	1
	5	–	–	–	–	–	–	1
	6	–	–	–	–	–	–	1
	7	–	–	–	–	–	–	1
	8	–	–	–	–	–	–	1
	9	–	–	–	–	–	–	1
	10	–	–	–	–	–	–	1
	11	93	A	A (100 mA)	133	A	A (100 mA)	1
	12	–	–	–	–	–	–	1
	13	–	–	–	–	–	–	1
	14	92	A	A (100 mA)	132	A	A (100 mA)	1
	15	–	–	–	–	–	–	1
	16	–	–	–	131	A	A (100 mA)	1
B	17	–	–	–	–	–	–	1
	18	–	–	–	–	–	–	1
	19	–	–	–	–	–	–	1
	20	–	–	–	–	–	–	1
	21	–	–	–	138	B	A (100 mA)	1
	22	–	–	–	–	–	–	1
	23	–	–	–	–	–	–	1
	24	–	–	–	–	–	–	1
	25	97	B	A (100 mA)	137	B	A (100 mA)	1
	26	–	–	–	–	–	–	1
	27	96	B	A (100 mA)	136	B	A (100 mA)	1
	28	–	–	–	–	–	–	1
	29	–	–	–	–	–	–	1
	30	–	–	–	–	–	–	1
	31	–	–	–	–	–	–	1
	32	–	–	–	–	–	–	1

Table 44. EPM7512B I/O Pin-Outs & I/O Standards (Part 2 of 16)

LAB	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
C	33	–	–	–	142	B	A (100 mA)	1
	34	–	–	–	–	–	–	1
	35	–	–	–	–	–	–	1
	36	–	–	–	–	–	–	1
	37	100	B	A (100 mA)	141	B	A (100 mA)	1
	38	–	–	–	–	–	–	1
	39	–	–	–	–	–	–	1
	40	–	–	–	–	–	–	1
	41	99	B	A (100 mA)	140	B	A (100 mA)	1
	42	–	–	–	–	–	–	1
	43	–	–	–	–	–	–	1
	44	–	–	–	–	–	–	1
	45	–	–	–	–	–	–	1
	46	98	B	A (100 mA)	139	B	A (100 mA)	1
	47	–	–	–	–	–	–	1
	48	–	–	–	–	–	–	1
D	49	–	–	–	2	B	B (200 mA)	1
	50	–	–	–	–	–	–	1
	51	–	–	–	–	–	–	1
	52	–	–	–	–	–	–	1
	53	–	–	–	1	B	B (200 mA)	1
	54	–	–	–	–	–	–	1
	55	–	–	–	–	–	–	1
	56	–	–	–	–	–	–	1
	57	–	–	–	–	–	–	1
	58	–	–	–	–	–	–	1
	59	2	B	A (100 mA)	–	–	–	1
	60	–	–	–	–	–	–	1
	61	–	–	–	–	–	–	1
	62	–	–	–	–	–	–	1
	63	–	–	–	–	–	–	1
	64	1	B	A (100 mA)	143	B	A (100 mA)	1

Table 44. EPM7512B I/O Pin-Outs & I/O Standards (Part 3 of 16)

LAB	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
E	65	–	–	–	–	–	–	1
	66	–	–	–	–	–	–	1
	67	–	–	–	7	C	B (200 mA)	1
	68	–	–	–	–	–	–	1
	69	–	–	–	–	–	–	1
	70	–	–	–	–	–	–	1
	71	–	–	–	–	–	–	1
	72	–	–	–	–	–	–	1
	73	–	–	–	–	–	–	1
	74	–	–	–	–	–	–	1
	75	6	B	B (200 mA)	6	C	B (200 mA)	1
	76	–	–	–	–	–	–	1
	77	–	–	–	–	–	–	1
	78	5	B	B (200 mA)	5	C	B (200 mA)	1
	79	–	–	–	–	–	–	1
	80	4 *(1)*	B	B (200 mA)	4 *(1)*	C	B (200 mA)	1
F	81	–	–	–	–	–	–	1
	82	–	–	–	–	–	–	1
	83	–	–	–	–	–	–	1
	84	–	–	–	–	–	–	1
	85	9	B	B (200 mA)	11	C	B (200 mA)	1
	86	–	–	–	–	–	–	1
	87	–	–	–	–	–	–	1
	88	–	–	–	–	–	–	1
	89	–	–	–	–	–	–	1
	90	–	–	–	–	–	–	1
	91	8	B	B (200 mA)	10	C	B (200 mA)	1
	92	–	–	–	–	–	–	1
	93	–	–	–	–	–	–	1
	94	7	B	B (200 mA)	9	C	B (200 mA)	1
	95	–	–	–	–	–	–	1
	96	–	–	–	8	C	B (200 mA)	1

Table 44. EPM7512B I/O Pin-Outs & I/O Standards (Part 4 of 16)

LAB	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
G	97	–	–	–	–	–	–	1
	98	–	–	–	–	–	–	1
	99	–	–	–	15	D	B (200 mA)	1
	100	–	–	–	–	–	–	1
	101	12 *(2)*	C	B (200 mA)	14 *(2)*	D	B (200 mA)	1
	102	–	–	–	–	–	–	1
	103	–	–	–	–	–	–	1
	104	–	–	–	–	–	–	1
	105	–	–	–	–	–	–	1
	106	–	–	–	–	–	–	1
	107	–	–	–	–	–	–	1
	108	–	–	–	–	–	–	1
	109	–	–	–	–	–	–	1
	110	10	B	B (200 mA)	12	C	B (200 mA)	1
	111	–	–	–	–	–	–	1
	112	–	–	–	–	–	–	1
H	113	14	C	B (200 mA)	19	E	B (200 mA)	1
	114	–	–	–	–	–	–	1
	115	–	–	–	–	–	–	1
	116	–	–	–	–	–	–	1
	117	13	C	B (200 mA)	18	E	B (200 mA)	1
	118	–	–	–	–	–	–	1
	119	–	–	–	–	–	–	1
	120	–	–	–	–	–	–	1
	121	–	–	–	–	–	–	1
	122	–	–	–	–	–	–	1
	123	–	–	–	–	–	–	1
	124	–	–	–	–	–	–	1
	125	–	–	–	–	–	–	1
	126	–	–	–	–	–	–	1
	127	–	–	–	–	–	–	1
	128	–	–	–	16	D	B (200 mA)	1

Table 44. EPM7512B I/O Pin-Outs & I/O Standards (Part 5 of 16)

LAB	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
I	129	–	–	–	–	–	–	1
	130	–	–	–	–	–	–	1
	131	–	–	–	–	–	–	1
	132	–	–	–	–	–	–	1
	133	15 *(1)*	C	B (200 mA)	20 *(1)*	E	B (200 mA)	1
	134	–	–	–	–	–	–	1
	135	–	–	–	–	–	–	1
	136	–	–	–	–	–	–	1
	137	–	–	–	–	–	–	1
	138	–	–	–	–	–	–	1
	139	–	–	–	–	–	–	1
	140	–	–	–	–	–	–	1
	141	–	–	–	–	–	–	1
	142	–	–	–	–	–	–	1
	143	–	–	–	–	–	–	1
	144	–	–	–	–	–	–	1
J	145	–	–	–	–	–	–	1
	146	–	–	–	–	–	–	1
	147	–	–	–	–	–	–	1
	148	–	–	–	–	–	–	1
	149	20	C	C (200 mA)	26	E	C (200 mA)	1
	150	–	–	–	–	–	–	1
	151	–	–	–	–	–	–	1
	152	–	–	–	–	–	–	1
	153	19	C	C (200 mA)	25	E	C (200 mA)	1
	154	–	–	–	–	–	–	1
	155	–	–	–	23	E	B (200 mA)	1
	156	–	–	–	–	–	–	1
	157	–	–	–	–	–	–	1
	158	17	C	B (200 mA)	22	E	B (200 mA)	1
	159	–	–	–	–	–	–	1
	160	16	C	B (200 mA)	21	E	B (200 mA)	1

Table 44. EPM7512B I/O Pin-Outs & I/O Standards (Part 6 of 16)

LAB	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
K	161	22	C	C (200 mA)	29	E	C (200 mA)	1
	162	–	–	–	–	–	–	1
	163	–	–	–	–	–	–	1
	164	–	–	–	–	–	–	1
	165	–	–	–	–	–	–	1
	166	–	–	–	–	–	–	1
	167	–	–	–	–	–	–	1
	168	–	–	–	–	–	–	1
	169	21	C	C (200 mA)	28	E	C (200 mA)	1
	170	–	–	–	–	–	–	1
	171	–	–	–	–	–	–	1
	172	–	–	–	–	–	–	1
	173	–	–	–	–	–	–	1
	174	–	–	–	–	–	–	1
	175	–	–	–	–	–	–	1
	176	–	–	–	27	E	C (200 mA)	1
L	177	–	–	–	34	F	C (200 mA)	1
	178	–	–	–	–	–	–	1
	179	–	–	–	–	–	–	1
	180	–	–	–	–	–	–	1
	181	25	C	C (200 mA)	32	E	C (200 mA)	1
	182	–	–	–	–	–	–	1
	183	–	–	–	–	–	–	1
	184	–	–	–	–	–	–	1
	185	–	–	–	–	–	–	1
	186	–	–	–	–	–	–	1
	187	–	–	–	–	–	–	1
	188	–	–	–	–	–	–	1
	189	–	–	–	–	–	–	1
	190	24	C	C (200 mA)	31	E	C (200 mA)	1
	191	–	–	–	–	–	–	1
	192	23	C	C (200 mA)	30	E	C (200 mA)	1

Table 44. EPM7512B I/O Pin-Outs & I/O Standards (Part 7 of 16)

LAB	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
M	193	–	–	–	–	–	–	1
	194	–	–	–	–	–	–	1
	195	–	–	–	–	–	–	1
	196	–	–	–	–	–	–	1
	197	–	–	–	–	–	–	1
	198	–	–	–	–	–	–	1
	199	–	–	–	–	–	–	1
	200	–	–	–	–	–	–	1
	201	–	–	–	37	F	C (200 mA)	1
	202	–	–	–	–	–	–	1
	203	–	–	–	–	–	–	1
	204	–	–	–	–	–	–	1
	205	–	–	–	–	–	–	1
	206	27	D	C (200 mA)	36	F	C (200 mA)	1
	207	–	–	–	–	–	–	1
	208	–	–	–	35	F	C (200 mA)	1
N	209	30	D	C (200 mA)	42	F	C (200 mA)	1
	210	–	–	–	–	–	–	1
	211	–	–	–	–	–	–	1
	212	–	–	–	–	–	–	1
	213	29	D	C (200 mA)	41	F	C (200 mA)	1
	214	–	–	–	–	–	–	1
	215	–	–	–	–	–	–	1
	216	–	–	–	–	–	–	1
	217	28	D	C (200 mA)	40	F	C (200 mA)	1
	218	–	–	–	–	–	–	1
	219	–	–	–	39	F	C (200 mA)	1
	220	–	–	–	–	–	–	1
	221	–	–	–	–	–	–	1
	222	–	–	–	–	–	–	1
	223	–	–	–	–	–	–	1
	224	–	–	–	38	F	C (200 mA)	1

Table 44. EPM7512B I/O Pin-Outs & I/O Standards (Part 8 of 16)

LAB	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
O	225	–	–	–	47	F	C (200 mA)	1
	226	–	–	–	–	–	–	1
	227	33	D	C (200 mA)	46	F	C (200 mA)	1
	228	–	–	–	–	–	–	1
	229	–	–	–	45	F	C (200 mA)	1
	230	–	–	–	–	–	–	1
	231	–	–	–	–	–	–	1
	232	–	–	–	–	–	–	1
	233	–	–	–	–	–	–	1
	234	–	–	–	–	–	–	1
	235	32	D	C (200 mA)	44	F	C (200 mA)	1
	236	–	–	–	–	–	–	1
	237	–	–	–	–	–	–	1
	238	–	–	–	–	–	–	1
	239	–	–	–	–	–	–	1
	240	31	D	C (200 mA)	43	F	C (200 mA)	1
P	241	36	D	D (58 mA)	54	F	D (58 mA)	1
	242	–	–	–	–	–	–	1
	243	–	–	–	–	–	–	1
	244	–	–	–	–	–	–	1
	245	–	–	–	–	–	–	1
	246	–	–	–	–	–	–	1
	247	–	–	–	–	–	–	1
	248	–	–	–	–	–	–	1
	249	35	D	D (58 mA)	53	F	D (58 mA)	1
	250	–	–	–	–	–	–	1
	251	–	–	–	–	–	–	1
	252	–	–	–	–	–	–	1
	253	–	–	–	–	–	–	1
	254	–	–	–	49	F	C (200 mA)	1
	255	–	–	–	–	–	–	1
	256	–	–	–	48	F	C (200 mA)	1

Table 44. EPM7512B I/O Pin-Outs & I/O Standards (Part 9 of 16)

LAB	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
Q	257	–	–	–	55	F	D (58 mA)	1
	258	–	–	–	–	–	–	1
	259	–	–	–	–	–	–	1
	260	–	–	–	–	–	–	1
	261	–	–	–	–	–	–	1
	262	–	–	–	–	–	–	1
	263	–	–	–	–	–	–	1
	264	–	–	–	–	–	–	1
	265	37	D	D (58 mA)	56	F	D (58 mA)	1
	266	–	–	–	–	–	–	1
	267	–	–	–	–	–	–	2
	268	–	–	–	–	–	–	2
	269	–	–	–	–	–	–	2
	270	40	D	E (100 mA)	60	G	E (100 mA)	2
	271	–	–	–	–	–	–	2
	272	–	–	–	61	G	E (100 mA)	2
R	273	41	D	E (100 mA)	62	G	E (100 mA)	2
	274	–	–	–	–	–	–	2
	275	42	D	E (100 mA)	63	G	E (100 mA)	2
	276	–	–	–	–	–	–	2
	277	–	–	–	–	–	–	2
	278	–	–	–	–	–	–	2
	279	–	–	–	–	–	–	2
	280	–	–	–	–	–	–	2
	281	–	–	–	–	–	–	2
	282	–	–	–	–	–	–	2
	283	44	E	E (100 mA)	65	H	E (100 mA)	2
	284	–	–	–	–	–	–	2
	285	–	–	–	–	–	–	2
	286	–	–	–	–	–	–	2
	287	–	–	–	–	–	–	2
	288	–	–	–	–	–	–	2

Table 44. EPM7512B I/O Pin-Outs & I/O Standards (Part 10 of 16)

LAB	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
S	289	–	–	–	66	H	E (100 mA)	2
	290	–	–	–	–	–	–	2
	291	–	–	–	–	–	–	2
	292	–	–	–	–	–	–	2
	293	45	E	E (100 mA)	67	H	E (100 mA)	2
	294	–	–	–	–	–	–	2
	295	–	–	–	–	–	–	2
	296	–	–	–	–	–	–	2
	297	–	–	–	68	H	E (100 mA)	2
	298	–	–	–	–	–	–	2
	299	46	E	E (100 mA)	69	H	E (100 mA)	2
	300	–	–	–	–	–	–	2
	301	–	–	–	–	–	–	2
	302	–	–	–	–	–	–	2
	303	–	–	–	–	–	–	2
	304	–	–	–	70	H	E (100 mA)	2
T	305	–	–	–	–	–	–	2
	306	–	–	–	–	–	–	2
	307	–	–	–	–	–	–	2
	308	–	–	–	–	–	–	2
	309	–	–	–	–	–	–	2
	310	–	–	–	–	–	–	2
	311	–	–	–	–	–	–	2
	312	–	–	–	–	–	–	2
	313	47	E	E (100 mA)	71	H	E (100 mA)	2
	314	–	–	–	–	–	–	2
	315	48	E	E (100 mA)	72	H	E (100 mA)	2
	316	–	–	–	–	–	–	2
	317	–	–	–	–	–	–	2
	318	–	–	–	–	–	–	2
	319	–	–	–	–	–	–	2
	320	49	E	E (200 mA)	74	H	F (200 mA)	2

Table 44. EPM7512B I/O Pin-Outs & I/O Standards (Part 11 of 16)

LAB	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
U	321	50	E	E (200 mA)	75	H	F (200 mA)	2
	322	–	–	–	–	–	–	2
	323	–	–	–	–	–	–	2
	324	–	–	–	–	–	–	2
	325	–	–	–	–	–	–	2
	326	–	–	–	–	–	–	2
	327	–	–	–	–	–	–	2
	328	–	–	–	–	–	–	2
	329	–	–	–	–	–	–	2
	330	–	–	–	–	–	–	2
	331	–	–	–	–	–	–	2
	332	–	–	–	–	–	–	2
	333	–	–	–	–	–	–	2
	334	52	E	F (200 mA)	77	H	G (200 mA)	2
	335	–	–	–	–	–	–	2
	336	53	E	F (200 mA)	78	H	G (200 mA)	2
V	337	54	E	F (200 mA)	79	H	G (200 mA)	2
	338	–	–	–	–	–	–	2
	339	55	E	F (200 mA)	80	H	G (200 mA)	2
	340	–	–	–	–	–	–	2
	341	–	–	–	–	–	–	2
	342	–	–	–	–	–	–	2
	343	–	–	–	–	–	–	2
	344	–	–	–	–	–	–	2
	345	56	E	F (200 mA)	81	H	G (200 mA)	2
	346	–	–	–	–	–	–	2
	347	–	–	–	–	–	–	2
	348	–	–	–	–	–	–	2
	349	–	–	–	–	–	–	2
	350	–	–	–	–	–	–	2
	351	–	–	–	–	–	–	2
	352	–	–	–	–	–	–	2

Table 44. EPM7512B I/O Pin-Outs & I/O Standards (Part 12 of 16)

LAB	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
W	353	57	E	F (200 mA)	82	H	G (200 mA)	2
	354	–	–	–	–	–	–	2
	355	–	–	–	–	–	–	2
	356	–	–	–	–	–	–	2
	357	–	–	–	83	H	G (200 mA)	2
	358	–	–	–	–	–	–	2
	359	–	–	–	–	–	–	2
	360	–	–	–	–	–	–	2
	361	58	E	F (200 mA)	84	H	G (200 mA)	2
	362	–	–	–	–	–	–	2
	363	–	–	–	86	I	G (200 mA)	2
	364	–	–	–	–	–	–	2
	365	–	–	–	–	–	–	2
	366	60 *(2)*	F	F (200 mA)	87 *(2)*	I	G (200 mA)	2
	367	–	–	–	–	–	–	2
	368	61	F	F (200 mA)	88	I	G (200 mA)	2
X	369	62 *(1)*	F	F (200 mA)	89 *(1)*	I	G (200 mA)	2
	370	–	–	–	–	–	–	2
	371	–	–	–	–	–	–	2
	372	–	–	–	–	–	–	2
	373	–	–	–	–	–	–	2
	374	–	–	–	–	–	–	2
	375	–	–	–	–	–	–	2
	376	–	–	–	–	–	–	2
	377	–	–	–	–	–	–	2
	378	–	–	–	–	–	–	2
	379	–	–	–	–	–	–	2
	380	–	–	–	–	–	–	2
	381	–	–	–	–	–	–	2
	382	–	–	–	–	–	–	2
	383	–	–	–	–	–	–	2
	384	63	F	F (200 mA)	90	I	G (200 mA)	2

Table 44. EPM7512B I/O Pin-Outs & I/O Standards (Part 13 of 16)

LAB	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
Y	385	–	–	–	91	I	G (200 mA)	2
	386	–	–	–	–	–	–	2
	387	–	–	–	–	–	–	2
	388	–	–	–	–	–	–	2
	389	64	F	F (200 mA)	92	I	G (200 mA)	2
	390	–	–	–	–	–	–	2
	391	–	–	–	–	–	–	2
	392	–	–	–	–	–	–	2
	393	–	–	–	–	–	–	2
	394	–	–	–	–	–	–	2
	395	–	–	–	–	–	–	2
	396	–	–	–	–	–	–	2
	397	–	–	–	–	–	–	2
	398	–	–	–	–	–	–	2
	399	–	–	–	–	–	–	2
	400	65	F	F (200 mA)	93	I	G (200 mA)	2
Z	401	–	–	–	–	–	–	2
	402	–	–	–	–	–	–	2
	403	–	–	–	–	–	–	2
	404	–	–	–	–	–	–	2
	405	–	–	–	94	I	G (200 mA)	2
	406	–	–	–	–	–	–	2
	407	–	–	–	–	–	–	2
	408	–	–	–	–	–	–	2
	409	67	F	G (200 mA)	96	I	H (200 mA)	2
	410	–	–	–	–	–	–	2
	411	–	–	–	–	–	–	2
	412	–	–	–	–	–	–	2
	413	–	–	–	–	–	–	2
	414	68	F	G (200 mA)	97	I	H (200 mA)	2
	415	–	–	–	–	–	–	2
	416	–	–	–	–	–	–	2

Table 44. EPM7512B I/O Pin-Outs & I/O Standards (Part 14 of 16)

LAB	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
AA	417	–	–	–	–	–	–	2
	418	–	–	–	–	–	–	2
	419	–	–	–	–	–	–	2
	420	–	–	–	–	–	–	2
	421	69	F	G (200 mA)	98	I	H (200 mA)	2
	422	–	–	–	–	–	–	2
	423	–	–	–	–	–	–	2
	424	–	–	–	–	–	–	2
	425	–	–	–	–	–	–	2
	426	–	–	–	–	–	–	2
	427	70	F	G (200 mA)	99	I	H (200 mA)	2
	428	–	–	–	–	–	–	2
	429	–	–	–	–	–	–	2
	430	71	F	G (200 mA)	100	I	H (200 mA)	2
	431	–	–	–	–	–	–	2
	432	–	–	–	101	I	H (200 mA)	2
BB	433	–	–	–	–	–	–	2
	434	–	–	–	–	–	–	2
	435	72	F	G (200 mA)	102	I	H (200 mA)	2
	436	–	–	–	–	–	–	2
	437	–	–	–	–	–	–	2
	438	–	–	–	–	–	–	2
	439	–	–	–	–	–	–	2
	440	–	–	–	–	–	–	2
	441	–	–	–	–	–	–	2
	442	–	–	–	–	–	–	2
	443	–	–	–	103	I	H (200 mA)	2
	444	–	–	–	–	–	–	2
	445	–	–	–	–	–	–	2
	446	73 *(1)*	F	G (200 mA)	104 *(1)*	I	H (200 mA)	2
	447	–	–	–	–	–	–	2
	448	75	A	G (200 mA)	106	A	H (200 mA)	2

Table 44. EPM7512B I/O Pin-Outs & I/O Standards (Part 15 of 16)

LAB	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
CC	449	–	–	–	–	–	–	2
	450	–	–	–	–	–	–	2
	451	–	–	–	–	–	–	2
	452	–	–	–	–	–	–	2
	453	76	A	G (200 mA)	107	A	H (200 mA)	2
	454	–	–	–	–	–	–	2
	455	–	–	–	–	–	–	2
	456	–	–	–	–	–	–	2
	457	77	A	G (200 mA)	108	A	H (200 mA)	2
	458	–	–	–	–	–	–	2
	459	–	–	–	–	–	–	2
	460	–	–	–	–	–	–	2
	461	–	–	–	–	–	–	2
	462	–	–	–	–	–	–	2
	463	–	–	–	–	–	–	2
	464	78	A	G (200 mA)	109	A	H (200 mA)	2
DD	465	–	–	–	–	–	–	2
	466	–	–	–	–	–	–	2
	467	–	–	–	–	–	–	2
	468	–	–	–	–	–	–	2
	469	79	A	G (200 mA)	110	A	H (200 mA)	2
	470	–	–	–	–	–	–	2
	471	–	–	–	–	–	–	2
	472	–	–	–	–	–	–	2
	473	80	A	G (200 mA)	111	A	H (200 mA)	2
	474	–	–	–	–	–	–	2
	475	–	–	–	–	–	–	2
	476	–	–	–	–	–	–	2
	477	–	–	–	–	–	–	2
	478	–	–	–	112	A	H (200 mA)	2
	479	–	–	–	–	–	–	2
	480	–	–	–	–	–	–	2

Table 44. EPM7512B I/O Pin-Outs & I/O Standards (Part 16 of 16)

LAB	MC	100-Pin TQFP	IOGND Group for 100-Pin TQFP (200 mA)	IOVCC Group for 100-Pin TQFP	144-Pin TQFP	IOGND Group for 144-Pin TQFP (200 mA)	IOVCC Group for 144-Pin TQFP	I/O Bank
EE	481	–	–	–	–	–	–	2
	482	–	–	–	–	–	–	2
	483	–	–	–	–	–	–	2
	484	–	–	–	–	–	–	2
	485	–	–	–	113	A	H (200 mA)	2
	486	–	–	–	–	–	–	2
	487	–	–	–	–	–	–	2
	488	–	–	–	–	–	–	2
	489	81	A	G (200 mA)	114	A	H (200 mA)	2
	490	–	–	–	–	–	–	2
	491	83	A	H (100 mA)	116	A	I (100 mA)	2
	492	–	–	–	–	–	–	2
	493	–	–	–	–	–	–	2
	494	–	–	–	117	A	I (100 mA)	2
	495	–	–	–	–	–	–	2
	496	–	–	–	–	–	–	2
FF	497	–	–	–	118	A	I (100 mA)	2
	498	–	–	–	–	–	–	2
	499	–	–	–	–	–	–	2
	500	–	–	–	–	–	–	2
	501	–	–	–	–	–	–	2
	502	–	–	–	–	–	–	2
	503	–	–	–	–	–	–	2
	504	–	–	–	–	–	–	2
	505	84	A	H (100 mA)	119	A	I (100 mA)	2
	506	–	–	–	–	–	–	2
	507	–	–	–	120	A	I (100 mA)	2
	508	–	–	–	–	–	–	2
	509	–	–	–	–	–	–	2
	510	–	–	–	121	A	I (100 mA)	2
	511	–	–	–	–	–	–	2
	512	85	A	H (100 mA)	122	A	I (100 mA)	2

Table 45. EPM7512B I/O Pin-Outs & I/O Standards (Part 1 of 16)

LAB	MC	169-Pin Ultra FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
A	1	C6	A	B (200 mA)	173	B	A (100 mA)	1
	2	–	–	–	–	–	–	1
	3	–	–	–	–	–	–	1
	4	–	–	–	–	–	–	1
	5	–	–	–	–	–	–	1
	6	–	–	–	–	–	–	1
	7	–	–	–	–	–	–	1
	8	–	–	–	–	–	–	1
	9	–	–	–	175	A	A (100 mA)	1
	10	–	–	–	–	–	–	1
	11	B6	A	A (100 mA)	176 *(1)*	A	A (100 mA)	1
	12	–	–	–	–	–	–	1
	13	–	–	–	–	–	–	1
	14	A6	A	A (100 mA)	177	A	A (100 mA)	1
	15	–	–	–	–	–	–	1
	16	C7	A	A (100 mA)	178	A	A (100 mA)	1
B	17	–	–	–	169	B	A (100 mA)	1
	18	–	–	–	–	–	–	1
	19	–	–	–	–	–	–	1
	20	–	–	–	–	–	–	1
	21	B5	B	B (200 mA)	170	B	A (100 mA)	1
	22	–	–	–	–	–	–	1
	23	–	–	–	–	–	–	1
	24	–	–	–	–	–	–	1
	25	A5	B	B (200 mA)	171	B	A (100 mA)	1
	26	–	–	–	–	–	–	1
	27	F6	B	B (200 mA)	172	B	A (100 mA)	1
	28	–	–	–	–	–	–	1
	29	–	–	–	–	–	–	1
	30	–	–	–	–	–	–	1
	31	–	–	–	–	–	–	1
	32	–	–	–	–	–	–	1

Table 45. EPM7512B I/O Pin-Outs & I/O Standards (Part 2 of 16)

LAB	MC	169-Pin Ultra FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
C	33	–	–	–	163	B	B (200 mA)	1
	34	–	–	–	–	–	–	1
	35	–	–	–	–	–	–	1
	36	–	–	–	–	–	–	1
	37	A4	B	B (200 mA)	164	B	B (200 mA)	1
	38	–	–	–	–	–	–	1
	39	–	–	–	–	–	–	1
	40	–	–	–	–	–	–	1
	41	D5	B	B (200 mA)	166	B	A (100 mA)	1
	42	–	–	–	–	–	–	1
	43	–	–	–	167	B	A (100 mA)	1
	44	–	–	–	–	–	–	1
	45	–	–	–	–	–	–	1
	46	C5	B	B (200 mA)	168	B	A (100 mA)	1
	47	–	–	–	–	–	–	1
	48	–	–	–	–	–	–	1
D	49	C3	C	C (200 mA)	–	–	–	1
	50	–	–	–	–	–	–	1
	51	–	–	–	–	–	–	1
	52	–	–	–	–	–	–	1
	53	B3	C	C (200 mA)	–	–	–	1
	54	–	–	–	–	–	–	1
	55	–	–	–	–	–	–	1
	56	–	–	–	–	–	–	1
	57	–	–	–	159	B	B (200 mA)	1
	58	–	–	–	–	–	–	1
	59	C4	B	B (200 mA)	160	B	B (200 mA)	1
	60	–	–	–	–	–	–	1
	61	–	–	–	–	–	–	1
	62	–	–	–	161	B	B (200 mA)	1
	63	–	–	–	–	–	–	1
	64	B4	B	B (200 mA)	162	B	B (200 mA)	1

Table 45. EPM7512B I/O Pin-Outs & I/O Standards (Part 3 of 16)

LAB	MC	169-Pin Ultra FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
E	65	C2	D	C (200mA)	–	–	–	1
	66	–	–	–	–	–	–	1
	67	C1	D	C (200 mA)	153	C	B (200 mA)	1
	68	–	–	–	–	–	–	1
	69	–	–	–	–	–	–	1
	70	–	–	–	–	–	–	1
	71	–	–	–	–	–	–	1
	72	–	–	–	–	–	–	1
	73	B1	D	C (200 mA)	154	C	B (200 mA)	1
	74	–	–	–	–	–	–	1
	75	A1	D	C (200 mA)	155	C	B (200 mA)	1
	76	–	–	–	–	–	–	1
	77	–	–	–	–	–	–	1
	78	B2	D	C (200 mA)	156	C	B (200 mA)	1
	79	–	–	–	–	–	–	1
	80	E4	D	C (200 mA)	157	C	B (200 mA)	1
F	81	E2	E	C (200 mA)	147	D	B (200 mA)	1
	82	–	–	–	–	–	–	1
	83	–	–	–	148	D	B (200 mA)	1
	84	–	–	–	–	–	–	1
	85	D4	E	C (200 mA)	149	D	B (200 mA)	1
	86	–	–	–	–	–	–	1
	87	–	–	–	–	–	–	1
	88	–	–	–	–	–	–	1
	89	–	–	–	–	–	–	1
	90	–	–	–	–	–	–	1
	91	D3	E	C (200 mA)	150	D	B (200 mA)	1
	92	–	–	–	–	–	–	1
	93	–	–	–	–	–	–	1
	94	D2	E	C (200 mA)	151	D	B (200 mA)	1
	95	–	–	–	–	–	–	1
	96	D1	D	C (200 mA)	–	–	–	1

Table 45. EPM7512B I/O Pin-Outs & I/O Standards (Part 4 of 16)

LAB	MC	169-Pin Ultra FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
G	97	–	–	–	–	–	–	1
	98	–	–	–	–	–	–	1
	99	F2	F	D (200 mA)	141	D	C (200 mA)	1
	100	–	–	–	–	–	–	1
	101	G4	F	D (200 mA)	142	D	C (200 mA)	1
	102	–	–	–	–	–	–	1
	103	–	–	–	–	–	–	1
	104	–	–	–	–	–	–	1
	105	–	–	–	144	D	B (200 mA)	1
	106	–	–	–	–	–	–	1
	107	E5	E	C (200 mA)	145	D	B (200 mA)	1
	108	–	–	–	–	–	–	1
	109	–	–	–	–	–	–	1
	110	E3	E	C (200 mA)	146	D	B (200 mA)	1
	111	–	–	–	–	–	–	1
	112	–	–	–	–	–	–	1
H	113	G2	G	D (200 mA)	135	D	C (200 mA)	1
	114	–	–	–	–	–	–	1
	115	–	–	–	136	D	C (200 mA)	1
	116	–	–	–	–	–	–	1
	117	G1	G	D (200 mA)	137	D	C (200 mA)	1
	118	–	–	–	–	–	–	1
	119	–	–	–	–	–	–	1
	120	–	–	–	–	–	–	1
	121	–	–	–	–	–	–	1
	122	–	–	–	–	–	–	1
	123	F4	F	D (200 mA)	138	D	C (200 mA)	1
	124	–	–	–	–	–	–	1
	125	–	–	–	–	–	–	1
	126	–	–	–	139	D	C (200 mA)	1
	127	–	–	–	–	–	–	1
	128	F3	F	D (200 mA)	140	D	C (200 mA)	1

Table 45. EPM7512B I/O Pin-Outs & I/O Standards (Part 5 of 16)

LAB	MC	169-Pin Ultra FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
I	129	G6	H	D (200 mA)	–	–	–	1
	130	–	–	–	–	–	–	1
	131	–	–	–	129	E	C (200 mA)	1
	132	–	–	–	–	–	–	1
	133	J4	H	D (200 mA)	130 *(1)*	E	C (200 mA)	1
	134	–	–	–	–	–	–	1
	135	–	–	–	–	–	–	1
	136	–	–	–	–	–	–	1
	137	–	–	–	131	E	C (200 mA)	1
	138	–	–	–	–	–	–	1
	139	G5	H	D (200 mA)	–	–	–	1
	140	–	–	–	–	–	–	1
	141	–	–	–	–	–	–	1
	142	–	–	–	132	E	C (200 mA)	1
	143	–	–	–	–	–	–	1
	144	G3	H	D (200 mA)	133	E	C (200 mA)	1
J	145	–	–	–	122	E	D (200 mA)	1
	146	–	–	–	–	–	–	1
	147	–	–	–	–	–	–	1
	148	–	–	–	–	–	–	1
	149	J2	H	E (200 mA)	123	E	D (200 mA)	1
	150	–	–	–	–	–	–	1
	151	–	–	–	–	–	–	1
	152	–	–	–	–	–	–	1
	153	H4	H	E (200 mA)	124	E	D (200 mA)	1
	154	–	–	–	–	–	–	1
	155	H3	H	D (200 mA)	126	E	C (200 mA)	1
	156	–	–	–	–	–	–	1
	157	–	–	–	–	–	–	1
	158	H2	H	D (200 mA)	127 *(1)*	E	C (200 mA)	1
	159	–	–	–	–	–	–	1
	160	G7	H	D (200 mA)	128 *(2)*	E	C (200 mA)	1

Table 45. EPM7512B I/O Pin-Outs & I/O Standards (Part 6 of 16)

LAB	MC	169-Pin Ultra FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
K	161	K4	I	E (200 mA)	115	F	D (200 mA)	1
	162	–	–	–	–	–	–	1
	163	–	–	–	117	E	D (200 mA)	1
	164	–	–	–	–	–	–	1
	165	K1	H	E (200 mA)	118	E	D (200 mA)	1
	166	–	–	–	–	–	–	1
	167	–	–	–	–	–	–	1
	168	–	–	–	–	–	–	1
	169	J5	H	E (200 mA)	119	E	D (200 mA)	1
	170	–	–	–	–	–	–	1
	171	–	–	–	–	–	–	1
	172	–	–	–	–	–	–	1
	173	–	–	–	–	–	–	1
	174	–	–	–	120	E	D (200 mA)	1
	175	–	–	–	–	–	–	1
	176	J3	H	E (200 mA)	121	E	D (200 mA)	1
L	177	L1	J	E (200 mA)	109	F	D (200 mA)	1
	178	–	–	–	–	–	–	1
	179	–	–	–	–	–	–	1
	180	–	–	–	–	–	–	1
	181	L2	I	E (200 mA)	110	F	D (200 mA)	1
	182	–	–	–	–	–	–	1
	183	–	–	–	–	–	–	1
	184	–	–	–	–	–	–	1
	185	–	–	–	111	F	D (200 mA)	1
	186	–	–	–	–	–	–	1
	187	–	–	–	112	F	D (200 mA)	1
	188	–	–	–	–	–	–	1
	189	–	–	–	–	–	–	1
	190	K2	I	E (200 mA)	113	F	D (200 mA)	1
	191	–	–	–	–	–	–	1
	192	K3	I	E (200 mA)	114	F	D (200 mA)	1

Table 45. EPM7512B I/O Pin-Outs & I/O Standards (Part 7 of 16)

LAB	MC	169-Pin Ultra FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
M	193	–	–	–	101	F	F (200 mA)	1
	194	–	–	–	–	–	–	1
	195	–	–	–	–	–	–	1
	196	–	–	–	–	–	–	1
	197	M3	J	E (200 mA)	102	F	F (200 mA)	1
	198	–	–	–	–	–	–	1
	199	–	–	–	–	–	–	1
	200	–	–	–	–	–	–	1
	201	M2	J	G (200 mA)	103	F	F (200 mA)	1
	202	–	–	–	–	–	–	1
	203	–	–	–	104	F	F (200 mA)	1
	204	–	–	–	–	–	–	1
	205	–	–	–	–	–	–	1
	206	N1	J	F (200 mA)	106	F	E (200 mA)	1
	207	–	–	–	–	–	–	1
	208	M1	J	E (200 mA)	108	F	D (200 mA)	1
N	209	N5	J	G (200 mA)	95	F	F (200 mA)	1
	210	–	–	–	–	–	–	1
	211	–	–	–	–	–	–	1
	212	–	–	–	–	–	–	1
	213	L4	J	G (200 mA)	96	F	F (200 mA)	1
	214	–	–	–	–	–	–	1
	215	–	–	–	–	–	–	1
	216	–	–	–	–	–	–	1
	217	M4	J	G (200 mA)	97	F	F (200 mA)	1
	218	–	–	–	–	–	–	1
	219	N4	J	G (200 mA)	98	F	F (200 mA)	1
	220	–	–	–	–	–	–	1
	221	–	–	–	–	–	–	1
	222	–	–	–	99	F	F (200 mA)	1
	223	–	–	–	–	–	–	1
	224	L3	J	G (200 mA)	100	F	F (200 mA)	1

Table 45. EPM7512B I/O Pin-Outs & I/O Standards (Part 8 of 16)

LAB	MC	169-Pin Ultra FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
O	225	M6	K	G (200 mA)	88	G	F (200 mA)	1
	226	–	–	–	–	–	–	1
	227	N6	K	G (200 mA)	89	G	F (200 mA)	1
	228	–	–	–	–	–	–	1
	229	K5	K	G (200 mA)	90	G	F (200 mA)	1
	230	–	–	–	–	–	–	1
	231	–	–	–	–	–	–	1
	232	–	–	–	–	–	–	1
	233	–	–	–	91	G	F (200 mA)	1
	234	–	–	–	–	–	–	1
	235	L5	K	G (200 mA)	92	G	F (200 mA)	1
	236	–	–	–	–	–	–	1
	237	–	–	–	–	–	–	1
	238	–	–	–	–	–	–	1
	239	–	–	–	–	–	–	1
	240	M5	K	G (200 mA)	93	G	F (200 mA)	1
P	241	H6	K	H (58 mA)	79	G	G (58 mA)	1
	242	–	–	–	–	–	–	1
	243	–	–	–	–	–	–	1
	244	–	–	–	–	–	–	1
	245	–	–	–	80	G	G (58 mA)	1
	246	–	–	–	–	–	–	1
	247	–	–	–	–	–	–	1
	248	–	–	–	–	–	–	1
	249	J6	K	H (58 mA)	81	G	G (58 mA)	1
	250	–	–	–	–	–	–	1
	251	–	–	–	84	G	G (58 mA)	1
	252	–	–	–	–	–	–	1
	253	–	–	–	–	–	–	1
	254	K6	K	G (200 mA)	86	G	F (200 mA)	1
	255	–	–	–	–	–	–	1
	256	L6	K	G (200 mA)	87	G	F (200 mA)	1

Table 45. EPM7512B I/O Pin-Outs & I/O Standards (Part 9 of 16)

LAB	MC	169-Pin Ultra FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
Q	257	K7	K	H (58 mA)	78	G	G (58 mA)	1
	258	–	–	–	–	–	–	1
	259	–	–	–	–	–	–	1
	260	–	–	–	–	–	–	1
	261	–	–	–	77	G	G (58 mA)	1
	262	–	–	–	–	–	–	1
	263	–	–	–	–	–	–	1
	264	–	–	–	–	–	–	1
	265	L7	K	H (58 mA)	76	G	G (58 mA)	1
	266	–	–	–	–	–	–	1
	267	–	–	–	73	G	H (100 mA)	2
	268	–	–	–	–	–	–	2
	269	–	–	–	–	–	–	2
	270	H8	L	I (100 mA)	71	H	H (100 mA)	2
	271	–	–	–	–	–	–	2
	272	J8	–	I (100 mA)	70	H	H (100 mA)	2
R	273	K8	L	I (100 mA)	69	H	H (100 mA)	2
	274	–	–	–	–	–	–	2
	275	L8	L	I (100 mA)	68	H	H (100 mA)	2
	276	–	–	–	–	–	–	2
	277	–	–	–	67	H	H (100 mA)	2
	278	–	–	–	–	–	–	2
	279	–	–	–	–	–	–	2
	280	–	–	–	–	–	–	2
	281	–	–	–	66	H	H (100 mA)	2
	282	–	–	–	–	–	–	2
	283	M8	L	I (100 mA)	65	H	H (100 mA)	2
	284	–	–	–	–	–	–	2
	285	–	–	–	–	–	–	2
	286	–	–	–	–	–	–	2
	287	–	–	–	–	–	–	2
	288	N8	L	I (200 mA)	64	H	H (100 mA)	2

Table 45. EPM7512B I/O Pin-Outs & I/O Standards (Part 10 of 16)

LAB	MC	169-Pin Ultra FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
S	289	K9	L	J (200 mA)	62	H	I (200 mA)	2
	290	–	–	–	–	–	–	2
	291	–	–	–	–	–	–	2
	292	–	–	–	–	–	–	2
	293	L9	L	J (200 mA)	61	H	I (200 mA)	2
	294	–	–	–	–	–	–	2
	295	–	–	–	–	–	–	2
	296	–	–	–	–	–	–	2
	297	M9	L	J (200 mA)	60	H	I (200 mA)	2
	298	–	–	–	–	–	–	2
	299	N9	L	J (200 mA)	59	H	I (200 mA)	2
	300	–	–	–	–	–	–	2
	301	–	–	–	–	–	–	2
	302	–	–	–	58	H	I (200 mA)	2
	303	–	–	–	–	–	–	2
	304	L10	L	J (200 mA)	57	H	I (200 mA)	2
T	305	M10	L	J (200 mA)	56	H	I (200 mA)	2
	306	–	–	–	–	–	–	2
	307	–	–	–	–	–	–	2
	308	–	–	–	–	–	–	2
	309	–	–	–	55	H	I (200 mA)	2
	310	–	–	–	–	–	–	2
	311	–	–	–	–	–	–	2
	312	–	–	–	–	–	–	2
	313	N10	L	J (200 mA)	54	H	I (200 mA)	2
	314	–	–	–	–	–	–	2
	315	L11	L	J (200 mA)	53	H	I (200 mA)	2
	316	–	–	–	–	–	–	2
	317	–	–	–	–	–	–	2
	318	M11	L	K (200 mA)	52	H	I (200 mA)	2
	319	–	–	–	–	–	–	2
	320	N13	M	K (200 mA)	49	I	I (200 mA)	2

Table 45. EPM7512B I/O Pin-Outs & I/O Standards (Part 11 of 16)

LAB	MC	169-Pin Ultra FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
U	321	M12	M	K (200 mA)	48	I	I (200 mA)	2
	322	–	–	–	–	–	–	2
	323	–	–	–	–	–	–	2
	324	–	–	–	–	–	–	2
	325	–	–	–	47	I	I (200 mA)	2
	326	–	–	–	–	–	–	2
	327	–	–	–	–	–	–	2
	328	–	–	–	–	–	–	2
	329	M13	M	L (200 mA)	46	I	I (200 mA)	2
	330	–	–	–	–	–	–	2
	331	–	–	–	45	I	I (200 mA)	2
	332	–	–	–	–	–	–	2
	333	–	–	–	–	–	–	2
	334	L12	M	L (200 mA)	44	I	I (200 mA)	2
	335	–	–	–	–	–	–	2
	336	L13	M	L (200 mA)	43	I	I (200 mA)	2
V	337	K10	M	L (200 mA)	42	I	I (200 mA)	2
	338	–	–	–	–	–	–	2
	339	K11	M	M (200 mA)	40	I	J (200 mA)	2
	340	–	–	–	–	–	–	2
	341	–	–	–	39	I	J (200 mA)	2
	342	–	–	–	–	–	–	2
	343	–	–	–	–	–	–	2
	344	–	–	–	–	–	–	2
	345	K12	M	M (200 mA)	38	I	J (200 mA)	2
	346	–	–	–	–	–	–	2
	347	–	–	–	–	–	–	2
	348	–	–	–	–	–	–	2
	349	–	–	–	–	–	–	2
	350	K13	M	M (200 mA)	37	I	J (200 mA)	2
	351	–	–	–	–	–	–	2
	352	–	–	–	36	I	J (200 mA)	2

Table 45. EPM7512B I/O Pin-Outs & I/O Standards (Part 12 of 16)

LAB	MC	169-Pin Ultra FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
W	353	J9	M	M (200 mA)	35	I	J (200 mA)	2
	354	–	–	–	–	–	–	2
	355	–	–	–	–	–	–	2
	356	–	–	–	–	–	–	2
	357	G10	M	M (200 mA)	34	I	J (200 mA)	2
	358	–	–	–	–	–	–	2
	359	–	–	–	–	–	–	2
	360	–	–	–	–	–	–	2
	361	J11	M	M (200 mA)	33	I	J (200 mA)	2
	362	–	–	–	–	–	–	2
	363	J12	N	M (200 mA)	31	J	J (200 mA)	2
	364	–	–	–	–	–	–	2
	365	–	–	–	–	–	–	2
	366	H10	N	M (200 mA)	30 *(1)*	J	J (200 mA)	2
	367	–	–	–	–	–	–	2
	368	H11	N	M (200 mA)	29	J	J (200 mA)	2
X	369	J10	N	M (200 mA)	–	–	–	2
	370	–	–	–	–	–	–	2
	371	–	–	–	28	J	J (200 mA)	2
	372	–	–	–	–	–	–	2
	373	H12	N	M (200 mA)	27	J	J (200 mA)	2
	374	–	–	–	–	–	–	2
	375	–	–	–	–	–	–	2
	376	–	–	–	–	–	–	2
	377	–	–	–	26	J	J (200 mA)	2
	378	–	–	–	–	–	–	2
	379	G11	N	M (200 mA)	–	–	–	2
	380	–	–	–	–	–	–	2
	381	–	–	–	–	–	–	2
	382	–	–	–	25	J	J (200 mA)	2
	383	–	–	–	–	–	–	2
	384	G12	N	M (200 mA)	24	J	J (200 mA)	2

Table 45. EPM7512B I/O Pin-Outs & I/O Standards (Part 13 of 16)

LAB	MC	169-Pin Ultra FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
Y	385	G13	N	N (200 mA)	22 *(2)*	J	K (200 mA)	2
	386	–	–	–	–	–	–	2
	387	–	–	–	21	J	K (200 mA)	2
	388	–	–	–	–	–	–	2
	389	G9	N	N (200 mA)	20	J	K (200 mA)	2
	390	–	–	–	–	–	–	2
	391	–	–	–	–	–	–	2
	392	–	–	–	–	–	–	2
	393	–	–	–	–	–	–	2
	394	–	–	–	–	–	–	2
	395	G8	N	N (200 mA)	19	J	K (200 mA)	2
	396	–	–	–	–	–	–	2
	397	–	–	–	–	–	–	2
	398	–	–	–	18	J	K (200 mA)	2
	399	–	–	–	–	–	–	2
	400	F12	N	N (200 mA)	17	J	K (200 mA)	2
Z	401	F11	N	N (200 mA)	–	–	–	2
	402	–	–	–	–	–	–	2
	403	–	–	–	16	J	K (200 mA)	2
	404	–	–	–	–	–	–	2
	405	E12	N	N (200 mA)	15	J	K (200 mA)	2
	406	–	–	–	–	–	–	2
	407	–	–	–	–	–	–	2
	408	–	–	–	–	–	–	2
	409	E11	O	O (200 mA)	13	K	K (200 mA)	2
	410	–	–	–	–	–	–	2
	411	–	–	–	12	K	K (200 mA)	2
	412	–	–	–	–	–	–	2
	413	–	–	–	–	–	–	2
	414	F10	O	O (200 mA)	11	K	K (200 mA)	2
	415	–	–	–	–	–	–	2
	416	–	–	–	–	–	–	2

Table 45. EPM7512B I/O Pin-Outs & I/O Standards (Part 14 of 16)

LAB	MC	169-Pin Ultra FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
AA	417	–	–	–	10	K	K (200 mA)	2
	418	–	–	–	–	–	–	2
	419	–	–	–	9	K	K (200 mA)	2
	420	–	–	–	–	–	–	2
	421	E9	O	O (200 mA)	8	K	K (200 mA)	2
	422	–	–	–	–	–	–	2
	423	–	–	–	–	–	–	2
	424	–	–	–	–	–	–	2
	425	–	–	–	–	–	–	2
	426	–	–	–	–	–	–	2
	427	D10	O	O (200 mA)	7	K	K (200 mA)	2
	428	–	–	–	–	–	–	2
	429	–	–	–	–	–	–	2
	430	D11	O	O (200 mA)	6	K	K (200 mA)	2
	431	–	–	–	–	–	–	2
	432	D12	O	P (200 mA)	–	–	–	2
BB	433	–	–	–	–	–	–	2
	434	–	–	–	–	–	–	2
	435	D13	O	P (200 mA)	4	K	L (200 mA)	2
	436	–	–	–	–	–	–	2
	437	C12	O	P (200 mA)	–	–	–	2
	438	–	–	–	–	–	–	2
	439	–	–	–	–	–	–	2
	440	–	–	–	–	–	–	2
	441	C13	O	P (200 mA)	3	K	L (200 mA)	2
	442	–	–	–	–	–	–	2
	443	B13	O	P (200 mA)	2	K	L (200 mA)	2
	444	–	–	–	–	–	–	2
	445	–	–	–	–	–	–	2
	446	E10	O	P (200 mA)	1	K	L (200 mA)	2
	447	–	–	–	–	–	–	2
	448	A13	P	P (200 mA)	208	K	L (200 mA)	2

Table 45. EPM7512B I/O Pin-Outs & I/O Standards (Part 15 of 16)

LAB	MC	169-Pin Ultra FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
CC	449	–	–	–	–	–	–	2
	450	–	–	–	–	–	–	2
	451	–	–	–	–	–	–	2
	452	–	–	–	–	–	–	2
	453	–	–	–	–	–	–	2
	454	–	–	–	–	–	–	2
	455	–	–	–	–	–	–	2
	456	–	–	–	–	–	–	2
	457	B12	P	Q (200 mA)	206	K	M (200 mA)	2
	458	–	–	–	–	–	–	2
	459	–	–	–	205	K	M (200 mA)	2
	460	–	–	–	–	–	–	2
	461	–	–	–	–	–	–	2
	462	C11	P	Q (200 mA)	204	K	M (200 mA)	2
	463	–	–	–	–	–	–	2
	464	B11	P	Q (200 mA)	203	K	M (200 mA)	2
DD	465	–	–	–	202	K	M (200 mA)	2
	466	–	–	–	–	–	–	2
	467	–	–	–	–	–	–	2
	468	–	–	–	–	–	–	2
	469	C10	P	Q (200 mA)	201	K	M (200 mA)	2
	470	–	–	–	–	–	–	2
	471	–	–	–	–	–	–	2
	472	–	–	–	–	–	–	2
	473	B10	P	Q (200 mA)	199	A	M (200 mA)	2
	474	–	–	–	–	–	–	2
	475	–	–	–	198	A	M (200 mA)	2
	476	–	–	–	–	–	–	2
	477	–	–	–	–	–	–	2
	478	A10	P	Q (200 mA)	197	A	M (200 mA)	2
	479	–	–	–	–	–	–	2
	480	–	–	–	–	–	–	2

Table 45. EPM7512B I/O Pin-Outs & I/O Standards (Part 16 of 16)

LAB	MC	169-Pin Ultra FineLine BGA	IOGND Group for 169-Pin Ultra FineLine BGA (200 mA)	IOVCC Group for 169-Pin Ultra FineLine BGA	208-Pin PQFP *(4)*	IOGND Group for 208-Pin PQFP (200 mA)	IOVCC Group for 208-Pin PQFP	I/O Bank
EE	481	–	–	–	196	A	M (200 mA)	2
	482	–	–	–	–	–	–	2
	483	–	–	–	–	–	–	2
	484	–	–	–	–	–	–	2
	485	D9	P	Q (200 mA)	195	A	M (200 mA)	2
	486	–	–	–	–	–	–	2
	487	–	–	–	–	–	–	2
	488	–	–	–	–	–	–	2
	489	C9	P	Q (200 mA)	194	A	M (200 mA)	2
	490	–	–	–	–	–	–	2
	491	B9	P	R (100 mA)	193	A	M (200 mA)	2
	492	–	–	–	–	–	–	2
	493	–	–	–	–	–	–	2
	494	A9	P	R (100 mA)	–	–	–	2
	495	–	–	–	–	–	–	2
	496	–	–	–	–	–	–	2
FF	497	F8	P	R (100 mA)	192	A	M (200 mA)	2
	498	–	–	–	–	–	–	2
	499	–	–	–	–	–	–	2
	500	–	–	–	–	–	–	2
	501	–	–	–	–	–	–	2
	502	–	–	–	–	–	–	2
	503	–	–	–	–	–	–	2
	504	–	–	–	–	–	–	2
	505	C8	A	R (100 mA)	190	A	N (100 mA)	2
	506	–	–	–	–	–	–	2
	507	B8	A	R (100 mA)	189 *(1)*	A	N (100 mA)	2
	508	–	–	–	–	–	–	2
	509	–	–	–	–	–	–	2
	510	A8	A	R (100 mA)	188	A	N (100 mA)	2
	511	–	–	–	–	–	–	2
	512	F7	A	R (100 mA)	187	A	N (100 mA)	2

Table 46. EPM7512B I/O Pin-Outs & I/O Standards (Part 1 of 16)

LAB	MC	256-Pin BGA	IOGND Group for 256-Pin BGA (200 mA)	IOVCC Group for 256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin FineLine BGA (200 mA)	IOVCC Group for 256-Pin FineLine BGA	I/O Bank
A	1	H3	B	B (200 mA)	D7	B	B (200 mA)	1
	2	–	–	–	–	–	–	1
	3	–	–	–	–	–	–	1
	4	–	–	–	–	–	–	1
	5	H2	B	B (200 mA)	C7	B	B (200 mA)	1
	6	–	–	–	–	–	–	1
	7	–	–	–	–	–	–	1
	8	–	–	–	–	–	–	1
	9	H1	A	A (100 mA)	B7	A	A (100 mA)	1
	10	–	–	–	–	–	–	1
	11	J4	A	A (100 mA)	A7	A	A (100 mA)	1
	12	–	–	–	–	–	–	1
	13	–	–	–	–	–	–	1
	14	J3	A	A (100 mA)	F8	A	A (100 mA)	1
	15	–	–	–	–	–	–	1
	16	J2	A	A (100 mA)	B8	A	A (100 mA)	1
B	17	G4	C	B (200 mA)	D6	C	B (200 mA)	1
	18	–	–	–	–	–	–	1
	19	–	–	–	–	–	–	1
	20	–	–	–	–	–	–	1
	21	F1	C	B (200 mA)	C6	C	B (200 mA)	1
	22	–	–	–	–	–	–	1
	23	–	–	–	–	–	–	1
	24	–	–	–	–	–	–	1
	25	G3	C	B (200 mA)	B6	C	B (200 mA)	1
	26	–	–	–	–	–	–	1
	27	G2	C	B (200 mA)	A6	C	B (200 mA)	1
	28	–	–	–	–	–	–	1
	29	–	–	–	–	–	–	1
	30	G1	B	B (200 mA)	F7	B	B (200 mA)	1
	31	–	–	–	–	–	–	1
	32	H4	B	B (200 mA)	E7	B	B (200 mA)	1

Table 46. EPM7512B I/O Pin-Outs & I/O Standards (Part 2 of 16)

LAB	MC	256-Pin BGA	IOGND Group for 256-Pin BGA (200 mA)	IOVCC Group for 256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin FineLine BGA (200 mA)	IOVCC Group for 256-Pin FineLine BGA	I/O Bank
C	33	F4	C	C (200 mA)	E4	C	C (200 mA)	1
	34	–	–	–	–	–	–	1
	35	–	–	–	–	–	–	1
	36	–	–	–	–	–	–	1
	37	E3	C	C (200 mA)	C5	C	C (200 mA)	1
	38	–	–	–	–	–	–	1
	39	–	–	–	–	–	–	1
	40	–	–	–	–	–	–	1
	41	E2	C	B (200 mA)	A5	C	B (200 mA)	1
	42	–	–	–	–	–	–	1
	43	F3	C	B (200 mA)	D5	C	B (200 mA)	1
	44	–	–	–	–	–	–	1
	45	–	–	–	–	–	–	1
	46	E1	C	B (200 mA)	E5	C	B (200 mA)	1
	47	–	–	–	–	–	–	1
	48	F2	C	B (200 mA)	E6	C	B (200 mA)	1
D	49	B3	D	D (200 mA)	B2	D	D (200 mA)	1
	50	–	–	–	–	–	–	1
	51	–	–	–	–	–	–	1
	52	–	–	–	–	–	–	1
	53	C2	D	D (200 mA)	A2	D	D (200 mA)	1
	54	–	–	–	–	–	–	1
	55	–	–	–	–	–	–	1
	56	–	–	–	–	–	–	1
	57	B1	C	C (200 mA)	B4	C	C (200 mA)	1
	58	–	–	–	–	–	–	1
	59	C1	C	C (200 mA)	A4	C	C (200 mA)	1
	60	–	–	–	–	–	–	1
	61	–	–	–	–	–	–	1
	62	D2	C	C (200 mA)	C4	C	C (200 mA)	1
	63	–	–	–	–	–	–	1
	64	D1	C	C (200 mA)	C3	C	C (200 mA)	1

Table 46. EPM7512B I/O Pin-Outs & I/O Standards (Part 3 of 16)

LAB	MC	256-Pin BGA	IOGND Group for 256-Pin BGA (200 mA)	IOVCC Group for 256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin FineLine BGA (200 mA)	IOVCC Group for 256-Pin FineLine BGA	I/O Bank
E	65	B5	E	D (200 mA)	E3	E	D (200 mA)	1
	66	–	–	–	–	–	–	1
	67	C5	E	D (200 mA)	C1	E	D (200 mA)	1
	68	–	–	–	–	–	–	1
	69	D6	E	D (200 mA)	B1	E	D (200 mA)	1
	70	–	–	–	–	–	–	1
	71	–	–	–	–	–	–	1
	72	–	–	–	–	–	–	1
	73	A4	E	D (200 mA)	A1	E	D (200 mA)	1
	74	–	–	–	–	–	–	1
	75	B4	E	D (200 mA)	D2	E	D (200 mA)	1
	76	–	–	–	–	–	–	1
	77	–	–	–	–	–	–	1
	78	A3	E	D (200 mA)	D3	E	D (200 mA)	1
	79	–	–	–	–	–	–	1
	80	A2 *(1)*	E	D (200 mA)	D4 *(1)*	E	D (200 mA)	1
F	81	B7	F	D (200 mA)	F2	F	D (200 mA)	1
	82	–	–	–	–	–	–	1
	83	C7	F	D (200 mA)	F3	F	D (200 mA)	1
	84	–	–	–	–	–	–	1
	85	A6	F	D (200 mA)	F1	F	D (200 mA)	1
	86	–	–	–	–	–	–	1
	87	–	–	–	–	–	–	1
	88	–	–	–	–	–	–	1
	89	D7	F	D (200 mA)	F4	F	D (200 mA)	1
	90	–	–	–	–	–	–	1
	91	B6	F	D (200 mA)	E1	F	D (200 mA)	1
	92	–	–	–	–	–	–	1
	93	–	–	–	–	–	–	1
	94	A5	F	D (200 mA)	D1	F	D (200 mA)	1
	95	–	–	–	–	–	–	1
	96	C6	E	D (200 mA)	E2	E	D (200 mA)	1

Table 46. EPM7512B I/O Pin-Outs & I/O Standards (Part 4 of 16)

LAB	MC	256-Pin BGA	IOGND Group for 256-Pin BGA (200 mA)	IOVCC Group for 256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin FineLine BGA (200 mA)	IOVCC Group for 256-Pin FineLine BGA	I/O Bank
G	97	C9	G	E (200 mA)	H6	G	E (200 mA)	1
	98	–	–	–	–	–	–	1
	99	D9	G	E (200 mA)	G5	G	E (200 mA)	1
	100	–	–	–	–	–	–	1
	101	A8	G	E (200 mA)	G4	G	E (200 mA)	1
	102	–	–	–	–	–	–	1
	103	–	–	–	–	–	–	1
	104	–	–	–	–	–	–	1
	105	B8	F	D (200 mA)	G2	F	D (200 mA)	1
	106	–	–	–	–	–	–	1
	107	C8	F	D (200 mA)	G1	F	D (200 mA)	1
	108	–	–	–	–	–	–	1
	109	–	–	–	–	–	–	1
	110	D8	F	D (200 mA)	G6	F	D (200 mA)	1
	111	–	–	–	–	–	–	1
	112	A7	F	D (200 mA)	F5	F	D (200 mA)	1
H	113	A11	H	E (200 mA)	J1	H	E (200 mA)	1
	114	–	–	–	–	–	–	1
	115	A10	H	E (200 mA)	H7	H	E (200 mA)	1
	116	–	–	–	–	–	–	1
	117	B10	H	E (200 mA)	H5	H	E (200 mA)	1
	118	–	–	–	–	–	–	1
	119	–	–	–	–	–	–	1
	120	–	–	–	–	–	–	1
	121	D10	H	E (200 mA)	H2	H	E (200 mA)	1
	122	–	–	–	–	–	–	1
	123	C10	G	E (200 mA)	H3	G	E (200 mA)	1
	124	–	–	–	–	–	–	1
	125	–	–	–	–	–	–	1
	126	A9	G	E (200 mA)	H1	G	E (200 mA)	1
	127	–	–	–	–	–	–	1
	128	B9	G	E (200 mA)	H4	G	E (200 mA)	1

Table 46. EPM7512B I/O Pin-Outs & I/O Standards (Part 5 of 16)

LAB	MC	256-Pin BGA	IOGND Group for 256-Pin BGA (200 mA)	IOVCC Group for 256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin FineLine BGA (200 mA)	IOVCC Group for 256-Pin FineLine BGA	I/O Bank
I	129	D12	I	E (200 mA)	K1	I	E (200 mA)	1
	130	–	–	–	–	–	–	1
	131	C12 *(2)*	I	E (200 mA)	J7	I	E (200 mA)	1
	132	–	–	–	–	–	–	1
	133	B12 *(1)*	I	E (200 mA)	J6 *(1)*	I	E (200 mA)	1
	134	–	–	–	–	–	–	1
	135	–	–	–	–	–	–	1
	136	–	–	–	–	–	–	1
	137	A12	I	E (200 mA)	J5	I	E (200 mA)	1
	138	–	–	–	–	–	–	1
	139	D11	I	E (200 mA)	J4 *(2)*	I	E (200 mA)	1
	140	–	–	–	–	–	–	1
	141	–	–	–	–	–	–	1
	142	C11	I	E (200 mA)	J3	I	E (200 mA)	1
	143	–	–	–	–	–	–	1
	144	B11	I	E (200 mA)	J2	I	E (200 mA)	1
J	145	C14	I	F (200 mA)	L2	I	F (200 mA)	1
	146	–	–	–	–	–	–	1
	147	B14	I	F (200 mA)	L1	I	F (200 mA)	1
	148	–	–	–	–	–	–	1
	149	A14	I	F (200 mA)	K6	I	F (200 mA)	1
	150	–	–	–	–	–	–	1
	151	–	–	–	–	–	–	1
	152	–	–	–	–	–	–	1
	153	D13	I	F (200 mA)	K5	I	F (200 mA)	1
	154	–	–	–	–	–	–	1
	155	C13	I	E (200 mA)	K4	I	E (200 mA)	1
	156	–	–	–	–	–	–	1
	157	–	–	–	–	–	–	1
	158	B13	I	E (200 mA)	K3	I	E (200 mA)	1
	159	–	–	–	–	–	–	1
	160	A13	I	E (200 mA)	K2	I	E (200 mA)	1

Table 46. EPM7512B I/O Pin-Outs & I/O Standards (Part 6 of 16)

LAB	MC	256-Pin BGA	IOGND Group for 256-Pin BGA (200 mA)	IOVCC Group for 256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin FineLine BGA (200 mA)	IOVCC Group for 256-Pin FineLine BGA	I/O Bank
K	161	B16	J	F (200 mA)	N4	J	F (200 mA)	1
	162	–	–	–	–	–	–	1
	163	C15	I	F (200 mA)	M2	I	F (200 mA)	1
	164	–	–	–	–	–	–	1
	165	A17	I	F (200 mA)	M1	I	F (200 mA)	1
	166	–	–	–	–	–	–	1
	167	–	–	–	–	–	–	1
	168	–	–	–	–	–	–	1
	169	B15	I	F (200 mA)	M4	I	F (200 mA)	1
	170	–	–	–	–	–	–	1
	171	D14	I	F (200 mA)	M5	I	F (200 mA)	1
	172	–	–	–	–	–	–	1
	173	–	–	–	–	–	–	1
	174	A16	I	F (200 mA)	L5	I	F (200 mA)	1
	175	–	–	–	–	–	–	1
	176	A15	I	F (200 mA)	L4	I	F (200 mA)	1
L	177	A20	K	F (200 mA)	R1	J	F (200 mA)	1
	178	–	–	–	–	–	–	1
	179	–	–	–	–	–	–	1
	180	–	–	–	–	–	–	1
	181	A19	J	F (200 mA)	P2	J	F (200 mA)	1
	182	–	–	–	–	–	–	1
	183	–	–	–	–	–	–	1
	184	–	–	–	–	–	–	1
	185	B17	J	F (200 mA)	N3	J	F (200 mA)	1
	186	–	–	–	–	–	–	1
	187	A18	J	F (200 mA)	N2	J	F (200 mA)	1
	188	–	–	–	–	–	–	1
	189	–	–	–	–	–	–	1
	190	D15	J	F (200 mA)	P1	J	F (200 mA)	1
	191	–	–	–	–	–	–	1
	192	C16	J	F (200 mA)	N1	J	F (200 mA)	1

Table 46. EPM7512B I/O Pin-Outs & I/O Standards (Part 7 of 16)

LAB	MC	256-Pin BGA	IOGND Group for 256-Pin BGA (200 mA)	IOVCC Group for 256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin FineLine BGA (200 mA)	IOVCC Group for 256-Pin FineLine BGA	I/O Bank
M	193	E18	K	H (200 mA)	P5	J	G (200 mA)	1
	194	–	–	–	–	–	–	1
	195	–	–	–	–	–	–	1
	196	–	–	–	–	–	–	1
	197	D20	K	H (200 mA)	N5	J	G (200 mA)	1
	198	–	–	–	–	–	–	1
	199	–	–	–	–	–	–	1
	200	–	–	–	–	–	–	1
	201	D19	K	H (200 mA)	T4	J	G (200 mA)	1
	202	–	–	–	–	–	–	1
	203	C20	K	H (200 mA)	R4	J	G (200 mA)	1
	204	–	–	–	–	–	–	1
	205	–	–	–	–	–	–	1
	206	C19	K	G (200 mA)	P4	J	F (200 mA)	1
	207	–	–	–	–	–	–	1
	208	B18	K	F (200 mA)	P3	J	F (200 mA)	1
N	209	G17	K	I (200 mA)	R6	J	H (200 mA)	1
	210	–	–	–	–	–	–	1
	211	–	–	–	–	–	–	1
	212	–	–	–	–	–	–	1
	213	F19	K	I (200 mA)	T6	J	H (200 mA)	1
	214	–	–	–	–	–	–	1
	215	–	–	–	–	–	–	1
	216	–	–	–	–	–	–	1
	217	E20	K	I (200 mA)	N6	J	H (200 mA)	1
	218	–	–	–	–	–	–	1
	219	F18	K	I (200 mA)	M6	J	H (200 mA)	1
	220	–	–	–	–	–	–	1
	221	–	–	–	–	–	–	1
	222	E19	K	I (200 mA)	R5	J	H (200 mA)	1
	223	–	–	–	–	–	–	1
	224	F17	K	H (200 mA)	T5	J	G (200 mA)	1

Table 46. EPM7512B I/O Pin-Outs & I/O Standards (Part 8 of 16)

LAB	MC	256-Pin BGA	IOGND Group for 256-Pin BGA (200 mA)	IOVCC Group for 256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin FineLine BGA (200 mA)	IOVCC Group for 256-Pin FineLine BGA	I/O Bank
O	225	H19	L	I (200 mA)	R7	K	H (200 mA)	1
	226	–	–	–	–	–	–	1
	227	H18	L	I (200 mA)	P7	K	H (200 mA)	1
	228	–	–	–	–	–	–	1
	229	H17	L	I (200 mA)	T7	K	H (200 mA)	1
	230	–	–	–	–	–	–	1
	231	–	–	–	–	–	–	1
	232	–	–	–	–	–	–	1
	233	G20	L	I (200 mA)	L8	K	H (200 mA)	1
	234	–	–	–	–	–	–	1
	235	G19	L	I (200 mA)	N7	K	H (200 mA)	1
	236	–	–	–	–	–	–	1
	237	–	–	–	–	–	–	1
	238	G18	L	I (200 mA)	M7	K	H (200 mA)	1
	239	–	–	–	–	–	–	1
	240	F20	L	I (200 mA)	L7	K	H (200 mA)	1
P	241	K20	L	J (58 mA)	M9	K	I (58 mA)	1
	242	–	–	–	–	–	–	1
	243	–	–	–	–	–	–	1
	244	–	–	–	–	–	–	1
	245	K19	L	J (58 mA)	L9	K	I (58 mA)	1
	246	–	–	–	–	–	–	1
	247	–	–	–	–	–	–	1
	248	–	–	–	–	–	–	1
	249	K17	L	J (58 mA)	R8	K	I (58 mA)	1
	250	–	–	–	–	–	–	1
	251	J18	L	J (58 mA)	T8	K	I (58 mA)	1
	252	–	–	–	–	–	–	1
	253	–	–	–	–	–	–	1
	254	J17	L	I (200 mA)	N8	K	H (200 mA)	1
	255	–	–	–	–	–	–	1
	256	H20	L	I (200 mA)	M8	K	H (200 mA)	1

Table 46. EPM7512B I/O Pin-Outs & I/O Standards (Part 9 of 16)

LAB	MC	256-Pin BGA	IOGND Group for 256-Pin BGA (200 mA)	IOVCC Group for 256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin FineLine BGA (200 mA)	IOVCC Group for 256-Pin FineLine BGA	I/O Bank
Q	257	L20	L	J (58 mA)	N9	K	I (58 mA)	1
	258	–	–	–	–	–	–	1
	259	–	–	–	–	–	–	1
	260	–	–	–	–	–	–	1
	261	L19	L	J (58 mA)	T9	K	I (58 mA)	1
	262	–	–	–	–	–	–	1
	263	–	–	–	–	–	–	1
	264	–	–	–	–	–	–	1
	265	L18	L	J (58 mA)	R9	K	I (58 mA)	1
	266	–	–	–	–	–	–	1
	267	M18	L	K (100 mA)	L10	K	J (100 mA)	2
	268	–	–	–	–	–	–	2
	269	–	–	–	–	–	–	2
	270	M17	M	K (100 mA)	M10	L	J (100 mA)	2
	271	–	–	–	–	–	–	2
	272	N20	M	K (100 mA)	N10	L	J (100 mA)	2
R	273	N19	M	K (100 mA)	R10	L	J (100 mA)	2
	274	–	–	–	–	–	–	2
	275	N18	M	K (100 mA)	T10	L	J (100 mA)	2
	276	–	–	–	–	–	–	2
	277	N17	N	K (100 mA)	M11	M	J (100 mA)	2
	278	–	–	–	–	–	–	2
	279	–	–	–	–	–	–	2
	280	–	–	–	–	–	–	2
	281	P20	N	K (100 mA)	N11	M	J (100 mA)	2
	282	–	–	–	–	–	–	2
	283	P19	N	K (100 mA)	P11	M	J (100 mA)	2
	284	–	–	–	–	–	–	2
	285	–	–	–	–	–	–	2
	286	P18	N	K (100 mA)	R11	M	J (100 mA)	2
	287	–	–	–	–	–	–	2
	288	R20	N	K (100 mA)	T11	M	J (100 mA)	2

Table 46. EPM7512B I/O Pin-Outs & I/O Standards (Part 10 of 16)

LAB	MC	256-Pin BGA	IOGND Group for 256-Pin BGA (200 mA)	IOVCC Group for 256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin FineLine BGA (200 mA)	IOVCC Group for 256-Pin FineLine BGA	I/O Bank
S	289	P17	N	L (200 mA)	K11	M	K (200 mA)	2
	290	–	–	–	–	–	–	2
	291	–	–	–	–	–	–	2
	292	–	–	–	–	–	–	2
	293	R19	N	L (200 mA)	M12	M	K (200 mA)	2
	294	–	–	–	–	–	–	2
	295	–	–	–	–	–	–	2
	296	–	–	–	–	–	–	2
	297	T20	N	L (200 mA)	N12	M	K (200 mA)	2
	298	–	–	–	–	–	–	2
	299	R18	N	L (200 mA)	T12	M	K (200 mA)	2
	300	–	–	–	–	–	–	2
	301	–	–	–	–	–	–	2
	302	T19	N	L (200 mA)	R12	M	K (200 mA)	2
	303	–	–	–	–	–	–	2
	304	T18	N	L (200 mA)	T13	M	K (200 mA)	2
T	305	R17	N	L (200 mA)	P12	M	K (200 mA)	2
	306	–	–	–	–	–	–	2
	307	–	–	–	–	–	–	2
	308	–	–	–	–	–	–	2
	309	U20	N	L (200 mA)	T14	M	K (200 mA)	2
	310	–	–	–	–	–	–	2
	311	–	–	–	–	–	–	2
	312	–	–	–	–	–	–	2
	313	U19	N	L (200 mA)	P13	M	K (200 mA)	2
	314	–	–	–	–	–	–	2
	315	V20	N	L (200 mA)	R13	M	K (200 mA)	2
	316	–	–	–	–	–	–	2
	317	–	–	–	–	–	–	2
	318	W20	N	M (200 mA)	R14	M	L (200 mA)	2
	319	–	–	–	–	–	–	2
	320	W18	O	M (200 mA)	R15	N	L (200 mA)	2

Table 46. EPM7512B I/O Pin-Outs & I/O Standards (Part 11 of 16)

LAB	MC	256-Pin BGA	IOGND Group for 256-Pin BGA (200 mA)	IOVCC Group for 256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin FineLine BGA (200 mA)	IOVCC Group for 256-Pin FineLine BGA	I/O Bank
U	321	Y19	O	M (200 mA)	P15	N	L (200 mA)	2
	322	–	–	–	–	–	–	2
	323	–	–	–	–	–	–	2
	324	–	–	–	–	–	–	2
	325	Y18	O	N (200 mA)	N15	N	L (200 mA)	2
	326	–	–	–	–	–	–	2
	327	–	–	–	–	–	–	2
	328	–	–	–	–	–	–	2
	329	W17	O	N (200 mA)	T16	N	L (200 mA)	2
	330	–	–	–	–	–	–	2
	331	Y17	O	N (200 mA)	R16	N	L (200 mA)	2
	332	–	–	–	–	–	–	2
	333	–	–	–	–	–	–	2
	334	U15	O	N (200 mA)	P16	N	L (200 mA)	2
	335	–	–	–	–	–	–	2
	336	V16	O	N (200 mA)	N14	N	L (200 mA)	2
V	337	W16	O	N (200 mA)	N16	N	L (200 mA)	2
	338	–	–	–	–	–	–	2
	339	V15	O	O (200 mA)	M14	N	M (200 mA)	2
	340	–	–	–	–	–	–	2
	341	Y16	O	O (200 mA)	N13	N	M (200 mA)	2
	342	–	–	–	–	–	–	2
	343	–	–	–	–	–	–	2
	344	–	–	–	–	–	–	2
	345	W15	O	O (200 mA)	M16	N	M (200 mA)	2
	346	–	–	–	–	–	–	2
	347	U14	O	O (200 mA)	M13	N	M (200 mA)	2
	348	–	–	–	–	–	–	2
	349	–	–	–	–	–	–	2
	350	Y15	O	O (200 mA)	L14	N	M (200 mA)	2
	351	–	–	–	–	–	–	2
	352	V14	O	O (200 mA)	L15	N	M (200 mA)	2

Table 46. EPM7512B I/O Pin-Outs & I/O Standards (Part 12 of 16)

LAB	MC	256-Pin BGA	IOGND Group for 256-Pin BGA (200 mA)	IOVCC Group for 256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin FineLine BGA (200 mA)	IOVCC Group for 256-Pin FineLine BGA	I/O Bank
W	353	W14	O	O (200 mA)	L16	N	M (200 mA)	2
	354	–	–	–	–	–	–	2
	355	Y14	O	O (200 mA)	L13	N	M (200 mA)	2
	356	–	–	–	–	–	–	2
	357	U13	O	O (200 mA)	L12	N	M (200 mA)	2
	358	–	–	–	–	–	–	2
	359	–	–	–	–	–	–	2
	360	–	–	–	–	–	–	2
	361	V13	O	O (200 mA)	K12	N	M (200 mA)	2
	362	–	–	–	–	–	–	2
	363	W13	P	O (200 mA)	K14	O	M (200 mA)	2
	364	–	–	–	–	–	–	2
	365	–	–	–	–	–	–	2
	366	Y13	P	O (200 mA)	K15	O	M (200 mA)	2
	367	–	–	–	–	–	–	2
	368	U12	P	O (200 mA)	K16	O	M (200 mA)	2
X	369	V12 *(1)*	P	O (200 mA)	J11 *(1)*	O	M (200 mA)	2
	370	–	–	–	–	–	–	2
	371	W12	P	O (200 mA)	J12	O	M (200 mA)	2
	372	–	–	–	–	–	–	2
	373	Y12	P	O (200 mA)	J13	O	M (200 mA)	2
	374	–	–	–	–	–	–	2
	375	–	–	–	–	–	–	2
	376	–	–	–	–	–	–	2
	377	V11	P	O (200 mA)	J14	O	M (200 mA)	2
	378	–	–	–	–	–	–	2
	379	U11	P	O (200 mA)	J15	O	M (200 mA)	2
	380	–	–	–	–	–	–	2
	381	–	–	–	–	–	–	2
	382	W11	P	O (200 mA)	K13	O	M (200 mA)	2
	383	–	–	–	–	–	–	2
	384	Y11	P	O (200 mA)	J16	O	M (200 mA)	2

Table 46. EPM7512B I/O Pin-Outs & I/O Standards (Part 13 of 16)

LAB	MC	256-Pin BGA	IOGND Group for 256-Pin BGA (200 mA)	IOVCC Group for 256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin FineLine BGA (200 mA)	IOVCC Group for 256-Pin FineLine BGA	I/O Bank
Y	385	Y10	P	P (200 mA)	H10	O	N (200 mA)	2
	386	–	–	–	–	–	–	2
	387	W10	P	P (200 mA)	H11 *(2)*	O	N (200 mA)	2
	388	–	–	–	–	–	–	2
	389	V10 *(2)*	P	P (200 mA)	H12	O	N (200 mA)	2
	390	–	–	–	–	–	–	2
	391	–	–	–	–	–	–	2
	392	–	–	–	–	–	–	2
	393	U10	P	P (200 mA)	H15	O	N (200 mA)	2
	394	–	–	–	–	–	–	2
	395	Y9	P	P (200 mA)	H16	O	N (200 mA)	2
	396	–	–	–	–	–	–	2
	397	–	–	–	–	–	–	2
	398	W9	P	P (200 mA)	H14	O	N (200 mA)	2
	399	–	–	–	–	–	–	2
	400	V9	P	P (200 mA)	H13	O	N (200 mA)	2
Z	401	U9	P	P (200 mA)	G12	O	N (200 mA)	2
	402	–	–	–	–	–	–	2
	403	Y8	P	P (200 mA)	G13	O	N (200 mA)	2
	404	–	–	–	–	–	–	2
	405	W8	P	P (200 mA)	G14	O	N (200 mA)	2
	406	–	–	–	–	–	–	2
	407	–	–	–	–	–	–	2
	408	–	–	–	–	–	–	2
	409	V8	Q	Q (200 mA)	G16	P	O (200 mA)	2
	410	–	–	–	–	–	–	2
	411	U8	Q	Q (200 mA)	G11	P	O (200 mA)	2
	412	–	–	–	–	–	–	2
	413	–	–	–	–	–	–	2
	414	Y7	Q	Q (200 mA)	F12	P	O (200 mA)	2
	415	–	–	–	–	–	–	2
	416	W7	Q	Q (200 mA)	F13	P	O (200 mA)	2

Table 46. EPM7512B I/O Pin-Outs & I/O Standards (Part 14 of 16)

LAB	MC	256-Pin BGA	IOGND Group for 256-Pin BGA (200 mA)	IOVCC Group for 256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin FineLine BGA (200 mA)	IOVCC Group for 256-Pin FineLine BGA	I/O Bank
AA	417	V7	Q	Q (200 mA)	F14	P	O (200 mA)	2
	418	–	–	–	–	–	–	2
	419	Y6	Q	Q (200 mA)	F15	P	O (200 mA)	2
	420	–	–	–	–	–	–	2
	421	U7	Q	Q (200 mA)	F16	P	O (200 mA)	2
	422	–	–	–	–	–	–	2
	423	–	–	–	–	–	–	2
	424	–	–	–	–	–	–	2
	425	W6	Q	Q (200 mA)	E12	P	O (200 mA)	2
	426	–	–	–	–	–	–	2
	427	Y5	Q	Q (200 mA)	E13	P	O (200 mA)	2
	428	–	–	–	–	–	–	2
	429	–	–	–	–	–	–	2
	430	V6	Q	Q (200 mA)	E14	P	O (200 mA)	2
	431	–	–	–	–	–	–	2
	432	W5	Q	R (200 mA)	E16	P	P (200 mA)	2
BB	433	V5	Q	R (200 mA)	D16	P	P (200 mA)	2
	434	–	–	–	–	–	–	2
	435	U6	Q	R (200 mA)	C16	P	P (200 mA)	2
	436	–	–	–	–	–	–	2
	437	Y4	Q	R (200 mA)	B16	P	P (200 mA)	2
	438	–	–	–	–	–	–	2
	439	–	–	–	–	–	–	2
	440	–	–	–	–	–	–	2
	441	W4	Q	R (200 mA)	A16	P	P (200 mA)	2
	442	–	–	–	–	–	–	2
	443	Y3	Q	R (200 mA)	D15	P	P (200 mA)	2
	444	–	–	–	–	–	–	2
	445	–	–	–	–	–	–	2
	446	Y2 *(1)*	Q	R (200 mA)	D13 *(1)*	P	P (200 mA)	2
	447	–	–	–	–	–	–	2
	448	W3	R	R (200 mA)	C15	Q	P (200 mA)	2

Table 46. EPM7512B I/O Pin-Outs & I/O Standards (Part 15 of 16)

LAB	MC	256-Pin BGA	IOGND Group for 256-Pin BGA (200 mA)	IOVCC Group for 256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin FineLine BGA (200 mA)	IOVCC Group for 256-Pin FineLine BGA	I/O Bank
CC	449	W1	R	S (200 mA)	B15	Q	Q (200 mA)	2
	450	–	–	–	–	–	–	2
	451	–	–	–	–	–	–	2
	452	–	–	–	–	–	–	2
	453	V1	R	S (200 mA)	A15	Q	Q (200 mA)	2
	454	–	–	–	–	–	–	2
	455	–	–	–	–	–	–	2
	456	–	–	–	–	–	–	2
	457	U2	R	S (200 mA)	B14	Q	Q (200 mA)	2
	458	–	–	–	–	–	–	2
	459	U1	R	S (200 mA)	A14	Q	Q (200 mA)	2
	460	–	–	–	–	–	–	2
	461	–	–	–	–	–	–	2
	462	T3	R	S (200 mA)	B13	Q	Q (200 mA)	2
	463	–	–	–	–	–	–	2
	464	R4	R	S (200 mA)	A13	Q	Q (200 mA)	2
DD	465	T2	R	S (200 mA)	C13	Q	Q (200 mA)	2
	466	–	–	–	–	–	–	2
	467	–	–	–	–	–	–	2
	468	–	–	–	–	–	–	2
	469	R3	R	S (200 mA)	D12	Q	Q (200 mA)	2
	470	–	–	–	–	–	–	2
	471	–	–	–	–	–	–	2
	472	–	–	–	–	–	–	2
	473	T1	S	S (200 mA)	C12	R	Q (200 mA)	2
	474	–	–	–	–	–	–	2
	475	R2	S	S (200 mA)	B12	R	Q (200 mA)	2
	476	–	–	–	–	–	–	2
	477	–	–	–	–	–	–	2
	478	P4	S	S (200 mA)	A12	R	Q (200 mA)	2
	479	–	–	–	–	–	–	2
	480	R1	S	S (200 mA)	E11	R	Q (200 mA)	2

Table 46. EPM7512B I/O Pin-Outs & I/O Standards (Part 16 of 16)

LAB	MC	256-Pin BGA	IOGND Group for 256-Pin BGA (200 mA)	IOVCC Group for 256-Pin BGA	256-Pin FineLine BGA	IOGND Group for 256-Pin FineLine BGA (200 mA)	IOVCC Group for 256-Pin FineLine BGA	I/O Bank
EE	481	P3	S	S (200 mA)	D11	R	Q (200 mA)	2
	482	–	–	–	–	–	–	2
	483	–	–	–	–	–	–	2
	484	–	–	–	–	–	–	2
	485	P2	S	S (200 mA)	C11	R	Q (200 mA)	2
	486	–	–	–	–	–	–	2
	487	–	–	–	–	–	–	2
	488	–	–	–	–	–	–	2
	489	P1	S	S (200 mA)	A11	R	Q (200 mA)	2
	490	–	–	–	–	–	–	2
	491	N4	S	T (200 mA)	B11	R	R (200 mA)	2
	492	–	–	–	–	–	–	2
	493	–	–	–	–	–	–	2
	494	N3	S	T (200 mA)	F10	R	R (200 mA)	2
	495	–	–	–	–	–	–	2
	496	N2	S	T (200 mA)	E10	R	R (200 mA)	2
FF	497	N1	S	T (200 mA)	D10	R	R (200 mA)	2
	498	–	–	–	–	–	–	2
	499	–	–	–	–	–	–	2
	500	–	–	–	–	–	–	2
	501	M4	S	T (200 mA)	C10	R	R (200 mA)	2
	502	–	–	–	–	–	–	2
	503	–	–	–	–	–	–	2
	504	–	–	–	–	–	–	2
	505	M3	A	U (100 mA)	A10	A	S (100 mA)	2
	506	–	–	–	–	–	–	2
	507	M2	A	U (100 mA)	J10	A	S (100 mA)	2
	508	–	–	–	–	–	–	2
	509	–	–	–	–	–	–	2
	510	M1	A	U (100 mA)	F9	A	S (100 mA)	2
	511	–	–	–	–	–	–	2
	512	L3	A	U (100 mA)	A9	A	S (100 mA)	2

Notes to tables:

(1) The EPM7512B device in the 208-pin PQFP package supports vertical migration from the EPM7256E, EPM7256S, and EPM7256B devices. The EPM7512B device contains additional I/O pins which are no connects on the EPM7256E, EPM7256S, and EPM7256B devices. To support these additional I/O pins, the EPM7512B device has two additional VCCIO (pins 105 and 207) and GNDIO (pins 51 and 158) pins that are no-connect pins on the EPM7256E, EPM7256S, and EPM7256B devices. To achieve vertical migration between the EPM7256B and EPM7512B devices, the no-connect pins 105 and 207 may be tied to VCCIO, and pins 51 and 158 may be tied to GNDIO on the EPM7256B devices. On the EPM7256E and EPM7256S devices, these no-connect pins must not be tied to VCCIO or GNDIO. EPM7512B devices have identical pin-outs.

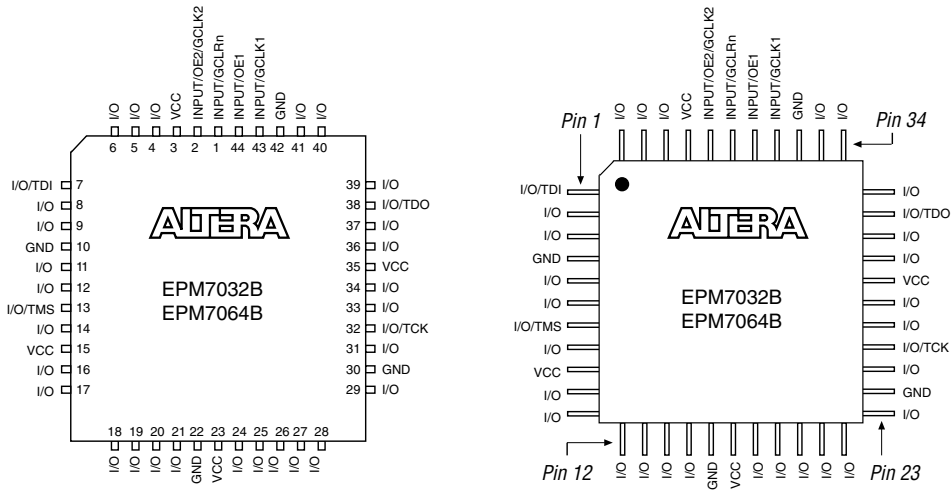
(2) This pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for in-system programming, this pin is not available as a user I/O pin.

(3) The user I/O pin count includes dedicated input pins and all I/O pins.

Figures 20 through 29 show the package pin-out diagrams for MAX 7000B devices.

Figure 20. 44-Pin PLCC/TQFP Package Pin-Out Diagram

Package outlines not drawn to scale.



44-Pin PLCC 44-Pin TQFP

Figure 21. 48-Pin VTQFP Package Pin-Out Diagram

Package outlines not drawn to scale.

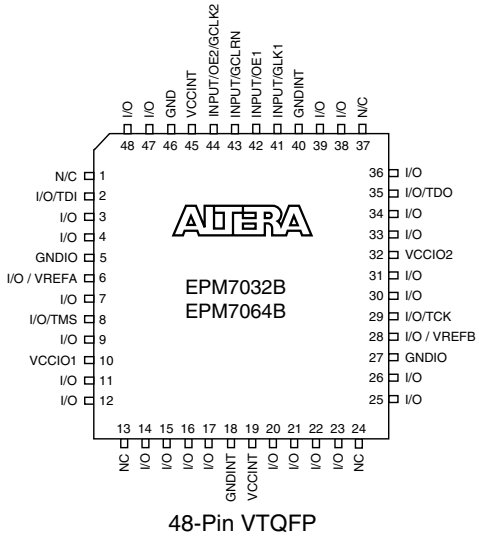


Figure 22. 49-Pin Ultra FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.

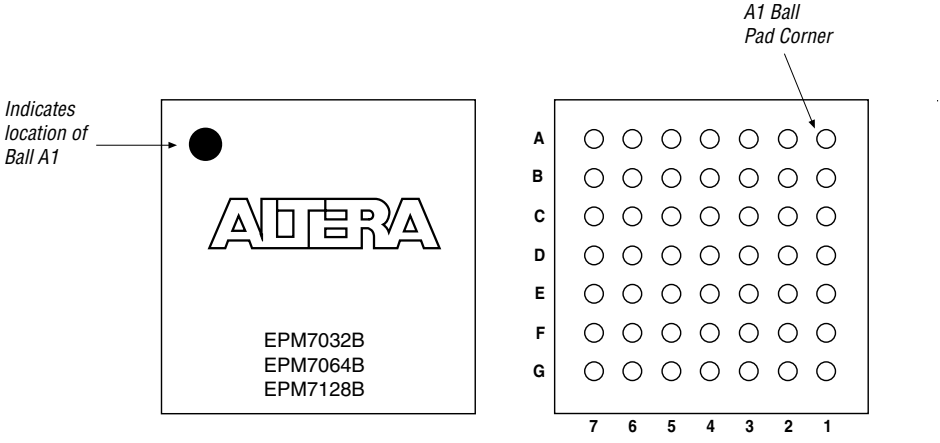


Figure 23. 100-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

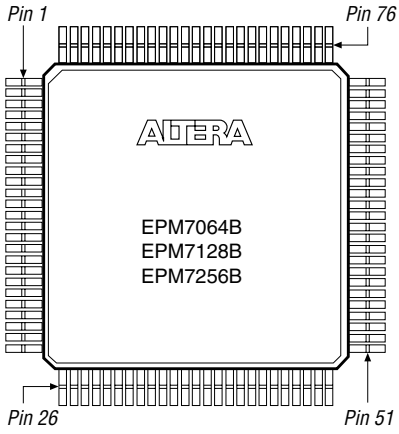


Figure 24. 100-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.

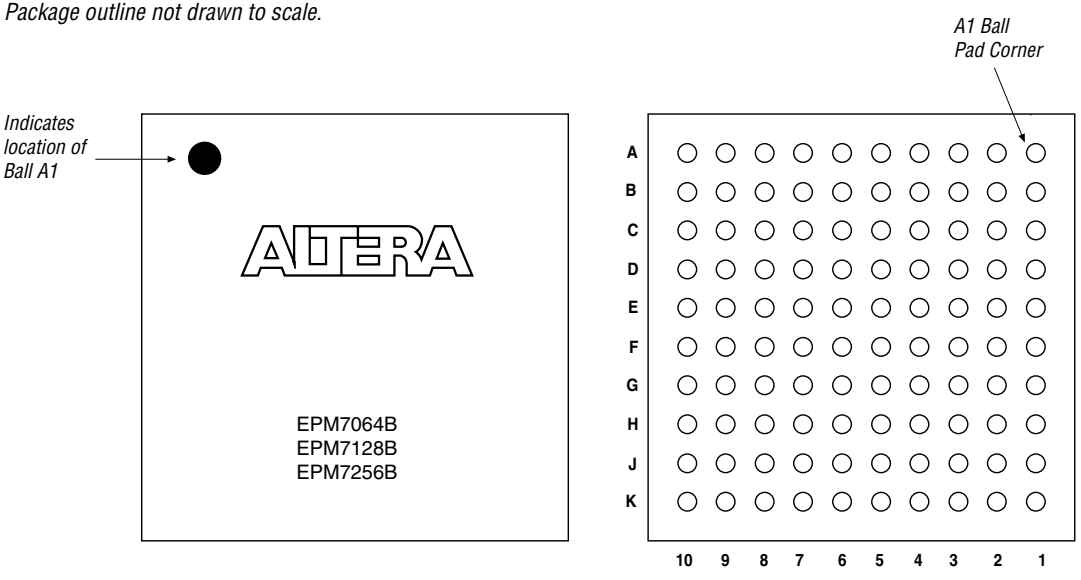


Figure 25. 144-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.

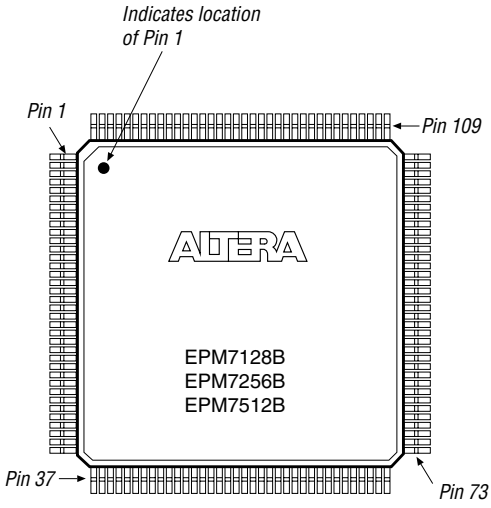


Figure 26. 169-Pin Ultra FineLine BGA Pin-Out Diagram

Package outline not drawn to scale.

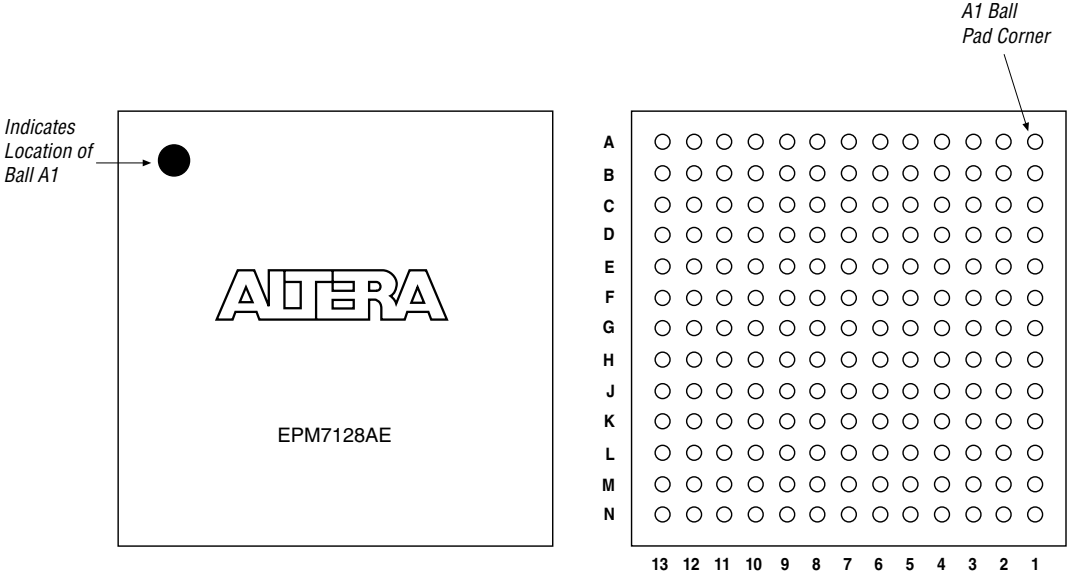


Figure 27. 208-Pin PQFP Package Pin-Out Diagram

Package outline not drawn to scale.

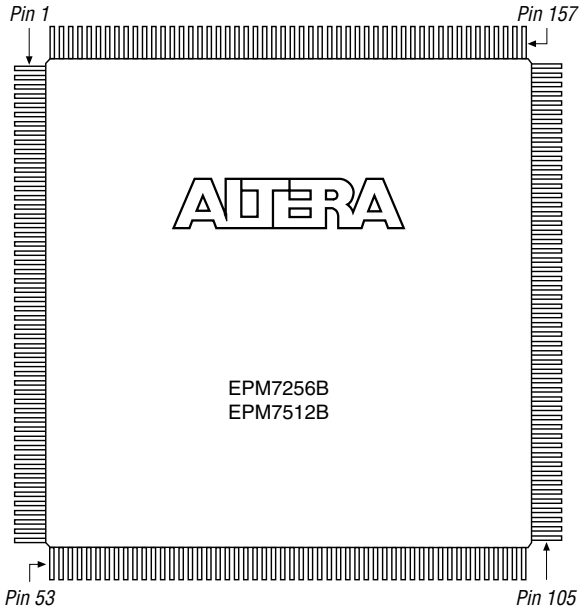


Figure 28. 256-Pin BGA Package Pin-Out Diagram

Package outline not drawn to scale.

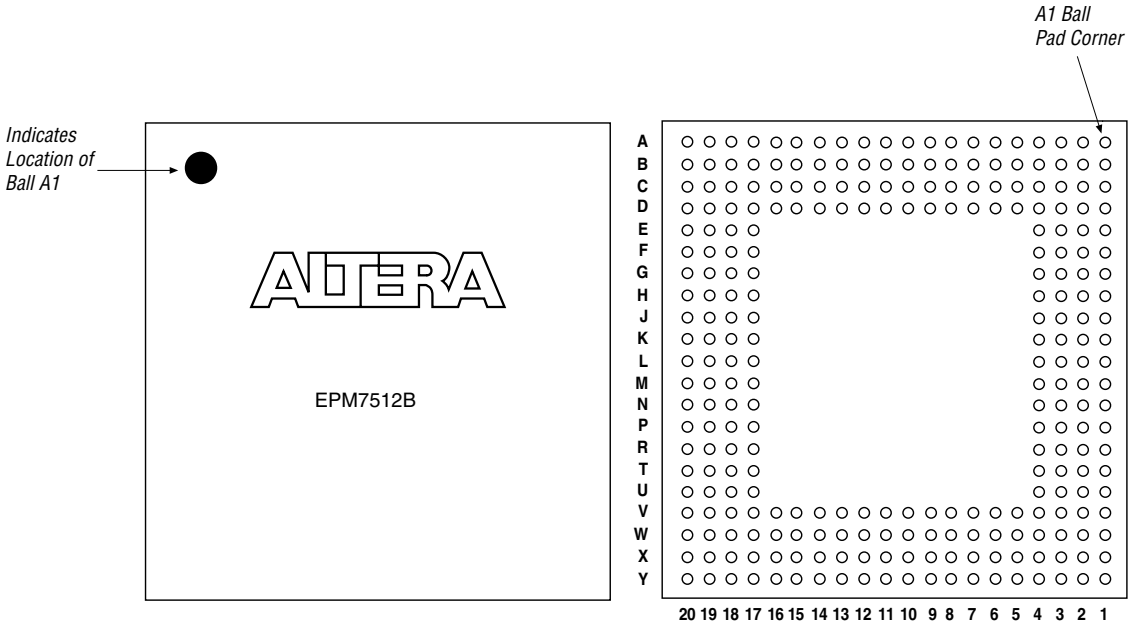
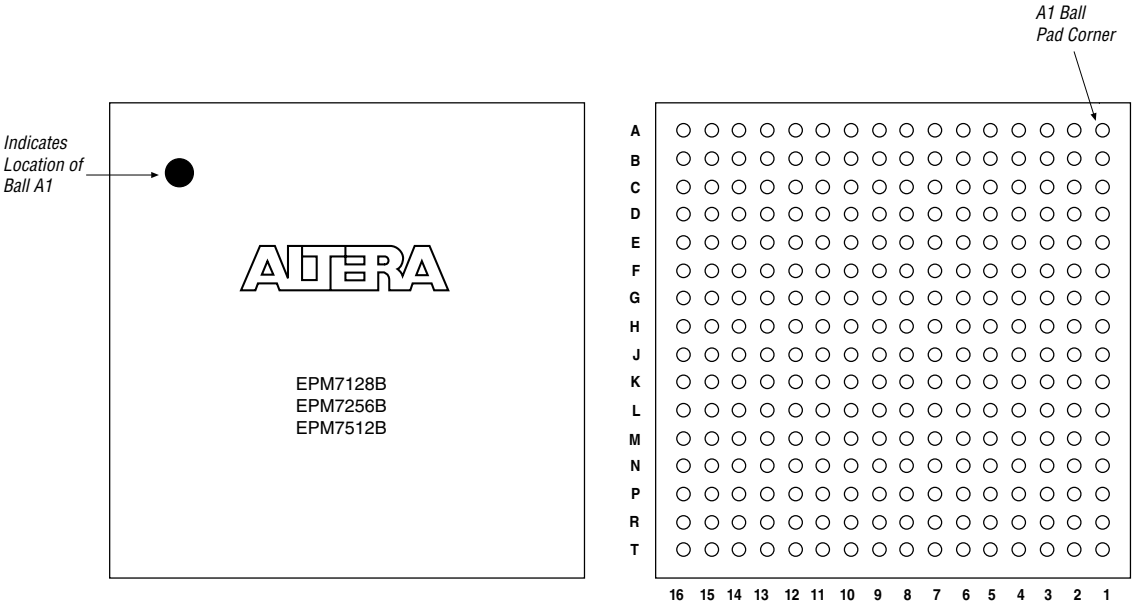


Figure 29. 256-Pin FineLine BGA Package Pin-Out Diagram

Package outline not drawn to scale.



Revision History

The information contained in the *MAX 7000B Programmable Logic Device Family Data Sheet* version 2.1 supersedes information published in previous versions. The following changes were made to the *MAX 7000B Programmable Logic Device Family Data Sheet* version 2.1:

- Updated timing in Tables 1, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, and 30.
- Updated pin counts in Table 3.
- Added "PCI Compatibility" on page 23.
- Added switches S1 and S2 to Figure 11.
- Updated Figure 12.
- Added 49-pin Ultra FineLine BGA package information to Tables 32, 33, 34, 35, 37, and 38, and Figure 22.
- Added 169-pin Ultra FineLine BGA package information to Tables 37, 39, 40, 42, and 43, and Figure 26.
- Minor formatting updates to text, tables, and figures throughout document.