MAX 7000A

Programmable Logic Device Family

January 1998, ver. 1 Data Sheet

Features...

Preliminary Information

- Formerly known as Michelangelo devices
- High-performance CMOS EEPROM-based programmable logic devices (PLDs) built on second-generation Multiple Array MatriX (MAX®) architecture (see Table 1)
- 3.3-V in-system programmability (ISP) through the built-in Joint Test Action Group (JTAG) interface with advanced pin-locking capability
- Built-in JTAG boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1-1990
- Enhanced ISP features (excluding EPM7128A and EPM7256A devices)
  - Enhanced ISP algorithm for faster programming
  - ISP_Done bit to ensure complete programming
  - Pull-up resistor on I/O pins during in-system programming
- Pin-compatible with the popular 5.0-V MAX 7000S devices
- High-density PLDs ranging from 600 to 20,000 usable gates
- 5-ns pin-to-pin logic delays with counter frequencies of up to 178.6 MHz
- MultiVolt™ I/O interface enabling device core to run at 3.3 V, while I/O pins are compatible with 5.0-V, 3.3-V, and 2.5-V logic levels
- Pin counts ranging from 44 to 256 in a variety of thin quad flat pack (TQFP), plastic quad flat pack (PQFP), ball-grid array (BGA), and plastic J-lead chip carrier (PLCC) packages

Table 1. MAX 7000A Device Features

Feature	EPM7032A	EPM7064A	EPM7128A	EPM7256A	EPM7384A	EPM7512A	EPM71024A
Usable gates	600	1,250	2,500	5,000	7,500	10,000	20,000
Macrocells	32	64	128	256	384	512	1,024
Logic array blocks	2	4	8	16	24	32	64
Maximum user I/O pins	36	68	100	164	212	212	212
t_{PD} (ns)	5	5	5	6	7.5	7.5	7.5
t_{SU} (ns)	4	4	4	5	6	6	6
t_{FSU} (ns)	2.5	2.5	2.5	2.5	3	3	3
t_{CO1} (ns)	3.5	3.5	3.5	4	4.5	4.5	4.5
f_{CNT} (MHz)	178.6	178.6	178.6	151.5	125	125	125

A-DS-M7000A-01

...and More Features

- Programmable interconnect array (PIA) continuous routing structure for fast, predictable performance
- Peripheral component interconnect (PCI) compliant
- Bus friendly architecture including programmable slew-rate control
- Open-drain output option
- Programmable macrocell flipflops with individual clear, preset, clock, and clock enable controls
- Programmable power-saving mode for 50% or greater power reduction in each macrocell
- Configurable expander product-term distribution, allowing up to 32 product terms per macrocell
- Programmable security bit for protection of proprietary designs
- Enhanced architectural features, including:
  - Six pin- or logic-driven output enable signals
  - Two global clock signals with optional inversion
  - Enhanced interconnect resources for improved routability
  - Fast input setup times provided by a dedicated path from I/O pin to macrocell registers
  - Programmable output slew-rate control
- Software design support and automatic place-and-route provided by the Altera® MAX+PLUS® II development system on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations
- Additional design entry and simulation support provided by EDIF 2 0 0 and 3 0 0 netlist files, library of parameterized modules (LPM), Verilog HDL, VHDL, and other interfaces to popular EDA tools from manufacturers such as Cadence, Exemplar Logic, Mentor Graphics, OrCAD, Synopsys, Synplicity, and VeriBest
- Programming support with Altera's Master Programming Unit (MPU), BitBlaster™ serial download cable, and ByteBlaster™ parallel port download cable, as well as programming hardware from third-party manufacturers and any Jam™-capable in-circuit tester (ICT)

General Description

MAX 7000A devices are high-density, high-performance devices based on Altera's second-generation MAX architecture. Fabricated with advanced CMOS technology, the EEPROM-based MAX 7000A devices operate with a 3.3-V supply voltage and provide 600 to 20,000 usable gates, ISP, pin-to-pin delays as fast as 5 ns, and counter speeds of up to 178.6 MHz. MAX 7000A devices in the -5, -6, -7, and -10 speed grades comply with the timing and drive characteristics of the peripheral component interconnect Special Interest Group (PCI-SIG) ***PCI Local Bus Specification, Revision 2.1***. See Table 2.

Table 2. MAX 7000A Speed Grades *Note (1)*

Device	Speed Grade				
	-5	-6	-7	-10	-15
EPM7032A	✓		✓	✓	
EPM7064A	✓		✓	✓	
EPM7128A	✓	✓	✓	✓	
EPM7256A		✓	✓	✓	
EPM7384A			✓	✓	✓
EPM7512A			✓	✓	✓
EPM71024A			✓	✓	✓

Note:
(1) This information is preliminary.

The MAX 7000A architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. It easily integrates multiple devices ranging from PALs, GALs, and 22V10s to MACH, pLSI, and FPGA devices. With speed, density, and I/O resources comparable to commonly used masked gate arrays, MAX 7000A devices are also ideal for gate-array prototyping. MAX 7000A devices are available in a wide range of packages, including PLCC, BGA, PQFP, and TQFP packages. See Table 3.

Table 3. MAX 7000A Maximum User I/O Pins *Notes (1), (2)*

Device	44-Pin PLCC	44-Pin TQFP	84-Pin PLCC	100-Pin TQFP	144-Pin TQFP	208-Pin PQFP	256-Pin BGA
EPM7032A	36	36					
EPM7064A	36	36	68	68			
EPM7128A			68	84	100		
EPM7256A				84	120	164	164
EPM7384A					120	176	212
EPM7512A					120	176	212
EPM71024A						176	212

Notes:
(1) Contact Altera for up-to-date information on available device package options.
(2) When using the JTAG interface for ISP or boundary-scan testing, four I/O pins become JTAG pins.

MAX 7000A devices use CMOS EEPROM cells to implement logic functions. The user-configurable MAX 7000A architecture accommodates a variety of independent combinatorial and sequential logic functions. The devices can be reprogrammed for quick and efficient iterations during design development and debug cycles, and can be programmed and erased over 100 times.

MAX 7000A devices contain from 32 to 1,024 macrocells that are combined into groups of 16 macrocells, called logic array blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable clock, clock enable, clear, and preset functions. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

MAX 7000A devices provide programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remaining portions run at reduced speed/low power. This speed/power optimization feature enables the designer to configure one or more macrocells to operate at 50% or lower power while adding only a nominal timing delay. MAX 7000A devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching. The output drivers of all MAX 7000A devices can be set for 2.5 V or 3.3 V and all input pins are 5.0-V tolerant, allowing MAX 7000A devices to be used in mixed-voltage systems.

MAX 7000A devices are supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text—including VHDL, Verilog HDL, and the Altera Hardware Description Language (AHDL)—and waveform design entry; compilation and logic synthesis; simulation and timing analysis; and device programming. The MAX+PLUS II software provides EDIF 2 0 0 and 3 0 0, LPM, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and UNIX-workstation-based EDA tools. The MAX+PLUS II software runs on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700/800, and IBM RISC System/6000 workstations.

For more information on development tools, go to the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book.

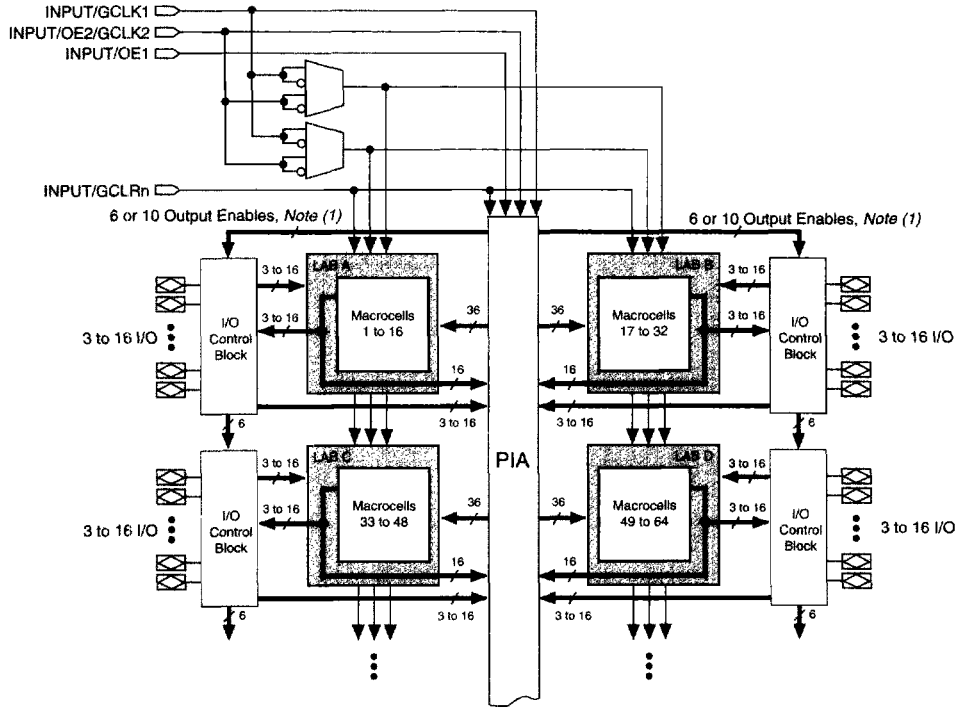
Functional Description

The MAX 7000A architecture includes the following elements:

- Logic array blocks (LABs)
- Macrocells
- Expander product terms (shareable and parallel)
- Programmable interconnect array
- I/O control blocks

The MAX 7000A architecture includes four dedicated inputs that can be used as general-purpose inputs or as high-speed, global control signals (clock, clear, and two output enable signals) for each macrocell and I/O pin. Figure 1 shows the architecture of MAX 7000A devices.

Figure 1. MAX 7000A Device Block Diagram



Note:

(1) EPM7032A, EPM7064A, EPM7128A, and EPM7256A devices have 6 output enables. EPM7384A, EPM7512A, and EPM71024A devices have 10 output enables.

Logic Array Blocks

The MAX 7000A device architecture is based on the linking of high-performance, flexible, logic array modules called logic array blocks (LABs). LABs consist of 16-macrocell arrays, as shown in Figure 1. Multiple LABs are linked together via the programmable interconnect array (PIA), a global bus that is fed by all dedicated inputs, I/O pins, and macrocells.

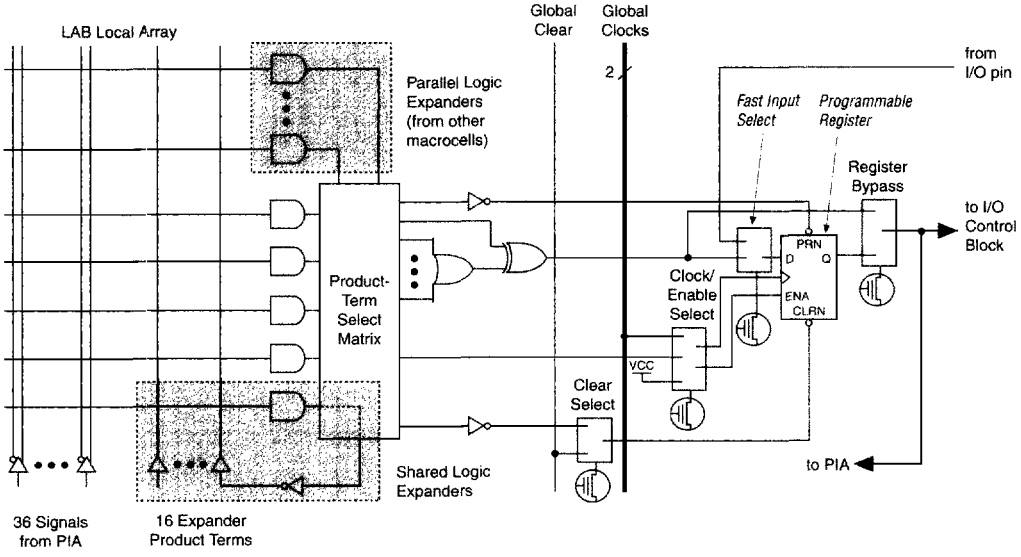
Each LAB is fed by the following signals:

- 36 signals from the PIA that are used for general logic inputs
- Global controls that are used for secondary register functions
- Direct input paths from I/O pins to the registers that are used for fast setup times

Macrocells

The MAX 7000A macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register. Figure 2 shows the MAX 7000A macrocell.

Figure 2. MAX 7000A Macrocell



Combinatorial logic is implemented in the logic array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register preset, clock, and clock enable control functions.

Two kinds of expander product terms ("expanders") are available to supplement macrocell logic resources:

- Shareable expanders, which are inverted product terms that are fed back into the logic array
- Parallel expanders, which are product terms borrowed from adjacent macrocells

The MAX+PLUS II development system automatically optimizes product-term allocation according to the logic requirements of the design.

For registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock control. The flipflop can be bypassed for combinatorial operation. During design entry, the designer specifies the desired flipflop type; the MAX+PLUS II software then selects the most efficient flipflop operation for each registered function to optimize resource utilization.

Each programmable register can be clocked in three different modes:

- By a global clock signal. This mode achieves the fastest clock-to-output performance.
- By a global clock signal and enabled by an active-high clock enable. Clock enable is generated by a product term. This mode provides an enable on each flipflop while still achieving the fast clock-to-output performance of the global clock.
- By an array clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global clock signals are available in MAX 7000A devices. As shown in Figure 1, these global clock signals can be the true or the complement of either of the global clock pins, GCLK1 or GCLK2.

Each register also supports asynchronous preset and clear functions. As shown in Figure 2, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven preset and clear of the register are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register clear function can be individually driven by the active-low dedicated global clear pin (GCLRn).

All MAX 7000A I/O pins have a fast input path to a macrocell register. This dedicated path allows a signal to bypass the PIA and combinatorial logic and be clocked to an input D flipflop with an extremely fast (3 ns) input setup time.

Expander Product Terms

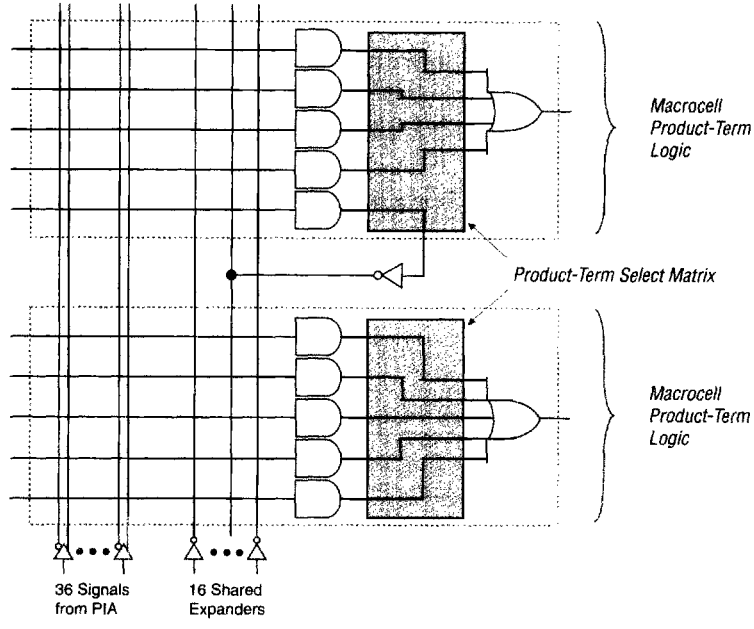
Although most logic functions can be implemented with the five product terms available in each macrocell, the more complex logic functions require additional product terms. Another macrocell can be used to supply the required logic resources; however, the MAX 7000A architecture also offers both shareable and parallel expander product terms ("expanders") that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the logic array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay (t_{SEXP}) is incurred when shareable expanders are used. Figure 3 shows how shareable expanders can feed multiple macrocells.

Figure 3. MAX 7000A Shareable Expanders

Shareable expanders can be shared by any or all macrocells in an LAB.



Parallel Expanders

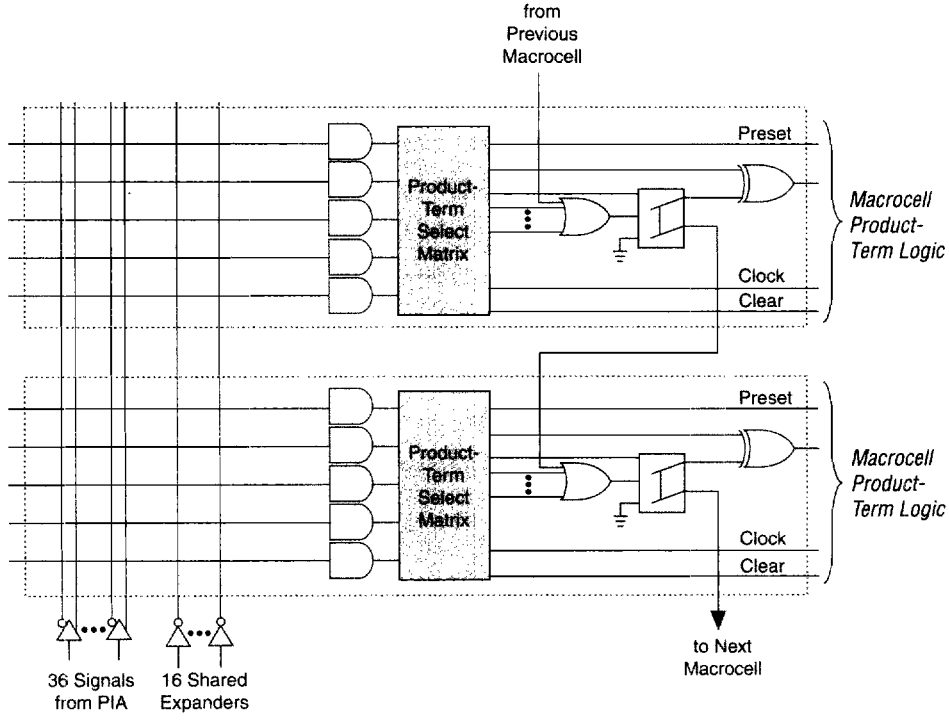
Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with 5 product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB.

The MAX+PLUS II Compiler can automatically allocate up to 3 sets of up to 5 parallel expanders to the macrocells that require additional product terms. Each set of 5 parallel expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the 5 dedicated product terms within the macrocell and allocates 2 sets of parallel expanders; the first set includes 5 product terms and the second set includes 4 product terms, increasing the total delay by $2 \times t_{PEXP}$.

Two groups of 8 macrocells within each LAB (e.g., macrocells 1 to 8 and 9 to 16) form 2 chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them. Figure 4 shows how parallel expanders can be borrowed from a neighboring macrocell.

Figure 4. MAX 7000A Parallel Expanders

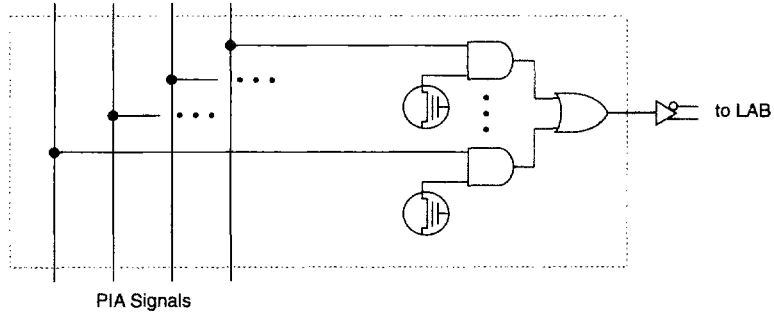
Unused product terms in a macrocell can be allocated to a neighboring macrocell.



Programmable Interconnect Array

Logic is routed between LABs on the programmable interconnect array (PIA). This global bus is a programmable path that connects any signal source to any destination on the device. All MAX 7000A dedicated inputs, I/O pins, and macrocell outputs feed the PIA, which makes the signals available throughout the entire device. Only the signals required by each LAB are actually routed from the PIA into the LAB. Figure 5 shows how the PIA signals are routed into the LAB. An EEPROM cell controls one input to a 2-input AND gate, which selects a PIA signal to drive into the LAB.

Figure 5. MAX 7000A PIA Routing

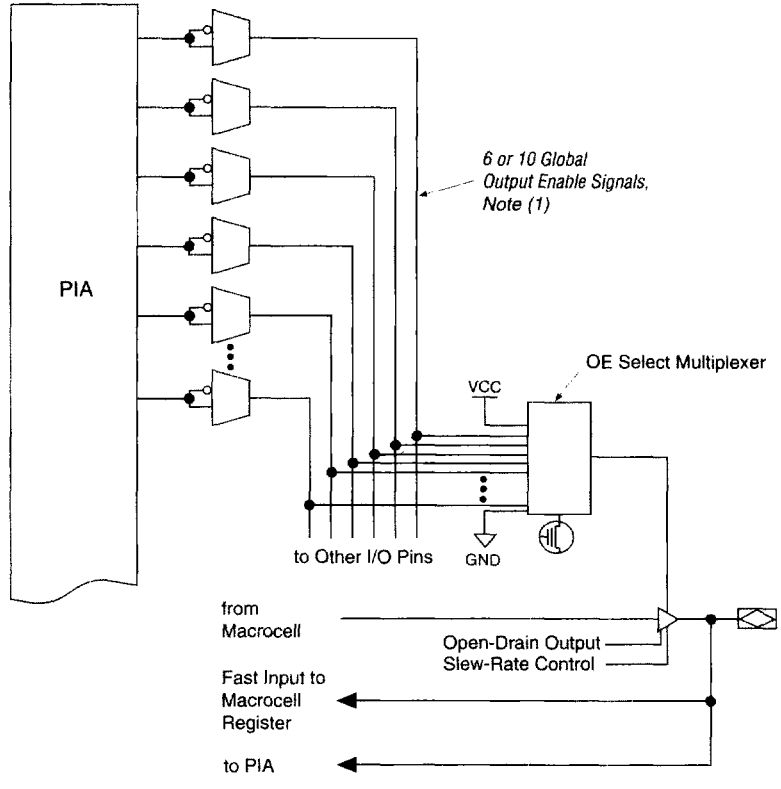


While the routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent, the MAX 7000A PIA has a fixed delay. The PIA thus eliminates skew between signals and makes timing performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is individually controlled by one of the global output enable signals or directly connected to ground or V_{CC}. Figure 6 shows the I/O control block for MAX 7000A devices. The I/O control block has six global output enable signals that are driven by the true or complement of two output enable signals, a subset of the I/O pins, or a subset of the I/O macrocells.

Figure 6. I/O Control Block of MAX 7000A Devices



Note:
(1) EPM7032A, EPM7064A, EPM7128A, and EPM7256A devices have 6 output enables. EPM7384A, EPM7512A, and EPM71024A devices have 10 output enables.

When the tri-state buffer control is connected to ground, the output is tri-stated (high impedance) and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to VCC, the output is enabled.

The MAX 7000A architecture provides dual I/O feedback, in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

In-System Programmability (ISP)

MAX 7000A devices can be programmed in-system via an industry-standard 4-pin JTAG interface (IEEE Std. 1149.1-1990). ISP offers quick, efficient iterations during design development and debugging cycles. The MAX 7000A architecture internally generates the high programming voltages required to program EEPROM cells, allowing in-system programming with only a single 3.3-V power supply. During ISP, the I/O pins are tri-stated to eliminate board conflicts.

MAX 7000A devices have an enhanced ISP algorithm for faster programming. These devices also offer an ISP_Done bit that allows for safe operation when in-system programming is interrupted. This ISP_Done bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed. This feature is available in EPM7032A, EPM7064A, EPM7384A, EPM7512A, and EPM71024A devices.

ISP simplifies the manufacturing flow by allowing devices to be mounted on a printed circuit board with standard pick-and-place equipment before they are programmed. MAX 7000A devices can be programmed by downloading the information via ICT, embedded processors, the Altera BitBlaster serial download cable, and the ByteBlaster parallel port download cable. Programming the devices after they are placed on the board eliminates lead damage on high-pin-count packages (e.g., QFP packages) due to device handling. MAX 7000A devices can be reprogrammed after a system has already shipped to the field. For example, product upgrades can be performed in the field via software or modem.

Programming with External Hardware

MAX 7000A devices can be programmed on 486- and Pentium-based PCs with an Altera Logic Programmer card, the MPU, and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device. For more information, see *Altera Programming Hardware* in this data book.

The MAX+PLUS II software can use text- or waveform-format test vectors created with the MAX+PLUS II Text Editor or Waveform Editor to test the programmed device. For added design verification, designers can perform functional testing to compare the functional behavior of a MAX 7000A device with the results of simulation.

Data I/O, BP Microsystems, and other programming hardware manufacturers provide programming support for Altera devices. For more information, see *Programming Hardware Manufacturers*.

IEEE 1149.1 (JTAG) Boundary-Scan Support

MAX 7000A devices support JTAG BST circuitry as specified by IEEE Std. 1149.1-1990. Table 4 describes the JTAG instructions supported by MAX 7000A devices. The pin-out tables starting on page 378 of this data sheet show the location of the JTAG control pins for each device. If the JTAG interface is not required, the JTAG pins are available as user I/O pins.

Table 4. MAX 7000A JTAG Instructions

JTAG Instruction	Description
SAMPLE/PRELOAD	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern output at the device pins.
EXTEST	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through a selected device to adjacent devices during normal device operation.
IDCODE	Selects the IDCODE register and places it between the TDI and TDO pins, allowing the IDCODE to be serially shifted out of TDO. Applies to EPM7128A and EPM7256A devices only.
USERCODE	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE value to be shifted out of TDO. Excludes the EPM7128A and EPM7256A devices.
UESCODE	Selects the user electronic signature (UESCODE) and allows the UESCODE to be serially shifted out of TDO.
ISP Instructions	These instructions are used when programming MAX 7000A devices via the JTAG ports with the BitBlaster or ByteBlaster download cable, or using a Jam File or Serial Vector Format (**.svf**) file via an embedded processor or test equipment.

Go to *Application Note 39 (JTAG Boundary-Scan Testing in Altera Devices)* for more information on JTAG BST.

Figure 7 shows the timing requirements for the JTAG signals.

Figure 7. MAX 7000A JTAG Waveforms

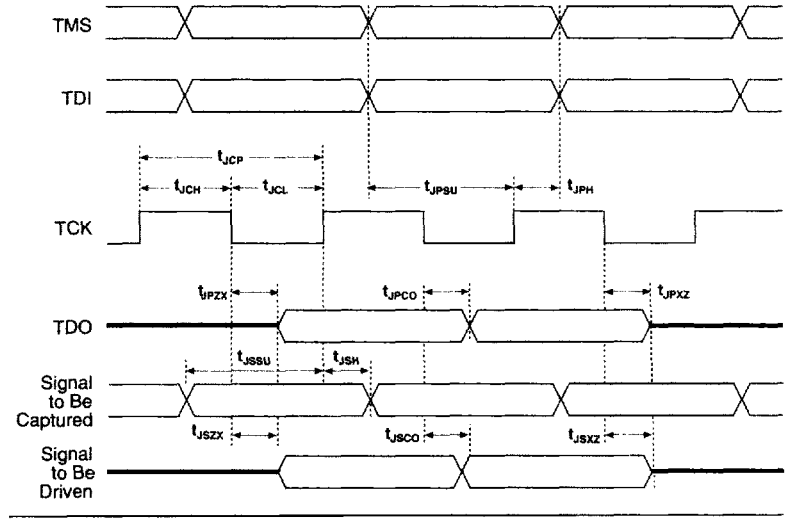


Table 5 shows the JTAG timing parameters and values for MAX 7000A devices.

Table 5. JTAG Timing Parameters & Values for MAX 7000A Devices

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	100		ns
t_{JCH}	TCK clock high time	50		ns
t_{JCL}	TCK clock low time	50		ns
t_{JPSU}	JTAG port setup time	20		ns
t_{JPH}	JTAG port hold time	45		ns
t_{JPCO}	JTAG port clock to output		25	ns
t_{JPZX}	JTAG port high impedance to valid output		25	ns
t_{JPXZ}	JTAG port valid output to high impedance		25	ns
t_{JSSU}	Capture register setup time	20		ns
t_{JSH}	Capture register hold time	45		ns
t_{JSCO}	Update register clock to output		25	ns
t_{JSZX}	Update register high impedance to valid output		25	ns
t_{JSXZ}	Update register valid output to high impedance		25	ns

Programmable Speed/Power Control

MAX 7000A devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, because most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 7000A device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters.

Output Configuration

MAX 7000A device outputs can be programmed to meet a variety of system-level requirements.

MultiVolt I/O Interface

The MAX 7000A device architecture supports the MultiVolt I/O interface feature, which allows MAX 7000A devices to interface with systems with differing supply voltages. MAX 7000A devices in all packages can be set for 2.5-V, 3.3-V, or 5.0-V I/O operation. These devices have one set of V_{CC} pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The VCCIO pins can be connected to either a 3.3-V or 2.5-V power supply, depending on the output requirements. When the VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is at 3.3 V and is therefore compatible with 3.3-V or 5.0-V systems. Devices operating with V_{CCIO} levels lower than 3.3 V incur a nominally greater timing delay of t_{OD2} instead of t_{OD1}. Input can always be driven by 2.5-V, 3.3-V, or 5.0-V signals.

Open-Drain Output Option

MAX 7000A devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (e.g., interrupt and write enable signals) that can be asserted by any of several devices. It can also provide an additional wired-OR plane.

Slew-Rate Control

The output buffer for each MAX 7000A I/O pin has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal delay of 4 to 5 ns. When the configuration cell is turned off, the slew rate is set for low noise performance. Each I/O pin has an individual EEPROM bit that controls the slew rate, allowing designers to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the output signal.

Design Security

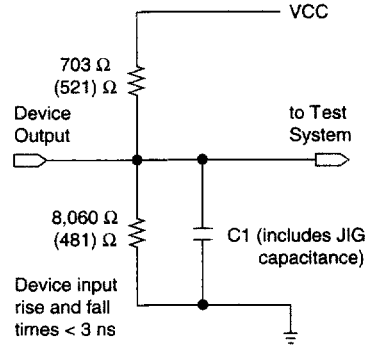
All MAX 7000A devices contain a programmable security bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, because programmed data within EEPROM cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is reprogrammed.

Generic Testing

MAX 7000A devices are fully functionally tested. Complete testing of each programmable EEPROM bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 8. Test patterns can be used and then erased during early stages of the production flow.

Figure 8. MAX 7000A AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result. Numbers in parentheses are for 2.5-V operation.



Operating Conditions

The following tables provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for MAX 7000A devices.

MAX 7000A Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground, *Note (2)*	–2.0	5.3	V
V_I	DC input voltage		–2.0	5.3	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_A	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		PQFP and RQFP packages, under bias		135	° C

MAX 7000A Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*Note (3)*	3.0	3.6	V
V_{CCIO}	Supply voltage for output drivers	*Note (3)*	3.0	3.6	V
V_{CCISP}	Supply voltage during ISP		3.0	3.6	V
V_I	Input voltage		0	5.3	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
T_J	Junction temperature	For commercial use	0	90	° C
		For industrial use	–40	105	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

MAX 7000A Device DC Operating Conditions *Notes (4), (5)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		1.7	5.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.00 V, *Note (6)*	2.4		V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.00 V, *Note (6)*	V_{CCIO} – 0.2		V
	2.5-V high-level output voltage	I_{OH} = –100 µA DC, V_{CCIO} = 2.30 V, *Note (6)*	2.1		V
		I_{OH} = –1 mA DC, V_{CCIO} = 2.30 V, *Note (6)*	2.0		V
		I_{OH} = –2 mA DC, V_{CCIO} = 2.30 V, *Note (6)*	1.7		V
V_{OL}	3.3-V low-level TTL output voltage	I_{OL} = 4 mA DC, V_{CCIO} = 3.00 V, *Note (7)*		0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V, *Note (7)*		0.2	V
	2.5-V low-level output voltage	I_{OL} = 100 µA DC, V_{CCIO} = 2.30 V, *Note (7)*		0.2	V
		I_{OL} = 1 mA DC, V_{CCIO} = 2.30 V, *Note (7)*		0.4	V
		I_{OL} = 2 mA DC, V_{CCIO} = 2.30 V, *Note (7)*		0.7	V
I_I	Input leakage current	V_I = V_{CCINT} or ground	–10	10	µA
I_{OZ}	Tri-state output off-state current	V_O = V_{CCINT} or ground	–40	40	µA

MAX 7000A Device Capacitance *Note (8)*

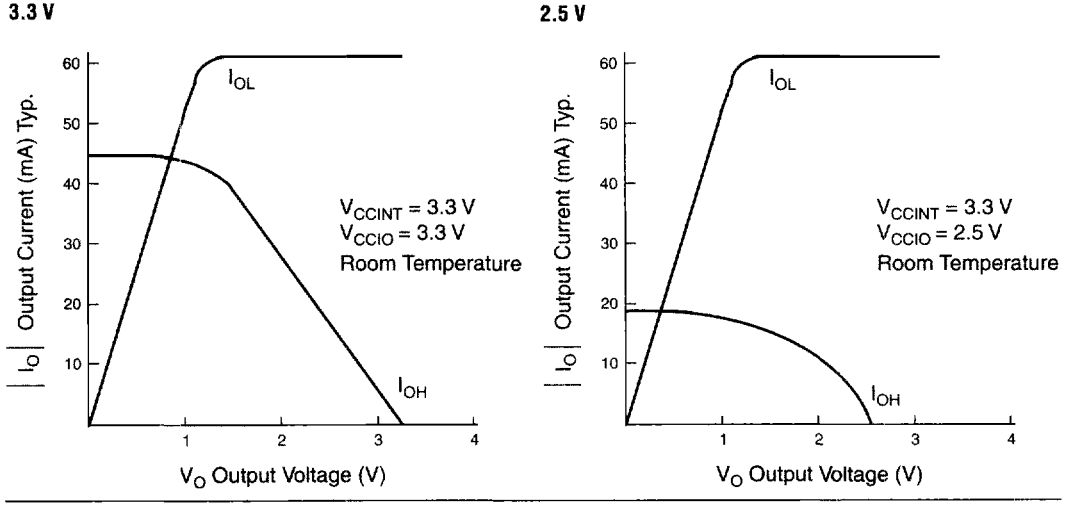
Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		8	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		8	pF

Notes to tables:

(1) See *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.3 V for periods shorter than 20 ns under no-load conditions.
(3) V_{CC} must rise monotonically.
(4) MultiVolt I/O operation is not available for 44-pin packages.
(5) These values are specified under the "MAX 7000A Device Recommended Operating Conditions" on page 368.
(6) The I_{OH} parameter refers to high-level TTL or CMOS output current.
(7) The I_{OL} parameter refers to low-level TTL or CMOS output current.
(8) Capacitance is measured at 25° C and is sample-tested only. The `OE1` pin (high-voltage pin during programming) has a maximum capacitance of 20 pF.

Figure 9 shows the typical output drive characteristics of MAX 7000A devices.

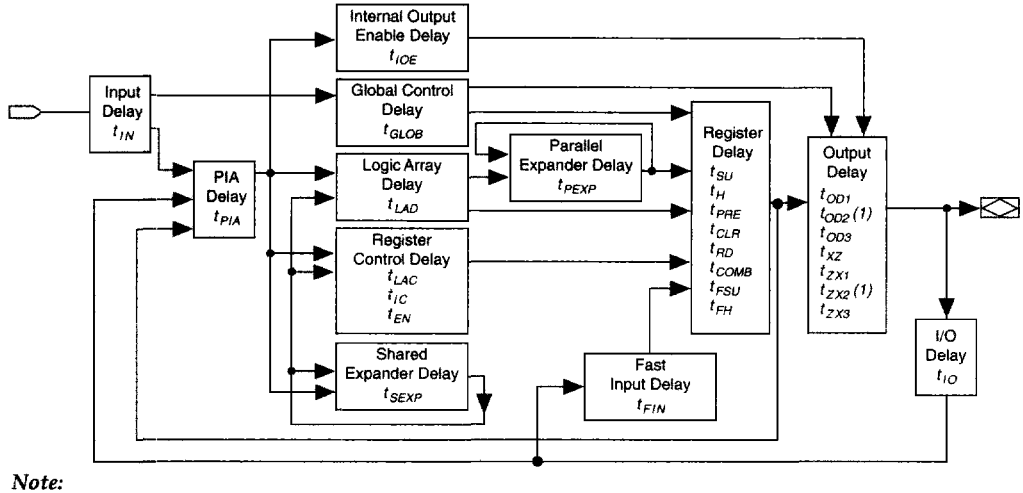
Figure 9. Output Drive Characteristics of MAX 7000A Devices



Timing Model

MAX 7000A device timing can be analyzed with the MAX+PLUS II software, with a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 10. MAX 7000A devices have fixed internal delays that enable the designer to determine the worst-case timing of any design. The MAX+PLUS II software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 10. MAX 7000A Timing Model



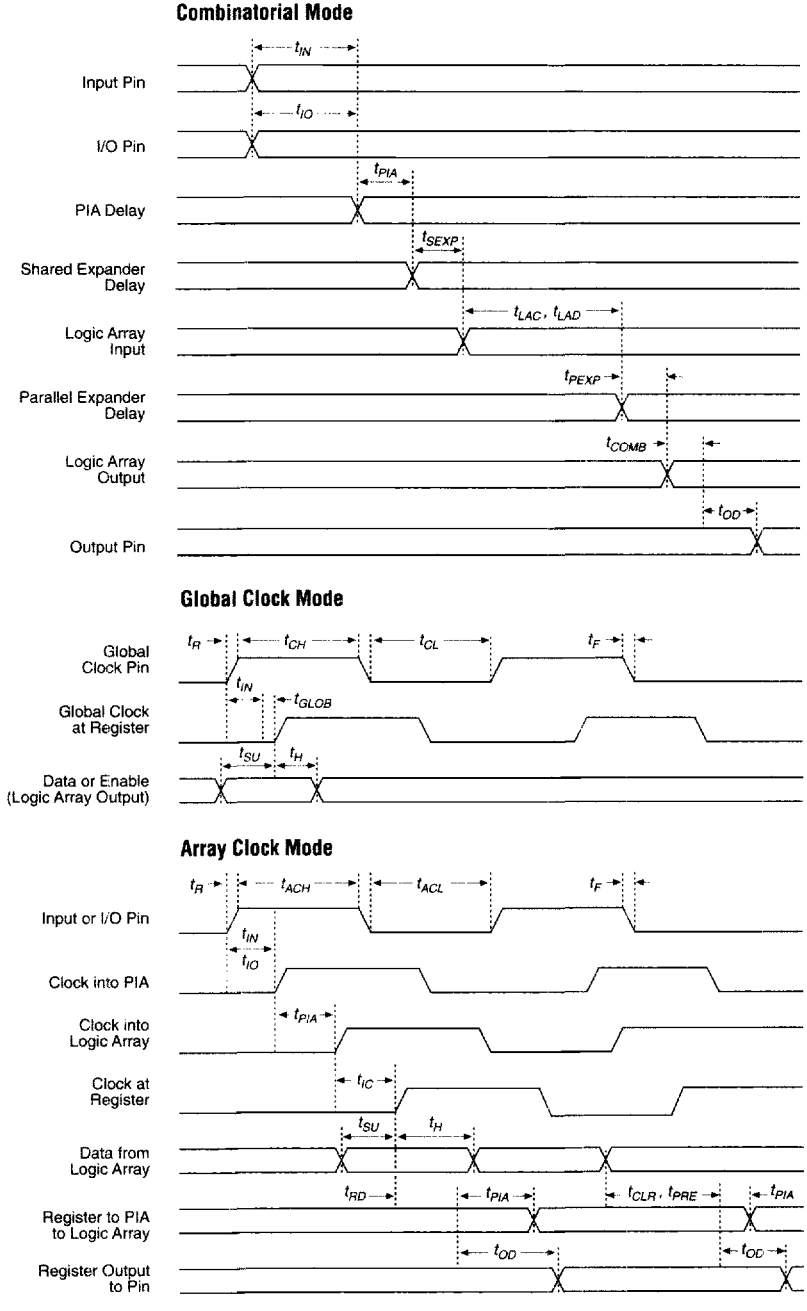
Note:
(1) Not available in 44-pin devices.

The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters. Figure 11 shows the timing relationship between internal and external delay parameters.

See *Application Note 94 (Understanding MAX 7000 Timing)* in this data book for more information.

Figure 11. Switching Waveforms

t_R & t_F < 2 ns.
Inputs are driven at 3 V for a logic high and 0 V for a logic low. All timing characteristics are measured at 1.5 V.



MAX 7000A AC Operating Conditions *Note (1)*

External Timing Parameters			Speed Grade						
			-5		-6		-7		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		5		6		7.5	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		5		6		7.5	ns
t_{SU}	Global clock setup time		4		5		6		ns
t_{H}	Global clock hold time		0		0		0		ns
t_{FSU}	Global clock setup time of fast input		2.5		2.5		3		ns
t_{FH}	Global clock hold time of fast input		0		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		3.5		4		4.5	ns
t_{CH}	Global clock high time		2		2.5		3		ns
t_{CL}	Global clock low time		2		2.5		3		ns
t_{ASU}	Array clock setup time		2		2.5		3		ns
t_{AH}	Array clock hold time		2		2		2		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		5.5		6.5		7.5	ns
t_{ACH}	Array clock high time		2.5		3		3		ns
t_{ACL}	Array clock low time		2.5		3		3		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF, *Note (2)*	1		1		1		ns
t_{CNT}	Minimum global clock period			5.6		6.6		8	ns
f_{CNT}	Maximum internal global clock frequency	*Note (3)*	178.6		151.5		125		MHz
t_{ACNT}	Minimum array clock period			5.6		6.6		8	ns
f_{ACNT}	Maximum internal array clock frequency	*Note (3)*	178.6		151.5		125		MHz
f_{MAX}	Maximum clock frequency	*Note (4)*	250		200		166.7		MHz

Internal Timing Parameters			Speed Grade						
			-5		-6		-7		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Min	Max	Unit
t_{IN}	Input pad and buffer delay			0.4		0.4		0.5	ns
t_{IO}	I/O input pad and buffer delay			0.4		0.4		0.5	ns
t_{FIN}	Fast input delay			0.8		0.8		1	ns
t_{SEXP}	Shared expander delay			3		3.5		4	ns
t_{PEXP}	Parallel expander delay			0.8		0.8		0.8	ns
t_{LAD}	Logic array delay			1.5		2		3	ns
t_{LAC}	Logic control array delay			1.5		2		3	ns
t_{IOE}	Internal output enable delay			2				2	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF, *Note (1)*		1.5		2		2	ns
t_{OD2}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF, *Note (5)*		2.0		2.5		2.5	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 3.3 V or 2.5 V	C1 = 35 pF		6.5		7		7	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF, *Note (1)*		4		4		4	ns
t_{ZX2}	Output buffer enable delay slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF, *Note (5)*		4.5		4.5		4.5	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 3.3 V or 2.5 V	C1 = 35 pF		9		9		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		4		4		4	ns
t_{SU}	Register setup time		2.5		3		3		ns
t_{H}	Register hold time		1.5		1.5		2		ns
t_{FSU}	Register setup time of fast input		2.5		2.5		3		ns
t_{FH}	Register hold time of fast input		0.5		0.5		0.5		ns
t_{RD}	Register delay			0.8		0.8		1	ns
t_{COMB}	Combinatorial delay			0.8		0.8		1	ns
t_{IC}	Array clock delay			2		2.5		3	ns
t_{EN}	Register enable time			1.5		2		3	ns
t_{GLOB}	Global control delay			0.8		0.8		1	ns
t_{PRE}	Register preset time			2		2		2	ns
t_{CLR}	Register clear time			2		2		2	ns
t_{PIA}	PIA delay			0.8		0.8		1	ns
t_{LPA}	Low-power adder	*Note (6)*		8		10		10	ns

External Timing Parameters			Speed Grade				
			-10		-15		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to non-registered output	C1 = 35 pF		10		15	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		10		15	ns
t_{SU}	Global clock setup time		7		11		ns
t_{H}	Global clock hold time		0		0		ns
t_{FSU}	Global clock setup time of fast input		3		3		ns
t_{FH}	Global clock hold time of fast input		0		0		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		5		5	ns
t_{CH}	Global clock high time		4		6		ns
t_{CL}	Global clock low time		4		6		ns
t_{ASU}	Array clock setup time		2		4		ns
t_{AH}	Array clock hold time		3		4		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		10		10	ns
t_{ACH}	Array clock high time		4		6.5		ns
t_{ACL}	Array clock low time		4		6.5		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF, *Note (2)*	1		1		ns
t_{CNT}	Minimum global clock period			10		10	ns
f_{CNT}	Maximum internal global clock frequency	*Note (3)*	100		76.9		MHz
t_{ACNT}	Minimum array clock period			10		10	ns
f_{ACNT}	Maximum internal array clock frequency	*Note (3)*	100		76.9		MHz
f_{MAX}	Maximum clock frequency	*Note (4)*	125		83.3		MHz

Internal Timing Parameters			Speed Grade				
			-10		-15		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Unit
t_{IN}	Input pad and buffer delay			0.5		1	ns
t_{IO}	I/O input pad and buffer delay			0.5		1	ns
t_{FIN}	Fast input delay			1		1	ns
t_{SEXP}	Shared expander delay			5		5	ns
t_{PEXP}	Parallel expander delay			0.8		0.8	ns
t_{LAD}	Logic array delay			5		5	ns
t_{LAC}	Logic control array delay			5		5	ns
t_{IOE}	Internal output enable delay			2		2	ns
t_{OD1}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF, *Note (1)*		1.5		2	ns
t_{OD2}	Output buffer and pad delay slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF, *Note (5)*		2		2.5	ns
t_{OD3}	Output buffer and pad delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		5.5		6	ns
t_{ZX1}	Output buffer enable delay slow slew rate = off V_{CCIO} = 3.3 V	C1 = 35 pF, *Note (1)*		5		5	ns
t_{ZX2}	Output buffer enable delay slow slew rate = off V_{CCIO} = 2.5 V	C1 = 35 pF, *Note (5)*		5.5		5.5	ns
t_{ZX3}	Output buffer enable delay slow slew rate = on V_{CCIO} = 2.5 V or 3.3 V	C1 = 35 pF		9		9	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5		5	ns
t_{SU}	Register setup time		2		3		ns
t_{H}	Register hold time		3		3		ns
t_{FSU}	Register setup time of fast input		3		3		ns
t_{FH}	Register hold time of fast input		0.5		0.5		ns
t_{RD}	Register delay			2		1	ns
t_{COMB}	Combinatorial delay			2		1	ns
t_{IC}	Array clock delay			5		5	ns
t_{EN}	Register enable time			5		5	ns
t_{GLOB}	Global control delay			1		1	ns
t_{PRE}	Register preset time			3		3	ns
t_{CLR}	Register clear time			3		3	ns
t_{PIA}	PIA delay			1		1	ns
t_{LPA}	Low-power adder	*Note (6)*		11		11	ns

Notes to tables:

(1) These values are specified under the "MAX 7000A Device Recommended Operating Conditions" on page 368.
(2) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies to both global and array clocking.
(3) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB.
(4) The f_{MAX} values represent the highest frequency for pipelined data.
(5) Operating conditions: $V_{CCIO} = 2.5 \pm 0.2$ V for commercial and industrial use.
(6) The t_{LPA} parameter must be added to the t_{LAD}, t_{LAC}, t_{IC}, t_{ACL}, t_{EN}, and t_{SEXP} parameters for macrocells running in the low-power mode.

Power Consumption

Supply power (P) versus frequency (f_{MAX} in MHz) for MAX 7000A devices is calculated with the following equation:

$$P = P_{INT} + P_{IO} = I_{CCINT} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines given in *Application Note 74 (Evaluating Power for Altera Devices)* in this data book.

The I_{CCINT} value depends on the switching frequency and the application logic. The I_{CCINT} value is calculated with the following equation:

$$I_{CCINT} =$$

$$(A \times MC_{TON}) + [B \times (MC_{DEV} - MC_{TON})] + (C \times MC_{USED} \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}})$$

The parameters in this equation are:

MC_{TON}	=	Number of macrocells with the Turbo Bit™ option turned on, as reported in the MAX+PLUS II Report File (**.rpt**)
MC_{DEV}	=	Number of macrocells in the device
MC_{USED}	=	Total number of macrocells in the design, as reported in the Report File
$\mathbf{f_{MAX}}$	=	Highest clock frequency to the device
$\mathbf{tog_{LC}}$	=	Average percentage of logic cells toggling at each clock (typically 12.5%)
A, B, C	=	Constants, contact Altera Applications for constant values

This calculation provides an I_{CC} estimate based on typical conditions using a pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Device Pin-Outs

Tables 6 and 7 show the pin names and numbers for the pins in each MAX 7000A device package.

Table 6. EPM7128A Dedicated Pin-Outs

Dedicated Pin	84-Pin J-Lead	100-Pin TQFP
INPUT/GCLK1	83	87
INPUT/GCLRn	1	89
INPUT/OE1	84	88
INPUT/OE2/GCLK2	2	90
TDI, *(1)*	14	4
TMS, *(1)*	23	15
TCK, *(1)*	62	62
TDO, *(1)*	71	73
GND	7, 19, 32, 47, 59, 72	11, 26, 43, 59, 74, 95
VCCINT (3.3 V only)	3, 43	39, 91
VCCIO (2.5 V or 3.3 V)	13, 26, 38, 53, 66, 78	3, 18, 34, 51, 66, 82
No Connect (N.C.)	–	–
Total User I/O Pins	64	80

Note:

(1) This pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for BST or for ISP, this pin is not available as a user I/O pin.

Table 7. EPM7128A I/O Pin-Outs (Part 1 of 2)

MC	LAB	84-Pin J-Lead	100-Pin TQFP	MC	LAB	84-Pin J-Lead	100-Pin TQFP
1	A	–	2	17	B	22	14
2	A	–	–	18	B	–	–
3	A	12	1	19	B	21	13
4	A	–	–	20	B	–	–
5	A	11	100	21	B	20	12
6	A	10	99	22	B	–	10
7	A	–	–	23	B	–	–
8	A	9	98	24	B	18	9
9	A	–	97	25	B	17	8
10	A	–	–	26	B	–	–
11	A	8	96	27	B	16	7
12	A	–	–	28	B	–	–
13	A	6	94	29	B	15	6
14	A	5	93	30	B	–	5
15	A	–	–	31	B	–	–
16	A	4	92	32	B	14 *(1)*	4 *(1)*
33	C	–	25	49	D	41	37
34	C	–	–	50	D	–	–
35	C	31	24	51	D	40	36
36	C	–	–	52	D	–	–
37	C	30	23	53	D	39	35
38	C	29	22	54	D	–	33
39	C	–	–	55	D	–	–
40	C	28	21	56	D	37	32
41	C	–	20	57	D	36	31
42	C	–	–	58	D	–	–
43	C	27	19	59	D	35	30
44	C	–	–	60	D	–	–
45	C	25	17	61	D	34	29
46	C	24	16	62	D	–	28
47	C	–	–	63	D	–	–
48	C	23 *(1)*	15 *(1)*	64	D	33	27

Table 7. EPM7128A I/O Pin-Outs (Part 2 of 2)

MC	LAB	84-Pin J-Lead	100-Pin TQFP	MC	LAB	84-Pin J-Lead	100-Pin TQFP
65	E	44	40	81	F	–	52
66	E	–	–	82	F	–	–
67	E	45	41	83	F	54	53
68	E	–	–	84	F	–	–
69	E	46	42	85	F	55	54
70	E	–	44	86	F	56	55
71	E	–	–	87	F	–	–
72	E	48	45	88	F	57	56
73	E	49	46	89	F	–	57
74	E	–	–	90	F	–	–
75	E	50	47	91	F	58	58
76	E	–	–	92	F	–	–
77	E	51	48	93	F	60	60
78	E	–	49	94	F	61	61
79	E	–	–	95	F	–	–
80	E	52	50	96	F	62 *(1)*	62 *(1)*
97	G	63	63	113	H	–	75
98	G	–	–	114	H	–	–
99	G	64	64	115	H	73	76
100	G	–	–	116	H	–	–
101	G	65	65	117	H	74	77
102	G	–	67	118	H	75	78
103	G	–	–	119	H	–	–
104	G	67	68	120	H	76	79
105	G	68	69	121	H	–	80
106	G	–	–	122	H	–	–
107	G	69	70	123	H	77	81
108	G	–	–	124	H	–	–
109	G	70	71	125	H	79	83
110	G	–	72	126	H	80	84
111	G	–	–	127	H	–	–
112	G	71 *(1)*	73 *(1)*	128	H	81	85

Note:

(1) This pin may function as either a JTAG port or a user I/O pin. If the device is configured to use the JTAG ports for BST or for ISP, this pin is not available as a user I/O pin.

Figures 12 and 13 show the package pin-out diagrams for MAX 7000A devices.

Figure 12. 84-Pin J-Lead Package Pin-Out Diagram

Package outline not drawn to scale.

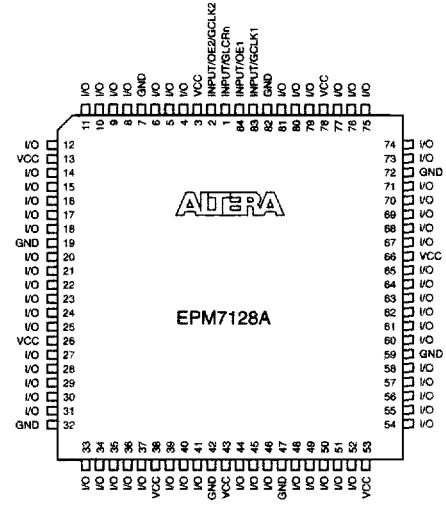


Figure 13. 100-Pin TQFP Package Pin-Out Diagram

Package outline not drawn to scale.