MAX 9000

Programmable Logic Device Family

October 1994, ver. 1 | Data Sheet

Features...

Preliminary Information

- ❑ High-performance programmable logic devices (PLDs) based on third-generation Multiple Array MatriX (MAX) architecture
- ❑ Fabricated on 0.7-micron CMOS EEPROM technology
- ❑ Complete EPLD family with logic densities ranging from 6,000 usable (12,000 available) gates to 12,000 usable (24,000 available) gates (see Table 1)
- ❑ 12-ns pin-to-pin logic delays with up to 118-MHz counter frequencies
- ❑ 5.0-V in-system programmability (ISP) through JTAG interface
- ❑ Built-in Joint Test Action Group (JTAG) boundary-scan test circuitry with internal scan capability
- ❑ Dual-output macrocell for independent use of combinatorial and registered logic
- ❑ FastTrack continuous routing structure for fast, predictable interconnect delays
- ❑ Input/output registers with Clock Enable on all I/O pins
- ❑ Programmable output slew-rate control to reduce switching noise
- ❑ 3.3-V or 5.0-V I/O operation on all devices
- ❑ Programmable power-saver mode for 50% or more power reduction in each macrocell
- ❑ Programmable macrocell flipflops with individual Clear, Preset, Clock, and Clock Enable controls
- ❑ Configurable expander product-term distribution allowing up to 32 product terms in each macrocell

Table 1. MAX 9000 Device Features

Feature	EPM9320	EPM9400	EPM9480	EPM9560
Available gates	12,000	16,000	20,000	24,000
Usable gates	6,000	8,000	10,000	12,000
Flipflops	484	580	676	772
Macrocells	320	400	480	560
Maximum user I/O	168	184	200	216
t_{PD} (ns)	12	12	15	15
t_{FSU} (ns)	3.5	3.5	3.5	3.5
t_{FCO} (ns)	6	6	6.5	6.5
f_{CNT} (MHz)	118	118	118	118

ALTES008

... and More Features

- Programmable Security Bit for total protection of proprietary designs
- Software design support provided by Altera's MAX+PLUS II development system on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, IBM RISC System/6000, and DEC Alpha AXP workstations
- Additional design entry and simulation support provided by EDIF, Verilog HDL, VHDL, and other interfaces to popular CAE tools from manufacturers such as Cadence, Data I/O, Exemplar, Intergraph, Mentor Graphics, OrCAD, Synopsys, and Viewlogic
- Programming support with Altera's Master Programming Unit (MPU) and BitBlaster, and programming hardware from other manufacturers
- Offered in a variety of packages with 84 to 304 pins (see Table 2)

Table 2. MAX 9000 Package Options and I/O Count

Device	Packages *(1)*	Maximum User I/O
EPM9320	84-pin PLCC	55
	160-pin RQFP	116
	208-pin RQFP	132
	280-pin PGA	168
EPM9400	84-pin PLCC	59
	208-pin RQFP	139
	240-pin RQFP	159
	280-pin PGA	184
EPM9480	160-pin RQFP	117
	208-pin RQFP	146
	240-pin RQFP	175
	280-pin PGA	200
EPM9560	208-pin RQFP	153
	240-pin RQFP	191
	280-pin PGA	216
	304-pin RQFP	216

Note:
(1) Contact Altera for up-to-date information on package availability.

General Description

The MAX 9000 family of in-system programmable, high-density, high-performance CMOS EPLDs is based on Altera's third-generation MAX architecture. Fabricated with advanced 0.7-micron CMOS EEPROM technology, the MAX 9000 family provides 6,000 to 12,000 usable gates, pin-to-pin delays as fast as 12 ns, and counter speeds of up to 118 MHz. Table 3 shows the internal performance of MAX 9000 devices for typical functions.

Table 3. MAX 9000 Performance

Application	Macrocells Used	Speed Grade			Unit
		-15	-20	-25	
16-bit loadable counter	16	118	100	80	MHz
16-bit up/down counter	16	118	100	80	MHz
16-bit prescaled counter	16	118	100	80	MHz
16-bit address decode	1	8.5	10.0	12.0	ns
16-to-1 multiplexer	1	10.9	13.0	15.0	ns

The MAX 9000 architecture supports high-density integration of system-level logic functions. It easily integrates multiple programmable logic devices ranging from PALs, GALs, and 22V10s to field programmable gate array (FPGA) devices and Erasable Programmable Logic Devices (EPLDs). With speed, density, and I/O resources comparable to commonly used masked gate arrays, MAX 9000 EPLDs are also ideal for gate-array prototyping.

All MAX 9000 device packages provide four dedicated inputs for global control signals with large fan-outs. Each I/O pin has an associated Enable register on the periphery of the device. As outputs, these registers provide fast Clock-to-output times; as inputs, they offer quick setup times.

MAX 9000 EPLDs provide 5.0-V in-system programmability (ISP). This feature allows the devices to be reprogrammed on the board for quick and efficient iterations during design development and debug cycles. MAX 9000 devices are guaranteed for 100 program and erase cycles.

MAX 9000 EPLDs contain from 320 to 560 macrocells that are combined into groups of 16 macrocells, called Logic Array Blocks (LABs). Each macrocell has a programmable-AND/fixed-OR array and a configurable register with independently programmable Clock, Clock Enable, Clear, and Preset functions. For increased flexibility, each macrocell offers a dual-output structure that allows the register and the product terms to be used independently. This feature allows register-rich and combinatorial-intensive designs to be efficiently implemented. The dual-output structure of the MAX 9000 macrocell also improves logic utilization, thus increasing the effective capacity of the MAX 9000 devices. To build complex logic functions, each macrocell can be supplemented with both shareable expander product terms and high-speed parallel expander product terms to provide up to 32 product terms per macrocell.

The MAX 9000 family provides programmable speed/power optimization. Speed-critical portions of a design can run at high speed/full power, while the remainder runs at reduced speed/low power. This speed/power optimization feature enables the user to configure one or more macrocells to operate at 50% or less power while adding only a nominal timing delay. MAX 9000 devices also provide an option that reduces the slew rate of the output buffers, minimizing noise transients when non-speed-critical signals are switching.

MAX 9000 output drivers can be set for either 3.3-V or 5.0-V operation, allowing MAX 9000 devices to be used in mixed-voltage systems.

The MAX 9000 family is supported by Altera's MAX+PLUS II development system, a single, integrated package that offers schematic, text, and waveform design entry; compilation and logic synthesis; simulation and timing analysis; and device programming. MAX+PLUS II provides EDIF, VHDL, Verilog HDL, and other interfaces for additional design entry and simulation support from other industry-standard PC- and workstation-based CAE tools. MAX+PLUS II runs on 486- and Pentium-based PCs, and Sun SPARCstation, HP 9000 Series 700, IBM RISC System/6000, and DEC Alpha AXP workstations.

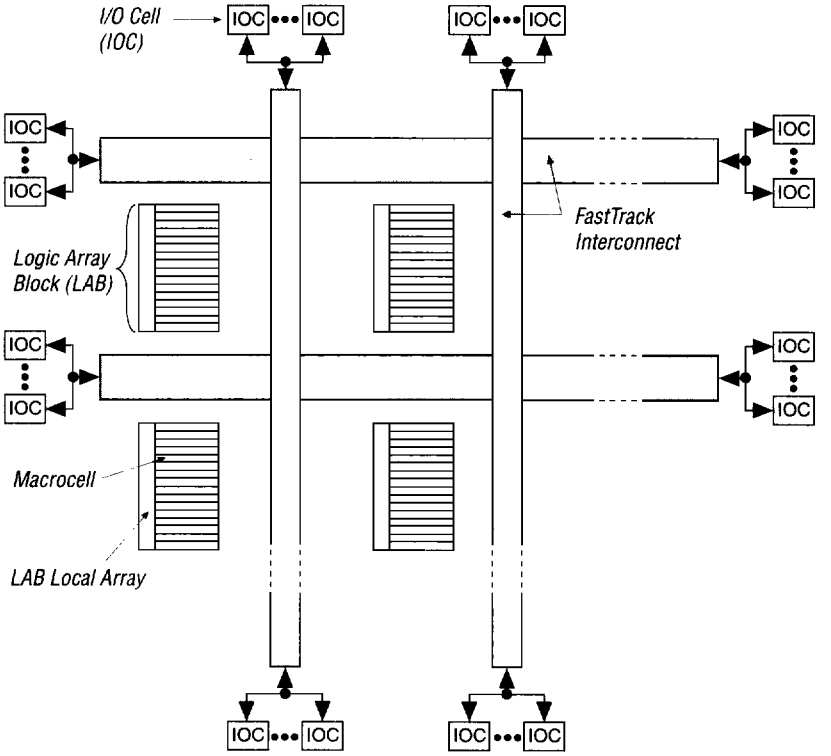
Functional Description

MAX 9000 devices use third-generation MAX architecture that yields both high performance and a high degree of utilization for most applications. This architecture also includes a FastTrack interconnect and dedicated I/O cells. The MAX 9000 architecture includes the following elements:

- Logic Array Blocks
- Macrocells
- Expander product terms (shareable and parallel)
- FastTrack Interconnect
- I/O cells

Figure 1 shows a block diagram of the MAX 9000 architecture.

Figure 1. MAX 9000 Device Block Diagram



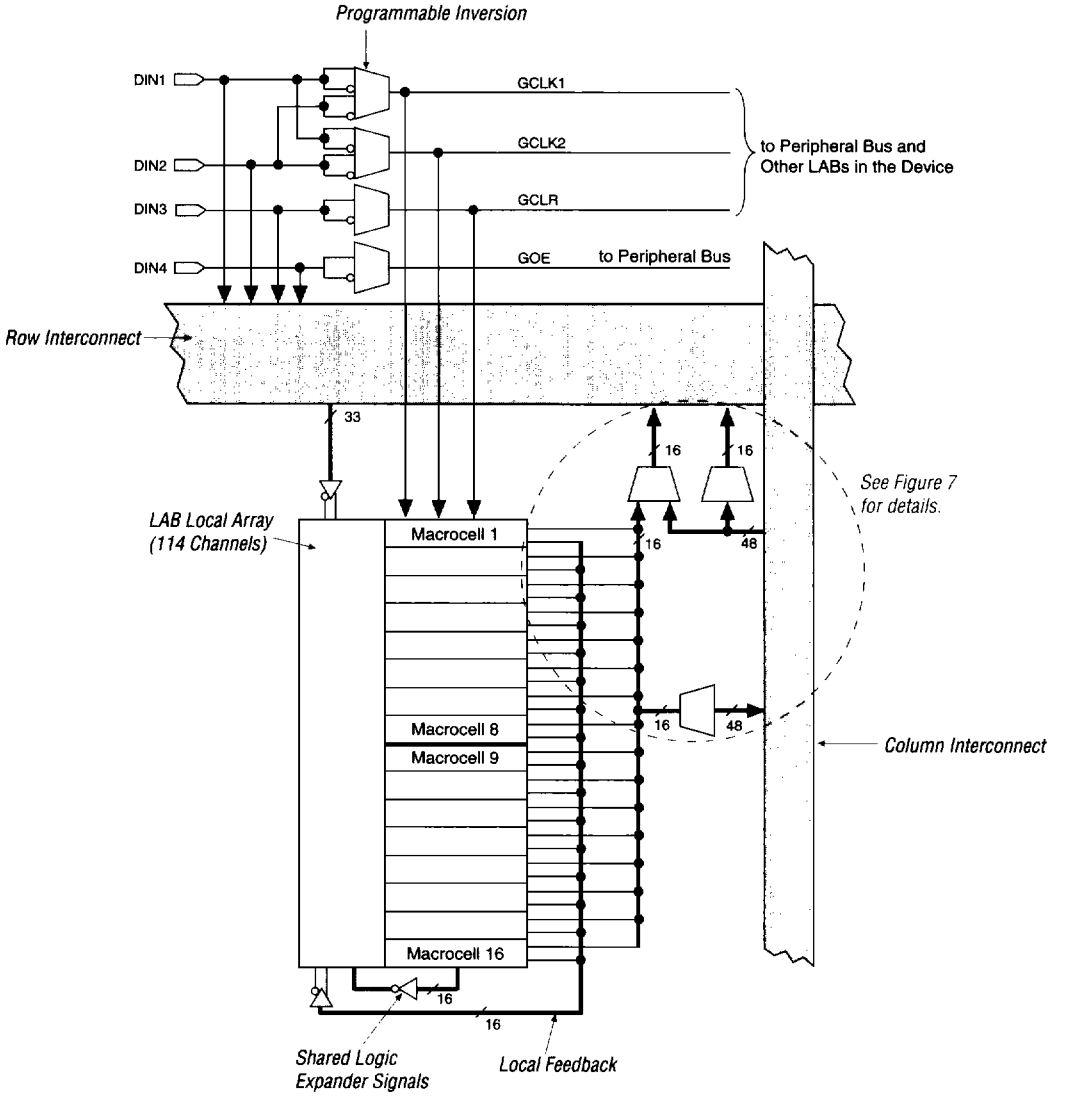
Logic Array Blocks

The MAX 9000 architecture is based on the concept of linking high-performance, flexible logic array modules called Logic Array Blocks (LABs). LABs consist of 16-macrocell arrays that are fed by the LAB local array, as shown in Figure 2. Multiple LABs are linked together via the FastTrack Interconnect, a series of fast, continuous channels that run the entire length and width of the device. The I/O pins are supported by IOCs located at the end of each row (horizontal) and column (vertical) of the FastTrack Interconnect path.

Each LAB is fed by 33 inputs from the row interconnect and 16 feedback signals from the macrocells within the LAB. All of these signals are available within the LAB in their true and inverted form. In addition, 16 shared expander product terms are available in their inverted form, for a total of 114 signals that feed each product term in the LAB. Each LAB is also fed by two low-skew global Clocks and one global Clear that can be used for register control signals in all 16 macrocells.

The LAB directly drives the row and column interconnect. Each macrocell can drive out of the LAB onto one or both of these routing resources. Once signals are on the row or column interconnect, they can quickly traverse to other LABs or to the IOCs.

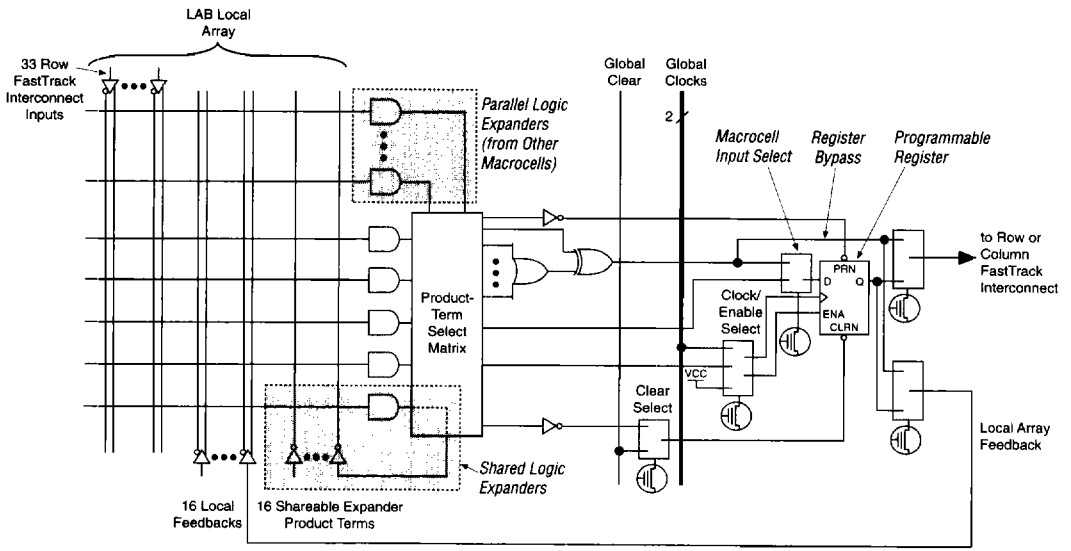
Figure 2. MAX 9000 Logic Array Block



Macrocells

The MAX 9000 macrocell consists of three functional blocks: the product terms, the product-term select matrix, and the programmable register. The macrocell can be individually configured for both sequential and combinatorial logic operation. See Figure 3.

Figure 3. MAX 9000 Macrocell & Local Array



Combinatorial logic is implemented in the local array, which provides five product terms per macrocell. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as secondary inputs to the macrocell's register Clear, Preset, Clock, and Clock Enable control functions. One product term per macrocell can be inverted and directly fed back into the local array. This "shareable" product term can be connected to any other product term within the LAB. Based on the logic requirements of the design, MAX+PLUS II automatically optimizes product-term allocation.

For registered functions, each macrocell flipflop can be individually programmed to emulate D, T, JK, or SR operation with programmable Clock control. If necessary, the flipflop can be bypassed for combinatorial operation. During design entry, the user specifies the desired flipflop type; MAX+PLUS II then selects the most efficient flipflop operation for each registered function to minimize the resources needed by the design.

Each programmable register can be clocked in three different modes:

- By either global Clock signal. This mode achieves the fastest Clock-to-output performance.
- By a global Clock signal and enabled by an active-high Clock Enable. This mode provides an Enable on each flipflop while still achieving the fast Clock-to-output performance of the global Clock.
- By an array Clock implemented with a product term. In this mode, the flipflop can be clocked by signals from buried macrocells or I/O pins.

Two global Clock signals are available. As shown in Figure 2, these global Clock signals can be the true or the complement of either of the global Clock pins, DIN1 (GCLK1) and DIN2 (GCLK2).

Each register also supports asynchronous Preset and Clear functions. As shown in Figure 3, the product-term select matrix allocates product terms to control these operations. Although the product-term-driven Preset and Clear inputs to registers are active high, active-low control can be obtained by inverting the signal within the logic array. In addition, each register Clear function can be individually driven by the dedicated global Clear pin (DIN3). The global Clear can be programmed for active-high or active-low operation.

All MAX 9000 macrocells offer a dual-output structure that provides independent register and combinatorial logic output within the same macrocell. When the dual-output mode is used, the product-term select matrix allocates one product term to the D input of the register, while the remaining product terms can be used to implement unrelated combinatorial logic. Both the registered and the combinatorial output of the macrocell can feed either the FastTrack Interconnect or the LAB local array.

Expander Product Terms

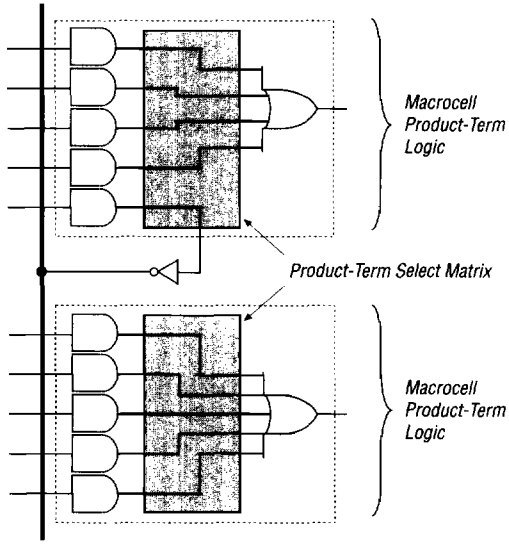
Although most logic functions can be implemented with the five product terms available in each macrocell, some logic functions are more complex and require additional product terms. Instead of using another macrocell to supply the required logic resources, the MAX 9000 architecture offers both shareable and parallel expander product terms ("expanders") that provide additional product terms directly to any macrocell in the same LAB. These expanders help ensure that logic is synthesized with the fewest possible logic resources to obtain the fastest possible speed.

Shareable Expanders

Each LAB has up to 16 shareable expanders that can be viewed as a pool of uncommitted single product terms (one from each macrocell) with inverted outputs that feed back into the LAB local array. Each shareable expander can be used and shared by any or all macrocells in the LAB to build complex logic functions. A small delay ($t_{LOCAL} + t_{SEXP}$) is incurred when shareable expanders are used. Figure 4 shows how shareable expanders can feed multiple macrocells.

Figure 4. Shareable Expanders

Shareable expanders can be shared by any or all macrocells in the LAB.

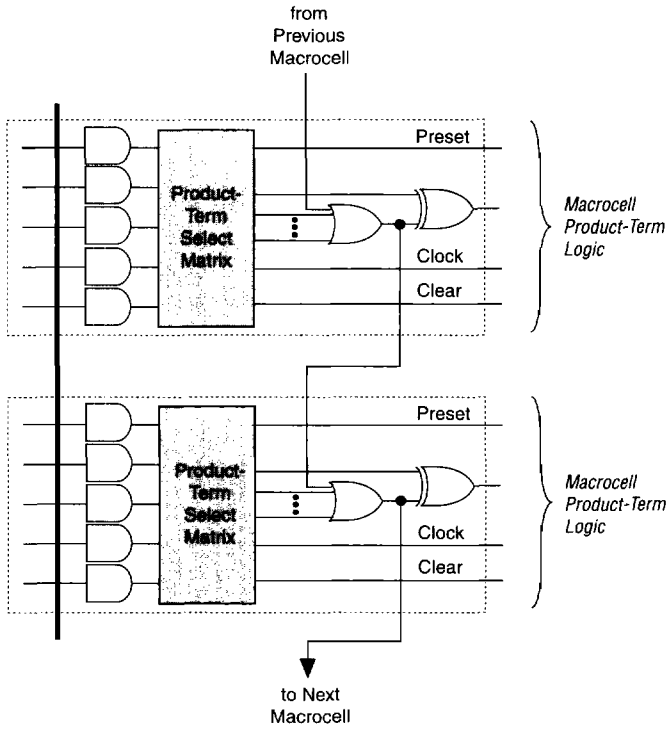


Parallel Expanders

Parallel expanders are unused product terms from macrocells that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 20 product terms to directly feed the macrocell OR logic, with 5 product terms provided by the macrocell and 15 parallel expanders provided by neighboring macrocells in the LAB. Figure 5 shows how parallel expanders can feed the neighboring macrocell.

Figure 5. Parallel Expanders

Unused product terms in a macrocell can be allocated to a neighboring macrocell.



The MAX+PLUS II Compiler can automatically route up to 3 sets of up to 5 parallel expanders to the necessary macrocells. Each set of expanders incurs a small, incremental timing delay (t_{PEXP}). For example, if a macrocell requires 14 product terms, the Compiler uses the 5 dedicated product terms within the macrocell and allocates 2 sets of parallel expanders; the first set includes 5 product terms and the second set includes 4 product terms, increasing the total delay by $2 \times t_{PEXP}$.

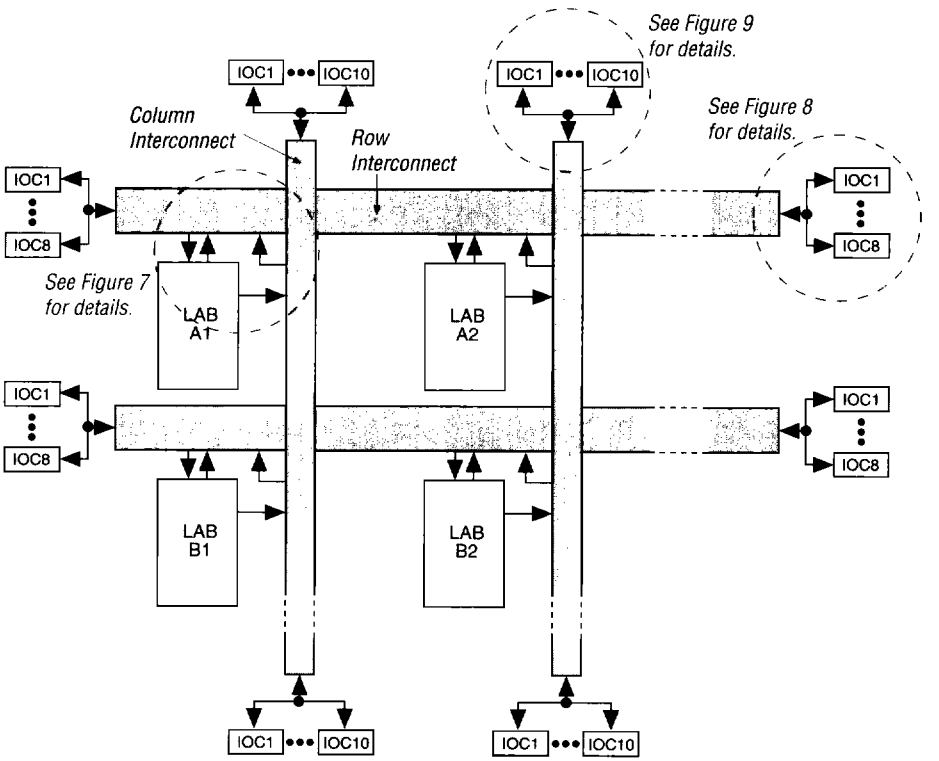
Two groups of 8 macrocells within the LAB (e.g., macrocells 1 to 8 and 9 to 16) form 2 chains to lend or borrow parallel expanders. A macrocell borrows parallel expanders from lower-numbered macrocells. For example, macrocell 8 can borrow parallel expanders from macrocell 7, from macrocells 7 and 6, or from macrocells 7, 6, and 5. Within each group of 8, the lowest-numbered macrocell can only lend parallel expanders and the highest-numbered macrocell can only borrow them.

FastTrack Interconnect

In the MAX 9000 architecture, connections between macrocells and device I/O pins are provided by the FastTrack Interconnect, a series of continuous horizontal and vertical routing channels that traverse the entire MAX 9000 device. This device-wide routing structure provides predictable performance even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance. Figure 6 shows the interconnection of four adjacent LABs with row and column interconnects.

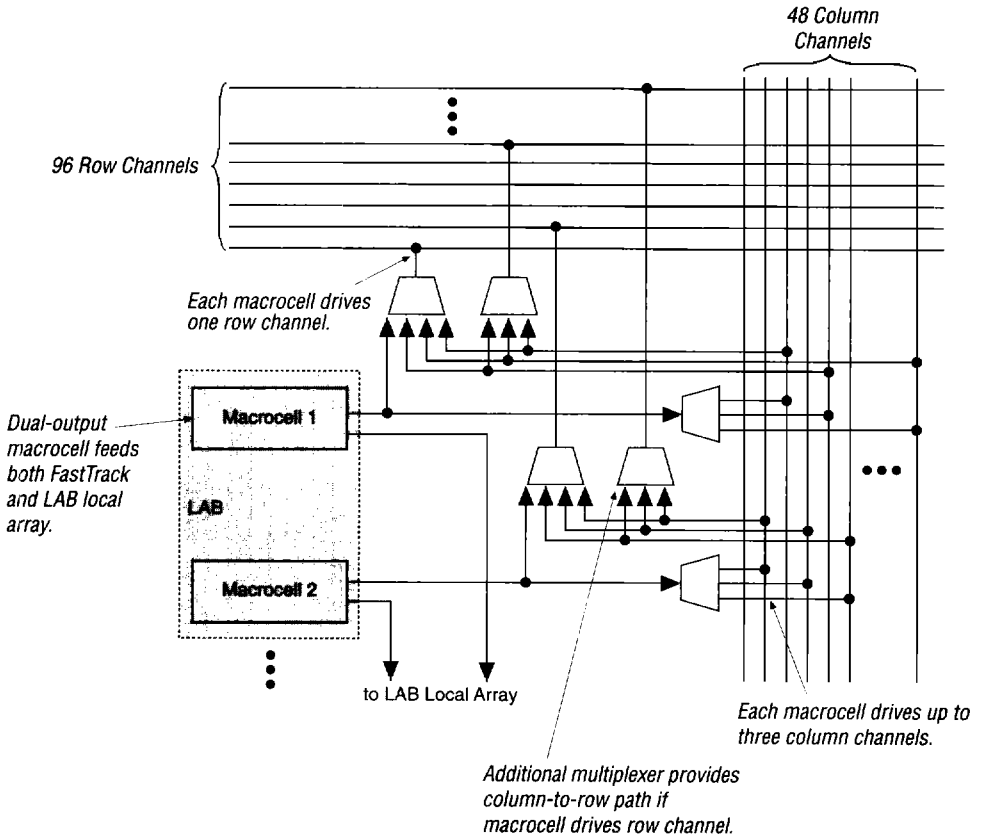
Figure 6. MAX 9000 Device Interconnect Resources

Each LAB is named on the basis of its physical row (A, B, C, etc.) and column (1, 2, 3, etc.) position within the device.



The LABs within MAX 9000 devices are arranged into a matrix of columns and rows. Each row of LABs has a dedicated row interconnect that routes signals both into and out of the LABs in the row. The row interconnect can then drive I/O pins or feed other LABs in the device. Each row interconnect has a total of 96 channels. Figure 7 shows how a macrocell drives the row and column interconnect.

Figure 7. LAB Connections to Row & Column Interconnect



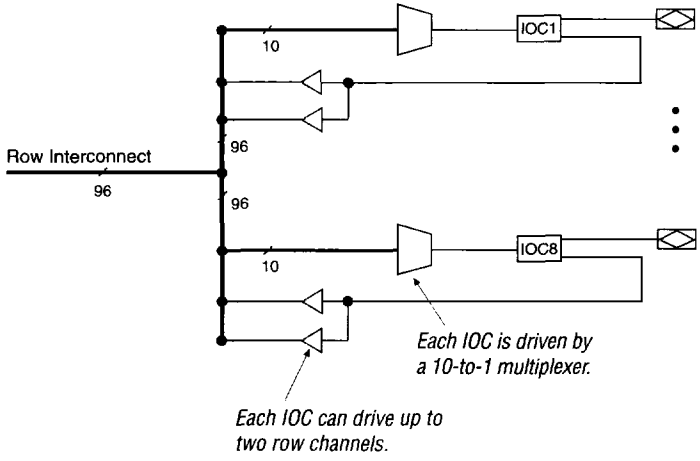
Each macrocell in the LAB can drive up to three separate column interconnect channels. The column channels run vertically across the entire device, and are shared by the macrocells in the same column. The MAX+PLUS II Compiler automatically optimizes connections to a column channel.

A row interconnect channel can be fed by the output of the macrocell through a 4-to-1 multiplexer that it shares with three column channels. If the multiplexer is used for macrocell-to-row connection, the three column signals can access another row channel via an additional 3-to-1 multiplexer. In the LAB, the multiplexers provide all 48 column channels with access to 32 row channels.

Row-to-IOC Connections

Figure 8 illustrates the connections between row interconnect channels and I/O cells (IOCs). An input signal from an IOC can drive two separate row channels. When an IOC is used as an output, the signal is driven by a 10-to-1 multiplexer that selects the row channels. Each end of the row channel feeds eight IOCs on the periphery of the device.

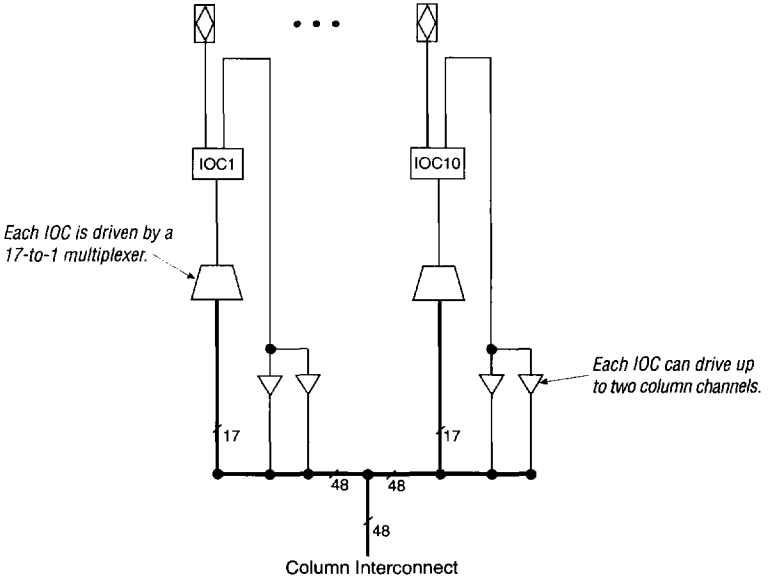
Figure 8. MAX 9000 Row-to-IOC Connections



Column-to-IOC Connections

On each end of the column channels are 10 IOCs (see Figure 9). An input signal from an IOC can drive two separate column channels. When an IOC is used as an output, the signal is driven by a 17-to-1 multiplexer that selects the column channels.

Figure 9. MAX 9000 Column-to-IOC Connections



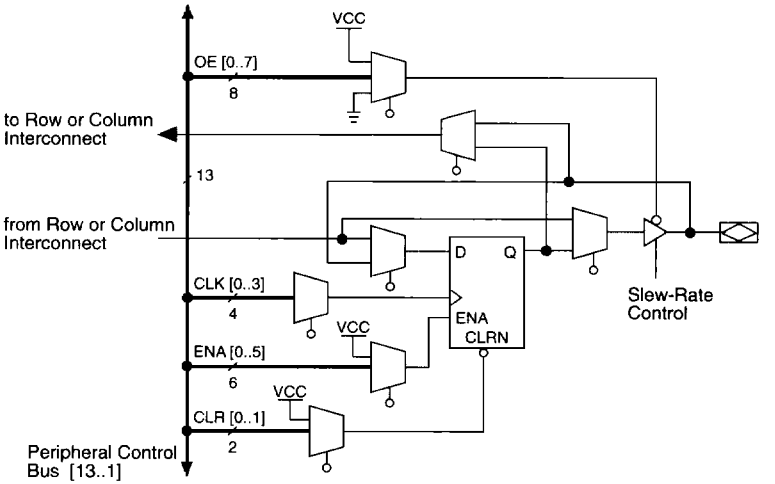
In addition to the general-purpose I/O pins, MAX 9000 devices have four dedicated input pins. These dedicated inputs provide low-skew device-wide signal distribution to the LABs and IOCs in the device, and are typically used for global Clock, Clear, and Output Enable control signals. The global control signals can feed the macrocell or IOC Clock and Clear inputs as well as the IOC Output Enable. The dedicated inputs can also be used as general-purpose data inputs because they can feed the row FastTrack Interconnect.

I/O Cells

Figure 10 shows the I/O cell (IOC) block diagram. Signals enter the MAX 9000 device either from the I/O pins that provide general-purpose input capability or the four dedicated inputs. The IOCs are located at the ends of the row and column interconnect channels.

I/O pins can be used as input, output, or bidirectional pins. Each I/O pin has a register with a Clock Enable input. This register can be used either as an input register for external data that requires fast setup times, or as an output register for data that requires fast Clock-to-output performance. The I/O register Clock Enable allows the global Clock to be used for fast Clock-to-output performance, while maintaining the flexibility required for selective clocking.

Figure 10. I/O Cell (IOC)



The Clock, Clock Enable, Clear, and Output Enable controls for the IOCs are provided by a network of I/O control signals. These signals can be supplied by either the dedicated input pins or internal logic. The IOC control-signal paths are designed to minimize the skew across the device. All control-signal sources are buffered onto high-speed drivers that drive the signals around the periphery of the device. This "peripheral bus" can be configured to provide up to eight Output Enable signals, up to four Clock signals, up to six Clock Enable signals, and up to two Clear signals. Table 4 shows the sources that drive the peripheral bus and how the IOC control signals share the peripheral bus.

The output buffer in each IOC has an adjustable output slew rate that can be configured for low-noise or high-speed performance. A slower slew rate reduces system noise and adds a nominal timing delay to the output buffer delay (t_{OD}) parameter. The fast slew rate should be used for speed-critical outputs in systems that are adequately protected against noise. Designers can specify the slew rate on a pin-by-pin basis during design entry or assign a default slew rate to all pins on a global basis.

Table 4. Peripheral Bus Sources *Note (1)*

Peripheral Control Signal	Source			
	EPM9320	EPM9400	EPM9480	EPM9560
OE0/ENA0	Row 3	C.F.	C.F.	Row 7
OE1/ENA1	Row 2	C.F.	C.F.	Row 6
OE2/ENA2	Row 1	C.F.	C.F.	Row 5
OE3/ENA3	Row 2	C.F.	C.F.	Row 2
OE4/ENA4	Row 1	C.F.	C.F.	Row 1
OE 5	Row 4	C.F.	C.F.	Row 4
OE6	Row 3	C.F.	C.F.	Row 3
OE7/CLR1	Row 2/GOE	C.F.	C.F.	Row 2/GOE
CLR0/ENA5	Row 1/GCLR	C.F.	C.F.	Row 1/GCLR
CLK0	GCLK1	C.F.	C.F.	GCLK1
CLK1	GCLK2	C.F.	C.F.	GCLK2
CLK2	Row 4	C.F.	C.F.	Row 4
CLK3	Row 3	C.F.	C.F.	Row 3

Note:
(1) C.F. = Consult factory.

3.3-V or 5.0-V I/O Operation

All MAX 9000 devices can be set to interface at 3.3 V or 5.0 V. These devices have one set of V_{CC} pins for internal operation and input buffers (V_{CCINT}), and another set for I/O output drivers (V_{CCIO}).

The V_{CCINT} pins must always be connected to a 5.0-V supply. With a 5.0-V V_{CCINT} level, input voltages are at TTL levels and are therefore compatible with 3.3-V and 5.0-V inputs. The V_{CCIO} pins can be connected to either a 3.3-V or 5.0-V supply, depending on the output requirements. When the V_{CCIO} pins are connected to a 5.0-V supply, the output levels are compatible with 5.0-V systems. When the V_{CCIO} pins are connected to a 3.3-V supply, the output high is at 3.3 V and is therefore compatible with 3.3-V systems. Devices operating with a 3.3-V V_{CCIO} level incur a nominal timing delay adder for the t_{OD} parameter.

In-System Programmability (ISP)

MAX 9000 devices are in-system programmable through a 4-pin JTAG interface. In-system programmability (ISP) allows for quick and efficient iterations during design development and debug cycles. The MAX 9000 architecture employs internal charge pumps to generate the 12.0-V programming voltage, eliminating the need for an external 12.0-V power supply to program the devices on the board.

ISP simplifies the manufacturing flow, by allowing the devices to be mounted on the printed circuit board before they are programmed with standard pick-and-place equipment. Programming can be completed as part of the board testing procedure, eliminating lead damage on high-pin-count packages, such as QFP devices, due to handling during programming. Product upgrades can be performed in the field via software or modem.

For more information on how to implement ISP in MAX 9000 devices, contact Altera Applications at (800) 800-EPLD.

MAX 9000 EPLDs can also be programmed on 486- and Pentium-based PCs with MAX+PLUS II, the Altera Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device.

JTAG Operation

All MAX 9000 devices provide JTAG boundary-scan testing circuitry. For detailed information on JTAG operation in MAX 9000 devices, contact Altera Applications at (800) 800-EPLD.

Programmable Speed/Power Control

MAX 9000 devices offer a power-saving mode that supports low-power operation across user-defined signal paths or the entire device. This feature allows total power dissipation to be reduced by 50% or more, since most logic applications require only a small fraction of all gates to operate at maximum frequency.

The designer can program each individual macrocell in a MAX 9000 EPLD for either high-speed (Turbo Bit on) or low-power (Turbo Bit off) operation. As a result, speed-critical paths in the design can run at high speed, while remaining paths can operate at reduced power. Macrocells that run at low power incur a nominal timing delay adder (t_{LPA}) for the t_{LOCAL} parameter.

Design Security

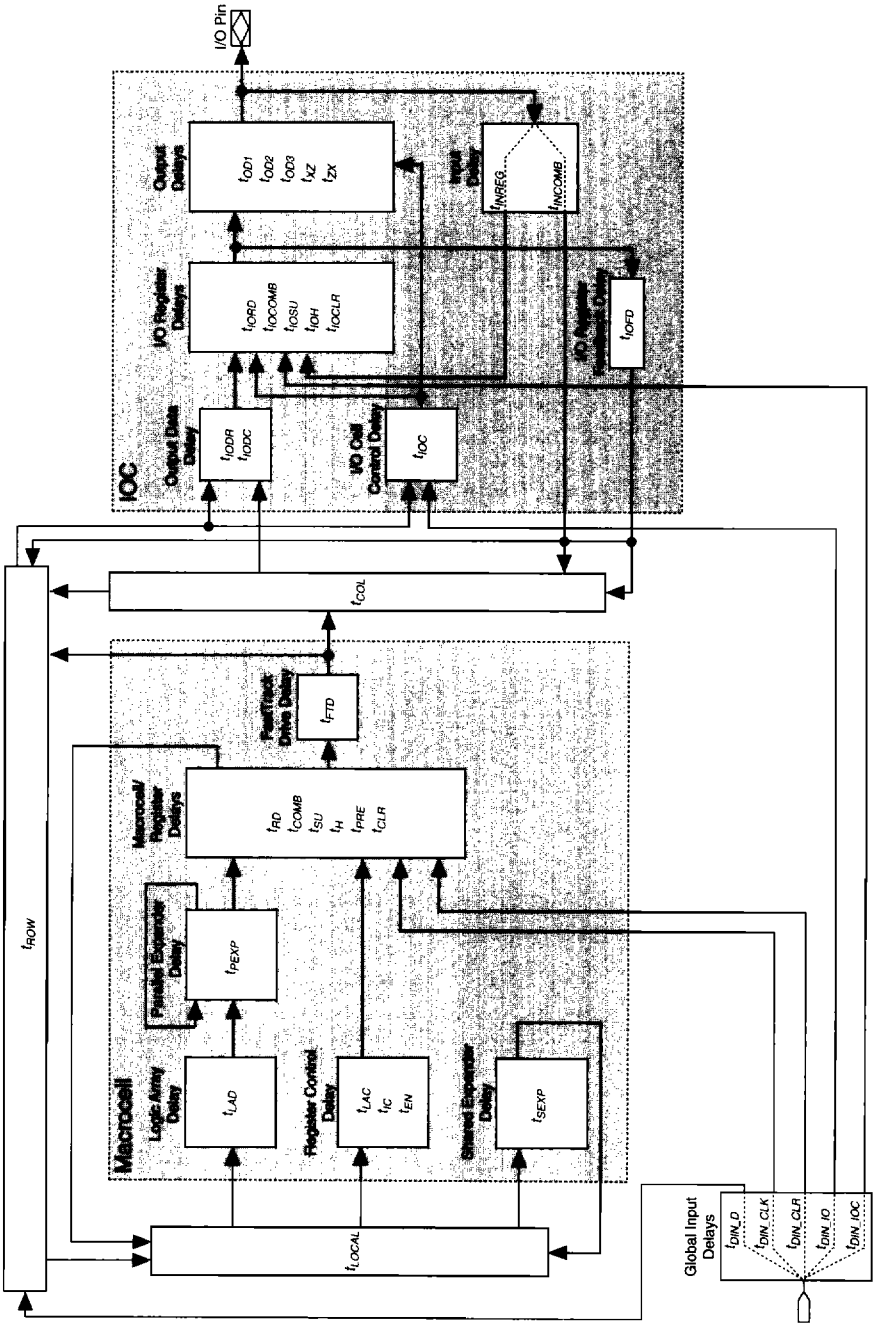
All MAX 9000 EPLDs contain a programmable Security Bit that controls access to the data programmed into the device. When this bit is programmed, a proprietary design implemented in the device cannot be copied or retrieved. This feature provides a high level of design security, since programmed data within EEPROM cells is invisible. The Security Bit that controls this function, as well as all other programmed data, is reset when the EPLD is erased.

Timing Model

The continuous, high-performance FastTrack Interconnect routing resources ensure predictable performance and accurate simulation analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and hence have unpredictable performance. Timing simulation and delay prediction are available with the MAX+PLUS II Simulator and Timing Analyzer, or with industry-standard CAE tools. The Simulator offers both pre-synthesis functional simulation to evaluate logic design accuracy and post-synthesis timing simulation with 0.1-ns resolution. The Timing Analyzer provides point-to-point timing delay information, setup and hold time prediction, and system-level performance analysis.

The MAX 9000 timing model in Figure 11 shows the delays that correspond to various paths and functions in the circuit. This model contains three distinct parts: the macrocell; the IOC; and the interconnect, including the row and column FastTrack Interconnect and LAB local array paths. Each parameter shown in Figure 11 is expressed as a worst-case value in the "Internal Timing Characteristics" tables in this data sheet. Hand-calculations that use the MAX 9000 timing model and these timing parameters can be used to calculate MAX 9000 device performance.

Figure 11. MAX 9000 Timing Model

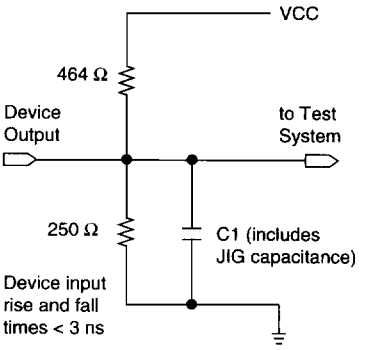


Generic Testing

MAX 9000 EPLDs are fully functionally tested and guaranteed. Complete testing of each programmable EEPROM bit and all logic functionality ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 12. Test patterns can be used and then erased during early stages of the production flow.

Figure 12. MAX 9000 AC Test Conditions

Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold test must not be performed under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.



MAX+PLUS II Development System

MAX 9000 devices are supported by Altera's MAX+PLUS II development system. MAX+PLUS II also supports the Altera Classic, MAX 5000, MAX 7000, FLEX 8000, and FLEX 8000M device families.

Designs can be entered as logic schematics with the Graphic Editor; as state machines, truth tables, conditional logic, and Boolean equations with the Altera Hardware Description Language (AHDL), VHDL, or Verilog HDL; or as waveforms with the Waveform Editor. Logic synthesis and minimization automatically optimize the logic of a design. MAX+PLUS II also provides automatic design partitioning into multiple devices from the same family. Design verification and timing analysis are performed with the built-in Simulator and Timing Analyzer. Errors in a design can be automatically located and highlighted in the original design files.

MAX+PLUS II software runs on 486- and Pentium-based PCs, as well as on Sun SPARCstation, HP 9000 Series 700, IBM RISC System/6000, and DEC Alpha AXP workstations. It gives designers the tools to create complex logic designs quickly and efficiently. MAX+PLUS II provides an EDIF netlist interface for additional design entry and simulation support with popular CAE tools from Cadence, Mentor Graphics, Synopsys, Viewlogic, Intergraph, Logic Modeling, and others. MAX+PLUS II also exports Verilog HDL and VHDL netlist files for use with other industry-standard design verification tools.

Go to the current *MAX+PLUS II Programmable Logic Development System & Software* and *CAE Software Support* data sheets for more information about MAX+PLUS II and other CAE tools.

Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	–2.0	7.0	V
V_I	DC input voltage	*Note (2)*	–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Under bias		150	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers		4.75	5.25	V
V_{CCIO}	Supply voltage for output drivers	5.0-V operation	4.75	5.25	V
		3.3-V operation	3.00	3.60	V
V_I	Input voltage		0	V_{CCINT}	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
T_C	Case temperature	For military use	–55	125	° C

DC Operating Conditions *Notes (3), (4)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CCINT} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC	2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA DC		0.45	V
I_I	Input leakage current	$V_I = V_{CC}$ or GND, *Note (5)*	–10	10	µA
I_{OZ}	Tri-state output off-state current	$V_O = V_{CC}$ or GND	–40	40	µA

Capacitance *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V, f = 1.0 MHz, *Note (7)*		10	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V, f = 1.0 MHz		20	pF

5.0-V Typical I_{CC} Supply Current Values

Symbol	Parameter	Conditions	EPM9320	EPM9400	EPM9480	EPM9560	Unit
I_{CC1}	V_{CC} supply current (low-power mode, standby, typical)	V_I = GND, No load, *Note (8)*	90	110	130	160	mA

Notes to tables:

(1) See *Operating Requirements for Altera Devices* in the current Altera ***Data Book***.
(2) Minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods shorter than 20 ns under no-load conditions.
(3) Typical values are for T_A = 25° C and V_{CC} = 5.0 V.
(4) Operating conditions: V_{CCINT} = 5.0 V ± 5%, T_A = 0° C to 70° C for commercial use.
V_{CCINT} = 5.0 V ± 10%, T_A = –40° C to 85° C for industrial use.
V_{CCINT} = 5.0 V ± 10%, T_C = –55° C to 125° C for military use.
V_{CCIO} = 5.0 V ± 5% for 5.0-V operation. V_{CCIO} = 3.3 V ± 10% for 3.3-V operation.
(5) JTAG input leakage typically –60 µA.
(6) Capacitance measured at 25 ° C. Sample-tested only.
(7) DIN1 and DIN2 input capacitance = 25 pF.
(8) Measured with a 16-bit loadable, enabled, up/down counter programmed into each LAB. I_{CC} measured at 0° C.

Figure 13 shows typical output drive characteristics for MAX 9000 devices with 5.0-V V_{CCIO}.

Figure 13. Output Drive Characteristics with 5.0-V V_{CCIO}

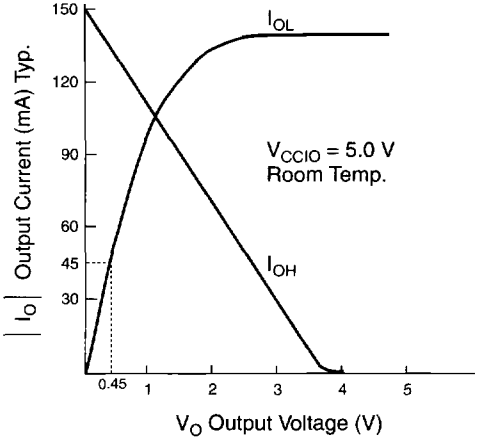
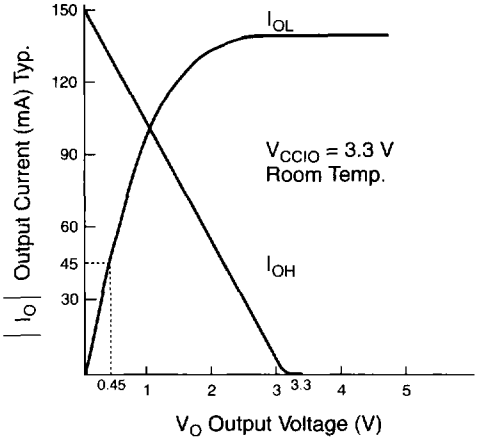


Figure 14 shows typical output drive characteristics for MAX 9000 devices with 3.3-V V_{CCIO}.

Figure 14. Output Drive Characteristics with 3.3-V V_{CCIO}



Calculating the Supply Current

Supply current (I_{CC} in mA) versus frequency (f_{MAX} in MHz) for MAX 9000 devices is calculated with the following equation:

$$I_{CC} = (A \times MC_{TON}) + (B \times MC_{TOFF}) + (C \times MC) \times f_{MAX}$$

The parameters for this equation are:

MC_{TON} = Number of macrocells used with Turbo Bit on
MC_{TOFF} = Number of macrocells used with Turbo Bit off
MC = Total number of macrocells used in the design ($MC_{TON} + MC_{TOFF}$)
f_{MAX} = Highest Clock frequency to the device

Table 5 lists the values for the constants A, B, and C.

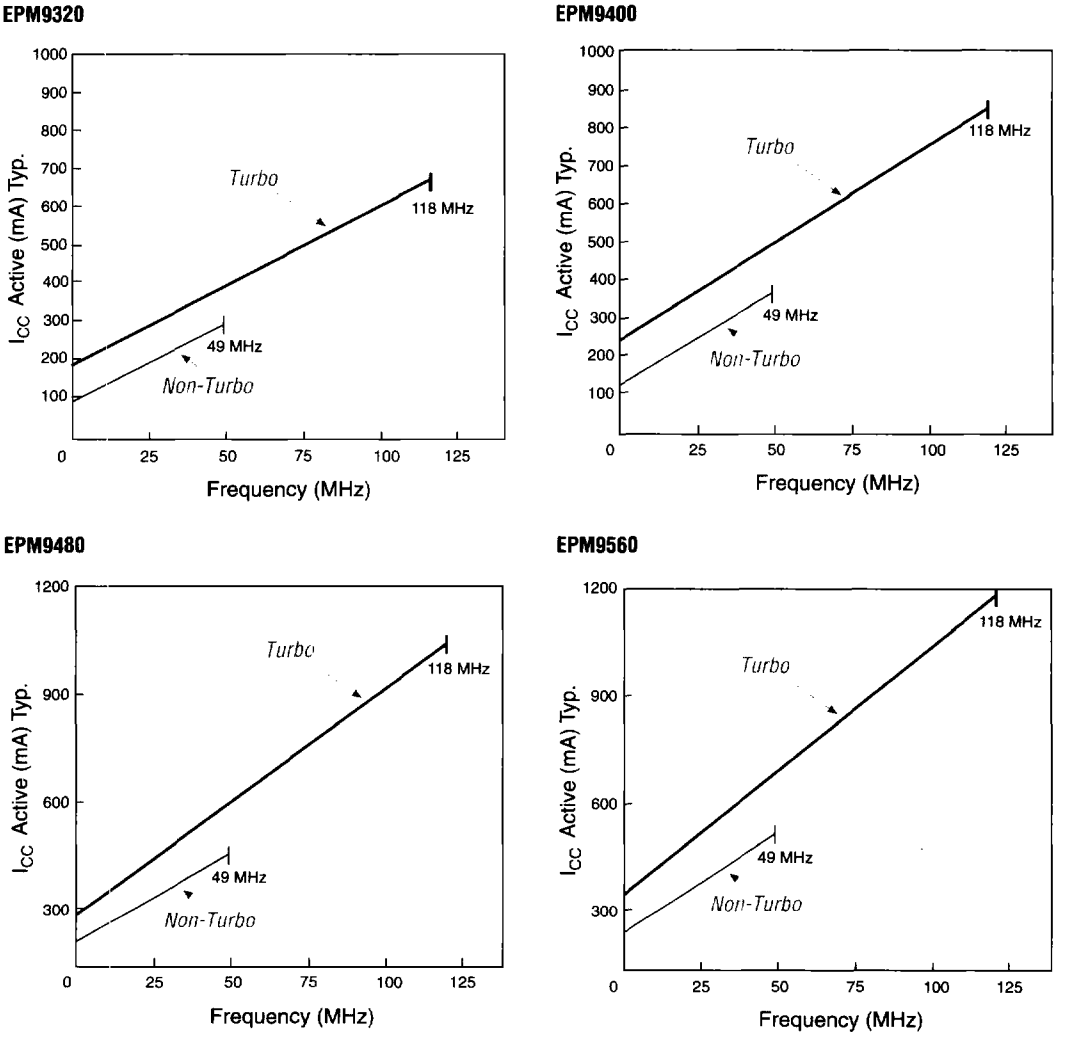
Table 5. MAX 9000 I_{CC} Equation Constants

Device	Constant A	Constant B	Constant C
EPM9320	0.59	0.28	0.013
EPM9400	0.59	0.28	0.013
EPM9480	0.59	0.28	0.013
EPM9560	0.59	0.28	0.013

This calculation provides an I_{CC} estimate based on typical conditions using a typical pattern of a 16-bit, loadable, enabled, up/down counter in each LAB with no output load. Actual I_{CC} should be verified during operation since the measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 15 shows typical supply current versus frequency for the MAX 9000 devices listed in Table 5.

Figure 15. I_{CC} vs. Frequency for MAX 9000 Devices



MAX 9000 External Timing Characteristics *Note (1)*

			EPM9560-15		EPM9560-20		EPM9560-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD}	I/O pin input to row I/O pin output	C1 = 35 pF		15		20		25	ns
t_{FSU}	Global Clock setup time for I/O cell		3.5		4.0		5.0		ns
t_{FH}	Global Clock hold time for I/O cell		0		0		0		ns
t_{FCO}	Global Clock to I/O cell output delay	C1 = 35 pF		6.5		8.5		12	ns
t_{SU}	Global Clock setup time for macrocell		7.5		9.5		13		ns
t_{H}	Global Clock hold time for macrocell		0		0		0		ns
t_{CO}	Global Clock to macrocell output delay	C1 = 35 pF		10.5		15		19.5	ns
t_{CNT}	Minimum internal global Clock period			8.5		10.5		15	ns
f_{CNT}	Maximum internal global Clock frequency	*Note (2)*	117.6		95.2		66.7		MHz
t_{ACNT}	Minimum internal array Clock period			8.5		10.5		15	ns
f_{ACNT}	Maximum internal array Clock frequency	*Note (2)*	117.6		95.2		66.7		MHz

MAX 9000 Internal Timing Characteristics *Note (1)*

Macrocell Delays			EPM9560-15		EPM9560-20		EPM9560-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LAD}	Logic array delay			4		4.5		5.5	ns
t_{LAC}	Logic control array delay			4		4.5		5.5	ns
t_{IC}	Array clock delay			4		4.5		5.5	ns
t_{EN}	Register enable time			4		4.5		5.5	ns
t_{SEXP}	Shared expander delay			4		6		7.5	ns
t_{PEXP}	Parallel expander delay			0.8		1		1	ns
t_{RD}	Register delay			1		1		1	ns
t_{COMB}	Combinatorial delay			1		1		1	ns
t_{SU}	Register setup time		3		4		5		ns
t_{H}	Register hold time		4.5		5.5		7		ns
t_{PRE}	Register preset time			4		4.5		5	ns
t_{CLR}	Register clear time			4		4.5		5	ns
t_{FTD}	FastTrack drive delay			2		2.5		3	ns
t_{LPA}	Low-power adder	*Note (3)*		12		14		16	ns

IOC Delays			EPM9560-15		EPM9560-20		EPM9560-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IODR}	I/O row output data delay			0.2		1.5		2	ns
t_{IODC}	I/O column output data delay			0.2		1.5		2	ns
t_{IOC}	I/O control delay			1		2		2	ns
t_{IORD}	I/O register Clock-to-output delay			1		1.5		1.5	ns
t_{IOCOMB}	I/O combinatorial delay			1		1.5		1.5	ns
t_{IOSU}	I/O register setup time before Clock		2		2		2		ns
t_{IOH}	I/O register hold time after Clock		1.5		1.5		2		ns
t_{IOCLR}	I/O register clear delay			3		3		3	ns
t_{IOFD}	I/O register feedback delay			0		0.5		0.5	ns
t_{INREG}	I/O input pad and buffer to I/O register delay			4.5		5.5		7	ns
t_{INCOMB}	I/O input pad and buffer to row and column delay			1		2		3	ns
t_{OD1}	Output buffer and pad delay, Slow slew rate = off, V_{CCIO} = 5.0 V	*Note (4)*		2.5		2.5		3	ns
t_{OD2}	Output buffer and pad delay, Slow slew rate = off, V_{CCIO} = 3.3 V	*Note (5)*		3.5		3.5		4	ns
t_{OD3}	Output buffer & pad delay, Slow slew rate = on, V_{CCIO} = 5.0 V or 3.3 V	*Notes (4), (5)*		5.5		5.5		6	ns
t_{XZ}	Output buffer disable delay			2.5		2.5		3	ns
t_{ZX}	Output buffer enable delay			2.5		2.5		3	ns

Interconnect Delays			EPM9560-15		EPM9560-20		EPM9560-25		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LOCAL}	LAB local array delay			0.5		0.5		1	ns
t_{ROW}	FastTrack row delay			1.5		2		2.5	ns
t_{COL}	FastTrack column delay			1.7		3		3.5	ns
t_{DIN_D}	Dedicated input data delay			2.5		3		3.5	ns
t_{DIN_CLK}	Dedicated input Clock delay			2.5		3.5		4.5	ns
t_{DIN_CLR}	Dedicated input Clear delay			5		5.5		6	ns
t_{DIN_IOC}	Dedicated input I/O register Clock delay			3		4		5	ns
t_{DIN_IO}	Dedicated input I/O register Control delay			6		6.5		7	ns

Notes to tables:

(1) Operating conditions: V_{CCINT} = 5.0 V ± 5%, V_{CCIO} = 5.0 V ± 5% (except where noted).
(2) Measured with a 16-bit loadable, enabled, up/down counter programmed in each LAB.
(3) The t_{LPA} parameter must be added to the t_{LOCAL} parameter for macrocells running in low-power mode.
(4) Operating conditions: V_{CCIO} = 5.0 V ± 5%.
(5) Operating conditions: V_{CCIO} = 3.3 V ± 10%.

Device Pin-Outs

Table 6 shows the pin names and numbers for each EPM9560 package.

Table 6. EPM9560 Dedicated Pin-Outs

Dedicated Pin	240-Pin RQFP	280-Pin PGA	304-Pin RQFP
DIN1 (GCLK1)	210	V10	266
DIN2 (GCLK2)	211	U10	267
DIN3 (GCLR)	187	V17	237
DIN4 (GOE)	234	W2	296
TCK	91	A9	114
TMS	68	D6	85
TDI	92	C11	115
TDO	114	A18	144
GND	5, 14, 25, 34, 45, 54, 65, 66, 81, 96, 110, 115, 126, 127, 146, 147, 166, 167, 186, 200, 216, 229	D4, D5, D16, E4, E5, E6, E15, E16, F5, F15, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, P4, P5, P15, P16, R4, R5, R15, R16, T4, T5, T16	13, 22, 33, 42, 53, 62, 73, 74, 102, 121, 138, 155, 166, 167, 186, 187, 206, 207, 226, 254, 273, 290
VCCINT (5.0 V only)	4, 64, 24, 157, 117, 44, 177, 137	D15, E8, E10, E12, E14, R7, R9, R11, R13, R14, T14	12, 32, 52, 72, 157, 177, 197, 217
VCCIO (3.3 or 5.0 V)	15, 35, 55, 73, 86, 101, 116, 136, 156, 176, 192, 205, 220, 235	D14, E7, E9, E11, E13, R6, R8, R10, R12, T13, T15	3, 23, 43, 63, 91, 108, 127, 176, 156, 196, 216, 243, 260, 279
No Connect (N.C.)		B6, F6, W1	1, 2, 76, 77, 78, 79, 80, 81, 82, 83, 84, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 297, 298, 299, 300, 301, 302, 303, 304
VPP	67	C4	75

Package Outlines

Figures 16 through 20 show the package outlines for all MAX 9000 devices. Package outlines are listed here in ascending pin count order. For information on device package ordering codes, see *Ordering Information* in the current ***Data Book***. Package outline dimensions are shown in the following formats:

min. inches (min. millimeters)
max. inches (max. millimeters)

or:

nominal inches ± tolerance
(nominal millimeters ± tolerance)

or:

inches
(millimeters) BSC, Min., Max., Ref., Typ.

Figure 16. 84-Pin Plastic J-Lead Chip Carrier (PLCC)

See page 29 for dimension formats. Controlling measurement is in inches.

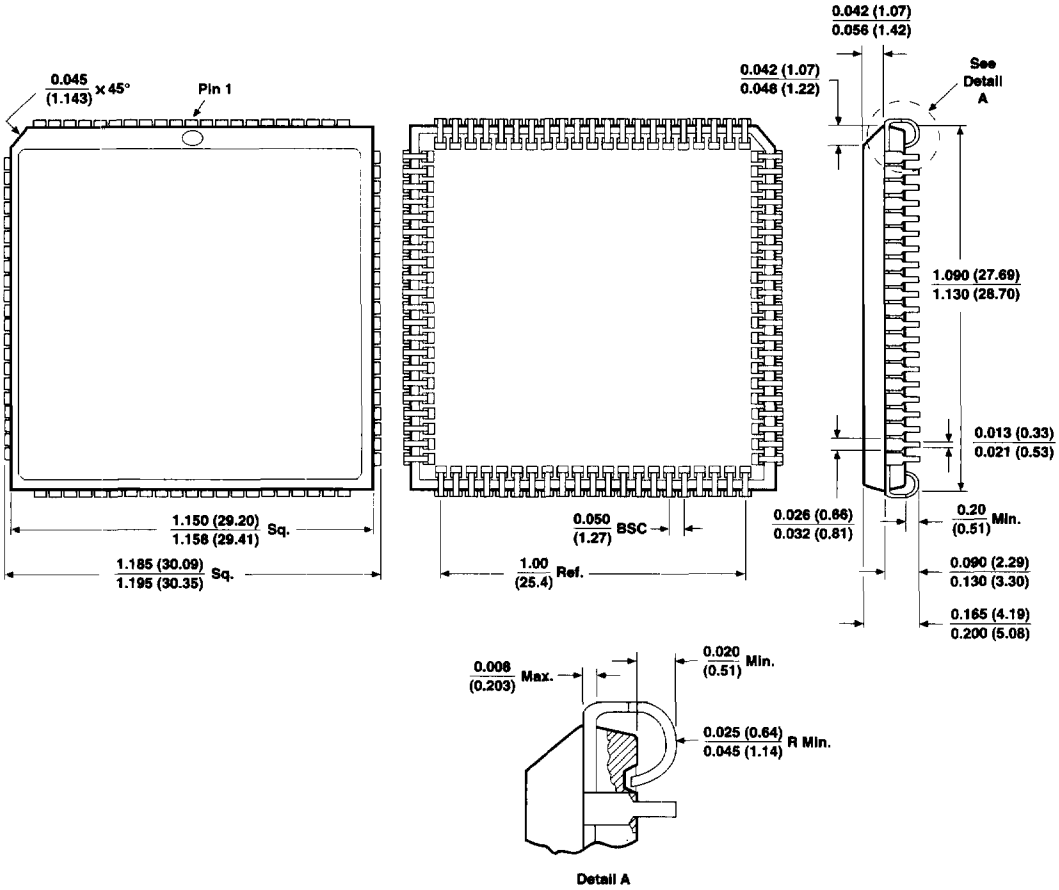


Figure 17. 208-Pin Power Quad Flat Pack (RQFP)

See page 29 for dimension formats. Controlling measurement is in millimeters.

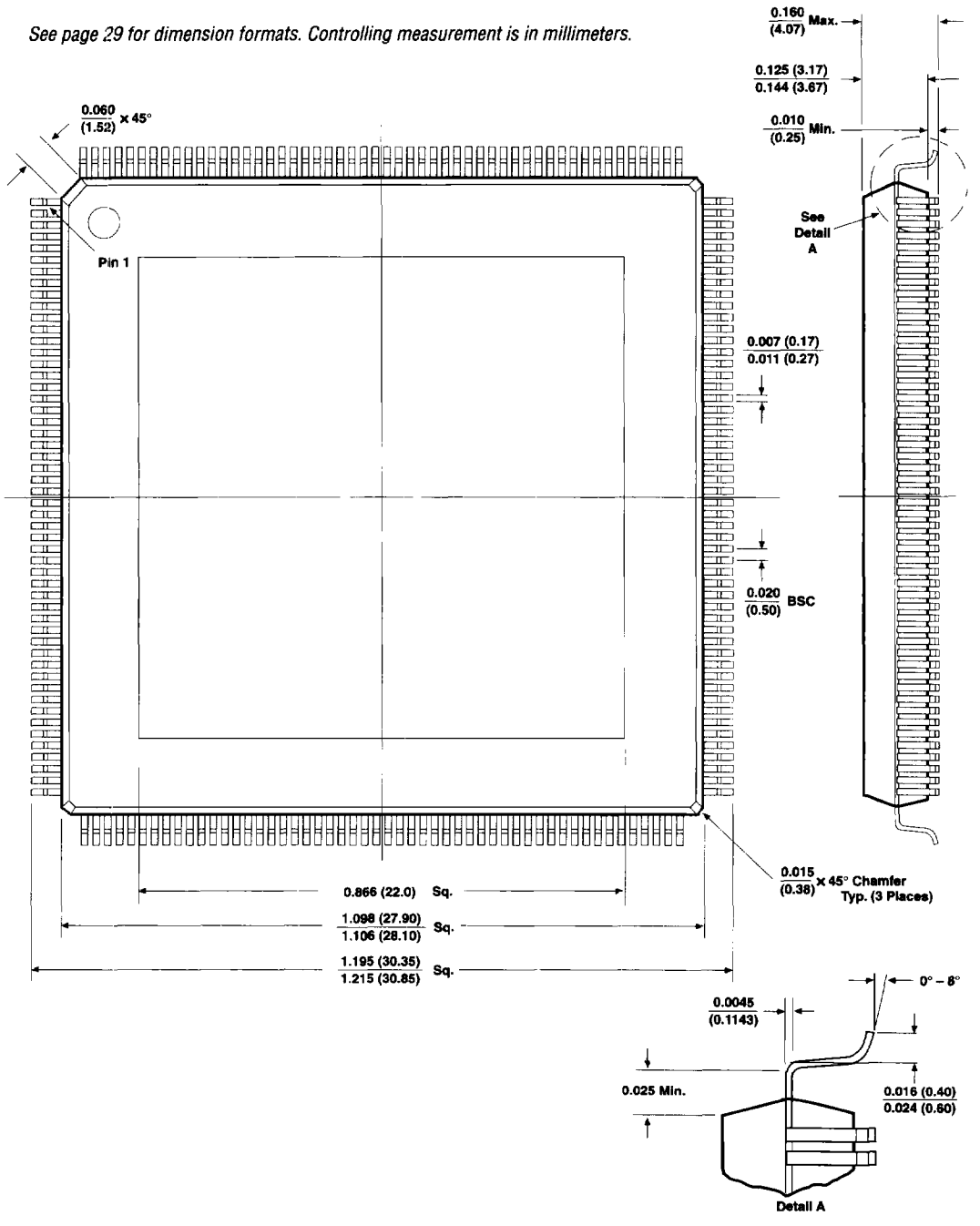


Figure 18. 240-Pin Power Quad Flat Pack (RQFP)

See page 29 for dimension formats. Controlling measurement is in millimeters.

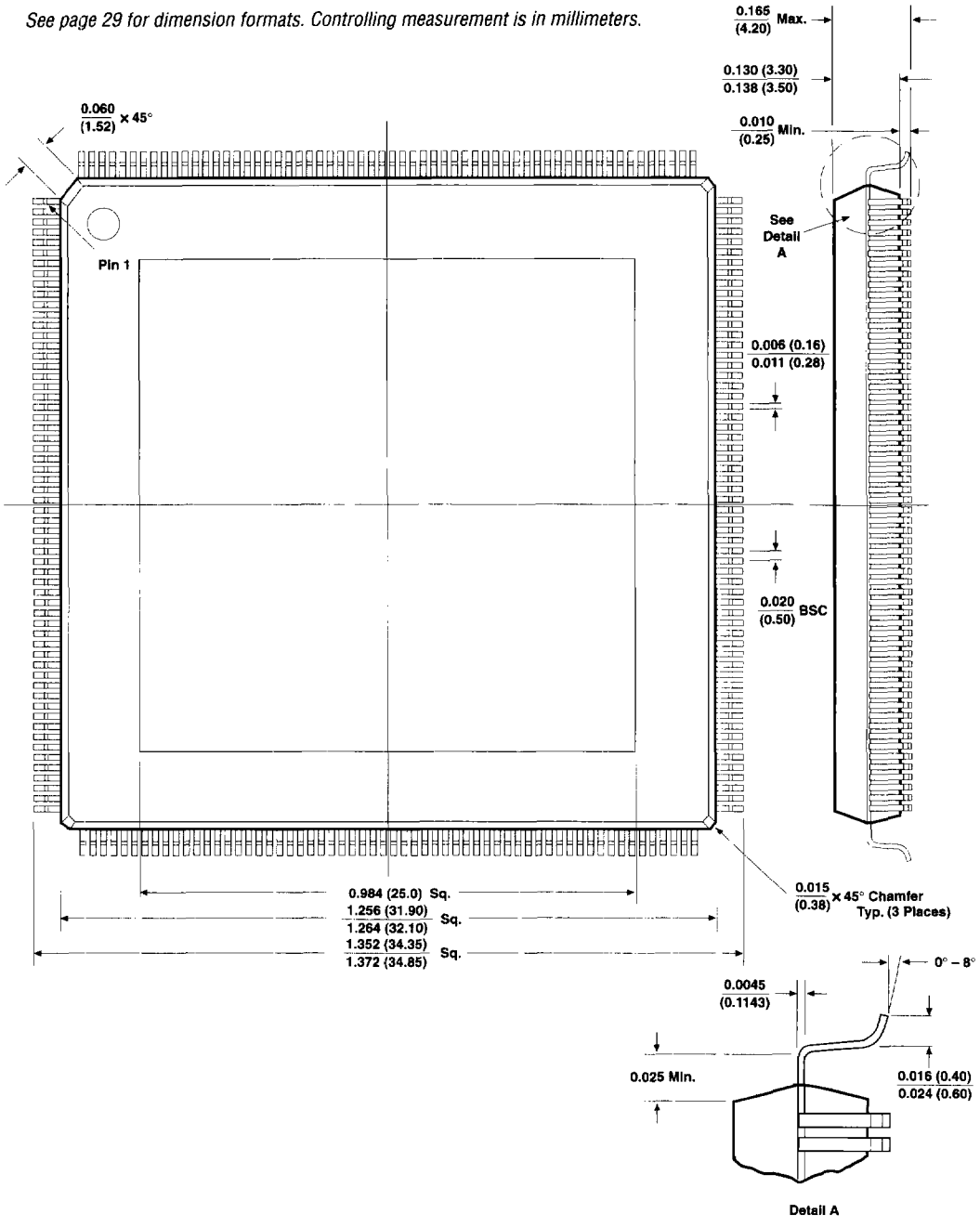


Figure 19. 280-Pin Pin-Grid Array (PGA)

See page 29 for dimension formats. Controlling measurement is in inches.

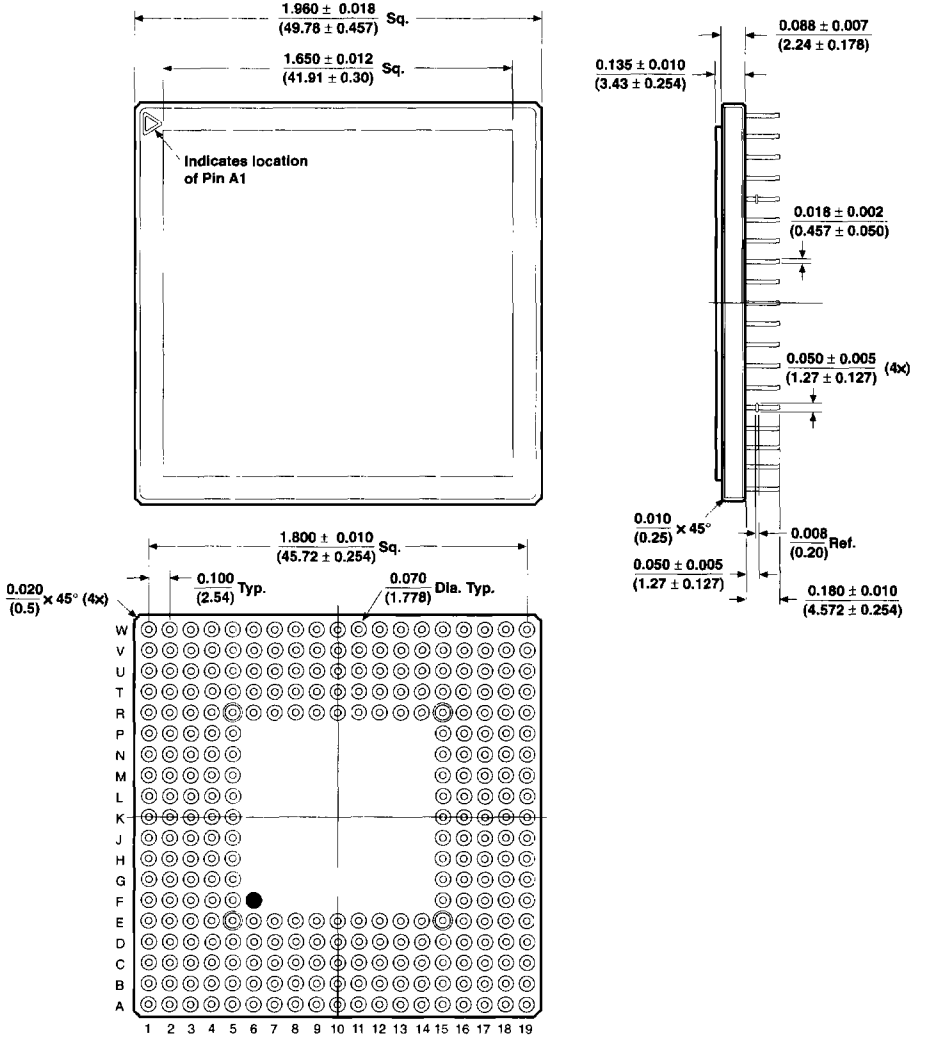
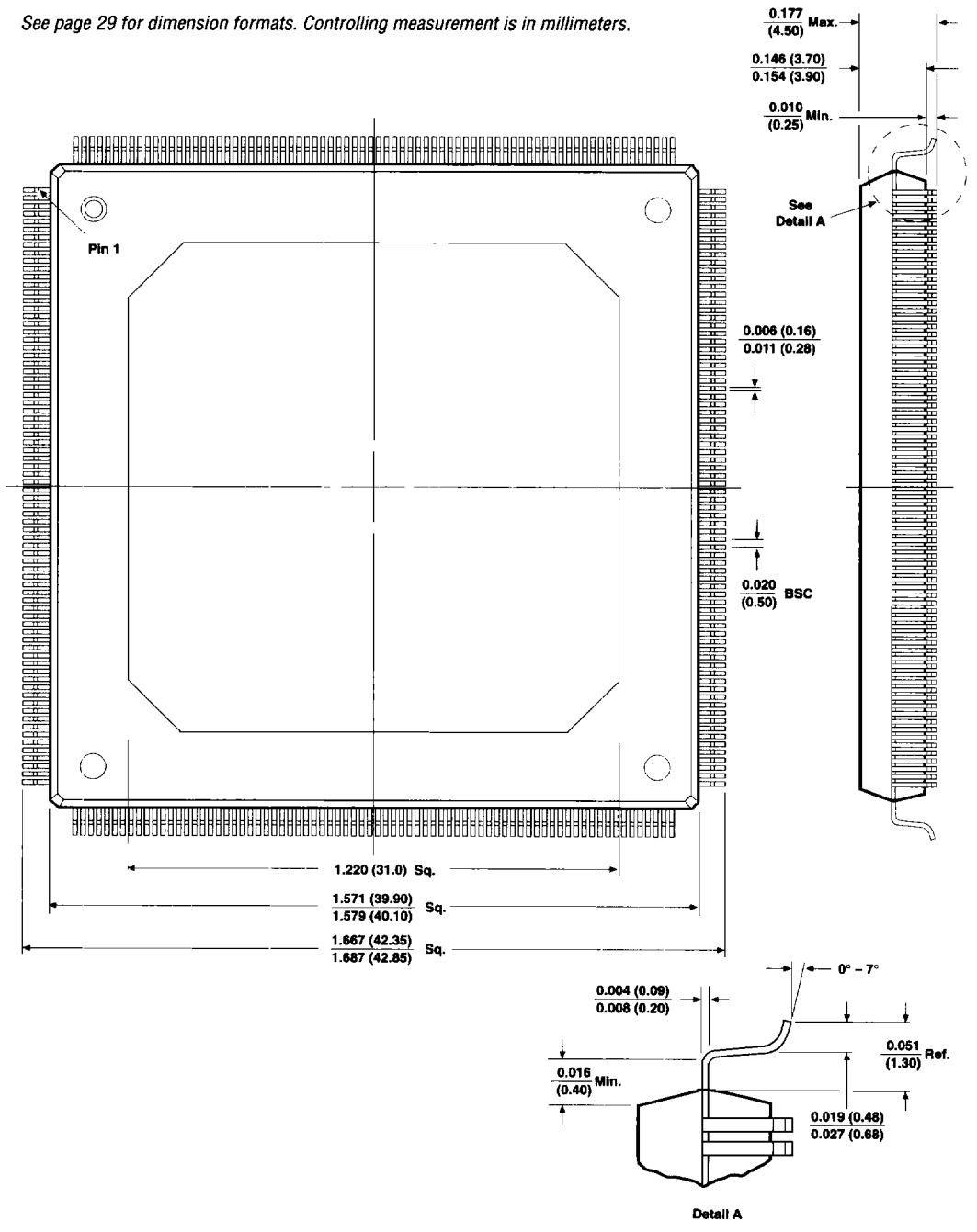


Figure 20. 304-Pin Power Quad Flat Pack (RQFP)

See page 29 for dimension formats. Controlling measurement is in millimeters.



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U.S. and European patents pending

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