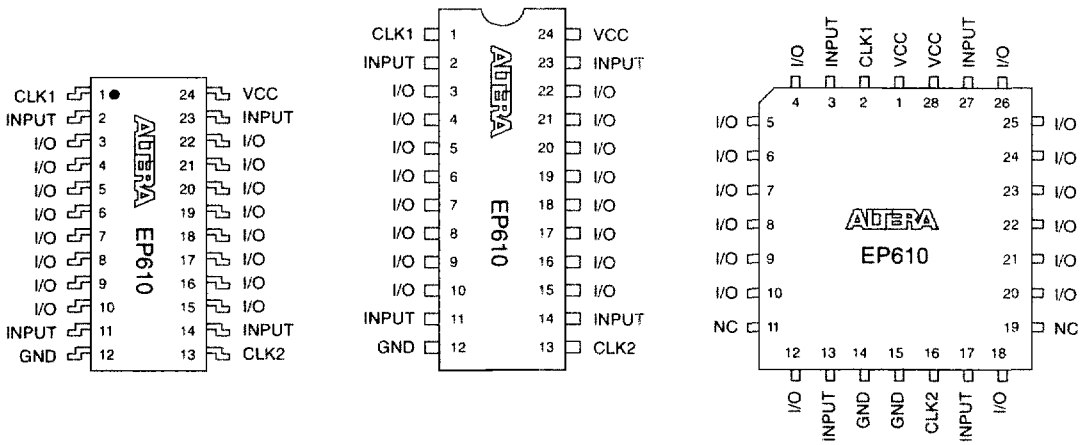
EP610 EPLD

Features

- High-performance, 16-macrocell Classic EPLD
  - Combinatorial speeds with t_{PD} as fast as 10 ns
  - Counter frequencies of up to 100 MHz
  - Pipelined data rates of up to 125 MHz
- Programmable I/O architecture with up to 20 inputs or 16 outputs and 2 clock pins
- EP610 and EP610I devices are pin-, function-, and programming file-compatible
- Programmable clock option for independent clocking of all registers
- Macrocells individually programmable as D, T, JK, or SR flipflops, or for combinatorial operation
- Available in the following packages (see Figure 7):
  - 24-pin small-outline integrated circuit (plastic SOIC only)
  - 24-pin ceramic and plastic dual in-line package (CerDIP and PDIP)
  - 28-pin plastic J-lead chip carrier (PLCC)

Figure 7. EP610 Package Pin-Out Diagrams

Package outlines not drawn to scale. Windows in ceramic packages only.



24-Pin SOIC

EP610

24-Pin DIP

EP610
EP610I

28-Pin PLCC

EP610
EP610I

General Description

EP610 devices have 16 macrocells, 4 dedicated input pins, 16 I/O pins, and 2 global clock pins (see Figure 8). Each macrocell can access signals from the global bus, which consists of the true and complement forms of the dedicated inputs and the true and complement forms of either the output of the macrocell or the I/O input. The CLK1 signal is a dedicated global clock input for the registers in macrocells 9 through 16. The CLK2 signal is a dedicated global clock input for registers in macrocells 1 through 8.

Figure 8. EP610 Block Diagram

Numbers without parentheses are for DIP and SOIC packages. Numbers in parentheses are for J-lead packages.

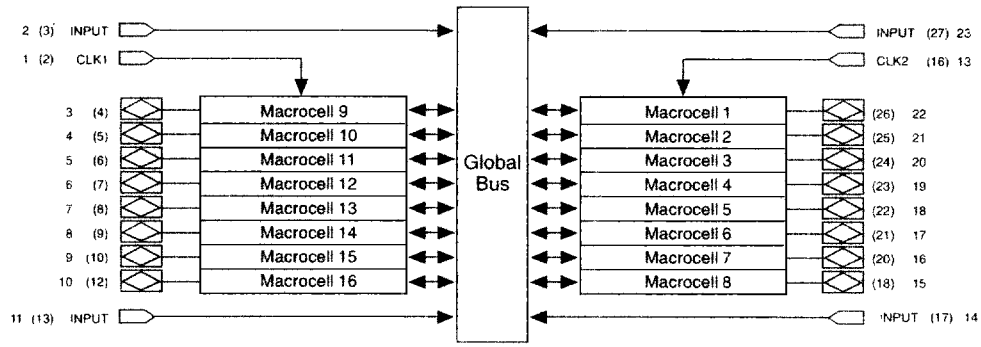


Figure 9 shows the typical supply current (I_{CC}) versus frequency of EP610 devices.

Figure 9. I_{CC} vs. Frequency of EP610 Devices

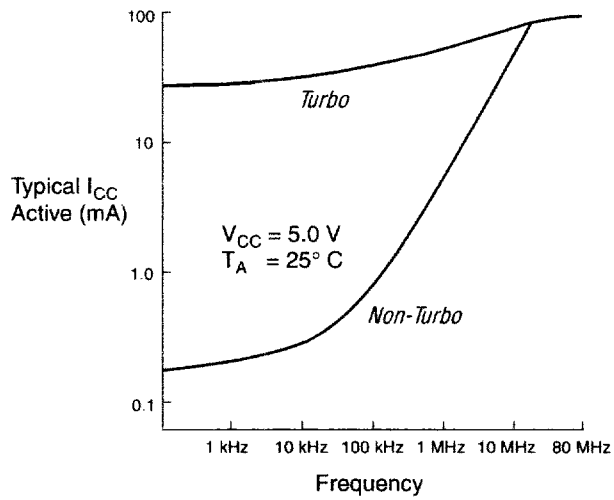
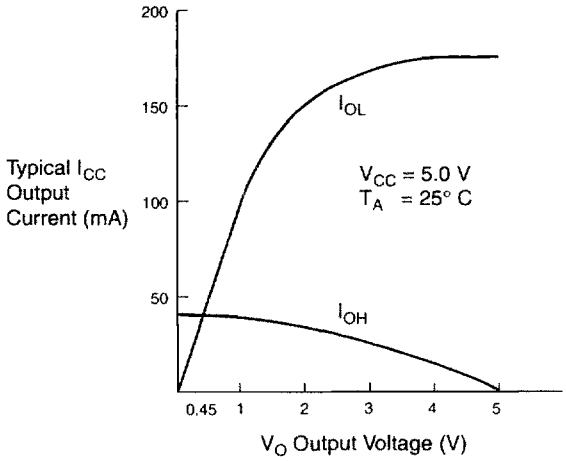


Figure 10 shows the typical output drive characteristics of EP610 devices.

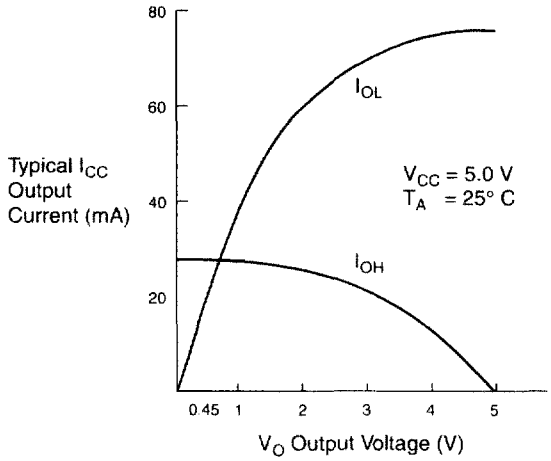
Figure 10. Output Drive Characteristics of EP610 Devices

Drive characteristics may exceed shown curves.

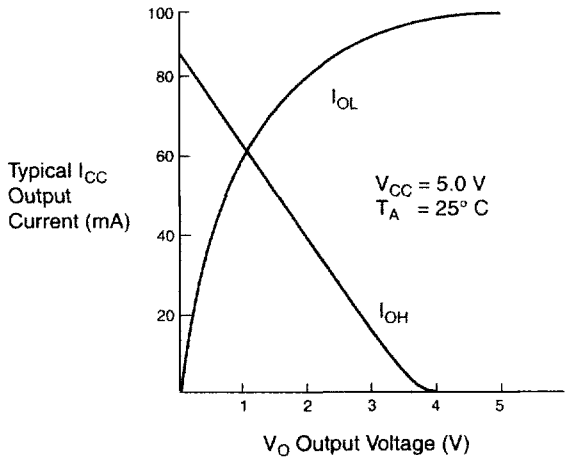
EP610-15 & EP610-20 EPLDs



EP610-25, EP610-30 & EP610-35 EPLDs



EP610I EPLDs



Operating Conditions

Tables 2 through 7 provide information on absolute maximum ratings, recommended operating conditions, operating conditions, and capacitance for EP610 and EP610I devices.

Table 2. EP610 & EP610I Device Absolute Maximum Ratings *Notes (1), (2)*

Symbol	Parameter	Conditions	EP610		EP610I		Unit
			Min	Max	Min	Max	
V_{CC}	Supply voltage	With respect to ground *(3)*	–2.0	7.0	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	–0.5	V_{CC} + 0.5	V
I_{MAX}	DC V_{CC} or ground current		–175	175			mA
I_{OUT}	DC output current, per pin		–25	25			mA
T_{STG}	Storage temperature	No bias	–65	150	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150		150	° C
		Plastic packages, under bias		135		135	° C

Table 3. EP610 & EP610I Device Recommended Operating Conditions *Note (2)*

Symbol	Parameter	Conditions	EP610		EP610I		Unit
			Min	Max	Min	Max	
V_{CC}	Supply voltage	*(4)*	4.75 (4.5)	5.25 (5.5)	4.75	5.25	V
V_I	Input voltage		–0.3	V_{CC} + 0.3	–0.3	V_{CC} + 0.3	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
T_A	Operating temperature	For commercial use	0	70	0	70	° C
		For industrial use	–40	85	–40	85	° C
t_R	Input rise time	*(5)*		100 (50)		500	ns
t_F	Input fall time	*(5)*		100 (50)		500	ns

Table 4. EP610 & EP610I Device DC Operating Conditions *Note (6)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	High-level TTL output voltage	I_{OH} = –4 mA DC *(7)*	2.4		V
	High-level CMOS output voltage	I_{OH} = –0.6 mA DC *(7)*, *(8)*	3.84		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA DC *(7)*		0.45	V
I_I	I/O pin leakage current of dedicated input pins	V_I = V_{CC} or ground	–10	10	µA
I_{OZ}	Tri-state output leakage current	V_O = V_{CC} or ground	–10	10	µA

Table 5. EP610 & EP610I Device Capacitance *Note (9)*

Symbol	Parameter	Conditions	EP610-15 EP610-20		EP610-25 EP610-30 EP610-35		EP610I		Unit
			Min	Max	Min	Max	Min	Max	
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10		20		8	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12		20		8	pF
C_{CLK1}	CLK1 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		20		10	pF
C_{CLK2}	CLK2 pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		20		50		12	pF

Table 6. EP610 Device I_{CC} Supply Current *Notes (2), (10)*

Symbol	Parameter	Conditions	Speed Grade	EP610			Unit
				Min	Typ	Max	
I_{CC1}	V_{CC} supply current (non-Turbo, standby)	$V_I = V_{CC}$ or ground, no load *(11), (12)*			20	150	µA
I_{CC2}	V_{CC} supply current (non-Turbo, active)	$V_I = V_{CC}$ or ground, no load, f = 1.0 MHz *(11), (12)*			5	10 (15)	mA
I_{CC3}	V_{CC} supply current (Turbo, active)	$V_I = V_{CC}$ or ground, no load, f = 1.0 MHz *(12)*	-15, -20		60	90 (115)	mA
			-25, -30, -35		45	60 (75)	mA

Table 7. EP610I Device I_{CC} Supply Current *Note (10)*

Symbol	Parameter	Conditions	EP610I			Unit
			Min	Typ	Max	
I_{CC1}	V_{CC} supply current (non-Turbo, standby)	$V_I = V_{CC}$ or ground, no load, *(11), (12)*		20	150	µA
I_{CC2}	V_{CC} supply current (non-Turbo, active)	$V_I = V_{CC}$ or ground, no load, f = 1.0 MHz *(11), (12)*		3	8	mA
I_{CC3}	V_{CC} supply current (Turbo, active)	$V_I = V_{CC}$ or ground, no load, f = 1.0 MHz *(12)*		65	105	mA

Notes to tables:

(1) See the *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) Numbers in parentheses are for industrial-temperature-range devices.
(3) The minimum DC input is –0.3 V. During transitions, the inputs may undershoot to –2.0 V (EP610) or –0.5 V (EP610I) or overshoot to 7.0 V (EP610) or V_{CC} + 0.5 V (EP610I) for input currents less than 100 mA and periods less than 20 ns.
(4) For EP610 devices, maximum V_{CC} rise time is 50 ms. For EP610I devices, maximum V_{CC} rise time is unlimited with monotonic rise.
(5) For EP610-15 and EP610-20 devices: t_R and t_F = 40 ns.
For EP610-15 and EP610-20 clocks: t_R and t_F = 20 ns.
(6) These values are specified in Table 3 on page 758.
(7) The I_{OH} parameter refers to high-level TTL or CMOS output current; the I_{OL} parameter refers to low-level TTL output current.
(8) This parameter does not apply to EP610I devices.
(9) The device capacitance is measured at 25° C and is sample-tested only.
(10) Typical values are for T_A = 25° C and V_{CC} = 5 V.
(11) When the Turbo Bit option is not set (non-Turbo mode), EP610 devices enter standby mode if no logic transitions occur for 100 ns after the last transition. When the Turbo Bit option is not set, EP610I devices enter standby mode if no logic transitions occur for 75 ns after the last transition.
(12) Measured with a device programmed as a 16-bit counter.

Tables 8 and 9 show the timing parameters for EP610-15 and EP610-20 devices.

Table 8. EP610-15 & EP610-20 External Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	EP610-15		EP610-20		Non-Turbo Adder	Unit
			Min	Max	Min	Max	*(3)*	
t_{PD1}	Input to non-registered output	C1 = 35 pF		15.0		20.0	20.0	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		17.0		22.0	20.0	ns
t_{PZX}	Input to output enable	C1 = 35 pF		15.0		20.0	20.0	ns
t_{PXZ}	Input to output disable	C1 = 5 pF *(4)*		15.0		20.0	20.0	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		15.0		20.0	20.0	ns
f_{MAX}	Maximum clock frequency	*(5)*	83.3		62.5		0.0	MHz
t_{SU}	Global clock input setup time		9.0		11.0		20.0	ns
t_{H}	Global clock input hold time		0.0		0.0		0.0	ns
t_{CH}	Global clock high time		6.0		8.0		0.0	ns
t_{CL}	Global clock low time		6.0		8.0		0.0	ns
t_{CO1}	Global clock to output delay			11.0		13.0	0.0	ns
t_{CNT}	Global clock minimum period			12.0		16.0	0.0	ns
f_{CNT}	Maximum internal global clock frequency	*(6)*	83.3		62.5		0.0	MHz
t_{ASU}	Array clock input setup time		6.0		8.0		20.0	ns
t_{AH}	Array clock input hold time		6.0		8.0		0.0	ns
t_{ACH}	Array clock high time		7.0		9.0		0.0	ns
t_{ACL}	Array clock low time		7.0		9.0		0.0	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(7)*	1.0		1.0		1.0	ns
t_{ACO1}	Array clock to output delay			15.0		20.0	20.0	ns
t_{ACNT}	Array clock minimum period			14.0		18.0	0.0	ns
f_{ACNT}	Array clock internal maximum frequency	*(6)*	71.4		55.6		0.0	MHz

Table 9. EP610-15 & EP610-20 Internal Timing Parameters (Part 1 of 2)

Symbol	Parameter	Conditions	EP610-15		EP610-20		Unit
			Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			4.0		4.0	ns
t_{IO}	I/O input pad and buffer delay			2.0		2.0	ns
t_{LAD}	Logic array delay			6.0		11.0	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		5.0		5.0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		5.0		5.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		5.0		5.0	ns

Table 9. EP610-15 & EP610-20 Internal Timing Parameters (Part 2 of 2)

Symbol	Parameter	Conditions	EP610-15		EP610-20		Unit
			Min	Max	Min	Max	
t_{SU}	Register setup time		5.0		4.0		ns
t_{H}	Register hold time		4.0		7.0		ns
t_{IC}	Array clock delay			6.0		11.0	ns
t_{ICS}	Global clock delay			2.0		4.0	ns
t_{FD}	Feedback delay			1.0		1.0	ns
t_{CLR}	Register clear time			6.0		11.0	ns

Tables 10 and 11 show the timing parameters for EP610-25, EP610-30 and EP610-35 devices.

Table 10. EP610-25, EP610-30 & EP610-35 External Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	EP610-25		EP610-30		EP610-35		Non-Turbo Adder	Unit
			Min	Max	Min	Max	Min	Max	*(3)*	
t_{PD1}	Input to non-registered output	C1 = 35 pF		25.0		30.0		35.0	30.0	ns
t_{PD2}	I/O input to non-registered output			27.0		32.0		37.0	30.0	ns
t_{PZX}	Input to output enable			25.0		30.0		35.0	30.0	ns
t_{PXZ}	Input to output disable	C1 = 5 pF *(4)*		25.0		30.0		35.0	30.0	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		27.0		32.0		37.0	30.0	ns
f_{MAX}	Maximum frequency	*(5)*	47.6		41.7		37.0		0.0	MHz
t_{SU}	Global clock input setup time		21.0		24.0		27.0		30.0	ns
t_{H}	Global clock input hold time		0.0		0.0		0.0		0.0	ns
t_{CH}	Global clock high time		10.0		11.0		12.0		0.0	ns
t_{CL}	Global clock low time		10.0		11.0		12.0		0.0	ns
t_{CO1}	Global clock to output delay			15.0		17.0		20.0	0.0	ns
t_{CNT}	Global clock minimum period			25.0		30.0		35.0	0.0	ns
f_{CNT}	Maximum internal global clock frequency	*(6)*	40.0		33.3		28.6		0.0	MHz
t_{ASU}	Array clock input setup time		8.0		8.0		8.0		30.0	ns
t_{AH}	Array clock input hold time		12.0		12.0		12.0		0.0	ns
t_{ACH}	Array clock high time		10.0		11.0		12.0		0.0	ns
t_{ACL}	Array clock low time		10.0		11.0		12.0		0.0	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(7)*	1.0		1.0		1.0			ns
t_{ACO1}	Array clock to output delay			27.0		32.0		37.0	30.0	ns
t_{ACNT}	Array clock minimum period			25.0		30.0		35.0	0.0	ns
f_{ACNT}	Maximum internal global clock frequency	*(6)*	40.0		33.3		28.6		0.0	MHz

Table 11. EP610-25, EP610-30 & EP610-35 Internal Timing Parameters

Symbol	Parameter	Condition	EP610-25		EP610-30		EP610-35		Unit
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			8.0		9.0		11.0	ns
t_{IO}	I/O input pad and buffer delay			2.0		2.0		2.0	ns
t_{LAD}	Logic array delay			11.0		14.0		15.0	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		6.0		7.0		9.0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		6.0		7.0		9.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6.0		7.0		9.0	ns
t_{SU}	Register setup time		11.0		11.0		12.0		ns
t_{H}	Register hold time		10.0		10.0		10.0		ns
t_{IC}	Array clock delay			13.0		16.0		17.0	ns
t_{ICS}	Global clock delay			1.0		1.0		0.0	ns
t_{FD}	Feedback delay			3.0		5.0		8.0	ns
t_{CLR}	Register clear time			13.0		16.0		17.0	ns

Notes to tables:

(1) These values are specified in Table 3 on page 758.

(2) See *Application Note 78 (Understanding MAX 5000 & Classic Timing)* in this data book for information on internal timing parameters.

(3) The non-Turbo adder must be added to this parameter when the Turbo Bit option is off.

(4) Sample-tested only for an output change of 500 mV.

(5) The f_{MAX} values represent the highest frequency for pipelined data.

(6) Measured with a device programmed as a 16-bit counter.

(7) Sample-tested only. This parameter is a guideline based on extensive device characterization. This parameter applies for both global and array clocking.

Tables 12 and 13 show the timing parameters for EP610I devices.

Table 12. EP610I External Timing Parameters *Notes (1), (2)*

Symbol	Parameter	Conditions	EP610I-10		EP610I-12		EP610I-15		Non-Turbo Adder	Unit
			Min	Max	Min	Max	Min	Max	*(3)*	
t_{PD1}	Input to non-registered output	C1 = 35 pF		10.0		12.0		15.0	25.0	ns
t_{PD2}	I/O input to non-registered output			10.0		12.0		15.0	25.0	ns
t_{PZX}	Input to output enable			15.0		15.0		18.0	25.0	ns
t_{PXZ}	Input to output disable	C1 = 5 pF *(4)*		13.0		15.0		18.0	25.0	ns
t_{CLR}	Asynchronous output clear time	C1 = 35 pF		13.0		15.0		18.0	25.0	ns
f_{MAX}	Maximum frequency	*(5)*	125.0		100.0		83.3		0.0	MHz
t_{SU}	Global clock input setup time		7.0		9.0		12.0		25	ns
t_{H}	Global clock input hold time		0.0		0.0		0.0		0.0	ns
t_{CH}	Global clock high time		5.0		5.0		5.0		0.0	ns
t_{CL}	Global clock low time		5.0		5.0		5.0		0.0	ns
t_{CO1}	Global clock to output delay			6.5		8.0		8.0	0.0	ns
t_{CNT}	Global clock minimum period			10.0		12.0		15.0	25.0	ns
f_{CNT}	Maximum internal global clock frequency	*(6)*	100.0		83.3		66.0		0.0	MHz
t_{ASU}	Array clock input setup time		1.5		3.0		4.0		25.0	ns
t_{AH}	Array clock input hold time		5.5		6.0		6.0		0.0	ns
t_{ACH}	Array clock high time		5.0		5.0		6.0		0.0	ns
t_{ACL}	Array clock low time		5.0		5.0		6.0		0.0	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *(7)*	1.0		1.0		1.0			ns
t_{ACO1}	Array clock to output delay			12.0		14.0		16.0	25.0	ns
t_{ACNT}	Array clock minimum period			10.0		12.0		15.0	25.0	ns
f_{ACNT}	Maximum internal array clock frequency	*(6)*	100.0		83.3		66.0		0.0	MHz

Table 13. EP610 Internal Timing Parameters

Symbol	Parameter	Conditions	EP610I-10		EP610I-12		EP610I-15		Unit
			Min	Max	Min	Max	Min	Max	
t_{IN}	Input pad and buffer delay			1.5		4.0		4.0	ns
t_{IO}	I/O input pad and buffer delay			0.0		0.0		0.0	ns
t_{LAD}	Logic array delay			5.5		6.0		9.0	ns
t_{OD}	Output buffer and pad delay	C1 = 35 pF		3.0		2.0		2.0	ns
t_{ZX}	Output buffer enable delay	C1 = 35 pF		8.0		5.0		6.0	ns
t_{XZ}	Output buffer disable delay	C1 = 5 pF		6.0		5.0		6.0	ns
t_{SU}	Register setup time		3.5		5.0		5.0		ns
t_{H}	Register hold time		3.5		4.0		7.0		ns
t_{IC}	Array clock delay			7.5		8.0		10.0	ns
t_{ICS}	Global clock delay			2.0		2.0		2.0	ns
t_{FD}	Feedback delay			1.0		1.0		1.0	ns
t_{CLR}	Register clear time			8.5		9.0		12.0	ns

Notes to tables:

(1) These values are specified in Table 3 on page 758.

(2) See *Application Note 78 (Understanding MAX 5000 & Classic Timing)* in this data book for more information on Classic timing parameters.

(3) The non-Turbo adder must be added to this parameter when the Turbo Bit option is off.

(4) Sample-tested only for an output change of 500 mV.

(5) The f_{MAX} values represent the highest frequency for pipelined data.

(6) Measured with a device programmed as a 16-bit counter.

(7) Sample-tested only. This parameter is a guideline based on extensive device characterization. This parameter applies for both global and array clocking.